



US005915124A

# United States Patent [19] Morris, III

[11] Patent Number: **5,915,124**  
[45] Date of Patent: **Jun. 22, 1999**

[54] **METHOD AND APPARATUS FOR A FIRST DEVICE ACCESSING COMPUTER MEMORY AND A SECOND DEVICE DETECTING THE ACCESS AND RESPONDING BY PERFORMING SEQUENCE OF ACTIONS**

5,247,650	9/1993	Judd et al.	395/500
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5,710,712	1/1998	Labun	364/528.21
5,732,283	3/1998	Rose et al.	395/836
5,765,022	6/1998	Kaiser et al.	395/842

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*Attorney, Agent, or Firm*—Gates & Cooper

[21] Appl. No.: **08/778,938**

[57] **ABSTRACT**

[22] Filed: **Jan. 3, 1997**

A method of controlling an input/output (I/O) device connected to a computer to facilitate fast I/O data transfers. An address space for the I/O device is created in the virtual memory of the computer, wherein the address space comprises virtual registers that are used to directly control the I/O device. In essence, control registers and/or memory of the I/O devices are mapped into the virtual address space, and the virtual address space is backed by control registers and/or memory on the I/O device. Thereafter, the I/O device detects writes to the address space. As a result, a pre-defined sequence of actions can be triggered in the I/O device by programming specified values into the data written into the mapped virtual address space.

[51] Int. Cl.<sup>6</sup> ..... **G06F 13/00**

[52] U.S. Cl. .... **395/829; 395/826; 395/836; 395/856; 711/146**

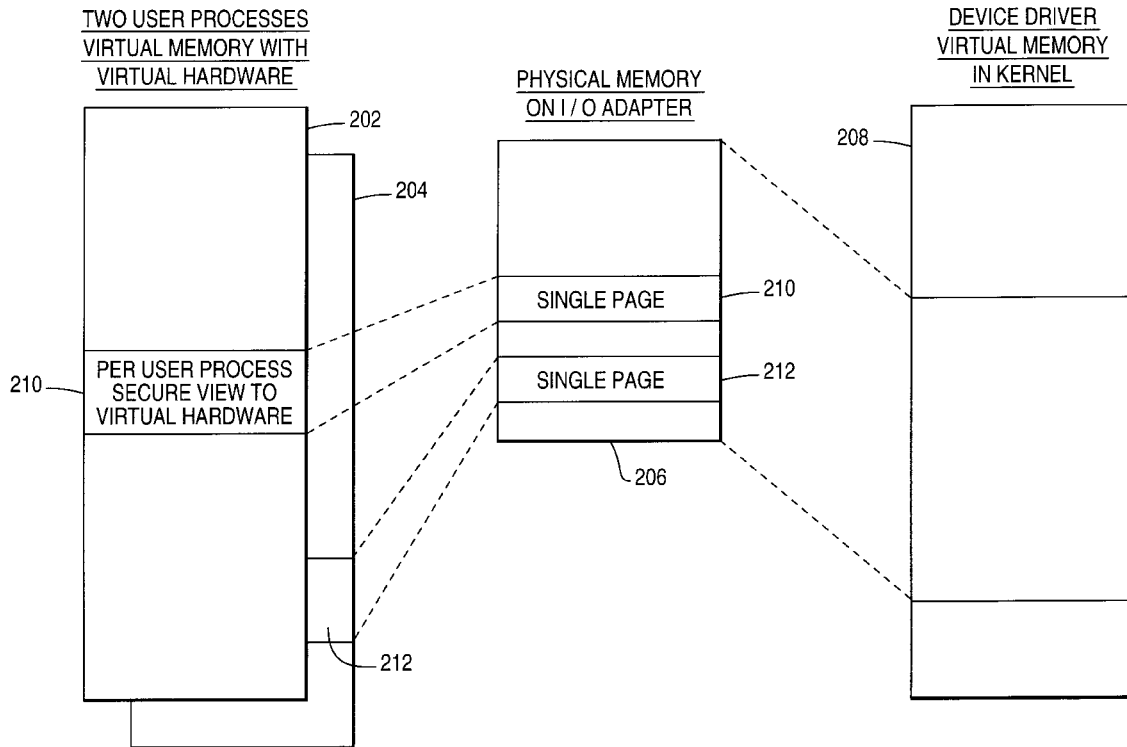
[58] Field of Search ..... 370/218; 395/520, 395/872, 828, 847, 836, 842, 829, 473; 707/201; 364/578, 528.21

[56] **References Cited**

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**27 Claims, 8 Drawing Sheets**



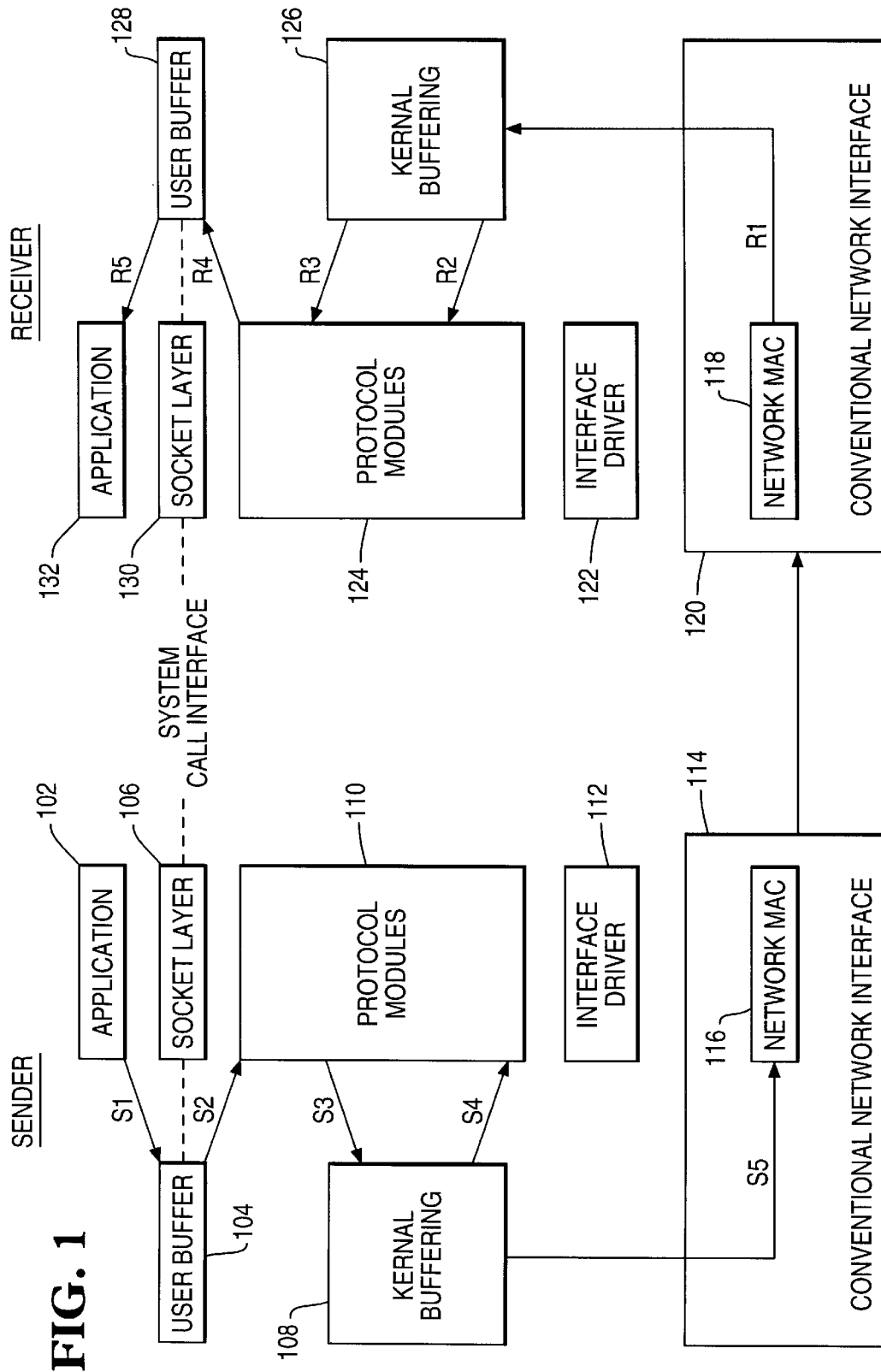


FIG. 1

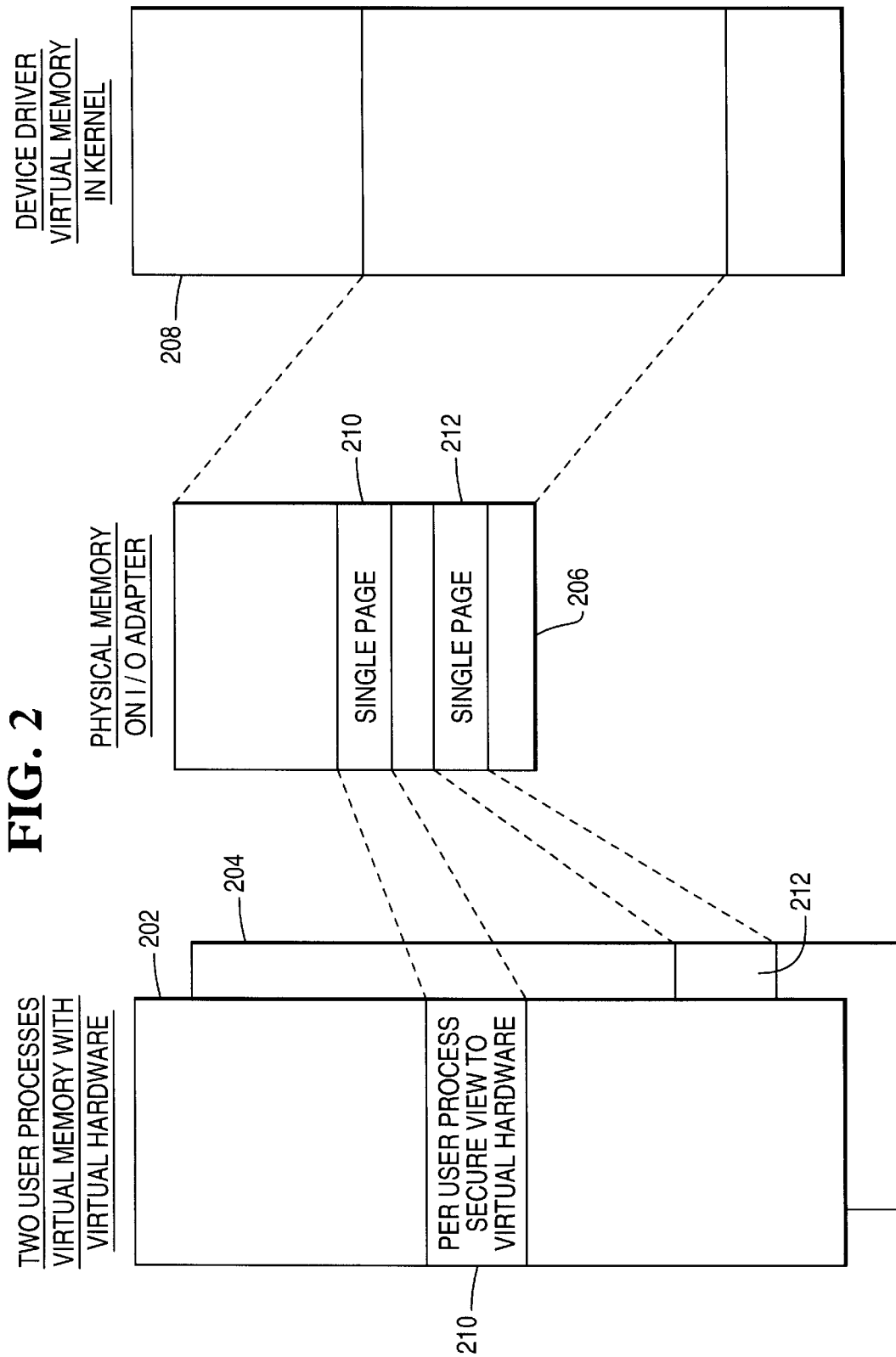


FIG. 3

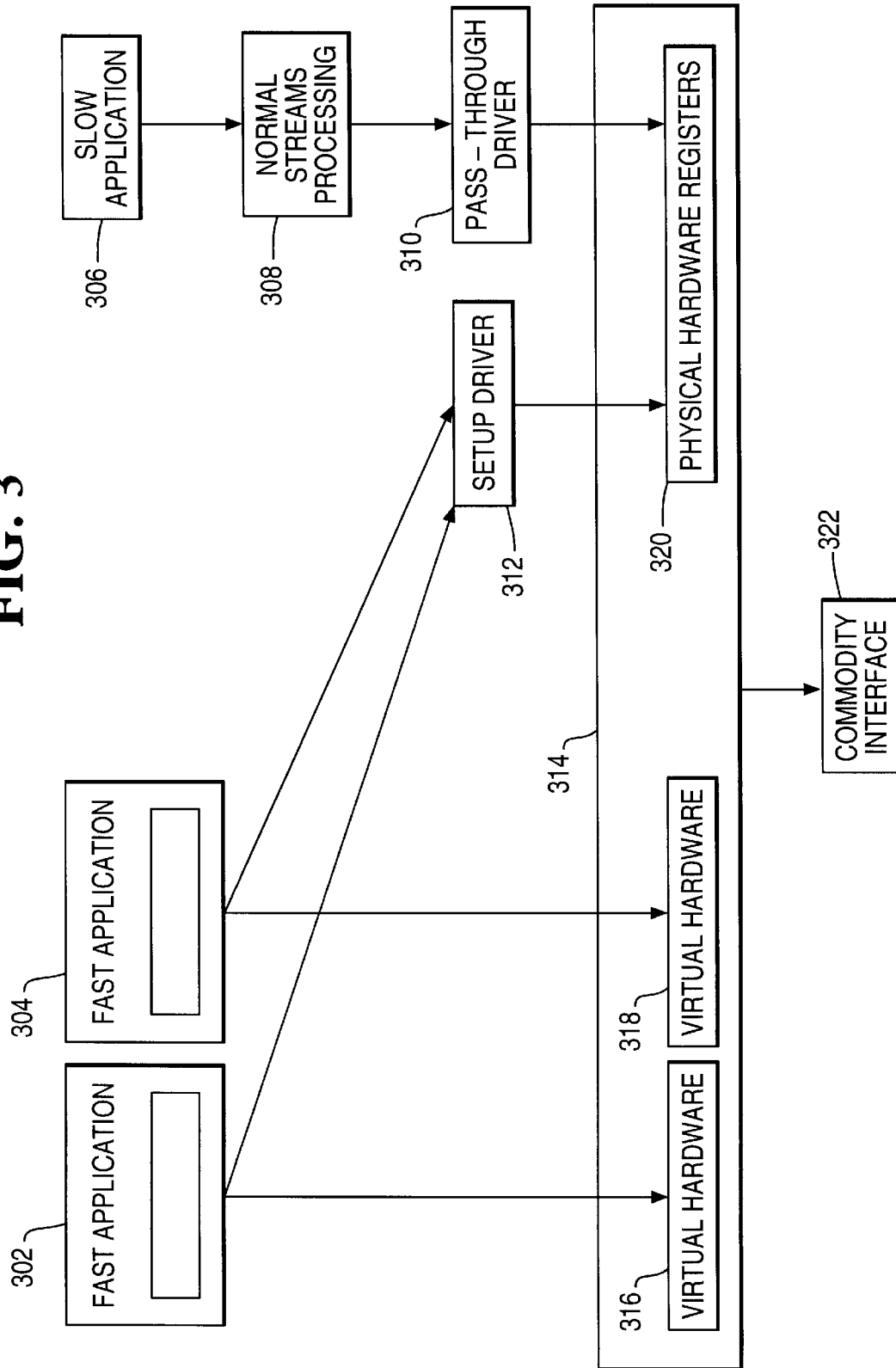
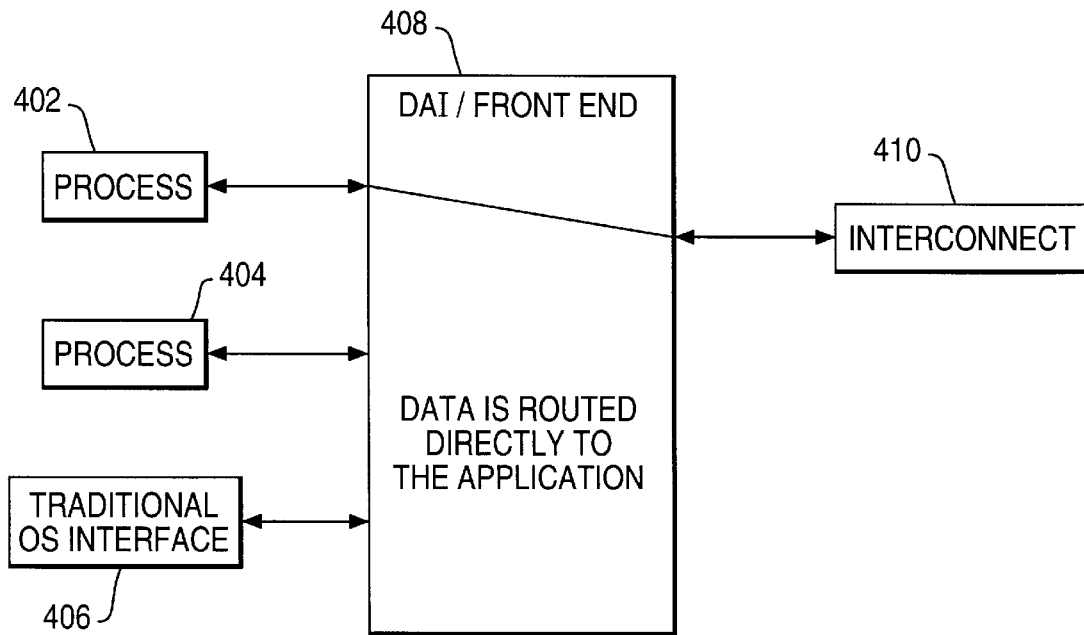


FIG. 4



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