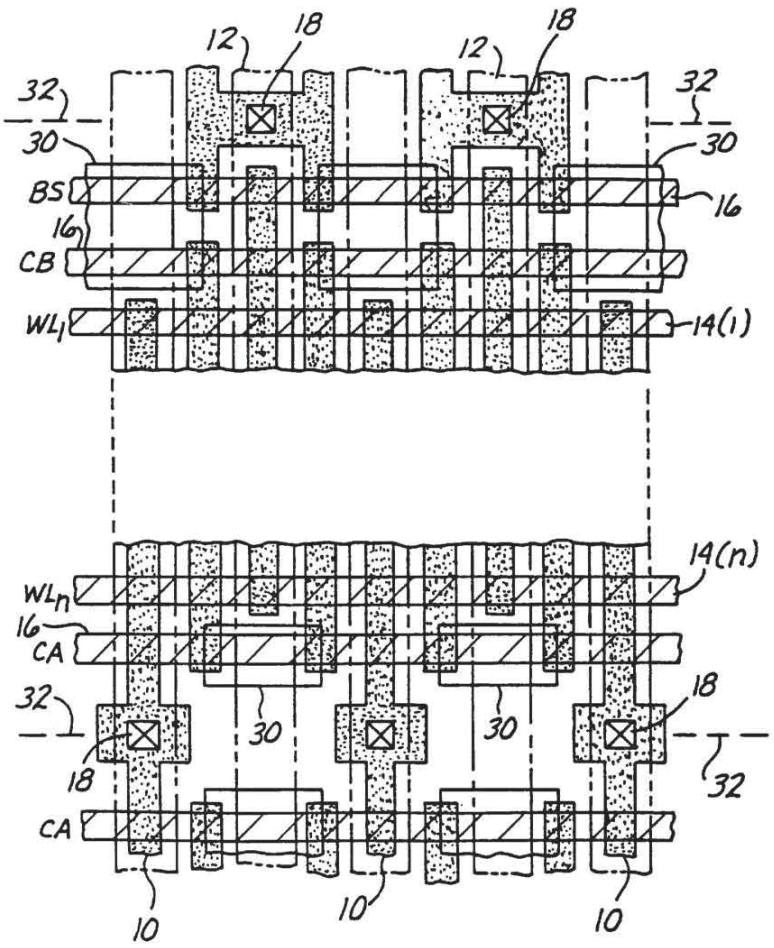

12
18
12
18
32
32
30
30
BS
16
16
CB
WL1
14(1)
14(n)
WLn
16
CA
32
18
30
30
18
32
18
CA
10
10
10

Fig. 1

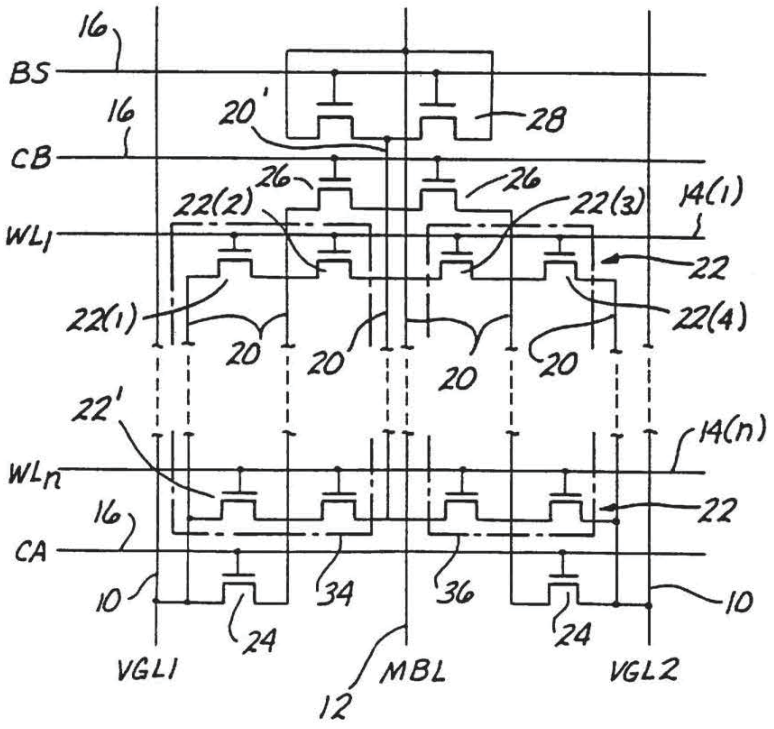

16
BS
16
CB
20'
28
26
26
22(2)
22(3)
14(1)
WL1
22
22(1)
22(4)
20
20
20
20
22'
14(n)
WLn
16
22
CA
10
34
36
10
24
24
VGL1
MBL
VGL2
12

Fig. 2

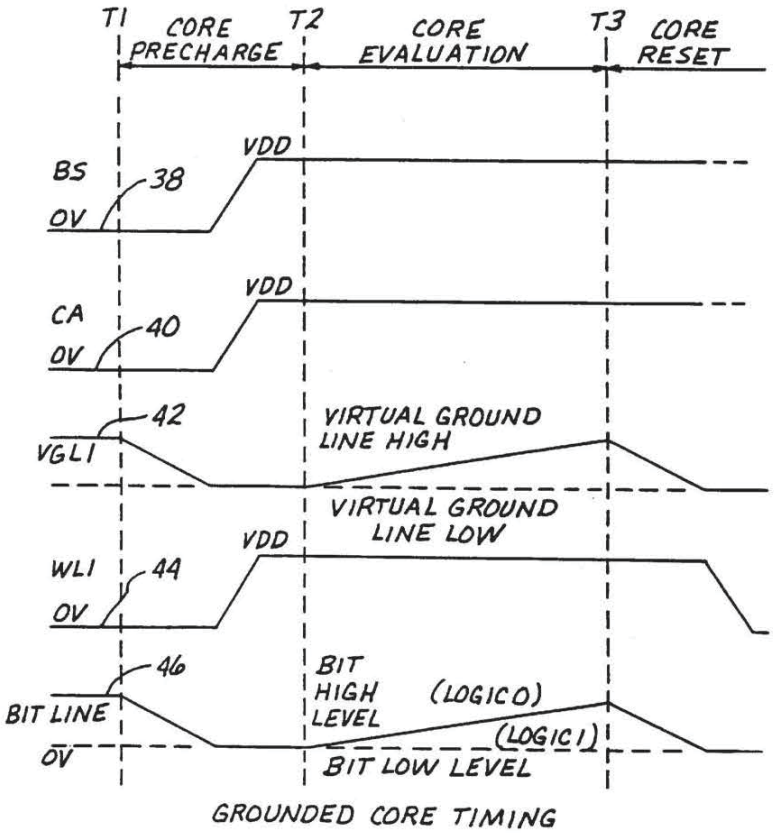

T1
CORE PRECHARGE
T2
CORE EVALUATION
T3
CORE RESET
BS
VDD
38
0V
CA
VDD
40
0V
42
VGLI
VIRTUAL GROUND LINE HIGH
VIRTUAL GROUND LINE LOW
WLI
VDD
44
0V
46
BIT LINE
BIT HIGH LEVEL
(LOGIC 0)
(LOGIC 1)
0V
BIT LOW LEVEL
GROUNDED CORE TIMING

Fig. 3

Fig. 4

LOGIC ZERO MAXIMUM VOLTAGE
MAIN BIT LINE
GROUNDED CORE

	CORE FETS ON WL1				MAXIMUM VOLTAGE
	22(2)	22(1)	22(3)	22(4)	MAIN BIT LINE 12
1	C	IC	IC	IC	VGL1
2	C	IC	IC	C	VGL1
3	C	IC	C	IC	0.46 VGL1
4	C	IC	C	C	0.38 VGL1
5	C	C	IC	IC	VGL1
6	C	C	IC	C	VGL1
7	C	C	C	IC	0.53 VGL1
8	C	C	C	C	0.46 VGL1

C: LOW THRESHOLD VOLTAGE
IC: HIGH THRESHOLD VOLTAGE
VGL1: VIRTUAL GROUND LINE 1 VOLTAGE = 2 VOLT
VGL2: VIRTUAL GROUND LINE 2 VOLTAGE = GROUND

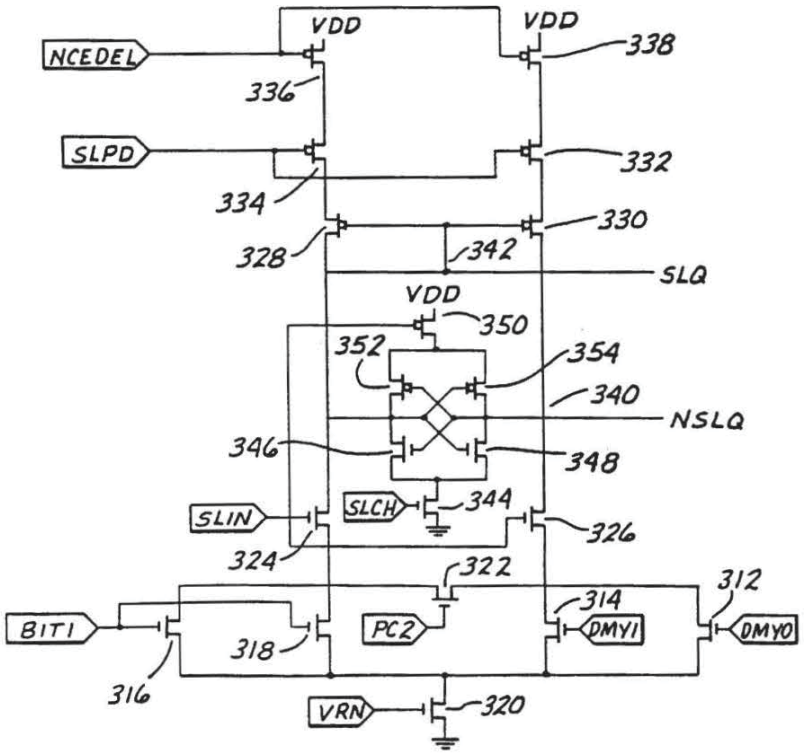

VDD
VDD
NCEDEL
338
336
SLPD
332
334
330
328
342
SLQ
VDD
350
352
354
340
NSLQ
346
348
SLIN
SLCH
344
326
324
322
312
314
BITI
PC2
DMYI
DMYO
318
316
VRN
320

Fig. 5

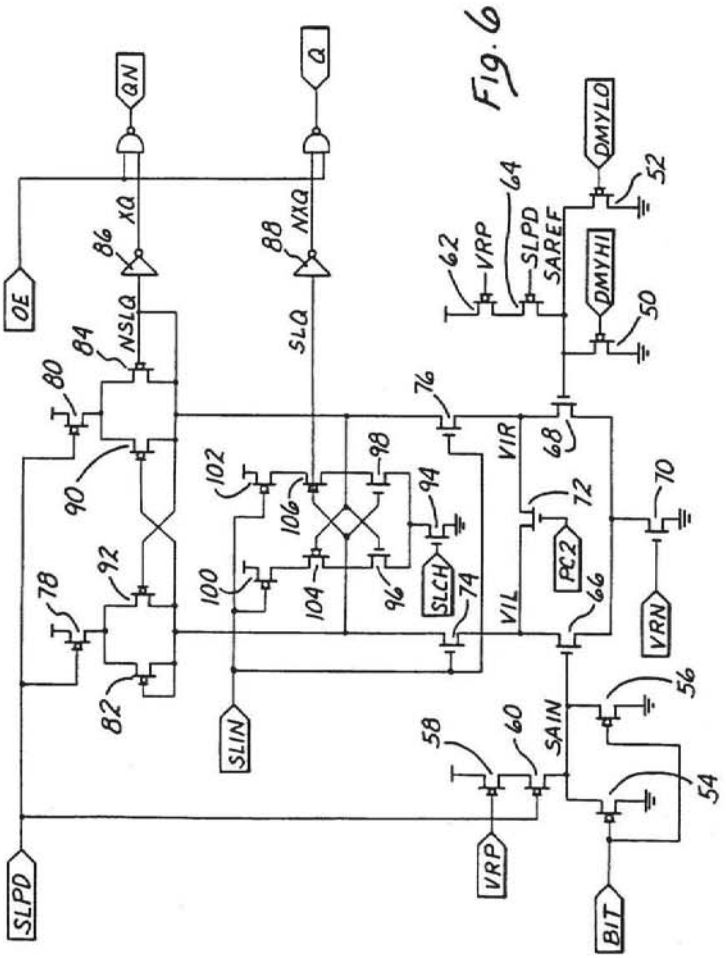

QN
Q
OE
XQ
NXQ
NSLQ
SLQ
SLPD
SLIN
SLCH
VRP
VIR
VIL
PC2
VRN
SAIN
BIT
DMYLO
DMYHI
SAREF
80
82
84
86
88
90
92
94
96
98
100
102
104
106
50
52
54
56
58
60
62
64
66
68
70
72
74
76
78

Fig. 6

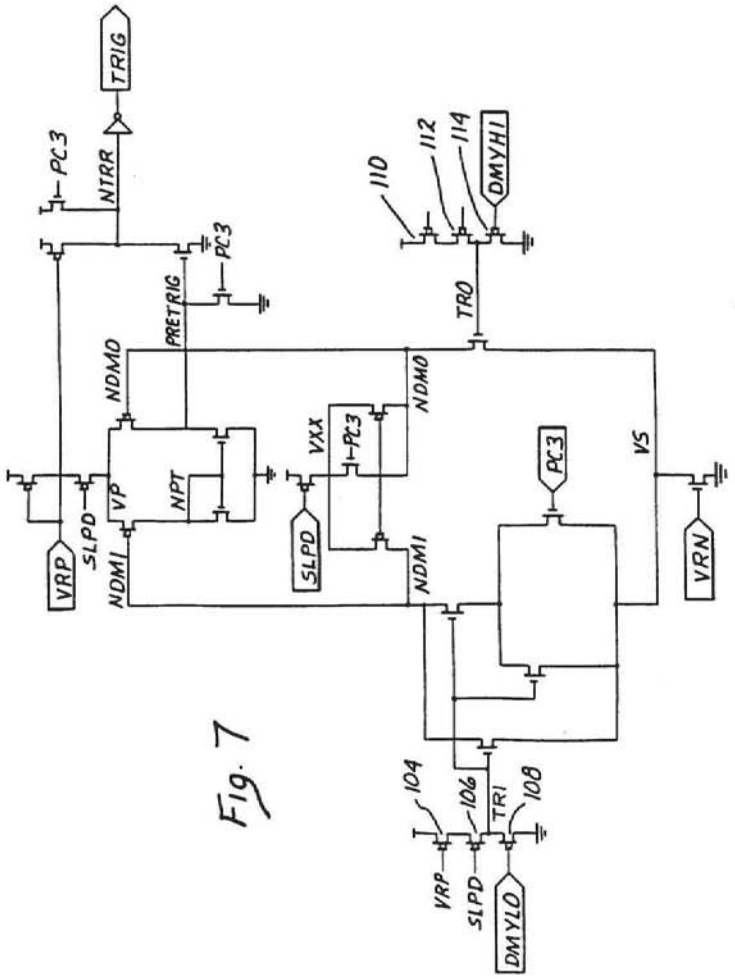

TRIG
PC3
NTRR
PC3
PRETRIG
110
112
114
DMYH1
TRO
NDM0
NDM0
VXX
PC3
PC3
VS
NPT
VP
SLPD
SLPD
VRP
NDM1
NDM1
VRN
104
106
TRI
108
VRP
SLPD
DMYLO

Fig. 7

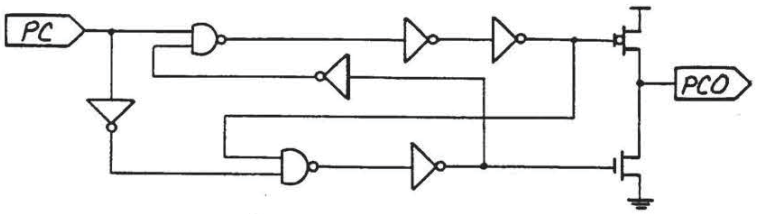
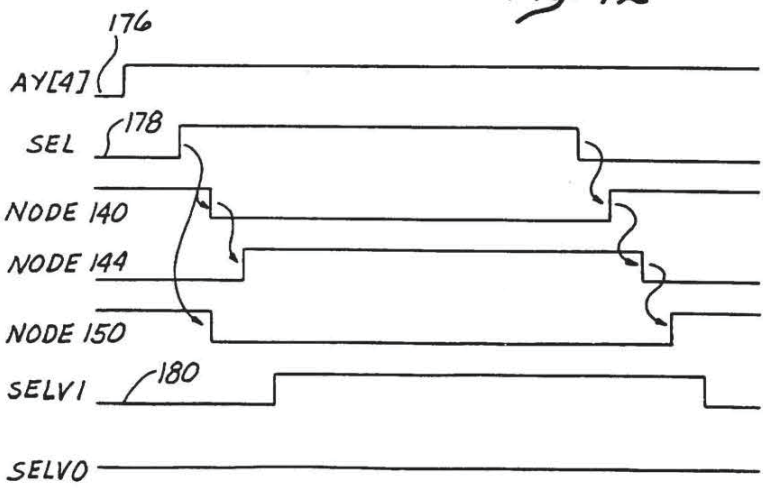

PC
PCO

Fig. 8

Fig. 12


176
AY[4]
178
SEL
NODE 140
NODE 144
NODE 150
180
SELV1
SELV0

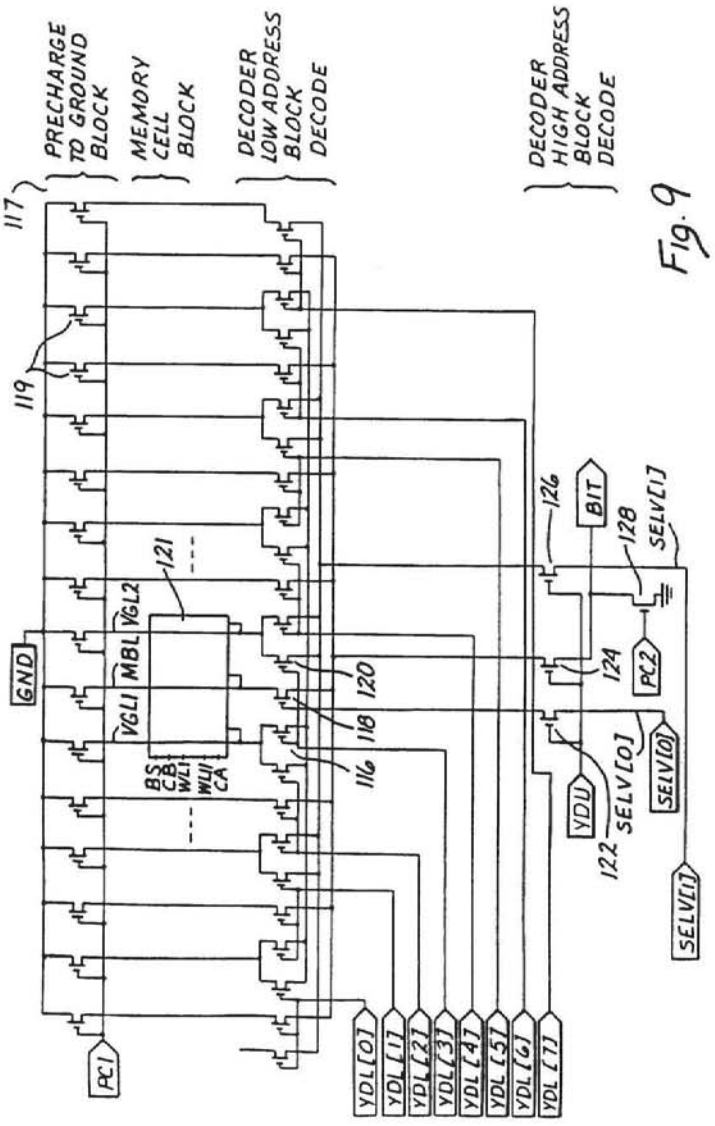

PRECHARGE TO GROUND BLOCK
MEMORY CELL BLOCK
DECODER LOW ADDRESS BLOCK DECODE
DECODER HIGH ADDRESS BLOCK DECODE
117
119
121
126
BIT
128
SELVL[1]
GND
VGL1
MBL
VGL2
120
118
116
124
PC2
BS
CB
WL1
WLi
CA
YDLi
122
SELVL[0]
SELVI[0]
PC1
YDL[0]
YDL[1]
YDL[2]
YDL[3]
YDL[4]
YDL[5]
YDL[6]
YDL[7]
SELVI[1]

Fig. 9

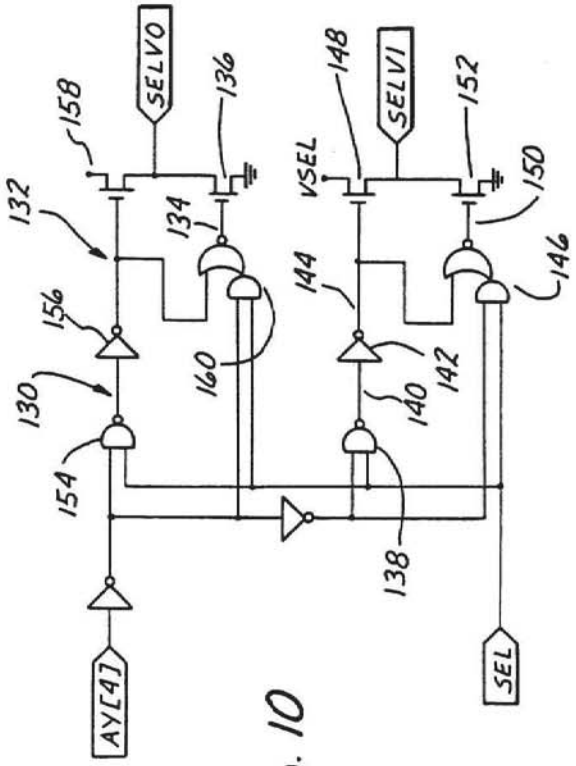

SELV0
158
136
148
SELV1
152
VSEL
132
134
150
144
146
156
160
142
130
140
154
138
AY[4]
SEL

Fig. 10

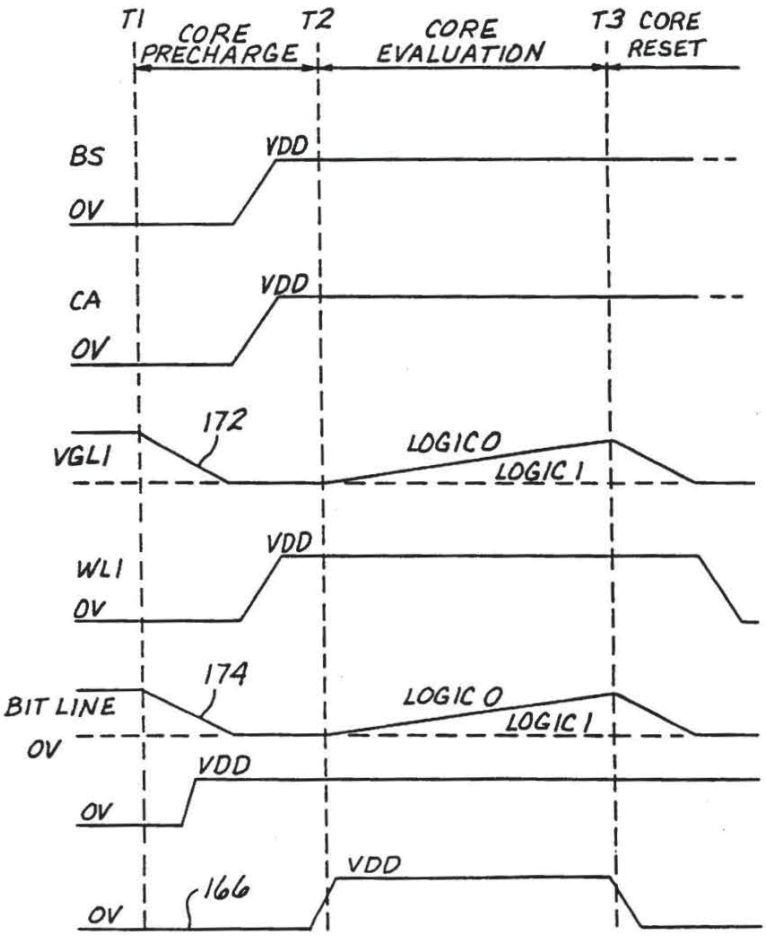
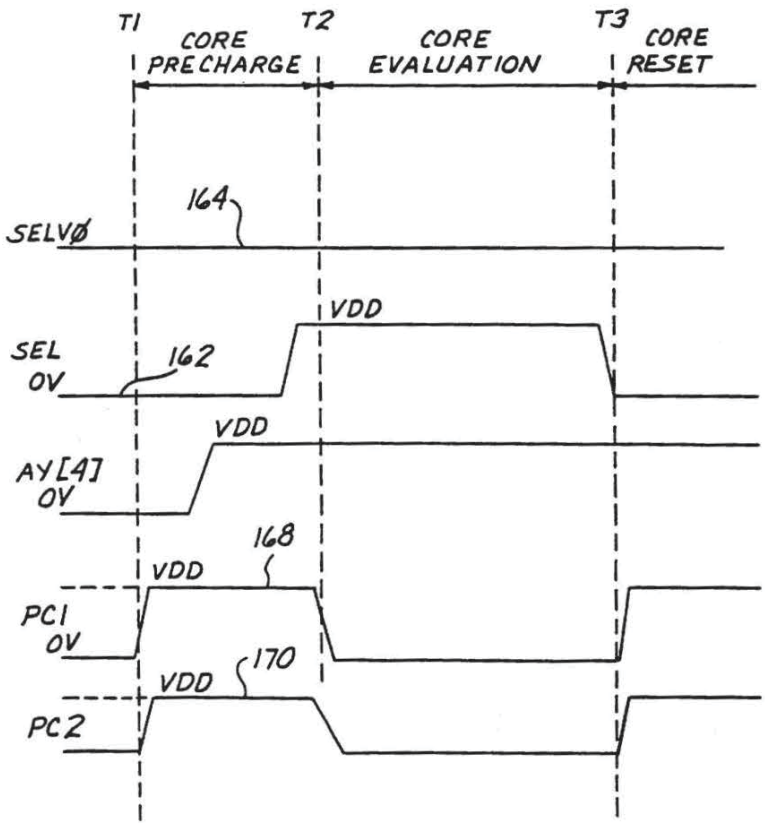

T1
CORE PRECHARGE
T2
CORE EVALUATION
T3 CORE RESET
BS
VDD
0V
CA
VDD
0V
172
VGL1
LOGIC 0
LOGIC 1
VDD
WL1
0V
174
BIT LINE
LOGIC 0
LOGIC 1
0V
VDD
0V
VDD
166
0V

Fig. 11a

Fig. 11b


T1
CORE PRECHARGE
T2
CORE EVALUATION
T3
CORE RESET
164
SELVØ
VDD
SEL
0V
162
VDD
AY[4]
0V
168
VDD
PC1
0V
170
VDD
PC2

DRIVER CIRCUIT FOR ADDRESSING CORE MEMORY AND A METHOD FOR THE SAME

RELATED APPLICATIONS

This is a divisional of application Ser. No. 08/487,841 filed on Jun. 7, 1995, U.S. Pat. No. 5,594,696, which is a continuation in part of application Ser. No. 07/912,112 entitled VLSI Memory with Increased Memory Access Speed, Increased Memory Cell Density and Decreased Parasitic Capacitance, filed on Jul. 9, 1992, which issued as U.S. Pat. No. 5,241,497, and which in turn is a file wrapper continuation of application Ser. No. 07/538,185 filed on Jun. 14, 1990, and now abandoned. This application is also a continuation in part of application Ser. No. 08/016,811, entitled Improvements in a Very Large Scale Integrated Planar Read Only Memory, filed on Feb. 11, 1993, which issued as U.S. Pat. No. 5,459,693. Each of the foregoing referenced parent applications are explicitly incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to the field of semiconductor memories and in particular to memory cores for read only memories (ROM, EPROM) or flash memories (EEPROM). Specifically, the invention relates to improvements in a method of precharging a memory core, sensing of the data lines in a memory core, and address decoding of the memory core.

2. Description of the Prior Art

Grounded Memory Core Design and Methodology

Architectures for very large scale integrated (VLSI) ROMs using virtual ground lines and diffusion bits lines to access banks of core cells are well known Descriptions of such architectures can be found in Okada, et.al. "18 *Mb ROM Design Using Bank Select Architecture,*" Integrated Circuits Group, Sharp Corp. However, such architectures are subject to several limitations and drawbacks as a discussed in the parent applications of this application and as are implicitly further detailed in the brief summary below wherein the improvements of the invention of the prior art and over the art of the parent application are explained.

Differential Sense Amplifier

Although not prior art, the parent application shows a sense amplifier approach using a current mirror. A schematic drawing of this previous sense amplifier is presented in FIG. **21** of the parent, which is reproduced here as FIG. **5**, since many of the improvements of the invention are best understood in comparison to the design in the parent application.

Both approaches use the same clocking signals and have the same timing. Also, both approaches amplify voltage differences of about 0.15 volts. The previous design amplifies voltages that are close to 2.0 volts with differences of about 0.15 volts.

The current mirror approach used in the previous design loads the differential amplifier output nodes with an unbalanced capacitive load. This unbalanced load favors one side of the latch over the other side of the latch. It would be possible to add capacitance to the previous design to balanced the nodes, but extra capacitance slows the latch and reduces the transient response of the latch.

Because of the small difference in voltages being sensed, small imbalances in the previous design of the differential amplifier may have a large enough effect to cause the differential amplifier to fall into the wrong state.

Virtual Ground and Bit Line Decoder

A design for a virtual ground and bit line decoder is described in the copending parent application in connection with FIGS. **18–20** (N387). Another design for a virtual ground and bit line decoder is shown in copending application N051-D in connection with FIGS. **1–2**.

A previous interlock method was used in the CMOS 4 Megabyte ROM circuit. A schematic diagram of a previous interlock method is presented in FIG. **8**.

The designs in the parent application both show approaches to decoding virtual ground lines and bit lines in a ROM. These previous decoder circuits are similar to the present decoder circuit, but the methods of decoding are different as will be described below.

The interlock method shown in FIG. **8** is an example of a previous interlock method. The present interlock method is an improvement of this design.

BRIEF SUMMARY OF THE INVENTION

Grounded Memory Core Design and Methodology

The memory core design of the invention is diagrammatically shown in the chip layout depiction of FIG. **1** and in the corresponding schematic of FIG. **2**. The operation of the bit lines and virtual ground lines of the circuit of the invention as shown in FIGS. **1** and **2** is very different from that described in the copending parent of this application. The operation of the polysilicon word lines, WL1–WLn, or the polysilicon select lines BS, CA, and CB are the same as described in the parent, which is expressly incorporated herein by reference, and therefore will not be described in a detail greater than necessary to provide contextual support in this specification.

There are at least five separate improvements in operation for the invention. First, the bit lines and virtual ground lines are all precharged to ground instead of being precharged to an internal low supply voltage of about 2 volts. In the parent application, the internal low voltage supply or precharge voltage is referred to as VPC. The VPC voltage is not required for the invention.

Second, the operation of the virtual ground lines in the parent was to first precharge all virtual ground lines to VPC, then select one of the two virtual ground lines for the selected bit and switch it from VPC to ground.. The second virtual ground line for the selected bit remained floating at the VPC voltage level.

In the invention, both of the two virtual ground lines are selected for the selected bit and both selected virtual ground lines are driven to ground during the precharge phase. At the top of the memory array, all virtual ground lines in the memory array are precharged to ground during the precharge phase. Next, during the sensing phase, the operation of the two virtual ground lines for the selected bit is changed to selectively hold one virtual ground line at ground and switch the second virtual ground line to a positive voltage. This is accomplished by means of a modified virtual ground line decoder and driver which are new with the invention.

Third, the operation of the bit lines in the prior art is to precharge all bit lines to VPC, and the then the selected bit line is discharged toward ground if the selected memory core FET is programmed with a low threshold voltage. If the selected memory core FET is programmed with a high threshold voltage, the bit line remains floating at the VPC voltage level.

In the invention, all bit lines are precharged to ground during the precharge phase. In the following sensing phase,

the selected bit line is driven positive by the selected memory core FET if it is programmed with a low threshold voltage. If the selected memory core FET is programmed with a high threshold voltage, the bit line remains floating at the ground level, or it may be held at ground by means of the second virtual ground line, which is held at ground, and low threshold core FETs, adjacent to the selected core FET, which are connected to the selected word line.

Fourth, a core FET programmed with a low threshold voltage is used to define a logic zero at the ROM output, and a core FET programmed with a high threshold voltage is used to define a logic one at the ROM output. By these definitions, the total diffusion capacitance on a virtual ground line is minimized when the memory cells connected to the line are programmed with more logic zeros than logic ones. The definitions take advantage of the fact that a core FET programmed with a low threshold voltage, a logic zero, has a significantly lower diffusion junction capacitance. Also, the definitions take advantage of the fact that unused code space in a ROM code pattern is usually filled with logic zeros, and that some ROM code patterns, like a font code for generating alphanumeric characters, have more logic zeros than logic ones in the total code pattern.

Fifth, the memory core as illustrated in FIG. **2** is not the only core circuit which can be used in the grounded core operating mode defined by the current invention. Other memory core designs which are compatible with the following circuit functions can be used, such as:

1) a voltage sensing or current sense amplifier;

2) a virtual ground line decoder circuit which selects both virtual ground lines VGL**1** and VGL**2** associated with the selected main bit line bit line;

3) a virtual ground line driver circuit to drive both of the two selected metal virtual ground lines, and if a precharge phase is used, both of the two selected metal virtual ground lines are driven to precharge ground level, then, during the sensing phase, one of the two metal virtual ground lines is held at ground and the other of the two metal virtual ground lines is switched to a voltage source; and

4) If a precharge phase is used, a precharge circuit is used to drive all metal virtual ground lines and metal bit lines to ground during the precharge phase. During the sensing phase, the precharge circuit is turned off.

Changing the operation of the memory core from the protocol described in the above referenced parent application to that of the invention provides significant advantages. First, the low voltage supply, VPC, is eliminated. Some ROMS, having 8 megabits or more, may have a standby current specification of 100 microamperes maximum from the VDD supply voltage. Prior art technology of maintaining an 8 megabit memory core at the VPC voltage during standby is impractical due to the junction leakage current drawn by the memory core arrays in the ROM.

Using a memory core precharged to ground eliminates VPC and resolves the standby junction leakage current problem. Using a memory core without a precharge phase and with current sensing as defined by the invention eliminates VPC and resolves the standby junction leakage current problem.

Second, in the invention the selected bit line is driven positive by the selected memory core FET if it is programmed with a low threshold voltage. The current from the selected core FET supplies the current to charge the bit line capacitance. It also supplies the selected memory core sector junction leakage current and supplies charge to compensate for negative noise voltage capacitively coupled to the bit line from the core precharge clocks turning off.

In the designs described in the parent application referenced above, the bit line may remain floating at the VPC voltage level during the core sensing time, if the selected core FET is programmed with a high threshold voltage. To supply the selected memory core sector junction leakage current, and to supply charge to compensate for negative noise capacitively coupled to the bit line, a circuit, such as the one shown in FIG. **4** of the parent application is necessary.

This type of circuit is not needed in the invention. Elimination of this circuit provides a significant improvement in the sensing performance of the invention. The circuit provides a small pull-up current to the selected bit line to compensate for both negative capacitively coupled noise and core junction leakage to the grounded memory substrate. When a selected memory cell switches the bit line toward ground, the memory cell must also switch the small pull-up current to ground. The "bit-low" switching time and voltage level is achieved more easily in the invention than in prior types of designs for ROMS using this type of circuit.

Third, a ROM utilizing the invention can operate with a VDD supply voltage of 3 volts because the memory core is precharged to ground. Prior designs of ROMS with a memory core precharged to a low supply voltage, such as VPC which is about 2 volts, require an operating VDD supply voltage more than 1.5 volts greater than VPC for operation of the precharge clocks, polysilicon word lines, and polysilicon sector select lines in the memory core.

Fourth, a ROM utilizing the current invention can precharge the memory core to ground, the precharge voltage level, in significantly less time than required for ROMS with the memory core precharged to a low supply voltage, such as VPC, which is about 2 volts. The current invention utilizes an NFET with a grounded source for switching the memory core virtual ground lines and main bit lines to ground. This NFET has the full VDD voltage applied from the gate terminal to the source terminal during the entire precharge time. The prior designs utilize an NFET in a source follower configuration for switching the memory core virtual ground lines and main bit lines to a low voltage such as VPC. With this configuration, the voltage applied from the gate terminal to the source terminal, which is connected to VPC, decreases during the precharge time. This increases the required precharge time, and requires an operating VDD supply voltage more than 1.5 volts greater than VPC for minimizing the precharge time to VPC.

The invention is an improvement in a memory having a memory core with a plurality of memory cells and a predetermined memory core substrate voltage. The memory cells are accessed at least in part by selection of corresponding bit lines and virtual ground lines coupled thereto. The improvement comprises precharging circuitry for precharging the virtual ground lines and bit lines in the memory core to the memory core substrate voltage. Virtual ground line and bit line decoder and precharging circuitry precharges previously selected virtual ground lines and bit lines in the memory core to ground. Virtual ground line driver circuitry first drives both selected virtual ground lines to ground during a precharge phase and then selectively drives one virtual ground line to ground and the second virtual ground line to a positive voltage level. Memory core junction leakage current from the virtual ground lines and bit lines in the memory core is reduced to zero when the memory core is precharged to the memory core substrate voltage. The need for an internal low voltage supply for a precharge level is elimi-

nated. VDD standby current and operating voltage level required for the memory is significantly reduced.

The time required to precharge the memory core to the precharged voltage level at the beginning of a memory read cycle is significantly reduced. The precharging circuitry, virtual ground line and bit line decoder and precharging circuitry, virtual ground line driver circuitry and the memory core provide the main bit line with bit-low level and bit-high level voltages which are negligibly affected by capacitively coupled negative noise voltages or by memory core junction leakage currents to the memory core substrate. The precharging circuitry, virtual ground line and bit line decoder and precharging circuitry, virtual ground line driver circuitry, and the memory core provide a positive current to the main bit line for providing a positive voltage defined as a logic zero level or bit-high level and a precharged zero voltage level to the main bit line for a logic one or bit-low level.

The improvement further comprises bit line voltage sensing circuitry to sense bit-low level and bit-high level voltages on the main bit line at high speed with a bit-high voltage level of at least 150 millivolts and with a bit-low level of approximately zero volts.

Each memory cell comprises a core FET. The core FET of at least one of the memory cells is programmed with a low threshold voltage defining a logic zero output. The precharging circuitry, virtual ground line and bit line decoder and precharging circuitry, virtual ground line driver circuitry, and the memory core for minimizing total diffusion capacitance on the virtual ground line coupled to the memory cells when the memory cells are programmed with more logic zeros than logic ones, and for reducing capacitance associated with the core FET programmed with a low threshold voltage due to minimized total diffusion capacitance.

The virtual ground line and bit line decoder and precharging circuitry precharges previously selected virtual ground lines and bit lines in the memory core to approximately zero voltage.

The invention is also an improvement in a method of operation of a memory having a memory core with a plurality of memory cells and a predetermined memory core substrate voltage. The memory cells are accessed at least in part by selection of corresponding bit lines and two associated virtual ground lines coupled thereto from a plurality of bit lines and associated virtual ground lines in the memory. The improvement comprises the steps of precharging the virtual ground lines and bit lines in the memory core to the memory core substrate voltage. A pair of the virtual ground lines is selected in the memory. Both selected virtual ground lines are driven to ground during a precharge phase. One of the selected virtual ground line is selectively driven to ground and the other one of the selected virtual ground line to a positive voltage level.

Differential Sense Amplifier

The parent application shows a similar sense amplifier approach using a current mirror instead of a cross coupled current source. A schematic drawing of this previous sense amplifier is presented in FIG. **21** of the parent, which is reproduced here as FIG. **5**, since many of the improvements of the invention are best understood in comparison to the design in the parent application.

Both approaches use the same clocking signals and have the same timing. Also, both approaches amplify voltage differences of about 0.15 volts. The previous design amplifies voltages that are close to 2.0 volts with differences of about 0.15 volts. The present design amplifies voltages that are close to ground with differences of about 0.15 volts. The use of voltage level shifters, a cross coupled current source and inverters is unique to the present design.

The present sense amplifier design amplifies voltage differences of signals that are about 0.15 volts. The previous sense amplifier design amplifies voltage differences of signals that are about 2.0 volts.

The idea of using a cross coupled current source instead of a current mirror is not limited to the present design. This idea will work equally well in the previous sense amplifier and may be used without the voltage level shifting circuitry.

The current mirror approach used in the previous design loads the differential amplifier output nodes with an unbalanced capacitive load. This unbalanced load favors one side of the latch over the other side of the latch. The cross coupled current source approach loads the differential amplifier with a balanced load. It would be possible to add capacitance to the previous design to balanced the nodes, but extra capacitance would slow the latch and reduce the transient response of the latch.

The voltage level shifters in the present design are important because they allow the differential amplifier to sense signals that are close to ground with a voltage difference of about 0.15 volts. The voltage level shifters also shift the signals to a voltage that increases the gain of the differential amplifier. In the previous design, the differential amplifier was limited to amplifying signals that were at the internal precharge voltage of the memory core, i.e. about 2.0 volts. By level shifting inputs to the differential amplifier from zero volts to about 2.2 volts, the differences of these level shifted signals can now be amplified with a conventional differential amplifier.

It is important to note that the use of level shifters is not limited to only sense amplifiers. FIG. **7** shows a timing circuit that employs voltage level shifting circuits and a differential amplifier.

It is very desirable to have a symmetric design in a differential amplifier.

The cross coupled current source approach is symmetric while the current mirror approach is not. Because of the small difference in voltages being sensed, small imbalances in the differential amplifier may have a large enough effect to cause the differential amplifier to fall into the wrong state. The idea of using symmetry to improve the balance of the sense amplifier extends beyond the design to the layout of the design. A symmetric and balanced layout may sense smaller voltage differences and operate faster than would otherwise be possible.

The cross coupled current source approach can provide more gain than the current mirror approach. The gain of the cross coupled current source is controlled by four FETs.

The present design uses two inverters to block half level signals from being outputted until the sense amplifier data has been latched. By blocking half level outputs of the differential amplifier, a race condition is eliminated and output enable signal, OE may switch sooner than would otherwise be possible.

The invention is an improvement in a detection circuit having an input signal which is sensed. The improvement comprises a level shifting circuit for receiving the input signal and for shifting the voltage of the input signal to a predetermined level to output a voltage shifted level of the input signal. The predetermined level is within an operative range of detection of the detection circuit.

The input signal sensed by the level shifting circuit has a voltage close to ground. The detection circuit in the operative range is capable of distinguishing signal level differences at least as small as about 0.15 volts so that input

signals at least as little as about 0.15 volts above ground are reliably sensed.

The level shifting circuit shifts the voltage of the input signal to the predetermined level within a wide range of selected voltages including the operative range of the detection circuit. The predetermined level is where the detection circuit has the most gain, speed and accuracy.

The detection circuit comprises a differential amplifier having two differential outputs and the detection circuit comprises a pair of cross coupled current sources to provide matched current sources to the differential amplifier. The pair of current sources are symmetric, balanced, have the same capacitive loading and the same impedance. The pair of cross coupled current sources initially provide two equal current sources, but become unmatched based on the output of the differential amplifier. The differential amplifier includes circuitry for providing positive feedback from the outputs to the pair of current sources to increase the gain and speed of the differential amplifier.

The pair of current sources have two cross coupled FETs and the gain of the cross coupled current source is controlled primarily by the two cross coupled FETs. A range of gains is provided to the differential amplifier by varying the width-to-length ratio of the two cross coupled FETs. The pair of current sources further comprise two FETs connected in parallel to the cross coupled FETs. The gain of the differential amplifier also is further controlled by varying the width-to-length ratio of the two parallel coupled FETs.

The improvement further comprises two inverters to block half-level outputs of the differential amplifier until both outputs of the detection circuit have been latched.

The invention is also an improvement in a method of detecting an input signal level the improvement comprising the steps of receiving the input signal, and shifting the voltage of the input signal to a voltage shifted output level. The voltage shifted output level is within an predetermined operative range of detection of a detection circuit. The voltage shifted output level is detected to distinguish the signal level of the input signal level.

Virtual Ground and Bit Line Decoder

The design described in the copending application, M387-D for the virtual ground and bit line decoder, and the present virtual ground and bit line decoder both multiplex a selected main bit line, mBL. The previous NMOS ROM decoder selects one virtual ground line and drives this line to ground. All other virtual ground lines are precharged to an internal low supply voltage of about 2 volts. The present design selects two virtual ground lines. These two lines are initially driven low. During the read cycle, one of the lines is driven high and the other line remains driven low. The virtual ground line that is driven high is determined by an address, AY[4].

Like the NMOS decoder described in copending application Ser. No. 08/016,811, entitled Improvements in a Very Large Scale Integrated Planar Read Only Memory, the CMOS virtual ground and bit line decoder multiplexes a selected main bit line and one virtual ground line. The CMOS decoder provides a better precharge than the NMOS decoder. In the CMOS design, PC**0** is an input to the addresses YDL[0–7] and YDU[0–7]. When PC**0** is high during core precharge, all the addresses YDL[0–7] and YDU[0–7] are high, all FETs in the decode are turned on, and all the virtual ground line and bit lines are precharged. This additional precharging technique is not used in the present design although this technique is compatible with the present design.

In comparison to the prior designs, the improved interlock method provides the same function with fewer gates. This method is inherently faster and uses less silicon die area because fewer gates are used.

In comparison to the previous NMOS ROM patent and the CMOS virtual ground and bit line decoder, the present decoder is designed for use with a memory core that is precharged to ground. The previous decoder was designed for use with a memory core that is precharged to a low voltage of about 2 volts. In the present design an additional decode is done by means of the SELV lines. Because this additional decode is done by means of the SELV lines, the present decoder uses fewer FETs and less area than would otherwise be possible.

Crowbar currents may be very large in inverters and logic gates with large FETs. When CMOS inverters and logic gates switch, there is a period of time where both the PMOS and the NMOS FETs are partially turned on. The current that flows through these FETs is called a "crowbar current". Crowbar current is normally not significant but can become very significant when large FETs are used. This interlock method avoids these crowbar currents.

The invention is an improvement in a method for decoding a plurality of virtual ground lines and bit lines in a memory comprising the steps of driving all virtual ground lines in the memory core low. Two virtual ground lines in a memory core are multiplexed by holding a selected first virtual ground line low and keeping a selected second virtual ground line low for memory core discharge, and by driving the selected second virtual ground line high for core evaluation. The core is then read or evaluated. All unselected virtual ground lines are kept floating during the step of evaluating the core. The second virtual ground line is then switched low for memory core discharge in preparation for subsequent core evaluation.

The improvement further comprising the step of precharging a BIT line to ground prior to the step of evaluating the core. The BIT line is selectively coupled to the bit lines in the memory.

The invention is also a decoder for producing two memory multiplexing signals, SELV**0** and SELV**1**, capable of driving a large capacitive memory load. The decoder comprises decode circuitry for selectively decoding an address signal to drive one of the two memory multiplexing signals, SELV**0** and SELV**1**, high and the other low. Drive circuitry generates the two memory multiplexing signals, SELV**0** and SELV**1**, in response to the decode circuitry. The drive circuitry is tristated.

The drive circuitry is comprised of a pair of two large FETs coupled in series. The memory multiplexing signals, SELV**0** and SELV**1**, are derived respectively from the coupling between one of the pair of the two large FETs. The drive circuitry comprises circuitry for turning each one of the two large FETs off before turning on the other one of the two large FETs in each of the pairs of FETs, so that one of the FETs of each pair will always be off when the other one of the pair of FETs is on.

The memory multiplexing signals, SELV**0** and SELV**1**, have a voltage level set by a decoder supply voltage, VSEL. The memory multiplexing signals, SELV**0** and SELV**1**, have the highest voltage level in the memory core. Voltage levels of the memory multiplexing signals, SELV**0** and SELV**1**, are set at a level low enough to avoid memory breakdowns in the memory core.

The invention is also an improved method of precharging a memory core having a plurality of virtual ground lines and main bit lines comprising the steps of precharging all of the virtual ground lines and main bit lines in the memory core to ground before the core is read through a precharge block

Two selected virtual ground lines are driven to ground before the core is read through precharge paths through the memory core independent of the precharge block.

The invention is still further a driver circuit for avoiding crowbar currents comprising two large FETs coupled in series. An output signal is derived from the coupling between the two large FETs. Circuitry is provided to turn each one of the two large FETs off before turning on the other one of the two large FETs, so that one of the FETs will always be off when the other one of the FETs is on.

The invention can be better visualized by turning to the following drawings, wherein like elements are referenced by like numerals.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a plan view of a chip layout of a memory core operated according to the invention.

FIG. **2** is a schematic of the memory core shown in FIG. **1**.

FIG. **3** is a timing diagram showing the waveforms of the control signals used to drive the memory core of FIGS. **1** and **2**.

FIG. **4** is a table of main bit line voltage values depending on the programmed states of memory cells in a row coupled to the main bit line.

FIG. **5** is a schematic of a sense amplifier used in the parent application.

FIG. **6** is a schematic of the sense amplifier of the invention.

FIG. **7** is a schematic of a timing circuit that employs voltage level shifting circuits and a differential amplifier.

FIG. **8** is a schematic drawing of a previous interlock method to avoid crowbar current.

FIG. **9** is a schematic of the virtual ground and bit line decoder circuit of the invention.

FIG. **10** is a schematic drawing of the interlock method to avoid crowbar current.

FIGS. **11***a* and *b* are a timing diagrams of the relevant decoder signals.

FIG. **12** is a timing diagram showing the function of the interlock method.

The various embodiments of the invention can now be understood by turning to the following detailed description.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Grounded Memory Core Design and Methodology

Consider now in detail the operation of the invention in a memory core schematically shown in FIG. **2**, and with the use of a voltage sensing sense amplifier circuit, modified virtual ground line decoder and driver which are described below. The invention incorporates a memory circuit having an array of addressable memory cells organized into blocks of memory cells. One block of cells is shown in FIG. **2**. A block is a segment of the core which is repeated in rows and columns to form the memory array. In the invention, a block is defined as shown in FIG. **2**. There are four columns of memory cells in a block. The word lines, CA, CB, and BS select one cell in the block to be connected to the metal bit line, or main bit line. A sector of memory is defined as a row of blocks placed across the memory core or array which have common word lines and BS, CA, and CB lines. The sector is repeated in n rows to form the complete memory core or memory array. A ROM can be partitioned into one or more memory cores.

CA, Column Select A, is a polysilicon line extending across the full width of a sector. It is the gate terminal of core FETs which connect specific diffusion bit lines in the block to each other. CB, Column Select B, is a polysilicon line extending across the full width of a sector. It is the gate terminal of core FETs which connect specific diffusion bit lines in the block to each other. BL is a diffusion line in the block, or sector, which is the drain or source terminal for four columns of core FETs and four column select FETs controlled by CA or CB. The bit line signal from one of the sectors in the memory array is coupled to a metal bit line by block select BS. BL may refer to the diffusion or metal line. The metal bit line may be referred to as mBL, or main bit line.

WL, Word Line, is a polysilicon line extending across the full width of a sector. It is the gate terminal of one row of programmable core FETs in the sector. BS, Block Select, is sometimes defined as Bank Select and is a polysilicon line extending across the full width of a sector. It is the gate terminal of the core FETs which connect a diffusion bit line in a block to the metal bit line, or main bit line mBL.

VGL, Virtual Ground Line, is a diffusion bit line in the block of memory cells shown in FIG. **2**. There are two diffusion bit lines which connect to the drain or source terminals for two columns of core FETs and for two column select FETs controlled by CA. Each of the two diffusion lines is connected to one of two metal buses which are also connected to corresponding diffusion lines in each block within a column of blocks in the memory array. Each of these two metal lines is defined as a virtual ground line.

The array of cells includes a plurality of metal virtual ground lines **10**, main bit lines **12**, polysilicon word lines **14(1)**–(n), and polysilicon select lines **16**. Each of polysilicon word lines **14**(i), and polysilicon select lines **16** extend through each row of blocks of memory cells, or sector. Each of metal virtual ground lines **10** and main bit lines **12** extend through each column of blocks of memory cells. The metal lines run straight as, shown in FIG. **1**, for an optimum layout design. The design comprises of a plurality of contacts **18** connecting metal virtual ground lines **10** and main bit lines **12** to corresponding ones of contacts **18** at each the end of each the blocks.

A decoder circuit selects a column of the blocks and couples a virtual ground line driver to the selected pair of metal virtual ground lines **10** and a sense amplifier to a main bit line **12** in the selected column of blocks. During the precharge phase, these circuits drive both of the two selected metal virtual ground lines **10** to ground, then, during the sensing phase, one of two metal virtual ground lines **10** is held at ground and the other of the two metal virtual ground lines is switched to a voltage source.

Each block has a first and a second end. The virtual ground line contacts **18** are disposed solely at one end of the block with main bit line contact **18** disposed solely at the opposite end of the block. A second block of memory cells identical in architecture to the first block of memory cells is laid out with mirror symmetry relative to an imaginary line perpendicular to the virtual ground lines and disposed at one end of the first block of memory cells. Contacts **18** with main bit line **12** and virtual ground lines **10** to the first block of memory cells are used in common with the mirror symmetrical second block of memory cells.

The plurality of memory cells **22** in the block is logically organized in columns. The columns of memory cells **22** are coupled together by diffusion bit lines **20**, which cell **22** in this case is comprised of a single FET. Each column has two

corresponding diffusion bit lines **20** disposed along the length of the block of memory cells **22**. Memory cells **22** are arranged and configured into four columns with the center bit diffusion line **20'** shared by the second and third columns of memory cells **22**. Two virtual ground lines **10** are symmetrically disposed relative to the center diffusion bit line **20'**. A first circuit **24** controlled by CA is disposed at one end of each block for selectively coupling the two diffusion bit lines **20** for the first column of memory cells together and two diffusion bit lines **20** for the fourth column of memory cells together. A second circuit **26** controlled by CB is disposed at the opposite end of each block for selectively coupling the center bit diffusion line **20'** with the two adjacent bit diffusion lines **20**.

As a result of the location of first and second circuits **24** and **26**, the length of the circuit path of a signal read from any one of the addressed memory cells through bit diffusion lines **20** does not exceed in aggregate substantially more than one length of the memory block. Parasitic capacitance is avoided, memory access speed is increased, and the capacity for memory cell density is increased.

The general structural architecture of the memory core now having been reviewed, consider the detailed description of operation of the grounded memory core of the invention. As shown in the schematic in FIG. **2**, main bit line **12** is coupled through core FETs **28** to a center bit line **20'**. Two memory cells **22**, for example particularly denoted by reference numeral **22(2)**, are coupled in series with each other in the memory core to form a pair. Other pairs of core FETs **22** are coupled in parallel between center line **20'** to the outer diffusion bit lines **20** which are connected to virtual ground lines **10**. The gates of memory cells **22** like cells **22(2)** are coupled to respective word lines **14(1)** through **14**(n). Column select core FETs **26** are coupled in parallel with N memory cells on each side of center bit line **20'**. Column select core FETs **24** are coupled in parallel with N memory cells which are connected to outer diffusion bit lines **20**.

Bit lines **20** and **20'** in FIG. **2**, are n-type diffusion wires while main bit line **12** and virtual ground lines **10** are metal wires of aluminum. Referring to FIG. **1**, word lines **14(1)** through **14**(n) and the column select signal lines **16**, CA, CB, and BS, are polysilicon wires. The metallic contacts **18** are denoted by the squares containing an X. Regions **30** denote ion-implanted regions. Threshold voltages in ion-implanted regions **30** exceeds the supply voltage so that core FETs disposed in regions **30** are not turned on even if the gate voltage goes to a logic high.

Metal contacts **18** connecting the diffusion wiring to main bit line **12**, and metal contacts **18** connecting the diffusion wiring to virtual ground lines **10** are positioned at opposite ends of the memory cell blocks as best depicted in FIG. **1**. Therefore, the resistance of the diffusion wiring elements from main bit line contact **18** to a virtual ground line contact **18** remains constant regardless of the position of selected memory cell **22(2)**, because the resistance corresponds to the distance between metal contacts **18** for main bit line **12** and virtual ground lines **10**. The memory layout is designed so that the memory cell blocks are mirror symmetrical about line **32** with respect to transverse or horizontal wires or lines (not shown) connecting contacts **18**. As a result, the number of contacts **18** in the array is reduced by fifty percent as compared to conventional layout. As a further consequence, the capacitance and junction leakage current parasitics due to main bit line contacts **18** is reduced by fifty percent, thereby increasing switching speeds.

Consider the operation of the grounded memory core with a voltage sensing sense amplifier. Referring to FIG. **2**, a column select signal, CA, is switched to a logic high level in order to select memory cells **22** in the second and third columns immediately adjacent to a main bit line **12** shown in the middle of the schematic in FIG. **2**. Column select signal, CA, turns on transistors **24** to short each outer pair of diffusion bit lines **20** together in a pairwise fashion. Outermost diffusion bit lines **20** are connected to virtual ground lines **10**, VGL**1** and VGL**2**.

When column select signal, CB, is switched to a logic high level, it shorts the innermost diffusion bit lines **20** to center bit line **20'** through transistors **26**. This will select the first and fourth columns in the array of FIG. **2**.

In other words, signal CA will select the second and third columns, while column select signal CB, will select the first and fourth columns, the columns being ordered and numbered from left to right in the array of FIG. **2**. For proper addressing, only one of these two signals, CA or CB, is logically high at the same time.

All left block cells, denoted by dotted outline **34**, are selected by switching the left virtual ground line **10** in FIG. **2** to a positive voltage level and holding the opposing or right virtual ground line **10** in FIG. **2** to the precharged ground level. In such an instance, the cells within block **34**, as opposed to the symmetrically disposed block of memory cells **36**, are read out while those in block **36** are not.

For the grounded memory core, the positive voltage level on a virtual ground line **10** is approximately two volts in amplitude at the end of the sensing phase. A bit-high level on the main bit line **12** is a positive voltage of approximately 150 millivolts in amplitude at the end of the sensing phase. A bit-line-low level is the precharge level of ground, or zero volts.

In order to select, for example, cell **22(2)**, block select signal, BS, line **16**, goes to a logical high selecting the block shown in FIG. **2**. See FIG. **3** for the signal wave forms for the example of selecting cell **22(2)**. The interval between T**1** and T**2** is the precharge cycle, between T**2** and T**3** the core evaluation cycle, and after T**3** the core reset cycle. Signal BS, on line **16**, is coupled to the gates of two transistors **28**. When switched high as shown on line **38** in FIG. **3**, BS couples main bit line **12** to center bit line **20'** of the cell matrix block. Column select signal, CA, is a logical high as shown on line **40** in FIG. **3**, and column select line, CB, is a logical low, thereby selecting the second and third columns. The leftmost virtual ground line **10** in FIG. **2**, VGL**1**, goes after time T**2** to a positive voltage as shown in FIG. **3**. Rightmost virtual ground line **10** in FIG. **2**, VGL**2**, is held at the precharged ground level thereby selecting the second column of cells and deselecting the third column of cells. Word line **14(1)** switches to a logical high as shown on line **44** of FIG. **3** with each of the remaining word lines **14(2)** to **14**(n) to a logical low thereby reading cell **22(2)** as shown on line **46** of FIG. **3**.

Assume the selected core FET **22(2)**, is programmed with a low threshold voltage. The current transmission path through the block of memory cells begins with the leftmost virtual ground line **10** and ends with the main bit line **12**, or mBL. The current flows from leftmost line **10** to the left outermost diffusion line **20** in FIG. **2**. See line **42** of FIG. **3** for the voltage wave form on VGL**1**, or line **10**. With core FET **24** controlled by CA, the current flows through FET **24** to the left innermost diffusion bit line **20**. The current flows along left innermost line **20** to the drain of the selected core FET **22(2)** and through core FET **22(2)** to center diffusion bit line **20'**. The current then flows through the two parallel core FETs **28** to the main bit line **12**, or mBL The approximate voltage wave form on line **12**, mBL, is shown on line **46** in FIG. **3**.

The magnitude of the resultant voltage on the main bit line **12** varies significantly, and is largely dependent upon the programmed threshold voltages of core FETs **22(1)**, **22(3)** and **22(4)** in the same row of the core as the selected cell **22(2)** in FIG. **2**. These FETs have gates connected to WL**1**, line **14(1)**, and may also be turned on when FET **22(2)** is selected. FIG. **4** shows the maximum voltage on the main bit line **12** as a function of the programmed threshold voltages of core FETs **22(1)** through **22(4)**. There are eight combinations for the programmed threshold voltages of the three core FETs **22(1)** through **22(4)** as shown in FIG. **4**. The right hand column shows the maximum main bit line voltage as a fraction of the virtual ground line voltage VGL**1**. VGL**2**, line **10**, and diffusion line **20** are switched to ground by means of a virtual ground line decoder and driver circuit shown in FIGS. **9** and **10**.

First consider the effect on the main bit line voltage level of core FET **22(1)** having a low threshold voltage. The low threshold voltage is denoted as C in FIG. **4**. Now there is a second current path from VGL**1** to the drain of the selected core FET **22(2)**. The second path is along the outermost left diffusion line **20** through core FET **22(1)**. Since the resistance of both left diffusion lines **20** are equal, the resistance from the VGL**1** line **10** to the drain of selected core FET **22(2)** is reduced to one-half the resistance of a single path. As a result, the voltage on mBL, line **12**, increases. Referring to FIG. **4**, a comparison of combination 8 to combination 4, or combination 7 to combination 3, shows how much the programmed state of core FET **22(1)** affects the maximum voltage on bit line **12**.

The programmed threshold voltage of core FET **22(3)** has the most pronounced effect on the main bit line voltage. If core FET **22(3)** has a high threshold voltage, the current in FET **22(3)** is approximately zero. There are no direct current paths from the center bit line **20'** to ground, and the maximum main bit line voltage is equal to the voltage on VGL**1**, approximately two volts for the illustrated embodiment.

If core FET **22(3)** is programmed with a low threshold voltage, a direct current path exists from the center diffusion bit line **20'** to VGL**2**, line **10**, by means of core FET **22(3)**, innermost right bit line **20**, core FET **24**, outermost right diffusion line **20**, to line **10**, VGL**2**. The resistance in this path from line **20'** to VGL**2** can be approximately equal to the resistance in the path from bit line **20'** to VGL**1** resulting in the voltage on line **20'** being approximately one-half of the voltage applied to VGL**1**.

If both core FETs **22(3)** and **22(4)** are programmed to a low threshold voltage, the current from the source terminal of FET **22(3)** can flow along innermost right bit line **20** and outermost right diffusion line **20** which reduces the resistance from the source terminal of FET **22(3)** to VGL**2**, line **10**, to one-half. The effect of the programmed threshold voltage of FET **22(4)** on the main bit line **12** can be seen by comparing combinations 3 and 4 or combinations 7 and 8 of FIG. **4**.

The lowest voltage on main bit line **12**, for a bit-high level occurs when core FET **22(1)** is a high threshold voltage, and both core FETs **22(3)** and **22(4)** are low threshold voltages. This is shown by combination 4 in FIG. **4**. For this case, the main bit line **12** voltage is a maximum of about 38% of the voltage on VGL**2**. The maximum voltages shown in FIG. **4** are the levels which could be reached if the core FET **22(2)** is allowed a long time to charge the bit line capacitance to a maximum value. For the invention, the main bit line **12** peak voltage, for a bit-high level, is about 25% of the levels shown in FIG. **4**. This is because the typical core evaluation time, or sensing time, does not provide time for main bit line **12** to charge to a higher voltage level. For example, for combination 4 in FIG. **4**, the typical voltage on the main bit line **12** is 200 millivolts with VGL**1** being about two volts. The ROM which uses the invention incorporates a sense amplifier which can detect a 150 millivolt bit-high level.

Now assume the selected core FET **22(2)** is programmed with a high threshold voltage which is greater than the voltage applied to WL**1**. The only current flowing through FET **22(2)** is a very low sub-threshold current which is negligible for bit line sensing. The current path from VGL**1** to center bit line **20'** is then open, which allows the center bit line **20'** and main bit line **12** to remain a precharged ground voltage level, a bit-low level.

Further assume that both selected core FET **22(2)** and core FET **22(3)** are programmed with a high threshold voltage. Center bit line **20'** is not coupled to either the innermost left or right bit lines **20** so it is floating at the precharged ground voltage, a bit-low level. The voltage on floating bit line **20'**, or main bit line **12**, can be affected by junction leakage currents or capacitively coupled noise voltages. Only noise voltages or junction leakage currents, which can shift the floating main bit line positive, can adversely affect the sense amplifier's reading of a bit-low level. For this reason, core junction leakage current to the grounded substrate does not affect the bit line which is floating at ground. Also, capacitively coupled negative noise voltages from the turning off of the memory core precharge clocks does not adversely affect the bit-low voltage level of zero volts.

Further, for a bit-high level which is a small positive voltage on the bit line, the negative noise voltages and the core junction leakage currents from the diffusion bit lines to substrate have negligible effect. This is because the selected core FET **22(2)**, with a programmed low threshold voltage, supplies a current to center bit line **20'** which is orders of magnitude greater than the combined negative noise current and the core junction leakage from diffusion bit line **20'**.

In summary, the memory core as defined in FIG. **2** can be used in the grounded core operating mode defined by the current invention with:

a) a voltage sensing sense amplifier;

b) a virtual ground line decoder circuit which selects both virtual ground lines **10**, VGL**1** and VGL**2**;

c) a virtual ground line driver circuit to drive both of the two selected metal virtual ground lines. During the precharge phase, both of the two selected metal virtual ground lines are driven to ground, then, during the sensing phase, one of the two metal virtual ground lines is held at ground and the other of the two metal virtual ground lines is switched to a voltage source; and

d) a precharge circuit to drive all metal virtual ground lines and metal bit lines to ground during the precharge phase. During the sensing phase, the precharge circuit is turned off.

Consider now the operation of the grounded memory core with a current sensing sense amplifier. The memory core shown in FIG. **2** can be used with other types of sense amplifiers than voltage sensing as described above. For example, a current sensing amplifier can be used. This type of sense amplifier supplies a sensing current through a bit line decoder to the main bit line **12**.

The operation of the word lines and column select lines is the same as described above. The operation of the virtual ground lines is essentially reversed from that described above for a voltage sensing amplifier. This is due to the fact that the selected core FET must switch the sensing current

to ground, if the selected core FET is programmed with a low threshold voltage. If the selected core FET is programmed with a high threshold voltage, the sensing current must be allowed to charge the selected main bit line to a positive voltage by opening the sensing current path to ground.

In order to select, for example, cell **22(2)**, block select signal, BS, line **16**, goes to a logical high thereby selecting the block shown in FIG. **2**. Signal BS, on line **16**, is coupled to the gates of the two transistors **28**. When switched high, BS couples main bit line **12** to a center bit line **20'** of the cell matrix block. Column select signal, CA, is a logical high, and column select line, CB, is a logical low thereby selecting the second and third columns. Left virtual ground line **10**, VGL**1**, is switched to ground. Right virtual ground line **10**, VGL**2**, could be allowed to float at the precharged ground level, or, for the preferred embodiment, it is driven to a small positive voltage having an amplitude which will minimize any current flowing in unselected core FETs **22(3)** and **22(4)**, thereby allowing the sensing current to more rapidly charge the main bit line to improve memory speed. The virtual ground lines VGL**1** and VGL**2** have thus selected the second column of cells and have deselected the third column of cells. Word line **14(1)** switches to a logical high with each of the remaining word lines **14(2)** to **14**(n) to a logical low thereby reading cell **22(2)**.

Assume the selected core FET **22(2)** is programmed with a low threshold voltage. The sensing current transmission path through the block of memory cells begins with the main bit line **12**, mBL, and ends with left virtual ground line **10**. With core FETs **28** controlled by BS, the sensing current flows from the main bit line **12** through FETs **28** to diffusion bit line **20'**. The current then flows along line **20'** to the drain of the selected core FET **22(2)** and through core FET **22(2)** to the left innermost diffusion bit line **20**. With core FET **24** controlled by CA, which is switched to a logical high, the current flows along left innermost line **20**, through FET **24**, and to left outermost diffusion bit line **20** which is connected to virtual ground line VGL**1**. As a result of the sensing current flowing through the low resistance path, the voltage on mBL, line **12**, is held to the a low level. This bit line voltage is defined herein as the bit-low level voltage.

The magnitude of the resistance in the sensing current path from the main bit line **12** to the left virtual ground line **10** varies significantly, depending upon the programmed threshold voltage of core FET **22(1)** in FIG. **2**. This FET has the gate connected to WL**1**, line **14(1)**, and may also be turned on when FET **22(2)** is selected.

Consider the effect, on the bit-low voltage level, of core FET **22(1)** having a low threshold voltage. Now there is a second current path from VGL**1** to the drain of the selected core FET **22(2)**. The second path is along the outermost left diffusion line **20** through core FET **22(1)**. Since the resistance of innermost and outermost left diffusion lines **20** are equal the resistance from the VGL**1** line **10** to the drain of selected core FET **22(2)** is reduced to one-half the resistance of a single path. As a result of the sensing current flowing through the low resistance paths, the bit line low voltage, on mBL, line **12**, is held to the lowest level for any combination of programmed threshold voltages of the core FETs shown in FIG. **2**.

Now assume the selected core FET **22(2)** is programmed with a high threshold voltage which is greater than the voltage applied to WL**1**. The only current flowing through FET **22(2)** is a very low sub-threshold current which is negligible for bit line sensing. The sensing current path from center bit line **20'** to VGL**1** is then open, which allows the center bit line **20'** and the main bit line **12** to be charged by the sensing current to a higher voltage level herein defined as a bit-high level voltage.

The programmed threshold voltage of core FET **22(3)**, FIG. **2**, has an effect on the main bit line voltage for a short time after the sensing current is switched to the main bit line **12**. If core FET **22(3)** has a high threshold voltage, the current in FET **22(3)** is approximately zero. There are no direct current paths from the center bit line **20'** to VGL**2**, line **114**. The sensing current can therefore charge diffusion bit line **20'** to the sensing voltage level, a bit-low level or a bit-high level, in less time.

If core FET **22(3)** is programmed with a low threshold voltage, an undesirable current path exists from the center diffusion bit line **20'** to VGL**2**, line **10**, by means of core FET **22(3)**, innermost right bit line **20**, core FET **24**, outermost right diffusion line **20**, to line **10**, VGL**2**. The resistance in this path from line **20'** to VGL**2** can be approximately equal to the resistance in the path from line **20'** to VGL**1**. If VGL**2** were floating at the precharged ground voltage level, approximately one-half of the sensing current would flow in this undesirable path for a significantly long time until the virtual ground line VGL**2** was charged to a small positive voltage. The diffusion junction capacitance on the virtual ground line VGL**2** is very high, since it is connected to all the memory cell blocks, typically 16, 32, or 64, in a column of the memory array. Because of the high capacitance on the virtual ground lines, the current sensing time is significantly long if, for this example, VGL**2** is initially floating at the ground voltage level.

The current invention solves the problem of high capacitance virtual ground lines by using a virtual ground line decoder circuit which selects both virtual ground lines, VGL**1** and VGL**2**, and a virtual ground line driver circuit which selectively drives one virtual ground line, VGL**1**, to ground and the second virtual ground line, VGL**2**, to a small positive voltage having an amplitude, approximately equal to the bit-low level voltage, which will minimize the undesirable current flowing in unselected core FET **22(3)**, thereby allowing the sensing current to more rapidly charge the main bit line to improve memory speed.

The voltage on the main bit line **12**, mBL, is only slightly affected by junction leakage currents or capacitively coupled noise voltages. Capacitively coupled negative noise voltages or junction leakage currents which can shift the main bit line negatively can adversely affect the current sensing sense amplifier's reading of a bit-high level. The magnitude of the sensing current is typically much higher than these currents. For this reason, core junction leakage current to the grounded substrate and capacitively coupled negative noise voltages from the turning off of the memory core precharge clocks have little effect on the bit-high level voltage.

In summary, the memory core as defined in FIG. **2** can be used in the grounded core operating mode with:

a) a current sensing sense amplifier;

b) a virtual ground line decoder circuit which selects both virtual ground lines VGL**1** and VGL**2**; and

c) a virtual ground line driver circuit which selectively drives one virtual ground line to ground and the second virtual ground line to a small positive voltage level approximately equal to the bit line low level defined herein.

Differential Sense Amplifier

A circuit which differentially amplifies voltages that are close to ground with differences of about 0.15 volts uses voltage level shifters, a cross coupled current source and inverters to provide increased speed, accuracy, and gain.

Symmetric cross coupled current sources are used in a differential amplifier to provide the differential amplifier with a balanced load. A symmetric and balanced layout senses smaller voltage differences and operates faster than would otherwise be possible. The gain of the cross coupled current source is controlled by four FETs.

Voltage level shifters at the input to the differential amplifier allow the differential amplifier to sense signals that are close to ground with a voltage difference of about 0.15 volts. The voltage level shifters also shift the signals to a voltage that increases the gain of the differential amplifier.

Two inverters block half level signals from being outputted until the sense amplifier data has been latched. By blocking half level outputs of the differential amplifier, a race condition is eliminated and output enable signal, OE, may then switch sooner than would otherwise be possible.

Consider first the architecture of the sense amplifier of FIG. **6**. Referring to FIG. **6**, DMYHI and DMYLO are connected to gates of FET **50** and **52** respectively. DMYLO is a dummy bit line in the ROM core with ROM cells programmed to prevent DMYLO from charging during a read cycle. DMYLO is precharged to ground. DMYLO has coupled noise voltages that are similar to those of a BIT line and the DMYHI line. It is used as a low voltage reference for all the sense amplifier circuits and the TRIG circuit. DMYHI is similar to DMYLO except the ROM cells on DMYHI are programmed to charge DMYHI from ground to a voltage level of about 0.15 volts. DMYHI is used as a BIT high voltage reference. BIT is the signal that carries the information from the memory core to the sense amplifier. Each BIT signal goes to a sense amplifier circuit. ROMs typically have more than one BIT and sense amplifier. ROMs with 8 or 16 BIT lines are common.

DMYHI serves as a BIT high voltage reference and DMYLO serves as a BIT low voltage reference. Because FETs **50** and **52** are connected in parallel the effective reference voltage is a level between the DMYLO and DMYHI levels. BIT is connected to the gates of both FETs **54** and **56**.

The sense amplifier has two level shifting circuits. These circuits shift the low voltage inputs up to a voltage that the differential amplifier can easily sense. FETs **54–60** form one level shifting circuit and FETs **50**, **52**, **62** and **64** form the other level shifting circuit. The outputs from these level shifting circuits are the signals, SAIN and SAREF. SAIN and SAREF are inputs to the differential amplifier. By selectively changing some of the widths of FETs **54–60** and FETs **50**, **52**, **62** and **64**, a wide range of voltages may be selected. A voltage that is optimal for the sense amplifier operation can thus be selected.

The differential amplifier is composed of FETs **66–84**. The differential amplifier compares the voltage of SAIN and SAREF. FETs **78–84** comprise a pair of cross coupled current sources that provides increased gain for the differential amplifier circuit. Inverters **86** and **88** block half level outputs of the differential amplifier until these outputs have been latched.

The operation of the sense amplifier of FIG. **6** is described in four phases. They are:

(a) precharging to ground the ROM core, DMYLO, DMYHI, and all of the BIT lines;

(b) sensing the ROM core to charge DMYHI and, depending upon the programmed data, the BIT line;

(c) latching the data; and

(d) automatically powering down the sense amplifier and retaining the latched data.

Consider the first phase of precharging the ROM core, DMYLO, DMYHI and BIT. Near the beginning of a ROM cycle, the precharge clocks, PC**1** and PC**2**, are either high from the end of the previous cycle, or they are switched high to precharge the ROM to ground. PC**1** is a precharge clock signal. PC**1** precharges to ground all the virtual ground and bit lines in the core before and after core evaluation. PC**2** is a precharge clock signal and precharges to ground BIT, DMYLO and DMYHI before and after memory core evaluation.

The time duration of the precharge is controlled by two circuits in the ROM called DCOK and OWDN (not shown). BIT is precharged to ground by PC**2** switching high. DMYLO and DMYHI are also precharged to ground by PC**2** switching high.

Referring to FIG. **6**, FET **72** is turned on by PC**2**. Since FETs **74** and **76** are turned on by SLIN, nodes SLQ and NSLQ are equalized to the same voltage level while PC**2** is high by means of FETs **72–76**. SLQ and NSLQ are the outputs of the differential amplifier comprised of FETs **66–76** in FIG. **6** and are both input to and output of the latch circuit comprised of FETs **94–102**. After the latching operation, SLQ and NSLQ are VDD/GND level signals representing the latched data. SLQ and NSLQ are inverted by inverters **86** and **88** to produce XQ and NXQ. XQ and NXQ connect to the output driver circuitry.

SLIN is high during memory core precharge to ground and while sensing the BIT, DMYLO and DMYHI inputs. When the data is latched by SLCH, SLIN switches low to disconnect the memory core and decode from the sense amplifier circuit. SLCH is a signal which is low during memory core precharge to ground and sensing, and is switched high to latch the data defined by the voltage levels on node SLQ and NSLQ at the start of the latch operation.

As long as the PC**2** clock is high, output nodes SLQ and NSLQ remain at the equalized voltage level and do not respond to inputs BIT, DMYLO and DMYHI. PC**2** is held high until the inputs BIT, DMYLO, and DMYHI are free of noise and/or have reached the appropriate voltage levels for sensing. By this means, outputs SLQ and NSLQ are preset to equal voltage levels from which they can respond quickly to the input signals.

Consider now the sensing the ROM core. Upon completion of the ROM core precharging, PC**1** and PC**2** are sequentially switched low. Address decoding is completed during the precharge phase to select (1) the sector of the ROM core to be sensed, (2) the word line within the sector, and (3) the bit and virtual ground lines within the sector. After PC**1** is switched low, selected virtual ground lines are switched high by control signals, SELV**0** or SELV**1** shown in FIGS. **11***a* and **11***b*. DMYHI then starts charging relatively slowly toward about 0.15 volt while DMYLO remains low at ground. All BIT lines, connected from the memory core to all the sense amplifier circuits, will either charge up like DMYHI, or remain at about the DMYLO voltage level, depending upon how the selected ROM cells are programmed.

Consider in particular the sensing operation when BIT remains at the DMYLO level. At the start of the sensing phase, DMYLO, DMYHI, and BIT are at the ground voltage level, namely the BIT gates of FETs **54** and **56**, DMYHI gate of FET **50** and DMYHI gate of FET **52**. BIT remains at zero volts. SAIN and SAREF are at the same voltage level of about 2.2 volts. The source of FETs **66** and **68** is node Vs which is coupled to ground through FET **70**. FET **70** has its gate controlled by VRN. VRN is an internal reference voltage for the differential amplifier current source, FET **70**, used in the sense amplifier circuit.

The gates of FETs **66** and **68** start out at a balanced voltage. As DMYHI ramps relatively slowly upward to

about 0.15 volts, the conductance of FET **50** becomes less, SAREF is driven higher, and SAIN remains at the same voltage level. As SAREF is driven higher, the conductivity of FET **68** increases and NSLQ is driven to a lower voltage level than SLQ.

Consider the sensing operation when BIT charges like DMYHI. At the start of the sensing phase, DMYLO, DMYHI, and BIT are at the ground voltage level, namely BIT gates of FETs **54** and **56**, DMYHI gate of FET **50** and DMYHI gates of FET **52**. SAIN and SAREF are at the same voltage level of about 2.2 volts. Both BIT and DMYHI then ramp relatively slowly from the initial ground level to about 0.15 volts. As DMYHI ramps up slowly, the conductance of FET **50** becomes less and SAREF is driven higher. At the same time BIT ramps up slowly, the parallel conductance of FETs **54** and **56** becomes less and SAIN is driven higher. Because BIT gates are the two FETs **54** and **56** and DMYHI gate is only one FET **50**, SAIN is driven high at a faster rate than SAREF. The gates of FETs **66** and **68** start out at a balanced voltage. As SAIN is driven higher at a faster rate than SAREF, the conductivity of FET **66** increases faster than the conductivity of FET **68** and SLQ is driven to a lower voltage level than NSLQ.

By selectively varying the gate widths of FETs **50–64**, the level shifting circuit can shift the voltages SAIN and SAREF over a wide range of different values. The widths are ratioed so that the differential amplifier operates with input voltage levels providing maximum gain. This setting of voltages improves the speed and accuracy of the differential amplifier. On the previous differential amplifier of FIG. **5**, the input levels were set at the internal precharge voltage of the memory core and could not be optimized for the best sense amplifier performance.

The present design employs a cross coupled current source to provide two current sources for the differential amplifier. Initially these current sources are matched and have the same capacitive load and impedance. As NSLQ and SLQ change, so do the current sources so that gain is provided to NSLQ and SLQ. For example, if BIT changes like DMYLO, then SLQ will start to go higher than NSLQ. As SLQ starts to go higher then the conductance of FET **90** is reduced which helps NSLQ to go lower and increases the voltage difference between NSLQ and SLQ. In the case where NSLQ starts to go higher, the conductance of FET **92** is reduced which helps SLQ to go lower and increases the voltage difference between SLQ and NSLQ.

FETs **90** and **92** can by themselves provide too much gain. FETs **82** and **84** are used in parallel to control the gain of the cross coupled current source. As the width-to-length ratio (W/L ratio) is increased for FETs **82** and **84**, the gain of the cross coupled current source is reduced. As the width to length ratio (W/L ratio) is increased for FETs **90** and **92**, the gain of the amplifier is increased. The desired gain for the amplifier is determined and controlled by the channel dimensions of FETs **82**, **84**, **90**, and **92**.

Consider now how the data is latched. The ROM has a circuit, herein called TRIG and shown in FIG. **7**, which detects when DMYHI is about 0.15 volts above DMYLO. When this occurs, another conventional timing circuit (not shown), herein called SAMPCNTL, sequentially and quickly switches SLCH high, then SLIN low, and then SLPD high. SLPD is low during memory core precharge to ground, sensing and latching of the data, then switches high. The high level reduces the power dissipation of the sense amplifier to zero. The latched data is retained.

As SLCH switches high, FET **94** in FIG. **6** drives the source terminals of FETs **96** and **98** toward ground. In the case when BIT remains low like DMYLO, node SLQ is at a higher voltage level than NSLQ at this time, and FET **98** conducts more current than FET **96**. FET **98** thus drives NSLQ toward ground faster than FET **96** drives SLQ, resulting in FET **96** being turned off, and NSLQ being driven low by FET **98**.

Next, as SUN switches low, FETs **100** and **102** drive the source terminals of FETs **104** and **106** high. Since NSLQ is held low by FET **98**, FET **104** conducts a higher current than FET **106**. FET **104** then drives SLQ to VDD. Also, as SLIN switches low, FETs **74** and **76** are turned off which isolates the input FETs **66** and **68** from the latch circuit. This prevents the subsequent precharge of BIT, DMYLO, and DMYHI from affecting the latched data.

In the case when BIT charges high like DMYHI, NSLQ is initially at a higher voltage level than SLQ, and NSLQ will be higher than SLQ after the latch operation. Since the latch circuit comprised of FETs **94–102** is symmetrical the latching operation is reversed for the case when BIT is low as compared to the case when BIT is high as described above.

The design of the differential amplifier is optimized so that the voltage level of SLQ and NSLQ is above the trigger point of the inverters **86** and **88** during the sensing time. The outputs of the sense amplifier, XQ and NXQ, are therefore both low until the data starts to latch. Before the data starts to latch, neither NSLQ nor SLQ falls below the trigger point of the inverter. The outputs of the differential amplifier, NSLQ and SLQ, are latched by the time that one of these outputs falls below the trigger point of either output inverter **86** and **88**. In this way, the inverters act to block half level outputs of the differential amplifier until data is latched.

In previous designs there existed a race condition between the output enable signal, OE, switching high and the outputs of the differential amplifier being latched. If OE switches high too soon, then incorrect data could be sent to the output drivers and this data may be outputted. OE can be delayed to ensure that OE does not switch high too soon, but this time would be added to the access time of the ROM. Since the inverters block half level outputs from the differential amplifier until the data is latched, the race condition does not exist and OE may switch high sooner than would otherwise be possible.

Finally consider the powering down of the sense amplifier. The sense amplifier automatically powers down at the end of a read cycle. When SLPD switches high at the end of a read cycle, FETs **78**, **80**, **60**, and **64** are switched off. There is no current path through the voltage level shifters from VDD to ground. The latch circuit comprised of FETs **94–102** drives SLQ and NSLQ to VDD or ground depending upon the data latched. With SLIN low, and SLPD high, there is no current path from VDD to ground, so the power dissipation is zero for the remainder of the memory cycle.

The sense amplifier also operates in a stand by mode. In the stand by mode, power consuming circuits in the ROM are shut down to save power. NCE is switched high and SLPD switches high. Because SLPD switches high, FETs **336** and **338** in FIG. **5** from the previous sense amplifier design are not needed. Power down in the stand by mode is the same as automatic power down at the end of a read cycle.

As stated, voltage level shifters can be used to advantage in other circuits. The use of the voltage level shifters in other circuits is demonstrated in FIG. **7**. In this case, the voltage level shifters are used with a differential amplifier to generate the signal, TRIG, in a timing circuit used in the ROM. DMYLO and DMYHI are reference voltages that are close to ground with a voltage difference of about 0.15 volts. FETs

104–108 and 110–114 are two voltage level shifters. The outputs of these voltage level shifters are TR0 and TR1. TR0 and TR1 are inputs to a differential amplifier that is used as a timing circuit. When the voltage difference between DMYLO and DMYHI becomes large enough, the differential amplifier detects this difference and TRIG switches from low to high. Voltage level shifting circuits may thus be used with conventional CMOS differential amplifiers.

Virtual Ground and Bit Line Decoder

A CMOS virtual ground and bit line decoder multiplexes a selected main bit line and two virtual ground lines. The CMOS decoder provides an improved precharge to the memory core as compared to NMOS decoders, because the decoder is designed for use with a memory core that is precharged to ground.

In the present design an additional decode is done by means of the SELV lines. Because this additional decode is done by means of the SELV lines, the present decoder uses fewer FETs and less area than would otherwise be possible.

An improved interlock method is provided in a circuit which is inherently faster and uses less silicon die area because fewer gates are used. Crowbar current is normally not significant but can become very significant when large FETs are used. This interlock method avoids these crowbar currents.

Consider first the architecture of the virtual ground and bit line decoder circuit. The virtual ground and bit line decoder circuit functions as a multiplexer. FIG. 9 shows a simplified schematic of how this function is implemented. In FIG. 9, SELV0 and SELV1 are mapped into many virtual ground lines in the core and one of many main bit lines from the core is mapped to the BIT line. The lines carrying the signals, SELV0 and SELV1, are collectively known as the SELV lines. SELV0 is a control signal from one of two voltage sources for the virtual ground lines. The present design has two virtual ground voltage sources. Both voltage sources are initially low, then one voltage source goes high while the other voltage source stays low. The voltage source that goes high is determined by an address decode. SELV1 is a control signal from the other one of the two voltage sources for the virtual ground lines. AY[4] is the address that determines whether SELV0 or SELV1 will go high during a read cycle. If AY[4] is low, then SELV0 will go high. If AY[4] is high, then SELV1 will go high. The signal, mBL, refers to the main bit line of the ROM. The main bit line is the selected bit line through which the selected core FET can output data. Data from the memory core is read through the main bit line.

The multiplexer has two sets of addresses as shown in FIG. 9. YDL[0] through YDL[7] are decoded lower addresses. YDU is a decoded upper address. These address lines go to the gates of FETs that act as pass transistors. These pass transistors are connected in series. For example, YDL[3] goes to the gate of FETs 116–120 and YDU goes to the gate of FETs 122–126. FET 116 is in series with FET 122, FET 118 is in series with FET 124, and FET 120 is in series with FET 126. Several different multiplexing designs are compatible with the invention and the one chosen is illustrated not by way of limitation but only by example for the purposes of clarity. The design of the low address block is unique. For example, multiplexing methods with any number of pass gates connected in series may be used. The present design has two FETs in series but will also work without the high address block decoder or with two high address blocks connected in series.

FIG. 9 also shows a precharge-to-ground block 117. Block 117 is composed of a plurality of FETs 119, all of which are connected in parallel. Each FET 119 has a source connected to ground, a gate connected to PC1, and a drain connected to either a main bit line or a virtual ground line in the memory core. PC1 is a precharge clock signal. PC1 precharges to ground all the virtual ground and bit lines in the core before and after core evaluation. VGL is the virtual ground line. The core has many virtual ground lines, but only two are selected for each selected bit. One selected virtual ground line stays low. The other selected virtual ground line is low at the beginning of the cycle to help discharge the memory core and then switches high to act as a voltage source for the memory core. After core evaluation, this selected virtual ground line switches low again to help discharge the memory core for the start of the next core evaluation. All virtual ground lines are precharged to ground during core precharge. All unselected virtual ground lines are floating at ground during core evaluation.

Every main bit line and virtual ground line in the memory core is connected to a precharge FET in precharge-to-ground block 117. A memory core block 121 is also shown in FIG. 9. Block 121 is repeated in rows and in columns to form the memory array. A detailed drawing of memory block 121 is described in connection with FIGS. 1 and 2.

FIG. 9 further shows that the drain of FET 128 is connected to BIT, its source is connected to ground, and its gate is connected to PC2. When PC2 switches high, BIT is precharged to ground through FET 128. PC2 is a precharge clock. PC2 precharges to ground all BIT lines before and after core evaluation.

Consider now the circuit which generates the multiplexing control signals, SELV0 and SELV1. FIG. 10 shows the circuit that generates SELV0 and SELV1. Address AY[4] is inverted once and used to generate SELV0. Address AY[4] is inverted again to generate SELV1. This address enables one SELV line to go high during a read cycle and forces the other SELV line low. For example, if AY[4] is high then node 130 is high, node 132 is low, and node 134 is high. FET 136 will be on and SELV0 will be forced low.

Consider now how the interlock circuit of FIG. 10 avoids crowbar currents in a driver that must switch large capacitive loads. NAND gate 138 has the inputs SEL and AY[4] inverted twice. SEL is a memory control signal which controls the rising and falling edges of SELV0 and SELV1. When SEL goes high, SELV0 or SELV1 will rise. When SEL goes low, SELV0 and SELV1 will go low.

The output of NAND gate 138 is node 140. Node 140 is the input of inverter 142 whose output is node 144. Node 144 is an input to a complex gate 146. Gate 146 also has inputs SEL and AY[4] inverted twice. Node 144 gates FET 148 and node 150 gates FET 152. The drain of FET 148 is connected to VSEL. VSEL is a voltage source for the SELV lines. VSEL may be shorted to VDD or may be at a lower voltage. The source of FET 148 and the drain of FET 152 are connected together and form SELV1. The interlock circuit is repeated in FETs 136, and 154–160 to generate SELV0 as described above.

Crowbar currents may be very large when inverters and logic gates use large FETs. When CMOS inverters and logic gates switch, there is a period of time where both the PMOS and the NMOS FETs are partially turned on. The current that flows through these FETs is called crowbar current. Crowbar current is normally not significant, but can become very significant when large FETs are used. This interlock method avoids these crowbar currents. If this method, FETs 148 and 152 are very large FETs because they must drive a very large capacitive load. The interlock method was devised to ensure that FET 148 turns off before FET 152 turns on, and that FET 152 turns off before FET 148 turns on. In this method

there can be no crowbar current through FETs **148** and **152** because one of these FETs will always be off when the other FET is on.

Consider the operation of the virtual line decoder circuit and bit line decoder circuit as improved in the invention. FIGS. **11***a* and *b* are timing diagrams of the virtual ground and bit line decoder operation. These timing diagrams are very similar to FIG. **3**, but additional timing signals have been added which are relevant to the operation of the virtual ground and bit line decoder. The time between T**1** and T**2** is the memory core precharge time. The interval between T**2** and T**3** the core evaluation period, and the interval after T**3** the core reset period. SEL is low on timing line **162** and both SELV**0** and SELV**1** are at ground on timing lines **164** and **166** respectively. It is at T**1** that PC**1** switches high on timing line **168** and the core is precharged to ground through precharge-to-ground block **117** as shown in FIG. **9**. Thus, before the start of each read cycle, all the virtual ground line and main bit line of the memory core are driven to ground by means of the PC**1** clock. The selected two virtual ground lines are additionally precharged to ground through another path in the decoder circuit. The upper and lower addresses are selected during the core precharge time and SELV**0** and SELV**1** are both driven to ground during the T**1** to T**2** interval. Thus there exists a precharge path to ground for the two selected virtual ground lines. For example, in FIG. **9**, if YDL[3] and YDU switch high during the core precharge time, SELV**0** and SELV**1** are both low and VGL**1** and VGL**2** are precharged to ground through FET **116**, FET **122**, FET **120** and FET **126**. PC**2** switches high on timing line **170** as PC**1** switches high on timing line **168**. BIT is precharged to ground through FET **128**.

After the core and the word line from the previous cycle have been adequately discharged, SEL switches high and then either SELV**0** or SELV**1** goes high. A FET in the ROM is selected by the appropriate combination of WL, BS, SELV**0** or SELV**1**, and CA or CB line. The signal BIT on the main bit line will rise if the selected memory core FET is programmed with a low threshold level. The signal BIT on the main bit line will stay low if the selected memory core FET is programmed with a high threshold level.

Different paths through the memory core are selected by SELV**0** and SELV**1**. If SELV**0** goes high, then one path through the memory core is selected. If SELV**1** goes high, then another path through the memory core is selected. The decoding of the two SELV lines is unique and necessary for proper addressing of the selected memory cell. By decoding an address in the two SELV lines, the virtual ground line decoder is made simpler, less FETs are needed and the silicon die area of the circuitry is reduced.

By controlling the voltage of VSEL we can control the voltage level of the SELV lines. The SELV lines have the highest voltage in the memory core. High voltages in the memory core can cause the FETs of the memory core to breakdown because of the very small dimensions of these FETs. By controlling the voltage level of VSEL, FET breakdowns in the memory core can be avoided.

At the end of the read cycle at time T**3**, the selected SELV line, SELV**1** for example on timing line **166**, is forced low as quickly as possible by SEL going low on timing line **162**. By forcing the selected SELV line low, the selected virtual ground line is quickly precharged to ground and made ready for the next read cycle during core reset as shown on timing line **172**. If the selected main bit line has been driven high during the previous read cycle, then there exists a path from the virtual ground lines to the main bit line. Switching the virtual ground lines low will therefore discharge the main bit line through the same path which charged the main bit line high as shown on timing line **174**. This is the case where it is important to discharge the main bit line. In the other case where there is no current path from the virtual ground lines to the main bit line, the main bit line has not risen and does not need this extra precharging to ground also shown on timing line **174**.

Proper operation of the interlock method requires that the two large output FETs **148** and **152** must never both be on at the same time. To ensure this condition, node **144** must be low before node **150** starts to switch high, and node **150** must be low before node **144** starts to switch high.

FIG. **12** shows a timing diagram of the interlock circuit. Signal AY[4] switches first on timing line **176** and later SEL goes high on timing line **178**. If AY[4] is high, then node **140** switches low, node **144** switches high, and FET **148** drives SELV**1** high as shown on timing line **180** after SEL switches high on timing line **178**. If AY[4] is low, then node **130** switches low, node **132** switches high, and FET **158** drives SELV**0** high after SEL switches high.

Assume that AY[4] switches high. When SEL switches high, there are two timing paths to consider. In one path, node **140** switches low, node **144** switches high, and FET **148** turns on. In the other path, node **150** switches low and FET **152** turns off. The path that turns FET **152** off has fewer stages than the path that turns FET **148** on. Because the path that turns FET **152** off has fewer stages, this path is faster than the path that turns FET **148** on. FET **152** is sufficiently turned off before FET **148** turns on so that crowbar current is negligible.

When SEL switches low at the end of a cycle, there is only one timing path to consider. Node **140** switches high, node **144** switches low, and node **150** switches high. Because node **144** switches low before node **150** switches high, FET **148** is sufficiently turned off before FET **152** turns on so that crowbar current is negligible.

Many alterations and modifications may be made by those having ordinary skill in the art without departing from the spirit and scope of the invention.

Therefore, it must be understood that the illustrated embodiment has been set forth only for the purposes of example and that it should not be taken as limiting the invention as defined by the following claims. The following claims are, therefore, to be read to include not only the combination of elements which are literally set forth, but all equivalent elements for performing substantially the same function in substantially the same way to obtain substantially the same result. The claims are thus to be understood to include what is specifically illustrated and described above, what is conceptionally equivalent, and also what essentially incorporates the essential idea of the invention.

We claim:

1. An improvement in a method for decoding a plurality of virtual ground lines and bit lines in a memory core comprising the steps of:

driving all virtual ground lines in said memory core low;

multiplexing two virtual ground lines in a memory core, by holding a selected first virtual ground line low and keeping a selected second virtual ground line low for memory core discharge; and by driving said selected second virtual ground line high for core evaluation;

evaluating said memory core;

keeping all unselected virtual ground lines floating during said step of evaluating said memory core; and

switching said second virtual ground line low for memory core discharge in preparation for subsequent memory core evaluation.

2. The improvement of claim 1 further comprising the step of precharging a BIT line to ground prior to said step of evaluating said core, said BIT line being selectively coupled to said bit lines in said memory.

3. A decoder for producing two memory multiplexing signals, SELV0 and SELV1, capable of driving a large capacitive memory load, said decoder coupled between a high voltage supply and around and comprising:

decode means for selectively decoding an address signal to drive one of said two memory multiplexing signals, SELV0 and SELV1, high and the other low; and

drive means coupled to said decode means and for generating said two memory multiplexing signals, SELV0 and SELV1, in response to said decode means, said drive means being tristated, without generating any current between said high voltage supply and ground when switching between said low and high logic levels of SELV0 and SELV1, whereby noise to ground is reduced.

4. The decoder of claim 3 wherein said drive means is comprised of a pair of two large FETs coupled in series, said memory multiplexing signals, SELV0 and SELV1, being derived respectively from said coupling between one of said pair of said two large FETs, said drive means comprising means for turning each one of said two large FETs off before turning on the other one of said two large FETs in each of said pairs of FETs, so that one of said FETs of each pair will always be off when the other one of said pair of FETs is on.

5. The decoder of claim 3 wherein said memory multiplexing signals, SELV0 and SELV1, have a voltage level set by said high voltage supply at a decoder supply voltage, VSEL, said memory multiplexing signals, SELV0 and SELV1, having the highest voltage level in said memory core, wherein voltage levels of said memory multiplexing signals, SELV0 and SELV1, are set at a level low enough to avoid memory breakdowns in said memory core.

6. A method for producing two memory multiplexing signals, SELV0 and SELV1, capable of driving a large capacitive memory load comprising the steps of:

selectively decoding an address signal to determine which one of said two memory multiplexing signals, SELV0 and SELV1, is to be driven high and the other to be driven low; and

generating said two memory multiplexing signals, SELV0 and SELV1, as tristated signals, without generating any crowbar current when switching between said low and high logic levels of SELV0 and SELV1, whereby noise to ground is reduced.

7. The method of claim 6 wherein said step of generating comprises the step of controlling one FET in a pair of two large FETs coupled in series, said memory multiplexing signals, SELV0 and SELV1, being derived respectively from said coupling between one of said pair of said two large FETs, said step of controlling comprises the steps of turning each one of said two large FETs off before turning on the other one of said two large FETs in each of said pairs of FETs, so that one of said FETs of each pair will always be off when the other one of said pair of FETs is on.

8. The method of claim 7 further comprising the step of setting the voltage levels of said memory multiplexing signals, SELV0 and SELV1, by a decoder supply voltage, VSEL, said memory multiplexing signals, SELV0 and SELV1, having the highest voltage level in said memory core, wherein voltage levels of said memory multiplexing signals, SELV0 and SELV1, are set at a level low enough to avoid memory breakdowns in said memory core.

9. A driver circuit for driving a large capacitve load while avoiding crowbar currents comprising:

two large FETs coupled in series, an output signal being derived from said coupling between said two large FETs; and

means for turning each one of said two large FETs off before turning on the other one of said two large FETs, so that one of said FETs will always be off when the other one of said FETs is on so that no crowbar current is generated as said two large FETs are switched, whereby noise to around is reduced.

* * * * *

CLIPPEDIMAGE= JP362120714A
PAT-NO: JP362120714A
DOCUMENT-IDENTIFIER: JP 62120714 A
TITLE: DISTORTION COMPENSATION CIRCUIT FOR DIGITAL SIGNAL

PUBN-DATE: June 2, 1987

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APPL-NO: JP60260254
APPL-DATE: November 20, 1985

INT-CL (IPC): H03K005/01; H03K019/00
US-CL-CURRENT: 326/30

ABSTRACT:
PURPOSE: To output a digital signal whose distortion is eliminated by applying differential constitution to an interface circuit recovering a digital signal in a reception circuit of a digital signal and supplying a differential output signal to a distortion compensation circuit comprising a couple of flip-flop circuits and a decoder circuit.

CONSTITUTION: A reception amplifier 11, an identification circuit 21 and a TTL level conversion circuit 31 have non-inverting and inverting outputs to apply differential constitution. The TTL level conversion circuit 31 is provided with a non-inverting switching TR 31 and an inverting TR 32. A signal at a non-inverting output 5 and an inverting output 6 is given to a clock input terminal of flip-flop circuits 51, 52 of the compensation circuit. From the output waveform of the circuits 51, 52, a recovery signal is

formed only at the
leading or trailing of the signals 5, 6 by the decoder circuit and a signal
having a waveform 9 is obtained as an output signal of the compensation circuit
by using the trailing only. Since the same delay time is given at the
leading/trailing of the input signal in an interface circuit 41 in this way,
the distortion of a code against the duty factor is cancelled.

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭62－120714

⑤1Int.Cl.⁴	識別記号	庁内整理番号	⑬公開 昭和62年(1987)6月2日
H 03 K 5/01 19/00	101	7259－5J Z－8326－5J	審査請求 未請求 発明の数 1 （全5頁）

⑤4発明の名称　ディジタル信号の歪補償回路

⑳特　願　昭60－260254
㉒出　願　昭60(1985)11月20日

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明　細　書

1．発明の名称

ディジタル信号の歪補償回路

2．特許請求の範囲

差動出力信号をそれぞれクロックとして入力される一対のフリップフロップ回路（51）、（52）と、該フリップフロップの各出力信号をデコードするゲート回路（53）とを備えてなることを特徴とするディジタル信号の歪補償回路。

3．発明の詳細な説明

〔概要〕

ディジタル信号の受信回路において、ディジタル信号を再生するインタフェイス回路を差動構成とし、差動出力信号を一対のフリップフロップ回路及びデコーダ回路からなる歪補償回路に供給することにより、入力信号の変化点の立上がりもしくは立下がりのみ使用することを可能とし、歪の除去されたディジタル信号を出力するようにしたものである。

〔産業上の利用分野〕

本発明はディジタル信号受信装置の受信信号再生時の歪補償回路に関する。

ディジタル信号受信装置は入力ディジタル信号を識別回路、TTL 変換回路を備えるインタフェース回路に入力し、受信入力信号から1、0レベルを判別し、TTL レベルに変換する。

この際、ディジタル信号を再生するインタフェース回路にて歪が生じるのでその補償をすることが望ましい。

〔従来の技術〕

従来のディジタル信号受信装置における、インタフェース回路の構成を第5図のブロック図にて示す。

図において、1は受信増幅器、2は識別回路、3はTTL レベル変換回路を示し、これらの回路が受

信装置の入力インタフェース回路4を構成する。

受信信号は受信増幅器1において忠実に平坦増幅された後、識別回路2において1、0レベルの判別が行われ、更にTTL レベル変換回路3にてTTL レベルへの変換が行われる。

再生されたTTL レベルをもつディジタル信号はインタフェース回路4の出力となる。

第6図は識別回路2とTTL レベル変換回路3の詳細図である。識別回路はトランジスタTR1 とTR2からなり、TTL レベル変換回路はTR3 から構成される。この回路の動作は第7図の波形図によって説明される。

第7図の①～④は第6図回路中の点①～④における波形を示す。

波形①と②の間ではエミッタフォロワのため波形歪は無視出来る。TR2 のコレクター電極の波形③は波形①に対して立上がり点においてtstg2+tf2、また立下がり点においてtd2+tr2の遅延を生じる。TR2 の出力はTR3 のベースに供給され、TR3 の出力波形は④に示される。

波形④は③の波形に対し、変化点において更に遅延される。即ち波形③の立上がり点に対応する④の立下がり点においてtd3+tr3の遅延を生じ、また波形③の立下がり点に対応する④の立上がり点においてtstg3+tf3の遅延を生じる。

結局、入力波形①の立上がり点に対応する出力波形④の立下がり点は

$$t_{stg2}+t_{f2}+t_{d3}+t_{r3}$$

また入力波形①の立下がり点に対応する出力波形④の立上がり点は

$$t_{d2}+t_{r2}+t_{stg3}+t_{f3}$$

の遅延を生じる。

ここで、td 、tr はスイッチング時の立上がりにおける遅延時間と上昇時間、tstg 、tf はスイッチング時の立下がりにおける蓄積時間と下降時間を示し、サフィックス2 、3 はトランジスタTR2 、TR3 に対応する。

識別回路2のTR2 は非飽和スイッチとして使用され、またTTL レベル変換回路3のTR3 は飽和スイッチとして使用されるため、同一IC基盤上に作られたトランジスタであったとしても、TR2 とTR3 とでは各パラメータが大きく異なり、もとの波形変化に対し出力波形④の立下がり点と立上がり点とでは遅延時間が等しくならない。

〔発明が解決しようとする問題点〕

この様に、従来のディジタル信号受信装置のインタフェース回路は再生したディジタル信号が立下がり点と立上がり点とで遅延時間が同じでなく、再生波形に歪を生じる。従って受信信号に歪が無くても、再生信号に歪を生じる欠点がある。

〔問題点を解決するための手段〕

上記の問題点は、

差動信号がそれぞれクロックとして入力される一対のフリップフロップ回路（51）、（52）と、該フリップフロップの各出力信号をデコードするゲート回路（53）とを備えてなる、

本発明のディジタル信号の歪補償回路により解決される。

〔作用〕

本発明においては、インタフェース回路を差動構成とし、正相、逆相の両信号をつくる。一対のフリップフロップ回路にクロックとしてこの信号を入力し、前記両信号の立上がり若しくは立下がりのみを使用することにより再生ディジタル信号を発生させ、インタフェース回路中で発生する歪を補償する。

〔実施例〕

図示実施例に従い本発明を詳細に説明する。

第1図は本発明による歪補償回路を使用した、インタフェース回路の一実施例のブロック構成図、第2図は差動構成された本発明による識別回路とTTL レベル変換回路の一実施例の接続構成図、第3図は本発明による歪補償回路の一実施例における回路構成図、第4図は本発明の歪補償回路の動作説明のための波形図である。

第1図において受信増幅器11、識別回路21、TTL レベル変換回路31は正相と逆相の出力をもち差動

構成とされる。TTL レベル変換回路31は正相、逆相用の各1個のスイッチングトランジスタTR31、TR32を備える。正相出力を⑭、逆相出力を⑮とする。これらの波形の変化は第4図の⑮、⑯に示す。受信入力信号①の波形はTTL レベル変換回路の正相出力で、立下がり、立上がりにおいて、それぞれTOFF21 ＋TON31、TON21＋TOFF31 の遅延、また逆相出力で、立上がり、立下がりにおいて、それぞれTON22＋TOFF32 、TOFF22 ＋TON32の遅延をもつ。

⑮、⑯の信号は第3図に示す補償回路のフリップフロップ回路51、52のクロック入力端子に与えられる。51、52のの出力波形はQ1出力においてⒽ、Q2出力にてⒾにて示され、AND ゲートとNOR ゲートからなるデコード回路にて⑮、⑯の信号の立上がり又は立下がりのみにより再生信号がつくられ、図示実施例は立下がりのみを使用して、補償回路の出力信号として⑰の波形の信号が得られる。波形⑰はその立上がりにおいて、

TOFF21 ＋TON31＋TD 、

立下がりにおいて、

TOFF22 ＋TON32＋TD

の遅延時間をもつが、

TOFF21 ≒ TOFF22

TON31 ≒ TON32

であるから、インタフェース回路においては入力信号の立上がり、立下がりにおいて同一の遅延時間が与えられるから、符号の専有率に対する歪は相殺される。

なお、TONn = tdn＋trn、

TOFFn = tstgn＋tfn

とし、またTD はゲート及びフリップフロップ回路の処理時間を示す。

〔発明の効果〕

本発明によれば、受信回路における歪の発生を補償し、再生信号の符号専有率の変化を小さくすることが出来、特に高速信号を扱う場合、その作用効果は極めて大きい。

4、図面の簡単な説明

第1図は本発明による歪補償回路を使用したインタフェース回路の一実施例のブロック構成図、

第2図は差動構成の識別回路とTTL レベル変換回路の一実施例の接続構成図、

第3図は本発明による歪補償回路の一実施例の回路構成図、

第4図は本発明の歪補償回路の動作説明のための波形図、

第5図は従来のディジタル信号受信装置における、インタフェース回路のブロック構成図、

第6図は従来の識別回路とTTL レベル変換回路の接続図、

第7図は従来のインタフェース回路の動作説明のための波形図である。

図において、

1、11は受信増幅器、

2、21は識別回路、

3、31はTTL レベル変換回路、

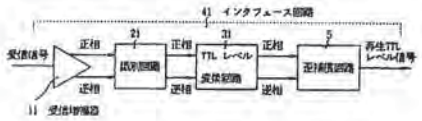
4、41は入力インタフェース回路、

5は歪補償回路、

51、52はフリップフロップ回路、

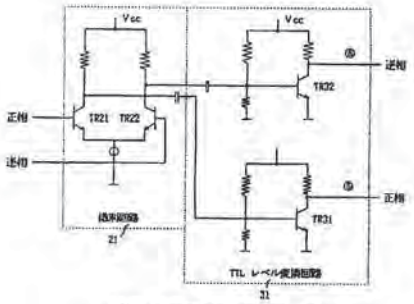
53はゲート回路である。

代理人弁理士　井桁貞一



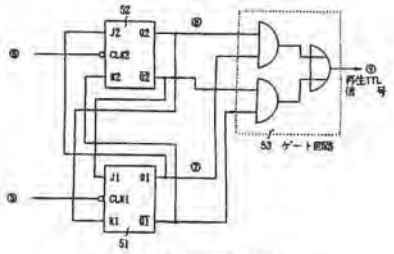
本発明によるインタフェース回路の
一実施例のブロック構成図

第 1 図



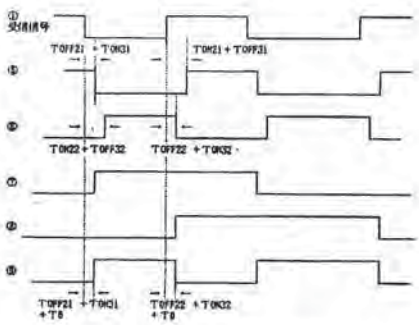
本発明による遅延回路とTTL レベル変換回路の
一実施例の詳細構成図

第 2 図



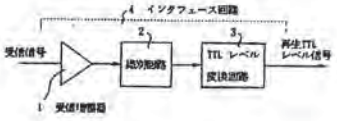
本発明による遅延回路の一実施例の
回路構成図

第 3 図



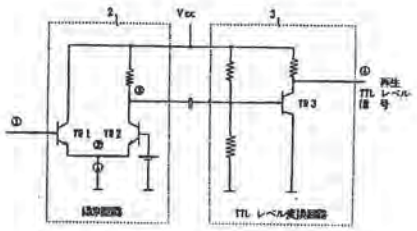
本発明の遅延回路の動作説明のための波形図

第 4 図



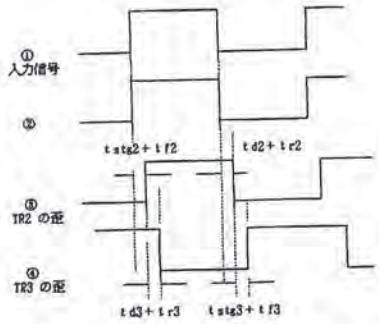
従来のインタフェース回路の
ブロック構成図

第 5 図



従来の遅延回路とTTL レベル変換回路
の詳細図

第 6 図



従来のインタフェース回路の動作説明のための波形図

第 7 図

UNITED STATES DEPARTMENT OF COMMERCE
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NOTICE OF ALLOWANCE AND ISSUE FEE DUE

[illegible]

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
First Named Applicant	[illegible]	35 USC 154(b) term ext. =	0 days.	

TITLE OF INVENTION: [illegible]

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
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PATENT

X-784 US
09/655,168

NON CORRESPONDENCE

IN THE UNITED STATES PATENT OFFICE

Applicant: Atul V. Ghia et al.
Assignee: Xilinx, Inc.
Title: Circuit for Producing Low-Voltage Differential Signals

Serial No.: 09/655,168 File Date: 9/5/00
Examiner: D. Chang Art Unit: 2819
Docket No.: X-784 US

VIA FACSIMILE 703-746-4000
Via Express Mail No. EV000378346US

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Dear Sir:

On December 7, 2001 applicants deposited payment of the Issue Fee for the above-referenced application with the United States Postal Service with sufficient postage for first class mailing. On January 18, 2002 all the documents mailed to pay the issue fee were returned to us as undeliverable. It is our understanding that our address label on the envelope was destroyed due to a decontamination process implemented as a result of September 11, 2001. In support of this declaration we submit, the Original envelope, Issue Fee Transmittal and Postcard.

PATENT

X-784 US
09/655,168

Applicants respectfully request that the delay in issue fee payment be recognized as unavoidable and accept this late payment of the issue fee. No additional fee is believed to be due. However, the Commissioner is hereby authorized to charge any additional fees required, and credit any overpayments to our deposit account No.: 24-0040. The examiner is requested to contact the Applicant's agent at 408-879-4969 if there any questions or comments.

Respectfully submitted,

Edel M Young

Edel M. Young
Agent for Applicants
Reg. No. 32,451

I hereby certify that this correspondence is being submitted via FACSIMILE to (703) 746-4000 on January 18, 2002; and
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Name

Julia K. Adams
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01/16/02 15:02 TEL 408 377 6137 Xilinx Legal 004

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2100 LOGIC DRIVE
SAN JOSE CA 95124

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
09/655168 ~~09/655,168~~	09/05/00	023	CHANG, D	2819	09/10/01

First Named Applicant	35 USC 154(b) term ext. =
CHIA	0 Days.

TITLE OF INVENTION: CIRCUIT FOR PRODUCING LOW-VOLTAGE DIFFERENTIAL SIGNALS

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
3 X-784 US	326-083,000	L68	UTILITY	NO	$1240.00	12/10/01

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1 Arthur J. Behiel,
2 Edel M. Young
3

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35,477

01/22/2002 MAHMED2 00000083 240040 09655168
01 FC:142 1280.00 CH

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PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 29, 1999

Application or Docket Number

CLAIMS AS FILED - PART I

	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA
FOR		
BASIC FEE		
TOTAL CLAIMS	23 minus 20=	*3
INDEPENDENT CLAIMS	3 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐			OR	OTHER THAN SMALL ENTITY	
RATE	FEE			RATE	FEE
	345.00		OR		690.00
X$ 9=			OR	X$18=	54
X39=			OR	X78=	
+130=			OR	+260=	
TOTAL			OR	TOTAL	744

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY			OR	OTHER THAN SMALL ENTITY	
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X$ 9=			OR	X$18=	
X39=			OR	X78=	
+130=			OR	+260=	
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	

AMENDMENT B

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Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDITIONAL FEE			RATE	ADDITIONAL FEE
X$ 9=			OR	X$18=	
X39=			OR	X78=	
+130=			OR	+260=	
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	

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X39=			OR	X78=	
+130=			OR	+260=	
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	

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(Rev. 12/99)

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US006366128B1

(12) **United States Patent**
Ghia et al.

(10) **Patent No.: US 6,366,128 B1**
(45) **Date of Patent: Apr. 2, 2002**

(54) **CIRCUIT FOR PRODUCING LOW-VOLTAGE DIFFERENTIAL SIGNALS**

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(73) Assignee: **Xilinx, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/655,168**

(22) Filed: **Sep. 5, 2000**

(51) **Int. Cl.**[7] **H03K 19/094**; H03K 19/173

(52) **U.S. Cl.** **326/83**; 326/44; 326/40; 326/49

(58) **Field of Search** 326/83, 86, 87, 326/38, 40, 44, 45, 46, 49, 30

(56) **References Cited**

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Jon Brunetti and Brian Von Herzen, "Multi–Drop LVDS with Virtex–E FPGAs," XAPP231 (Version 1.0) Sep. 23, 1999.
Application Report "LVDS Multidrop Connections" published by Texas Instruments, Jul. 1999.

* cited by examiner

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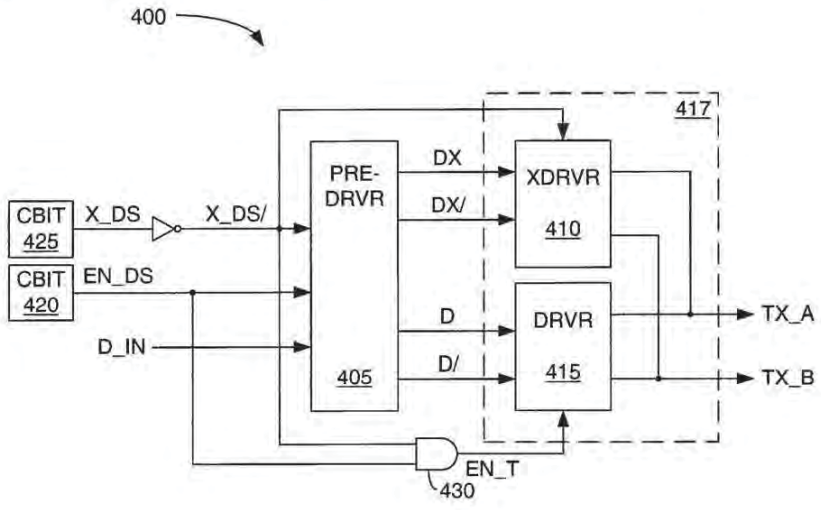
Assistant Examiner—Daniel D. Chang
(74) *Attorney, Agent, or Firm*—Arthur J. Behiel; Edel M. Young

(57) **ABSTRACT**

Described are systems for producing differential logic signals. These systems can be adapted for use with different loads by programming one or more programmable elements. One embodiment includes a series of driver stages, the outputs of which are connected to one another. The driver stages turn on successively to provide increasingly powerful differential amplification. This progressive increase in amplification produces a corresponding progressive decrease in output resistance, which reduces the noise associated with signal reflection. The systems can be incorporated into programmable IOBs to enable PLDs to provide differential output signals.

23 Claims, 10 Drawing Sheets



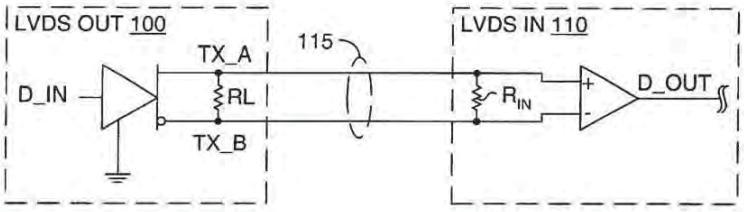


FIG. 1
(PRIOR ART)

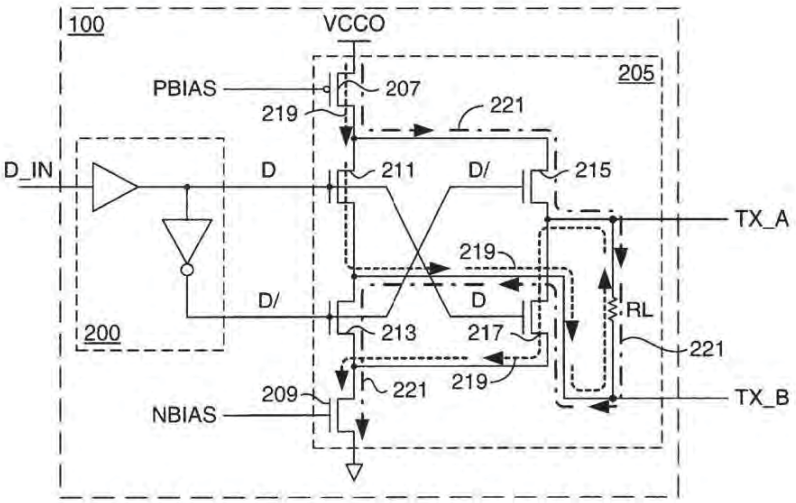


FIG. 2
(PRIOR ART)

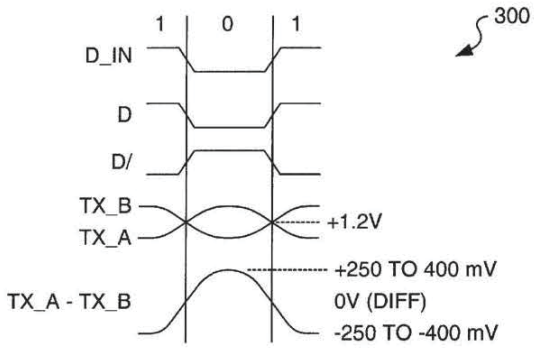
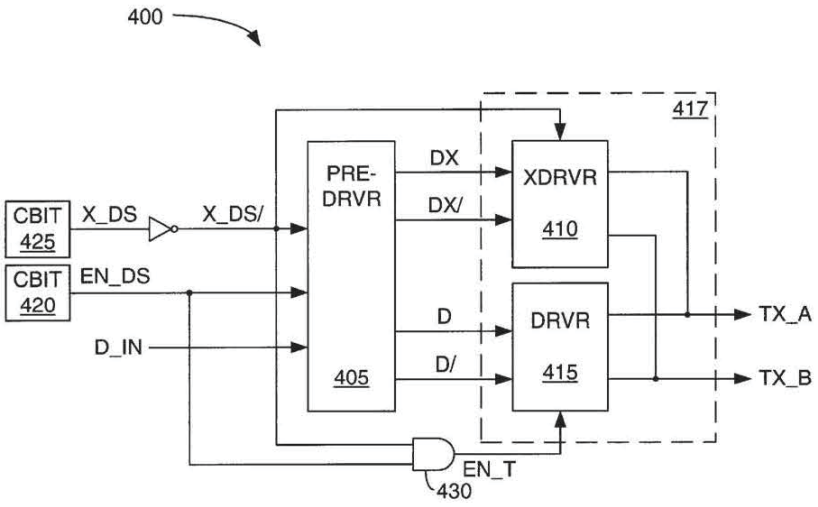


FIG. 3
(PRIOR ART)



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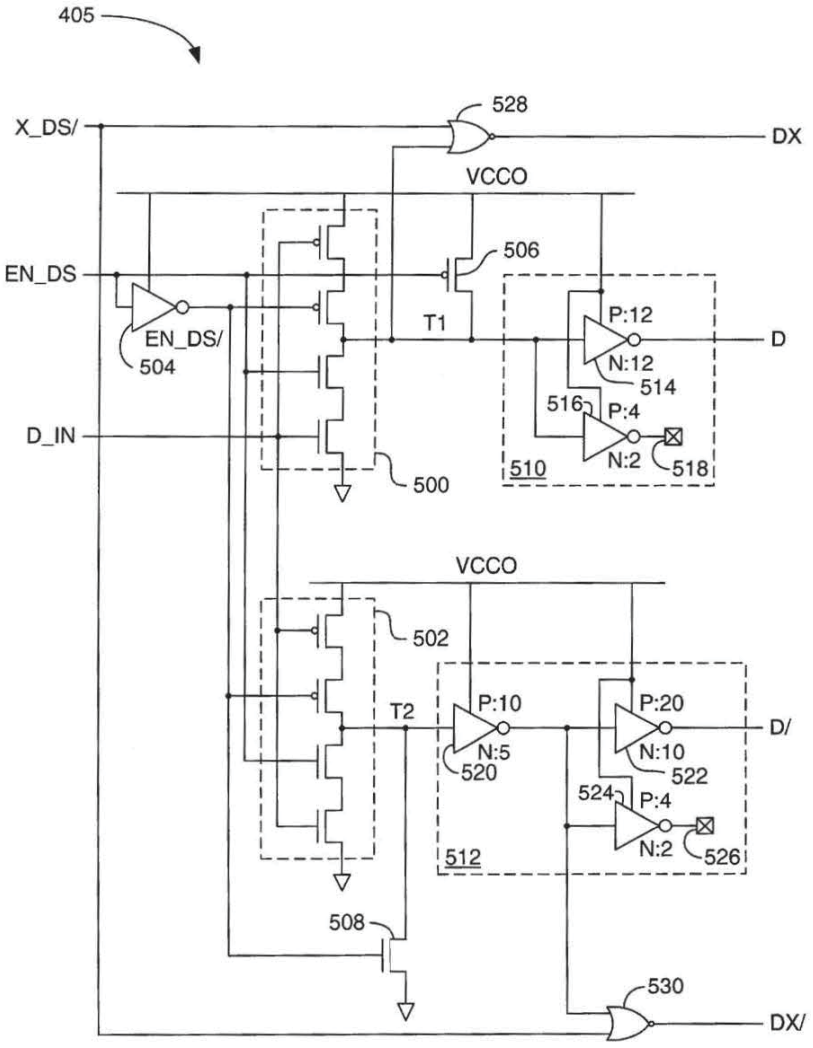
405
X_DS/
528
DX
VCCO
EN_DS
506
T1
P:12
D
EN_DS/
504
N:12
514
516
P:4
D_IN
N:2
518
510
500
VCCO
502
T2
P:10
P:20
D/
N:5
520
N:10
522
524
P:4
N:2
526
512
508
530
DX/

FIG. 5A

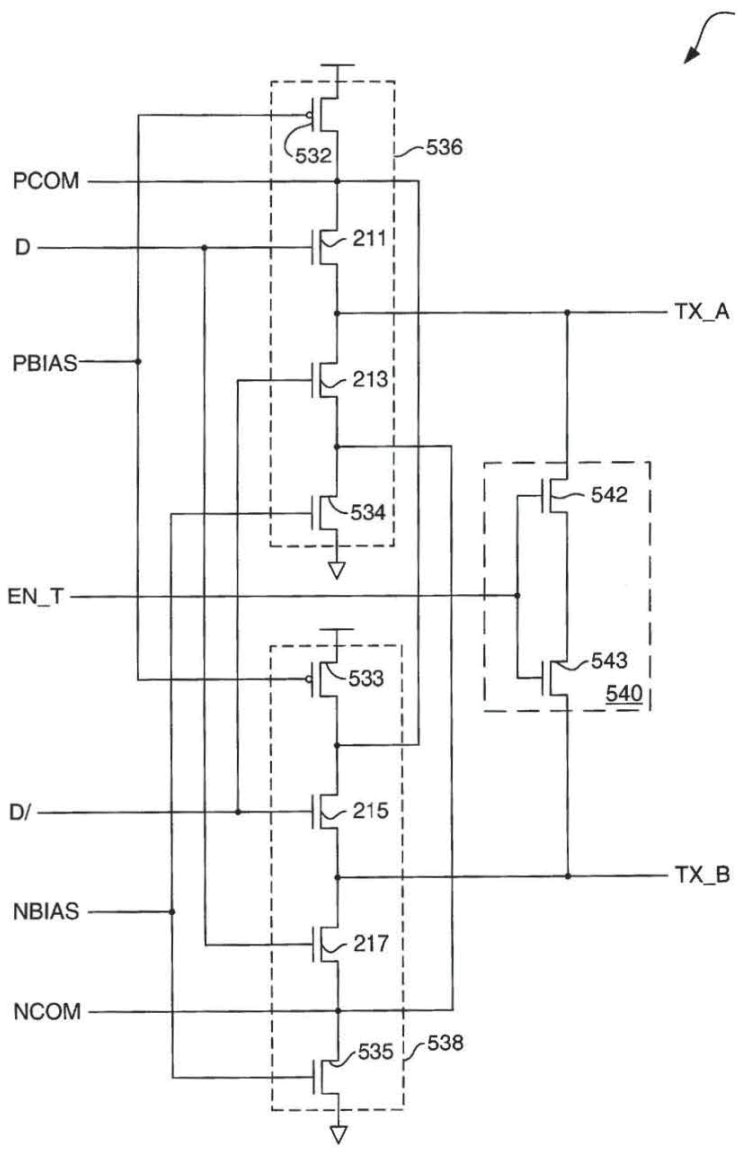
415
532
536
PCOM
D
211
TX_A
PBIAS
213
542
534
EN_T
543
540
533
D/
215
TX_B
NBIAS
217
NCOM
535
538

FIG. 5B

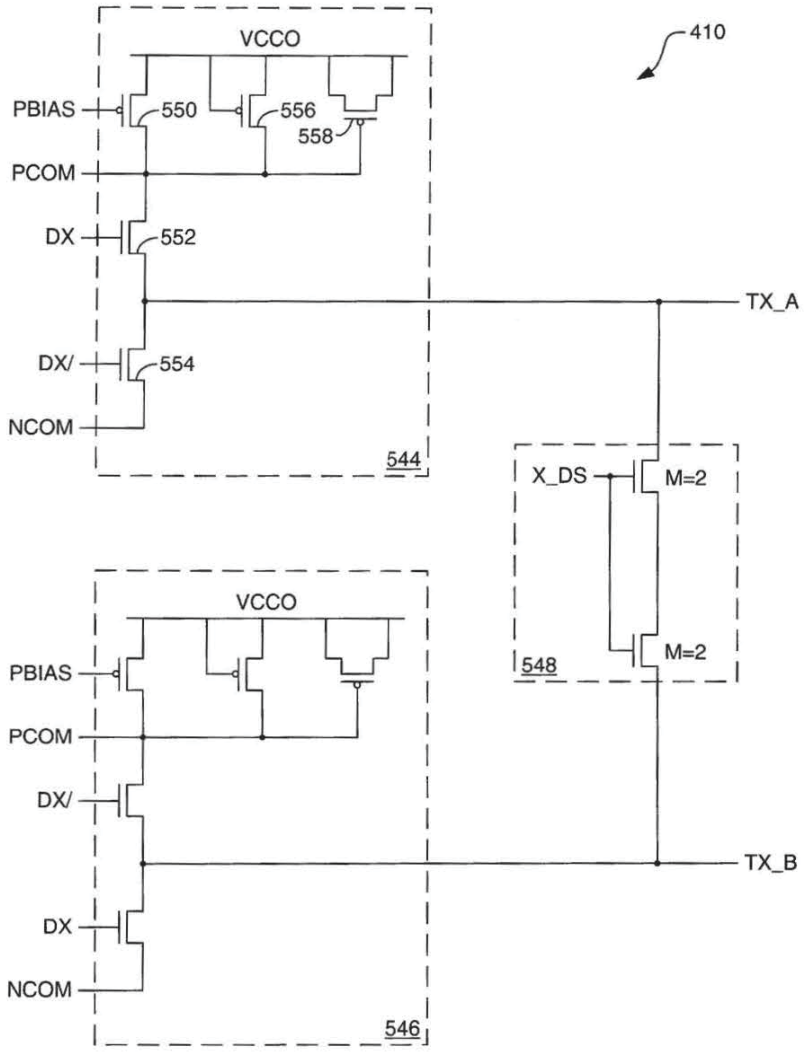
410
VCCO
PBIAS
550
556
558
PCOM
DX
552
TX_A
DX/
554
NCOM
544
X_DS
M=2
M=2
548
VCCO
PBIAS
PCOM
DX/
TX_B
DX
NCOM
546

FIG. 5C

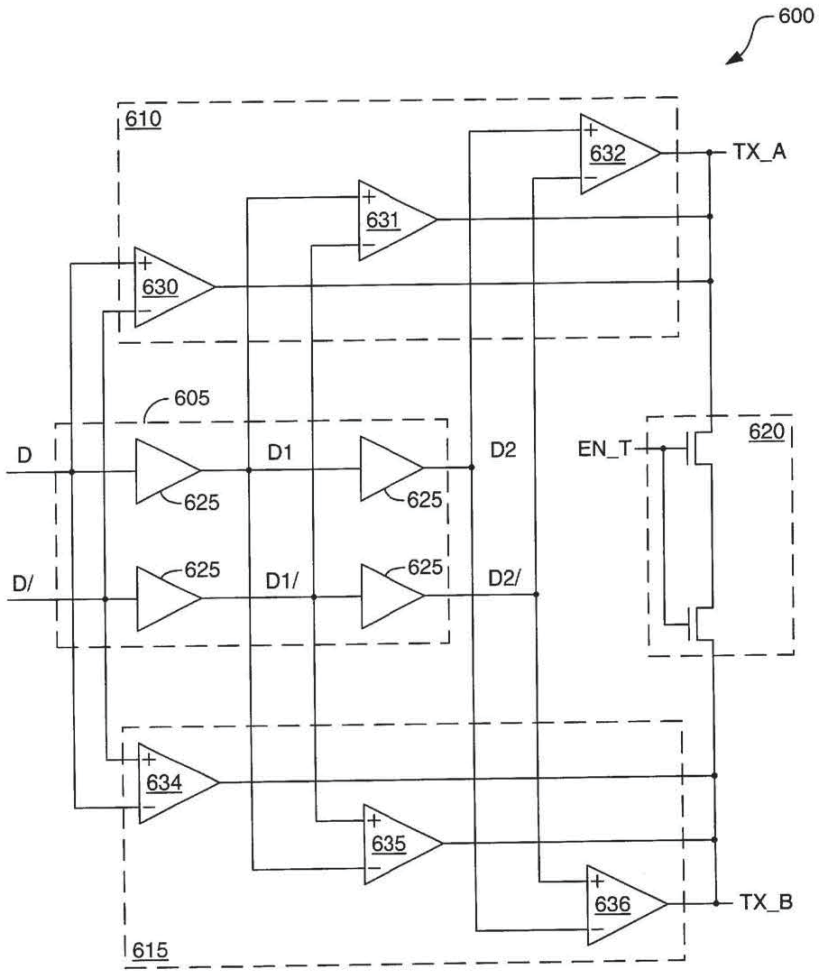
600
610
632
TX_A
631
630
605
D
D1
D2
EN_T
620
625
625
625
625
D/
D1/
D2/
634
635
636
TX_B
615

FIG. 6

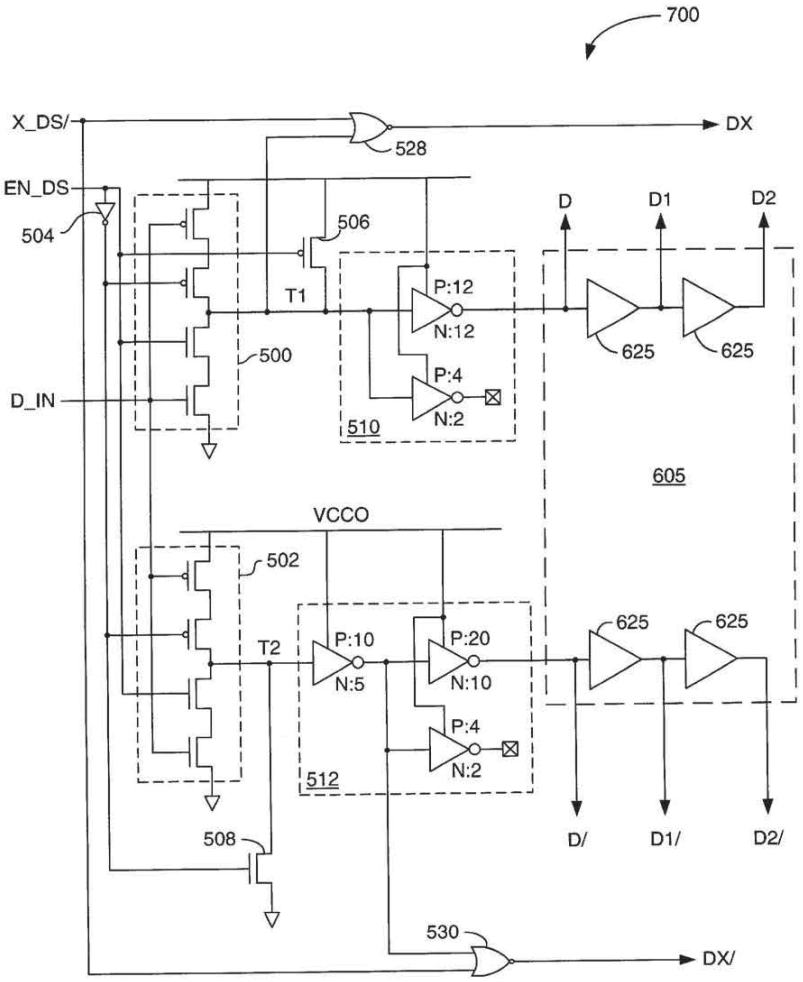
700
X_DS/
DX
528
EN_DS
504
506
D
D1
D2
T1
P:12
N:12
500
625
625
P:4
N:2
D_IN
510
605
VCCO
502
625
625
T2
P:10
N:5
P:20
N:10
P:4
N:2
512
508
D/
D1/
D2/
530
DX/

FIG. 7A

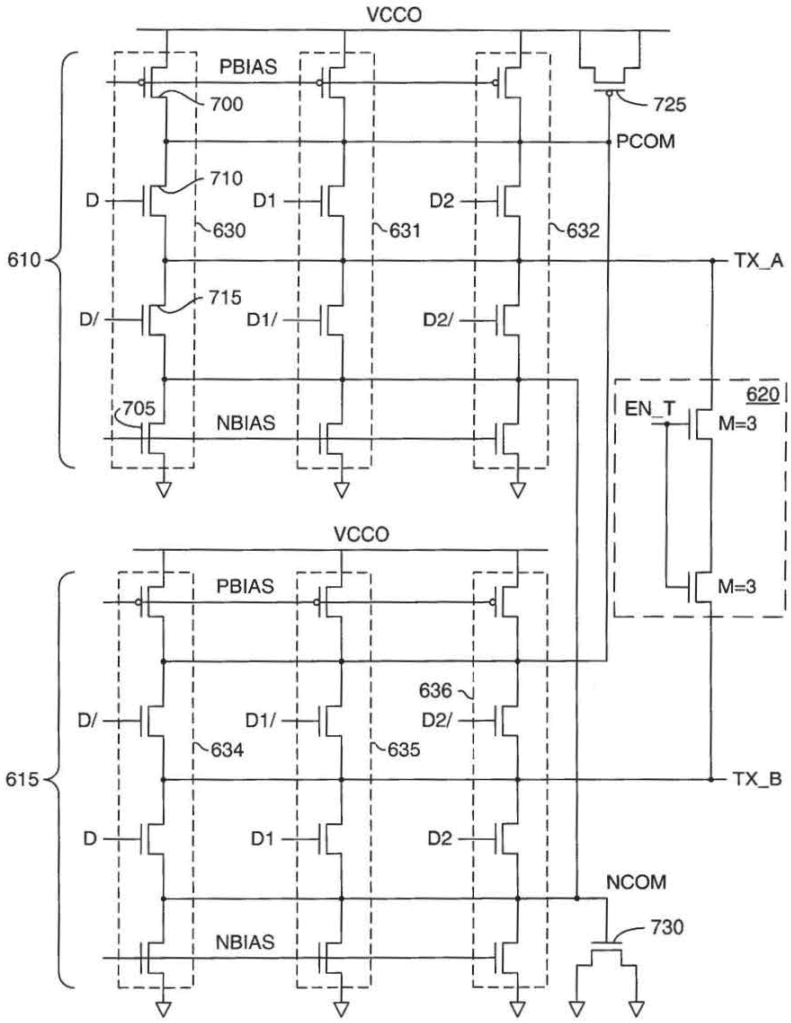
VCCO
PBIAS
700
725
PCOM
710
D
D1
D2
630
631
632
610
TX_A
715
D/
D1/
D2/
620
705
NBIAS
EN_T
M=3
M=3
VCCO
PBIAS
636
D/
D1/
D2/
634
635
615
TX_B
D
D1
D2
NCOM
730
NBIAS

FIG. 7B

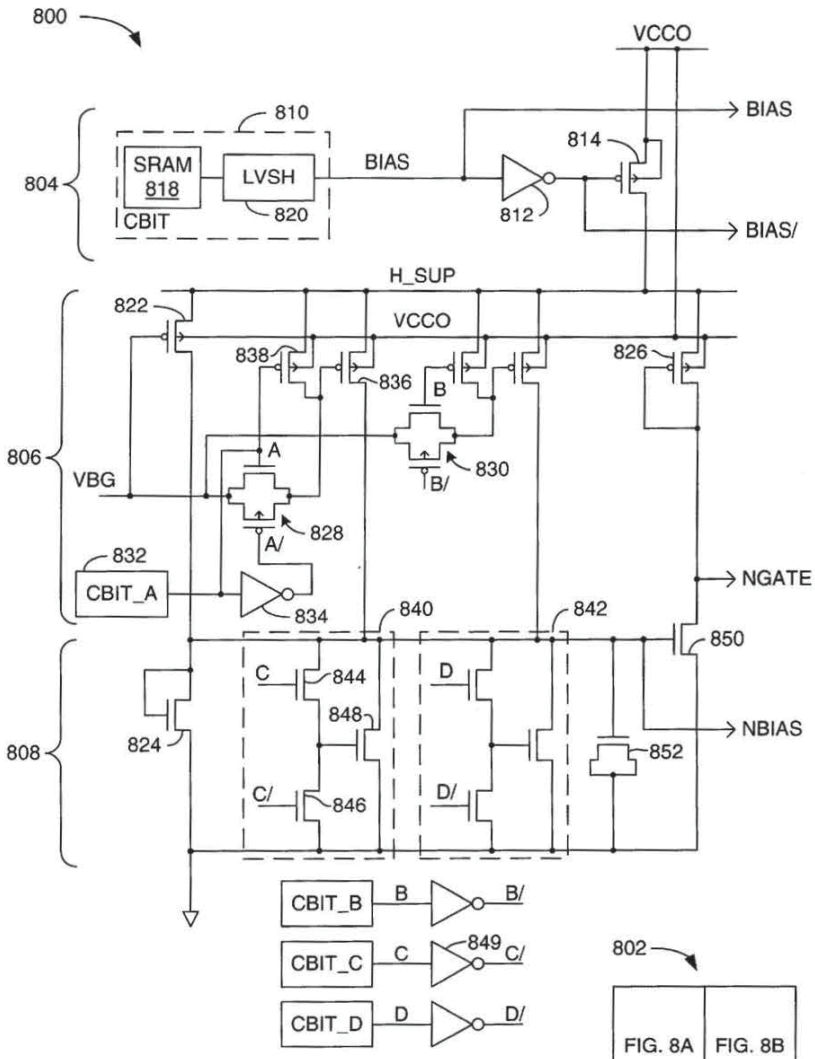
800
VCCO
BIAS
BIAS/
810
804
SRAM
818
LVSH
820
CBIT
BIAS
814
812
H_SUP
822
VCCO
838
836
826
B
B/
830
806
VBG
A
A/
828
832
CBIT_A
834
840
842
NGATE
850
808
824
C
844
848
C/
846
D
D/
852
NBIAS
CBIT_B
B
B/
CBIT_C
C
849
C/
CBIT_D
D
D/
802
FIG. 8A
FIG. 8B

FIG. 8A

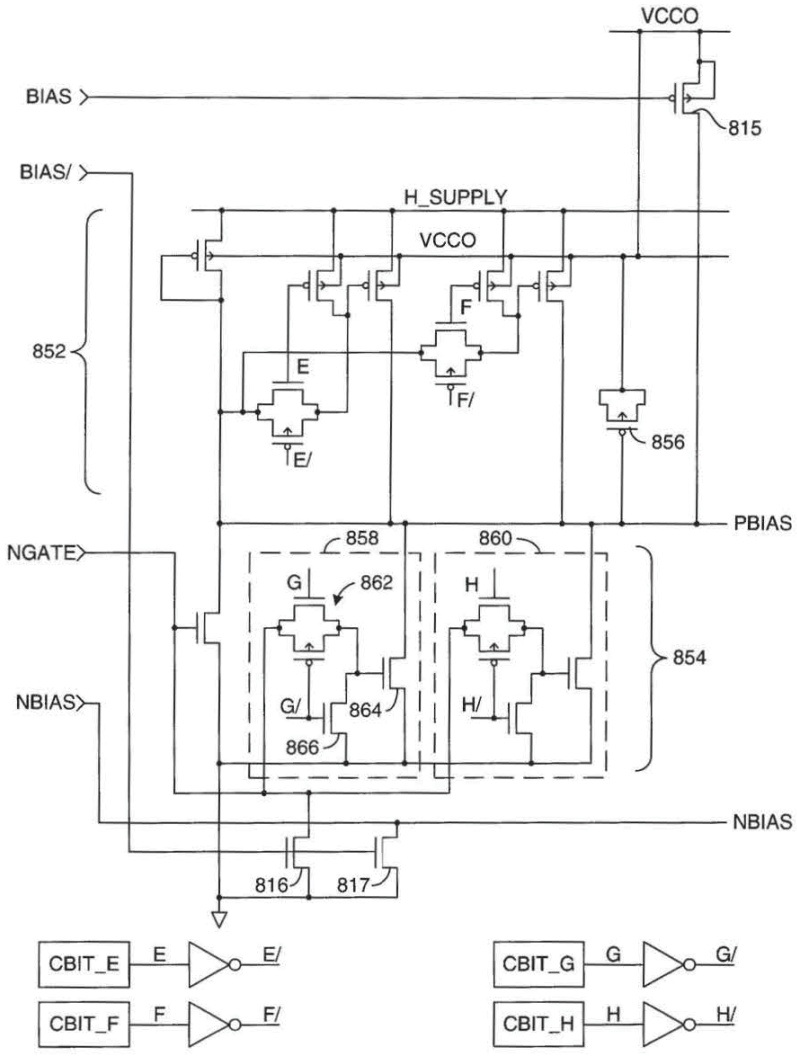
VCCO
BIAS
815
BIAS/
H_SUPPLY
VCCO
F
852
E
F/
E/
856
PBIAS
858
860
NGATE
G
862
H
854
NBIAS
G/
864
H/
866
NBIAS
816
817
CBIT_E
E
E/
CBIT_F
F
F/
CBIT_G
G
G/
CBIT_H
H
H/

FIG. 8B

CIRCUIT FOR PRODUCING LOW-VOLTAGE DIFFERENTIAL SIGNALS

FIELD OF THE INVENTION

This invention relates generally to methods and circuits for providing high-speed, low-voltage differential signals.

BACKGROUND

The Telecommunications Industry Association (TIA) published a standard specifying the electrical characteristics of low-voltage differential signaling (LVDS) interface circuits that can be used to interchange binary signals. LVDS employs low-voltage differential signals to provide high-speed, low-power data communication. The use of differential signals allows for cancellation of common-mode noise, and thus enables data transmission with exceptional speed and noise immunity. For a detailed description of this LVDS Standard, see "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits," TIA/EIA-644 (March 1996), which is incorporated herein by reference.

FIG. **1** (prior art) illustrates an LVDS generator **100** connected to an LVDS receiver **110** via a transmission line **115**. Generator **100** converts a single-ended digital input signal D_IN on a like-named input terminal into a pair of complementary LVDS output signals on differential output terminals TX_A and TX_B. A 100-ohm termination load RL separates terminals TX_A and TX_B, and sets the output impedance of generator **100** to the level specified in the above-referenced LVDS Standard.

LVDS receiver **110** accepts the differential input signals from terminals TX_A and TX_B and converts them to a single-ended output signal D_OUT. The LVDS Standard specifies the properties of LVDS receiver **110**. The present application is directed to differential-signal generators: a comprehensive discussion of receiver **110** is not included in the present application.

FIG. **2** (prior art) schematically depicts LVDS generator **100** of FIG. **1**. Generator **100** includes a preamplifier **200** connected to a driver stage **205**. Preamplifier **200** receives the single-ended data signal D_IN and produces a pair of complementary data signals D and D/ (signal names terminating in "/" are active low signals). Unless otherwise specified, each signal is referred to by the corresponding node designation depicted in the figures. Thus, for example, the input terminal and input signal to generator **100** are both designated D_IN. In each instance, the interpretation of the node designation as either a signal or a physical element is clear from the context.

Driver stage **205** includes a PMOS load transistor **207** and an NMOS load transistor **209**, each of which produces a relatively stable drive current in response to respective bias voltages PBIAS and NBIAS. Driver stage **205** additionally includes four drive transistors **211**, **213**, **215**, and **217**.

If signal D_IN is a logic one (e.g., 3.3 volts), preamplifier **200** produces a logic one on terminal D and a logic zero (e.g., zero volts) on terminal D/. The logic one on terminal D turns on transistors **211** and **217**, causing current to flow down through transistors **207** and **211**, up though termination load RL, and down through transistors **217** and **209** to ground (see the series of arrows **219**). The current through termination load RL develops a negative voltage between output terminals TX_A and TX_B.

Conversely, if signal D_IN is a logic zero, preamplifier **200** produces a logic zero on terminal D and a logic one on terminal D/. The logic one on terminal D/ turns on transistors **213** and **215**, causing current to flow down through transistor **207**, transistor **215**, termination load RL, transistor **213**, and transistor **209** to ground (see the series of arrows **221**). The current through termination load RL develops a positive voltage between output terminals TX_A and TX_B.

FIG. **3** (prior art) is a waveform diagram **300** depicting the signaling sense of the voltages appearing across termination load RL of FIGS. **1** and **2**. LVDS generator **100** produces a pair of differential output signals on terminals TX_A and TX_B. The LVDS Standard requires that the voltage between terminals TX_A and TX_B remain in the range of 250 mV to 450 mV, and that the voltage midway between the two differential voltages remains at approximately 1.2 volts. Terminal TX_A is negative with respect to terminal TX_B to represent a binary one and positive with respect to terminal B to represent a binary zero.

A programmable logic device (PLD) is a well-known type of IC that may be programmed by a user (e.g., a circuit designer) to perform specified logic functions. Most PLDs contain some type of input/output block (IOB) that can be configured either to receive external signals or to drive signals off chip. One type of PLD, the field-programmable gate array (FPGA), typically includes an array of configurable logic blocks (CLBS) that are programmably interconnected to each other and to the programmable IOBs. Configuration data loaded into internal configuration memory cells on the FPGA define the operation of the FPGA by determining how the CLBS, interconnections, block RAM, and IOBs are configured.

IOBs configured as output circuits typically provide single-ended logic signals to external devices. As with other types of circuits, PLDs would benefit from the performance advantages offered by driving external signals using differential output signals. There is therefore a need for IOBs that can be configured to provide differential output signals. There is also a need for LVDS output circuits that can be tailored to optimize performance for different loads.

SUMMARY

The present invention addresses the need for differential-signal output circuits that can be tailored for use with different loads. In accordance with one embodiment, one or more driver stages can be added, as necessary, to provide adequate power for driving a given load. Driver stages are added by programming one or more programmable elements, such as memory cells, fuses, and antifuses.

A differential driver in accordance with another embodiment includes a multi-stage delay element connected to a number of consecutive driver stages. The delay element produces two or more pairs of complementary input signals in response to each input-signal transition, each successive signal pair being delayed by some amount relative to the previous signal pair. The pairs of complementary signals are conveyed to respective driver stages, so that each driver stage successively responds to the input-signal transition. The output terminals of the driver stages are connected to one another and to the output terminals of the differential driver. The differential driver thus responds to each input-signal transition with increasingly powerful amplification. The progressive amplification produces a corresponding progressive reduction in output resistance, which reduces the noise normally associated with signal reflection.

Extendable and multi-stage differential amplifiers in accordance with the invention can be adapted for use in PLDs. In one embodiment, adjacent pairs of IOBs are each

provided with half of the circuitry required to produce LVDS signals. Adjacent pairs of IOBs can therefore be used either individually to provide single-ended input or output signals or can be combined to produce differential output signals.

This summary does not limit the invention, which is instead defined by the appended claims.

BRIEF DESCRIPTION OF THE FIGURES

FIG. **1** (prior art) illustrates an LVDS generator **100** connected to an LVDS receiver **110** via a transmission line **115**.

FIG. **2** (prior art) schematically depicts LVDS generator **100** of FIG. **1**

FIG. **3** (prior art) is a waveform diagram **300** depicting the signaling sense of the voltages appearing across termination load RL of FIGS. **1** and **2**.

FIG. **4** depicts an extensible differential amplifier **400** in accordance with an embodiment of the invention.

FIG. **5**A is a schematic diagram of predriver **405** of FIG. **4**.

FIG. **5**B is a schematic diagram of driver **415** of FIG. **4**.

FIG. **5**C is a schematic diagram of extended driver **410** of FIG. **4**.

FIG. **6** depicts a multi-stage driver **600** in accordance with another embodiment of the invention.

FIG. **7**A schematically depicts a predriver **700** in which a predriver is connected to delay circuit **605** of FIG. **6** to develop three complementary signal pairs.

FIG. **7**B schematically depicts differential-amplifier sequences **610** and **615** and termination load **620**, all of FIG. **6**.

FIGS. **8**A and **8**B schematically depict a programmable bias-voltage generator **800** in accordance with an embodiment of the invention.

DETAILED DESCRIPTION

FIG. **4** depicts an extensible differential amplifier **400** in accordance with an embodiment of the invention. Amplifier **400** includes a predriver **405** connected to a pair of driver stages **410** and **415**. The combination of predriver **405** and driver **415** operates as described above in connection with FIGS. **2** and **3** to convert the single-ended input on terminal D_IN into differential output signals on lines TX_A and TX_B. In accordance with the invention, driver **410** can be activated as needed to provide additional drive power. In one embodiment, drivers **410** and **415** reside within a pair of adjacent programmable IOBs (collectively labeled **417**) and lines TX_A and TX_B connect to the respective input/output (I/O) pads of the pair. This aspect of the invention is detailed below.

The program state of a configuration bit **420** determines whether amplifier **400** is enabled, and the program state of a second configuration bit **425** determines whether the driver stage of amplifier **400** is extended to include driver **410**. An exemplary configuration bit is described below in connection with FIG. **8**A.

If bit **420** is programmed to provide a logic one on "enable differential signaling" line EN_DS, then predriver **405** and driver **415** function in a manner similar to that described above in connection with FIG. **2**. If desired, the drive circuitry can be extended to include driver **410** by programming bit **425** to provide a logic one on "extended differential signaling" line X_DS. The signals on lines X_DS and EN_DS are logically combined using an AND gate **430** to produce an "enable termination load" signal EN_T to driver **415**. This signal and its purpose are described below in connection with FIG. **5**B.

FIG. **5**A is a schematic diagram of an embodiment of predriver **405** of FIG. **4**. Predriver **405** includes a pair of conventional tri-state drivers **500** and **502**. A conventional inverter **504** provides the complement of signal EN_DS.

Amplifier **400** is inactive when signals EN_DS and EN_DS/ are low and high, respectively. These logic levels cause tristate drivers **500** and **502** to disconnect input terminal D_IN from respective tristate output terminals T1 and T2. Signal EN_DS and its complementary signal EN_DS/ also connect terminals T1 and T2 to respective supply voltages VCCO and ground by turning on a pair of transistors **506** and **508**. Thus, terminals T1 and T2 do not change in response to changes on input terminal D_IN when differential signaling is disabled. In the case where amplifier **400** is implemented using IOBs in a programmable logic device, amplifier **400** may be disabled to allow the IOBs to perform some other input or output function.

Amplifier **400** is active when signals EN_DS and EN_DS/ are high and low, respectively. These logic levels cause tristate drivers **500** and **502** to connect input terminal D_IN to respective tristate output terminals T1 and T2. Signal EN_DS and its complementary signal EN_DS/ also disconnect terminals T1 and T2 from respective supply voltages VCCO and ground by turning off transistors **506** and **508**. Thus, terminals T1 and T2 change in response to signal D_IN when differential signaling is enabled.

Tristate output terminals T1 and T2 connect to the respective input terminals of an inverting predriver **510** and a non-inverting predriver **512**. Predriver **510** includes a pair of conventional inverters **514** and **516**. Inverter **514** produces a signal D, an inverted and amplified version of the signal on line T1; inverter **516** provides a similar signal to a test pin **518**. Predriver **512** includes three conventional inverters **520**, **522**, and **524**. Predriver **512** produces a signal D/, the complement of signal D. Inverter **524** provides a similar signal to a test pin **526**.

Each inverter within predrivers **510** and **512** is a CMOS inverter in which the ratios of the PMOS and NMOS transistors are as specified. These particular ratios were selected so that signals D and D/ transition simultaneously, or very nearly so. Different ratios may be appropriate, depending upon the process used to produce amplifier **400**. Adjusting layout and process parameters to produce synchronized complementary signals is within the skill of those in the art.

As discussed above in connection with FIG. **4**, amplifier **400** can be extended to include additional drive circuitry, which may be needed to drive some loads while remaining in compliance with the LVDS Standard. Returning to FIG. **5**A, a pair of NOR gates **528** and **530** facilitates this extension by producing a pair of complimentary extended-data signals DX and DX/ when signal X_DS/ is a logic zero, indicating the extended driver is enabled. Extended-data signal DX is substantially the same as signal D, and extended data signal DX/ is substantially the same as signal D/. Signals DX and DX/ are conveyed to extended driver **410**, the operation of which is detailed below in connection with FIG. **5**C.

FIG. **5**B is a schematic diagram of driver **415** of FIG. **4**. Driver **415** is similar to driver stage **205** of FIG. **2**, like-numbered elements being the same. Unlike driver **205**, however, driver **415** includes a programmable termination load **540**. Further, load transistors **207** and **209** of FIG. **2** are

replaced with pairs of parallel transistors, so that transistors **211** and **215** connect to VCCO via respective PMOS transistor **532** and **533**, instead of via a single transistor **207**, and transistors **213** and **217** connect to ground via respective NMOS transistors **534** and **535**, instead of via a single transistor **209**.

Employing pairs of load transistors allows driver **415** to be separated into two similar parts **536** and **538**, each associated with a respective one of terminals TX_A and TX_B. Such a configuration is convenient, for example, when driver **415** is implemented on a PLD in which terminals TX_A and TX_B connect to neighboring I/O pins. Each part **536** and **538** can be implemented as a portion of the IOB (not shown) associated with the respective one of terminals TX_A and TX_B. Termination load **540** can be part of either IOB, neither IOB, or can be split between the two. In one embodiment, transistor **542** is included in the IOB that includes part **536**, and transistor **543** is included in the IOB that includes part **538**.

Programmable termination load **540** includes a pair of transistors **542** and **543**, the gates of which connect to terminal EN_T. As shown in FIG. **4**, the signal EN_T is controlled through AND gate **430** by configuration bits **420** and **425**. Termination load **540** is active (conducting) only when differential signaling is enabled in the non-extended mode. This condition is specified when configuration bit **420** is set to a logic one and configuration bit **425** is set to a logic zero.

Driver **415** includes a number of terminals that provide appropriate bias voltages. Terminals PBIAS and NBIAS provide respective bias levels establish the gain driver **415**, and common terminals PCOM and NCOM conventionally establish the high and low voltage levels on output terminals TX_A and TX_B. Driver **415** shares the bias and common terminals with extended driver **410** (See FIG. **5**C).

The bias levels PBIAS and NBIAS are important in defining LVDS signal quality. In one embodiment, NMOS transistors **534** and **535** are biased to operate in saturation to sink a relatively stable current, whereas PMOS transistors **532** and **533** are biased to operate in a linear region. Operating transistors **532** and **533** in a linear region reduces the output resistances of those devices, and the reduced resistance tends to dissipate signal reflections returning to terminals TX_A and TX_B. Reduced reflections translate into reduced noise, and reduced noise allows signals to be conveyed at higher data rates. Circuits for developing appropriate bias levels for the circuits of FIGS. **5**A–**7**B are discussed below in connection with FIGS. **8**A and **8**B.

FIG. **5**C is a schematic diagram of one embodiment of extended driver **410** of FIG. **4**. Extended driver **410** includes a pair of driver stages **544** and **546** and a programmable termination load **548**. Driver stages **544** and **546** can be included, for example, in respective adjacent IOBs on a PLD. Termination load **548** can be part of either IOB, neither IOB, or can be split between the two. The various terminals of FIG. **5**C are connected to like-named terminals of FIGS. **5**A and **5**B.

Driver stage **544** includes a PMOS load transistor **550**, a pair of NMOS differential-driver transistors **552** and **554** having their gates connected to respective extended-driver input signals DX and DX/, a diode-connected PMOS transistor **556**, and a PMOS transistor **558** connected as a capacitor **14** between terminal VCCO and terminal PCOM. Transistors **550**, **552**, and **554** combined amplify the extended-driver signals DX and DX/ to produce an amplified output signal on output terminal TX_A. In one embodiment, transistor **556** is diode-connected between terminals PCOM and VCCO to establish the appropriate level for line PCOM, which is common to both drivers **410** and **415**. Finally, transistor **558** can be sized or eliminated as desired to minimize noise on line PCOM. Driver stage **546** is identical to driver stage **544**, except that lines DX and DX/ are connected to the opposite differential driver transistors. Consequently, the signals on output terminals TX_A and TX_B are complementary. Driver stages **544** and **546** thus supplement the drive strength provided by driver stage **415**.

As shown in FIG. **4**, the extend-differential-signaling signal X_DS is a logic one when CBIT **425** is programmed. However, programming CBIT **425** causes AND gate **430** to output a logic zero, disabling termination load **532** of FIG. **5**B. Thus, programming CBIT **425** substitutes termination load **548** for termination load **532**, thereby increasing the termination load resistance to an appropriate level. In one embodiment, the resistance of termination load **532** is selected so that the resulting output signal conforms to the LVDS Standard.

FIG. **6** depicts a multi-stage driver **600** in accordance with another embodiment of the invention. Driver **600** includes a multi-stage delay circuit **605**, a first sequence of differential amplifiers **610**, a second sequence of differential amplifiers **615**, and a termination load **620**. For illustrative purposes, the amplifiers of sequences **610** and **615** are referred to as "high-side" and "low-side" amplifiers, respectively. In different embodiments, each amplifier sequence **610** and **615** can be implemented as a portion of the IOB (not shown) associated with the respective one of terminals TX_A and TX_B. Termination load **620** can be part of either IOB, neither IOB, or can be split between the two.

Delay circuit **605** receives a pair of complementary signals D and D/ on a like-named pair of input terminals. A sequence of delay elements—conventional buffers **625** in the depicted example—provides a first pair of delayed complementary signals D1 and D1/ and a second pair of delayed complementary signals D2 and D2/.

Sequence **610** includes three differential amplifiers **630**, **631**, and **632**, the output terminals of which connect to one another and to output terminal TX_A. The differential input terminals of each of these high-side amplifiers connect to respective complementary terminals from delay circuit **605**. That is, the non-inverting (+) and inverting (−) terminals of differential amplifier **630** connect to respective input terminals D and D/, the non-inverting and inverting terminals of differential amplifier **631** connect to respective input terminals D1 and D1/, and the non-inverting and inverting terminals of differential amplifier **632** connect to respective input terminals D2 and D2/. When the signal on terminal D transitions from low to high, each of amplifiers **630**, **631**, and **632** consecutively joins in pulling the voltage level on terminal TX_A high as the signal edges on terminals D and D/ propagate through delay circuit **605**. Conversely, when the signal on terminal D transitions from high to low, each of amplifiers **630**, **631**, and **632** consecutively joins in pulling the voltage level on terminal TX_A low.

Sequence **615** includes three differential amplifiers **634**, **635**, and **636**, the output terminals of which connect to one another and to terminal TX_B. Sequence **615** is similar to sequence **610**, except that the differential input terminals of the various low-side differential amplifiers are connected to opposite ones of the complementary signals from delay circuit **605**. Thus, when the signal on terminal D transitions from low to high, each of amplifiers **634**, **635**, and **636** consecutively joins in pulling the voltage level on terminal

TX_B low as the signal edges on terminals D and D/ propagate through delay circuit **605**, and when the signal on terminal D transitions from high to low, each of amplifiers **634**, **635**, and **636** consecutively joins in pulling the voltage level on terminal TX_B high.

Driver stage **600** is similar to driver stage **415** of FIGS. **4** and **5**A, except that driver stage **600** progressively increases the drive strength used to provide amplified signals across termination load **620**, and consequently progressively reduces the output resistance of driver stage **600**. Progressively reducing the output resistance of amplifier **600** reduces the amplitude of reflected signals. This effect, in turn, reduces the noise and increases the useable data rate of the LVDS circuitry. While illustrated as having three driver stages, other embodiments of amplifier **600** include more or fewer stages. FIG. **7**A schematically depicts a predriver **700** in which predriver **405**, detailed in FIG. **5**A, is connected to delay circuit **605** of FIG. **6** to develop the three complementary signal pairs (e.g., D and D/) of FIG. **6**. The various elements of predriver **405** are described above in connection with FIG. **5**A, like-numbed elements being identical. In one embodiment, each buffer **625** is an instance of non-inverting delay circuit **512**. FIG. **7**B schematically depicts differential-amplifier sequences **610** and **615** and termination load **620**, all of FIG. **6**. The differential amplifiers in sequences **610** and **615** are substantially identical, except the D and D/ input terminals are reversed. The following description is limited to a single differential amplifier (**630**) for brevity. Differential amplifier **630** includes a PMOS load transistor **700**, an NMOS load transistor **705**, and a pair of active transistors **710** and **715** having their respective gates connected to data inputs D and D/. One embodiment of amplifier **400** of FIG. **4** employs driver stage **600** in place of driver **415** (detailed in FIG. **5**B). Amplifier sequence **610** may include a capacitor **725** between PCOM and VCCO, and amplifier sequence **615** may include a capacitor **730** connected between NCOM and ground. These capacitors can be sized to minimize noise. FIGS. **8**A and **8**B schematically depict a programmable bias-voltage generator **800** in accordance with an embodiment of the invention. A key **802** in the bottom right-hand corner of FIG. **8**A shows the relative arrangement of FIGS. **8**A and **8**B.

The portion of generator **800** depicted in FIG. **8**A may be divided into three general areas: bias-enable circuitry **804**, NBIAS pull-up circuitry **806**, and NBIAS pull-down circuitry **808**. As their respective names imply, bias-enable circuitry **804** determines whether bias generator **800** is active, NBIAS pull-up circuitry **806** can be used to raise the NBIAS voltage level, and NBIAS pull-down circuitry **808** can be used to reduce the NBIAS voltage level. The NBIAS pull-up and pull-down circuitry are programmable to allow users to vary the NBIAS voltage as desired.

Bias-enable circuitry **804** includes a configuration bit (CBIT) **810**, an inverter **812**, a PMOS transistor **814**, and, in FIG. **8**B, a PMOS transistor **815** and a pair of NMOS transistors **816** and **817**. CBIT **810** is conventional, in one embodiment including an SRAM configuration memory cell **818** connected to a level-shifter **820**. Level-shifter **820** is used because bias generator **800** is a portion of the output circuitry of a PLD, and operates at higher voltage (e.g., 3.3 volts) than the core circuitry (e.g., 1.5 volts) of the PLD: level-shifter **820** increases the output voltage of SRAM cell **816** to an appropriate voltage level. Some embodiments that employ lower core voltages use thicker gate insulators in the transistors of the I/O circuitry. The gate insulators of differing thickness can be formed using a conventional dual-oxide process. In one embodiment in which the circuits depicted in FIGS. **5**A–**8**B are part of the output circuitry of a PLD, each of the depicted devices employs relatively thick gate insulators.

Generator **800** is activated by programming SRAM cell **818** to include a logic one, thereby causing bias-enable circuitry **804** to output a logic one on line BIAS. This logic one connects high-supply-voltage line H_SUP to supply voltage VCCO through transistor **814** and disconnects line PBIAS from VCCO to enable line PBIAS to carry an appropriate bias voltage. The inverted signal BIAS/ from inverter **812**, a logic zero when active, disconnects lines NBIAS and NGATE from ground, thereby allowing those lines to carry respective bias voltages. The logic levels on lines PBIAS and NBIAS are one and zero, respectively, when SRAM cell **818** is set to logic zero.

NBIAS pull-up circuitry **806** has an input terminal VBG connected to a conventional band-gap reference, or some other suitable voltage reference. The voltage level and line VBG turns on a PMOS transistor **822** that, in combination with diode-connected transistors **824** and **826**, produces bias voltage levels on lines NGATE and NBIAS. Terminal VBG also connects to a pair of transmission gates **828** and **830**, each consisting of NMOS and PMOS transistors connected in parallel. The transmission gates are controlled by configuration bits similar to CBIT **810**. For example, transmission gate **828** can be turned on by programming CBIT_A to contain a logic one. The logic one produces a logic one on line A and, via an inverter **834**, a logic zero on line Al. Transmission gate **828** passes the reference voltage on line VBG to the gate of a PMOS transistor **836**, thereby reducing the resistance between VCCO and line NBIAS; consequently, the voltage level on line NBIAS rises. Transistor **838** can be turned on and both of transmission gate **828** and transistor **836** can be turned off by programming CBIT_A to contain a logic zero. Transmission gate **830** operates in the same manner as transmission gate **828**, but is controlled by a different CBIT (CBIT_B) and an associated inverter. One or both of transmission gates **828** and **830** can be turned on to raise the voltage level on line NBIAS.

NBIAS pull-down circuitry **808** includes a pair of programmable pull-down circuits **840** and **842** that can be programmed independently or collectively to reduce the bias voltage on terminal NBIAS. Pull-down circuits **840** and **842** work the same way, so only circuit **840** is described.

Pull-down circuit **840** includes three transistors **844**, **846**, and **848**. The gates of transistors **844** and **846** connect to terminals C and C/, respectively, from a configuration bit CBIT_C and an associated inverter **849**. When CBIT_C is programmed to contain a logic zero, transistors **844** and **848** are turned off, isolating line NBIAS from ground; when CBIT_C is programmed to contain a logic one, transistors **844** and **848** are turned on and transistor **846** turned off. The reduced resistance through transistor **848** reduces the voltage on line NBIAS.

Any change in the bias voltage on line NBIAS results in a change in voltage on line NGATE via a transistor **850**. A transistor **852** connected between line NBIAS and ground is an optional capacitor that can be sized or eliminated as desired.

The portion of bias-voltage generator **800** depicted in FIG. **8**A adjusts the level of NBIAS; the portion depicted in FIG. **8**B adjusts the level of PBIAS. Referring now to FIG. **8**B, the portion of FIG. **8**B includes PBIAS pull-up circuitry **852** and PBIAS pull-down circuitry **854**. PBIAS pull-up circuitry **852** operates in the same manner as NBIAS pull-up circuitry **806** of FIG. **8**A to raise the level of the bias voltage

on line PBIAS. A pair of configuration bits CBIT_E and CBIT_F and associated inverters control circuitry **852**. A capacitor **856** can be sized or eliminated as necessary.

PBIAS pull-down circuitry **854** includes a pair of programmable pull-down circuits **858** and **860** that can be programmed independently or collectively to reduce the bias voltage on terminal PBIAS. Pull-down circuits **858** and **860** work the same way, so only circuit **858** is described.

Pull-down circuit **858** includes a transmission gate **862** and a pair of transistors **864** and **866**. With CBIT_G programmed to contain a logic zero, transmission gate **862** is off, transistor **866** on, and transistor **864** off; with CBIT_G programmed to contain a logic one, transistor **866** is off, and transmission gate **862** passes the bias voltage NGATE to the gate of transistor **864**, thereby turning transistor **864** on. This reduces the voltage level on line PBIAS.

The present invention can be adapted to supply complementary LVDS signals to more than one LVDS receiver. For details of one such implementation, see "Multi-Drop LVDS with Virtex-E FPGAs," XAPP231 (Version 1.0) by Jon Brunetti and Brian Von Herzen Sep. 23, 1999, which is incorporated herein by reference.

While the present invention has been described in connection with specific embodiments, variations of these embodiments will be obvious to those of ordinary skill in the art. For example, while described in the context of SRAM-based FPGAS, the invention can also be applied to other types of PLDs that employ alternate programming technologies, and some embodiments can be used in non-programmable circuits. Moreover, the present invention can be adapted to convert typical dual-voltage logic signals to other types of differential signals, such as those specified in the Low-Voltage, Pseudo-Emitter-Coupled Logic (LVPECL) standard. Therefore, the spirit and scope of the appended claims should not be limited to the foregoing description.

What is claimed is:

1. A differential amplifier comprising:

a. a first differential-amplifier stage having:
   i. first and second differential input terminals adapted to receive a differential input signal; and
   ii. first and second differential output terminals;

b. a second differential-amplifier stage having:
   i. third and fourth differential input terminals adapted to receive the differential input signal;
   ii. third and fourth differential output terminals connected to the first and second differential output terminals; and
   iii. an amplifier-enable terminal; and

c. a programmable memory cell capable of maintaining a programmed state and a deprogrammed state, the memory cell having a memory-cell output terminal connected to the amplifier-enable terminal;

d. wherein the second differential amplifier stage amplifies the input signal when the memory cell is in the programmed state and does not amplify the input signal when the memory cell is in the deprogrammed state.

2. The differential amplifier of claim **1**, wherein the memory cell stores a voltage representative of a logic one when in the programmed state.

3. The differential amplifier of claim **1**, further comprising a predriver having:

a. a data input terminal adapted to receive an input data signal; and

b. first and second complementary output terminals connected to respective ones of the first and second differential input terminals.

4. The differential amplifier of claim **3**, wherein the predriver further comprises:

a. a first tri-state buffer having a first tri-state input terminal connected to the data input terminal;

b. a second tri-state buffer having a second tri-state input terminal connected to the data input terminal;

c. an inverter having an inverter input terminal connected to the data input terminal and an inverter output terminal connected to the first complementary output terminal; and

d. a non-inverting delay stage having a delay-stage input terminal connected to the data input terminal and a delay-stage output terminal connected to the second complementary output terminal.

5. The differential amplifier of claim **4**, wherein the inverter exhibits a first signal propagation delay and the non-inverting delay stage exhibits a second signal propagation delay substantially equal to the first signal propagation delay.

6. The differential amplifier of claim **1**, further comprising a programmable termination load connected between the first and second differential output terminals.

7. The differential amplifier of claim **6**, wherein the termination load includes a termination-load enable terminal connected to the memory-cell output terminal.

8. The differential amplifier of claim **6**, further comprising a second termination load connected between the first and second differential output terminals.

9. The differential amplifier of claim **8**, wherein the second termination load is programmable.

10. An amplifier comprising:

a. first and second differential input terminals adapted to receive first and second complementary input signals;

b. a first high-side differential amplifier having:
   i. a first high-side differential amplifier input terminal connected to the first differential input terminal;
   ii. a second high-side differential amplifier input terminal connected to the second differential input terminal; and
   iii. a first high-side differential-amplifier output terminal;

c. a first low-side differential amplifier having a first low-side differential amplifier input terminal connected to the first differential input terminal and a second low-side differential amplifier input terminal connected to the second differential input terminal;

d. a delay element having:
   i. a first delay-element input terminal connected to the first differential input terminal and a first delay-element output terminal, the delay element adapted to provide a delayed version of the first complementary input signal on the first delay-element output terminal; and
   ii. a second delay-element input terminal connected to the second differential input terminal and a second delay-element output terminal, the delay element adapted to provide a delayed version of the second complementary input signal on the second delay-element output terminal;

e. a second high-side differential amplifier having:
   i. a third high-side differential amplifier input terminal connected to the first delay-element output terminal;
   ii. a fourth high-side differential amplifier input terminal connected to the second delay-element output terminal; and
   iii. a second high-side differential-amplifier output terminal connected to the first high-side differential-amplifier output terminal; and

f. a second low-side differential amplifier having:

i. a third low-side differential amplifier input terminal connected to the first delay-element output terminal;

ii. a fourth low-side differential amplifier input terminal connected to the second delay-element output terminal; and

iii. a second low-side differential-amplifier output terminal connected to the first low-side differential-amplifier output terminal.

11. The amplifier of claim **10**, further comprising a termination load connected between the first high-side and first low-side differential-amplifier output terminals.

12. The amplifier of claim **11**, further comprising a programmable memory cell capable of maintaining a programmed state and a deprogrammed state, the memory cell having a memory-cell output terminal connected to the termination load.

13. The amplifier of claim **10**, further comprising a second delay element having:

a. a third delay-element input terminal connected to the first delay-element output terminal of the first-mentioned delay element;

b. a fourth delay-element input terminal connected to the second delay-element output terminal of the first-mentioned delay element;

c. a third delay-element output terminal; and

d. a fourth delay-element output terminal.

14. The amplifier of claim **13**, further comprising a third low-side differential amplifier and a third high-side differential amplifier, each having a pair of input terminals connected to respective ones of the third and forth delay-element output terminals.

15. The amplifier of claim **14**, wherein the third low-side differential amplifier includes a third low-side differential-amplifier output terminal connected to the first low-side differential-amplifier output terminal, and wherein the third high-side differential amplifier includes a third high-side differential-amplifier output terminal connected to the first high-side differential-amplifier output terminal.

16. The amplifier of claim **10**, wherein the first high-side differential amplifier comprises:

a. an input transistor having a control terminal connected to the first high-side differential-amplifier input terminal, a first input-transistor current-handling terminal connected to the first high-side differential-amplifier output terminal, and a second input-transistor current-handling terminal; and

b. a load transistor having a control terminal connected to a bias voltage, a first load-transistor current-handling terminal connected to a power terminal, and a second load-transistor current-handling terminal connected to the second input-transistor current-handling terminal.

17. The amplifier of claim **16**, further comprising a programmable bias generator adapted to provide the bias voltage on a bias-generator output terminal connected to the control terminal of the load transistor.

18. The amplifier of claim **16**, wherein the first high-side differential amplifier further comprises:

a. a second input transistor having a second control terminal connected to the second high-side differential-amplifier input terminal, a first input-transistor current-handling terminal connected to the first high-side differential-amplifier output terminal, and a second input-transistor current-handling terminal; and

b. a second load transistor having a control terminal connected to a second bias voltage, a first load-transistor current-handling terminal connected to a second power terminal, and a second load-transistor current-handling terminal connected to the second input-transistor current-handling terminal.

19. The amplifier of claim **18**, further comprising a programmable bias generator adapted to provide the first-mentioned bias voltage on a first bias-generator output terminal and the second bias voltage on a second bias-generator output terminal.

20. A programmable logic device comprising:

a. a predriver having:

i. a data input terminal adapted to receive an input data signal; and

ii. complementary first and second predriver output terminals;

b. first and second input/output pins adapted to convey signals from the programmable logic device;

c. a first programmable output block including a first differential amplifier, the first differential amplifier having a first differential-amplifier input terminal connected to the first predriver output terminal, a second differential-amplifier input terminal connected to the second predriver output terminal, and a first differential-amplifier output terminal connected to the first input/output pin; and

d. a second programmable output block including a second differential amplifier, the second differential amplifier having a third differential-amplifier input terminal connected to the first predriver output terminal and a fourth differential-amplifier input terminal connected to the second predriver output terminal, and a second differential-amplifier output terminal connected to the second input/output pin.

21. The programmable logic device of claim **20**, wherein the first pin is adjacent the second pin.

22. The programmable logic device of claim **20**, further comprising:

a. an enable terminal connected to at least one of the predriver and the first and second programmable output blocks; and

b. a programmable memory cell connected to the enable terminal.

23. The programmable logic device of claim **20**, further comprising a termination load connected between the first and second input/output pins.

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