Jc820 U.S. PTO
09/655168
09/05/00

Class	Subclass
326	83.

ISSUE CLASSIFICATION

PATENT NUMBER

6366128

6366128

U.S. UTILITY Patent Application

O.I.P.E. GH SCANNED BK③ Q.A. CK	PATENT DATE APR 0 2 2002

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/655168		326	83	2819	D. Chang

APPLICANTS
Atul Ghia
Suresh Menon
David Schultz

TITLE
Circuit for producing low-voltage differential signals

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)						
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
326	83	326	44	40	49			
INTERNATIONAL CLASSIFICATION								
H03K 19/094								
H03K 19/173								

☐ Continued on Issue Slip Inside File Jacket

2/25/02 Formal Drawings (10 shts) set 1 9/5/00

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
	10	12	4	23	1
☐ The term of this patent subsequent to ______ (date) has been disclaimed.	Daniel D. Chang 8/30/01 (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED 9/10/01	
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. ______	Michael J. Tokar Michael Tokar Supervisory Patent Examiner Technology Center 2800 9/6/01 (Primary Examiner) (Date)			ISSUE FEE CW	
				Amount Due 1240	Date Paid 12-7-01
☐ The terminal ___months of this patent have been disclaimed.	A Lange 9/11/01 (Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER L68	

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Formal Drawings (__ shts) set__

Issue Fee

(FACE)

PATENT APPLICATION

09655168

jc820 U.S. PTO
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INITIALS
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CONTENTS

No.		Date Received (Incl. C. of M.) or Date Mailed	No.		Date Received (Incl. C. of M.) or Date Mailed
1.	Application 10 papers.	9-8-00	42.		
2.	NTS		43.		
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ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	mg		9/3/01
O.I.P.E. CLASSIFIER		8	9/7/00
FORMALITY REVIEW			
RESPONSE FORMALITY REVIEW		6808	10/24/01

INDEX OF CLAIMS

✓ .... Rejected		N .... Non-elected	
= .... Allowed		I .... Interference	
— (Through numeral)... Canceled		A .... Appeal	
÷ .... Restricted		O .... Objected	

Claim Final	Claim Original	Date 8/3/01	Date	Date	Date	Date	Date	Date	Date	Date	Date
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SEARCHED

Class	Sub.	Date	Exmr.
326	83 86 87 38 40 44 45 46 49 30	8/29/01	OC

SEARCH NOTES
(INCLUDING SEARCH STRATEGY)

	Date	Exmr.
EAST	8/29/01	OC

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
Searched	above	8/29/01	OC

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UNITED STATES PATENT AND TRADEMARK OFFICE
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Bib Data Sheet

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/655,168	09/05/2000 RULE –	326	2819	X-784 US

APPLICANTS

Atul V. Ghia, San Jose, CA ;
Suresh M. Menon, Sunnyvale, CA ;
David P. Schulz, San Jose, CA ;

** CONTINUING DATA *************************
DC None

** FOREIGN APPLICATIONS ********************
DC None

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 10/23/2000

Foreign Priority claimed ☐ yes ☑ no 35 USC 119 (a-d) conditions met ☐ yes ☑ no ☐ Met after Allowance Verified and Acknowledged David Chang Examiner's Signature Initials	STATE OR COUNTRY CA	SHEETS DRAWING 10	TOTAL CLAIMS 23	INDEPENDENT CLAIMS 3

ADDRESS

Edel M Young
Xilinx Inc
2100 Logic Drive
San Jose ,CA 95124

TITLE

Circuit for producing low-voltage differential signals

FILING FEE RECEIVED 744	FEES: Authority has been given in Paper No. ________ to charge/credit DEPOSIT ACCOUNT No. ________ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other ____________ ☐ Credit

PATENT APPLICATION SERIAL NO. ____________________

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

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09/14/2000 MPEOPLES 00000035 240040   09655168
01 FC:101          690.00 CH
02 FC:103           54.00 CH
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PTO-1556
(5/87)

*U.S. GPO: 1999-459-082/19144

jc922 U.S. PTO
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jc929 U.S. PTO
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PTO/SB/05 (4/98)
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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Atty. Docket No.	X-784 US
First Inventor or Appl. Identifier	Atul V. Ghia
Title	Circuit for Producing Low-Voltage Differential Signals
Express Mail Label No.	EL539651200US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ *Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original, and a duplicate for fee processing)
2. ☒ Specification [Total Pages 26]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. ☒ Drawing(s) (35 USC 113) [Total Sheets 10]
4. Oath or Declaration [Total Pages 2]
   a. ☒ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR §1.63(d)) (for continuation/divisional with Box 16 completed)
      i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR § §1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. ☐ Microfiche Computer Program (Appendix)
6. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. ☐ Computer Readable Copy
   b. ☐ Paper Copy (identical to computer copy)
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☒ Assignment Papers (cover sheet & document(s))
8. ☐ 37 CFR §3.73(b) Statement (when there is an assignee) ☐ Power of Attorney
9. ☐ English Translation Document (if applicable)
10. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
13. ☐ *Small Entity Statement(s) (PTO/SB/09-12) ☐ Statement filed in prior application, Status still proper and desired
14. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
15. ☐ Other: ....

16. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information below and in a preliminary amendment:
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: ____________
Prior application information: Examiner ____________ Group / Art Unit: ____________

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. CORRESPONDENCE ADDRESS

☒ Customer Number or Bar Code Label **24309** (Insert Customer No. or Attach bar code label here) or ☐ Correspondence address below

Name	Attn: Edel M. Young				
Address					
City		State		Zip Code	
Country		Telephone	408-879-4969	Fax	408-377-6137

Name (Print/Type)	Edel M. Young	Registration No. (Attorney/Agent)	32,451
Signature	Lois D. Cartier Reg. No. 40,941 for Edel M. Young	Date	September 5, 2000

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FEE TRANSMITTAL for FY 2000

Patent fees are subject to annual revision
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12. See 37 C.F.R. §§ 1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT ($) 784.00

Complete if Known

Application Number	Not Yet Known
Filing Date	September 5, 2000
First Named Inventor	Atul V. Ghia
Examiner Name	Not Yet Known
Group / Art Unit	Not Yet Known
Attorney Docket No.	X-784

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 24-0040
Deposit Account Name: XILINX, INC.

☐ Charge the Issue Fee Required Under 37 CFR §§ 1.16 and 1.17

2. ☐ **Payment Enclosed:** ☐ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Fee ($)	Fee Description	Fee Paid
101	760	Utility filing fee	$690
106	330	Design filing fee	
107	540	Plant filing fee	
108	760	Reissue filing fee	
114	150	Provisional filing fee	

SUBTOTAL (1) ($) 690.00

2. EXTRA CLAIM FEES

			Extra		Fee from below		Fee Paid
Total Claims	23	-20** =	3	X	18	=	$54
Indep. Claims	3	- 3** =	0	X		=	$0
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**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Fee ($)	Fee Description
103	18	Claims in excess of 20
102	78	Independent claims in excess of 3
104	260	Multiple dependent claim, if not paid
109	78	**Reissue independent claims over original patent
110	18	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 54.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Fee ($)	Fee Description	Fee Paid
105	130	Surcharge - late filing fee or oath	
127	50	Surcharge - late provisional filing fee or cover sheet.	
147	2,520	For filing a request for reexamination	
112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	Requesting publication of SIR after Examiner action	
115	110	Extension for reply within first month	
116	380	Extension for reply within second month	
117	870	Extension for reply within third month	
118	1,360	Extension for reply within fourth month	
128	1,850	Extension for reply within fifth month	
119	300	Notice of Appeal	
120	300	Filing a brief in support of an appeal	
121	260	Request for oral hearing	
138	1,510	Petition to institute a public use proceeding	
140	110	Petition to revive - unavoidable	
141	1,210	Petition to revive - unintentional	
142	1,210	Utility issue fee (or reissue)	
122	130	Petitions to the Commissioner	
123	50	Petitions related to provisional applications	
126	240	Submission of Information Disclosure Stmt	
581	40	Recording each patent assignment per property (times number of properties)	$40
146	690	Filing a submission after final rejection (37 CFR 1.129(a))	
149	690	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) ____________________

Other fee (specify) ____________________

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($) 40.00

SUBMITTED BY

Complete (if applicable)

Name (*Print/Type*)	Edel M. Young	Registration No. (*Attorney/Agent*)	32,451	Telephone	408-879-4969
Signature	Reg. No. 40,941 for Edel M. Young			Date	09-05-2000

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

CIRCUIT FOR PRODUCING LOW-VOLTAGE DIFFERENTIAL SIGNALS

Atul V. Ghia
Suresh M. Menon
David P. Schultz

FIELD OF THE INVENTION

This invention relates generally to methods and circuits for providing high-speed, low-voltage differential signals.

BACKGROUND

The Telecommunications Industry Association (TIA) published a standard specifying the electrical characteristics of low-voltage differential signaling (LVDS) interface circuits that can be used to interchange binary signals. LVDS employs low-voltage differential signals to provide high-speed, low-power data communication. The use of differential signals allows for cancellation of common-mode noise, and thus enables data transmission with exceptional speed and noise immunity. For a detailed description of this LVDS Standard, see "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits," TIA/EIA-644 (March 1996), which is incorporated herein by reference.

Figure 1 (prior art) illustrates an LVDS generator 100 connected to an LVDS receiver 110 via a transmission line 115. Generator 100 converts a single-ended digital input signal D_IN on a like-named input terminal into a pair of complementary LVDS output signals on differential output terminals TX_A and TX_B. A 100-ohm termination load RL separates terminals TX_A and TX_B, and sets the output impedance of generator 100 to the level specified in the above-referenced LVDS Standard.

LVDS receiver 110 accepts the differential input signals from terminals TX_A and TX_B and converts them to a single-ended output signal D_OUT. The LVDS Standard specifies the properties of LVDS receiver 110. The present application is directed to differential-signal generators: a comprehensive discussion of receiver 110 is not included in the present application.

Figure 2 (prior art) schematically depicts LVDS generator 100 of Figure 1. Generator 100 includes a preamplifier 200 connected to a driver stage 205. Preamplifier 200 receives the single-ended data signal D_IN and produces a pair of complementary data signals D and D/ (signal names terminating in "/" are active low signals). Unless otherwise specified, each signal is referred to by the corresponding node designation depicted in the figures. Thus, for example, the input terminal and input signal to generator 100 are both designated D_IN. In each instance, the interpretation of the node designation as either a signal or a physical element is clear from the context.

Driver stage 205 includes a PMOS load transistor 207 and an NMOS load transistor 209, each of which produces a relatively stable drive current in response to respective bias voltages PBIAS and NBIAS. Driver stage 205 additionally includes four drive transistors 211, 213, 215, and 217.

If signal D_IN is a logic one (e.g., 3.3 volts), preamplifier 200 produces a logic one on terminal D and a logic zero (e.g., zero volts) on terminal D/. The logic one on terminal D turns on transistors 211 and 217, causing current to flow down through transistors 207 and 211, up though termination load RL, and down through transistors 217 and 209 to ground (see the series of arrows 219). The current through termination load RL develops a negative voltage between output terminals TX_A and TX_B.

Conversely, if signal D_IN is a logic zero, preamplifier 200 produces a logic zero on terminal D and a logic one on terminal D/. The logic one on terminal D/ turns on transistors 213 and 215, causing current to flow down through transistor 207, transistor 215, termination load RL, transistor 213, and transistor 209 to ground (see the series of arrows 221). The current through termination load RL develops a positive voltage between output terminals TX_A and TX_B.

Figure 3 (prior art) is a waveform diagram 300 depicting the signaling sense of the voltages appearing across termination load RL of Figures 1 and 2. LVDS generator 100 produces a pair of differential output signals on terminals TX_A and TX_B. The LVDS Standard requires that the voltage between terminals TX_A and TX_B remain in the range of 250 mV to 450 mV, and that the voltage midway between the two differential voltages remains at approximately 1.2 volts. Terminal TX_A is negative with respect to terminal TX_B to represent a binary one and positive with respect to terminal B to represent a binary zero.

A programmable logic device (PLD) is a well-known type of IC that may be programmed by a user (e.g., a circuit designer) to perform specified logic functions. Most PLDs contain some type of input/output block (IOB) that can be configured either to receive external signals or to drive signals off chip. One type of PLD, the field-programmable gate array (FPGA), typically includes an array of configurable logic blocks (CLBs) that are programmably interconnected to each other and to the programmable IOBs. Configuration data loaded into internal configuration memory cells on the FPGA define the operation of the FPGA by determining how the CLBs, interconnections, block RAM, and IOBs are configured.

IOBs configured as output circuits typically provide single-ended logic signals to external devices. As with other types of circuits, PLDs would benefit from the performance advantages offered by driving external signals using differential output signals. There is therefore a need for IOBs that can be configured to provide differential output signals. There is also a need for LVDS output circuits that can be tailored to optimize performance for different loads.

SUMMARY

The present invention addresses the need for differential-signal output circuits that can be tailored for use with different loads. In accordance with one embodiment, one or more driver stages can be added, as necessary, to provide adequate power for driving a given load. Driver stages are added by programming one or more programmable elements, such as memory cells, fuses, and antifuses.

A differential driver in accordance with another embodiment includes a multi-stage delay element connected to a number of consecutive driver stages. The delay element produces two or more pairs of complementary input signals in response to each input-signal transition, each successive signal pair being delayed by some amount relative to the previous signal pair. The pairs of complementary signals are conveyed to respective driver stages, so that each driver stage successively responds to the input-signal transition. The output terminals of the driver stages are connected to one another and to the output terminals of the differential driver. The differential driver thus responds to each input-signal transition with increasingly powerful amplification. The progressive amplification produces a corresponding progressive reduction in output resistance, which reduces the noise normally associated with signal reflection.

Extendable and multi-stage differential amplifiers in accordance with the invention can be adapted for use in PLDs. In one embodiment, adjacent pairs of IOBs are each provided with half of the circuitry required to produce LVDS signals. Adjacent pairs of IOBs can therefore be used either individually to provide single-ended input or output signals or can be combined to produce differential output signals.

This summary does not limit the invention, which is instead defined by the appended claims.

BRIEF DESCRIPTION OF THE FIGURES

Figure 1 (prior art) illustrates an LVDS generator 100 connected to an LVDS receiver 110 via a transmission line 115.

Figure 2 (prior art) schematically depicts LVDS generator 100 of Figure 1.

Figure 3 (prior art) is a waveform diagram 300 depicting the signaling sense of the voltages appearing across termination load RL of Figures 1 and 2.

Figure 4 depicts an extensible differential amplifier 400 in accordance with an embodiment of the invention.

Figure 5A is a schematic diagram of predriver 405 of Figure 4.

Figure 5B is a schematic diagram of driver 415 of Figure 4.

Figure 5C is a schematic diagram of extended driver 410 of Figure 4.

Figure 6 depicts a multi-stage driver 600 in accordance with another embodiment of the invention.

Figure 7A schematically depicts a predriver 700 in which a predriver is connected to delay circuit 605 of Figure 6 to develop three complementary signal pairs.

Figure 7B schematically depicts differential-amplifier sequences 610 and 615 and termination load 620, all of Figure 6.

Figures 8A and 8B schematically depict a programmable bias-voltage generator 800 in accordance with an embodiment of the invention.

DETAILED DESCRIPTION

Figure 4 depicts an extensible differential amplifier 400 in accordance with an embodiment of the invention. Amplifier

400 includes a predriver 405 connected to a pair of driver stages 410 and 415. The combination of predriver 405 and driver 415 operates as described above in connection with Figures 2 and 3 to convert the single-ended input on terminal D_IN into differential output signals on lines TX_A and TX_B. In accordance with the invention, driver 410 can be activated as needed to provide additional drive power. In one embodiment, drivers 410 and 415 reside within a pair of adjacent programmable IOBs (collectively labeled 417) and lines TX_A and TX_B connect to the respective input/output (I/O) pads of the pair. This aspect of the invention is detailed below.

The program state of a configuration bit 420 determines whether amplifier 400 is enabled, and the program state of a second configuration bit 425 determines whether the driver stage of amplifier 400 is extended to include driver 410. An exemplary configuration bit is described below in connection with Figure 8A.

If bit 420 is programmed to provide a logic one on "enable differential signaling" line EN_DS, then predriver 405 and driver 415 function in a manner similar to that described above in connection with Figure 2. If desired, the drive circuitry can be extended to include driver 410 by programming bit 425 to provide a logic one on "extended differential signaling" line X_DS. The signals on lines X_DS and EN_DS are logically combined using an AND gate 430 to produce an "enable termination load" signal EN_T to driver 415. This signal and its purpose are described below in connection with Figure 5B.

Figure 5A is a schematic diagram of an embodiment of predriver 405 of Figure 4. Predriver 405 includes a pair of conventional tri-state drivers 500 and 502. A conventional inverter 504 provides the complement of signal EN_DS.

Amplifier 400 is inactive when signals EN_DS and EN_DS/ are low and high, respectively. These logic levels cause tristate drivers 500 and 502 to disconnect input terminal D_IN from respective tristate output terminals T1 and T2. Signal EN_DS and its complementary signal EN_DS/ also connect terminals T1 and T2 to respective supply voltages VCCO and ground by turning on a pair of transistors 506 and 508. Thus, terminals T1 and T2 do not change in response to changes on input terminal D_IN when differential signaling is disabled. In the case where amplifier 400 is implemented using IOBs in a programmable logic device, amplifier 400 may be disabled to allow the IOBs to perform some other input or output function.

Amplifier 400 is active when signals EN_DS and EN_DS/ are high and low, respectively. These logic levels cause tristate drivers 500 and 502 to connect input terminal D_IN to respective tristate output terminals T1 and T2. Signal EN_DS and its complementary signal EN_DS/ also disconnect terminals T1 and T2 from respective supply voltages VCCO and ground by turning off transistors 506 and 508. Thus, terminals T1 and T2 change in response to signal D_IN when differential signaling is enabled.

Tristate output terminals T1 and T2 connect to the respective input terminals of an inverting predriver 510 and a non-inverting predriver 512. Predriver 510 includes a pair of conventional inverters 514 and 516. Inverter 514 produces a signal D, an inverted and amplified version of the signal on line T1; inverter 516 provides a similar signal to a test pin 518. Predriver 512 includes three conventional inverters 520, 522, and 524. Predriver 512 produces a signal D/, the complement of signal D. Inverter 524 provides a similar signal to a test pin 526.

Each inverter within predrivers 510 and 512 is a CMOS inverter in which the ratios of the PMOS and NMOS transistors are as specified. These particular ratios were selected so that signals D and D/ transition simultaneously, or very nearly so. Different ratios may be appropriate, depending upon the process used to produce amplifier 400. Adjusting layout and process parameters to produce synchronized complementary signals is within the skill of those in the art.

As discussed above in connection with Figure 4, amplifier 400 can be extended to include additional drive circuitry, which may be needed to drive some loads while remaining in compliance with the LVDS Standard. Returning to Figure 5A, a pair of NOR gates 528 and 530 facilitates this extension by producing a pair of complimentary extended-data signals DX and DX/ when signal X_DS/ is a logic zero, indicating the extended driver is enabled. Extended-data signal DX is substantially the same as signal D, and extended data signal DX/ is substantially the same as signal D/. Signals DX and DX/ are conveyed to extended driver 410, the operation of which is detailed below in connection with Figure 5C.

Figure 5B is a schematic diagram of driver 415 of Figure 4. Driver 415 is similar to driver stage 205 of Figure 2, like-numbered elements being the same. Unlike driver 205, however, driver 415 includes a programmable termination load 540. Further, load transistors 207 and 209 of Figure 2 are replaced with pairs of parallel transistors, so that transistors 211 and 215 connect to VCCO via respective PMOS transistor 532 and 533, instead of via a single transistor 207, and transistors 213 and 217 connect to ground via respective NMOS transistors 534 and 535, instead of via a single transistor 209.

Employing pairs of load transistors allows driver 415 to be separated into two similar parts 536 and 538, each associated with a respective one of terminals TX_A and TX_B. Such a configuration is convenient, for example, when driver 415 is implemented on a PLD in which terminals TX_A and TX_B connect to neighboring I/O pins. Each part 536 and 538 can be implemented as a portion of the IOB (not shown) associated with the respective one of terminals TX_A and TX_B.

Termination load 540 can be part of either IOB, neither IOB, or can be split between the two. In one embodiment, transistor 542 is included in the IOB that includes part 536, and transistor 543 is included in the IOB that includes part 538.

Programmable termination load 540 includes a pair of transistors 542 and 543, the gates of which connect to terminal EN_T. As shown in Figure 4, the signal EN_T is controlled through AND gate 430 by configuration bits 420 and 425. Termination load 540 is active (conducting) only when differential signaling is enabled in the non-extended mode. This condition is specified when configuration bit 420 is set to a logic one and configuration bit 425 is set to a logic zero.

Driver 415 includes a number of terminals that provide appropriate bias voltages. Terminals PBIAS and NBIAS provide respective bias levels establish the gain driver 415, and common terminals PCOM and NCOM conventionally establish the high and low voltage levels on output terminals TX_A and TX_B. Driver 415 shares the bias and common terminals with extended driver 410 (See Figure 5C).

The bias levels PBIAS and NBIAS are important in defining LVDS signal quality. In one embodiment, NMOS transistors 534 and 535 are biased to operate in saturation to sink a relatively stable current, whereas PMOS transistors 532 and 533 are biased to operate in a linear region. Operating transistors 532 and 533 in a linear region reduces ~~???? HOW~~ a ~~SO???????~~ the output resistances of those devices, and the reduced resistance tends to dissipate signal reflections returning to terminals TX_A and TX_B. Reduced reflections translate into reduced noise, and reduced noise allows signals to be conveyed at higher data rates. Circuits for developing appropriate bias levels for the circuits of Figures 5A-7B are discussed below in connection with Figures 8A and 8B.

Figure 5C is a schematic diagram of one embodiment of extended driver 410 of Figure 4. Extended driver 410 includes a pair of driver stages 544 and 546 and a programmable termination load 548. Driver stages 544 and 546 can be included, for example, in respective adjacent IOBs on a PLD. Termination load 548 can be part of either IOB, neither IOB, or can be split between the two. The various terminals of Figure 5C are connected to like-named terminals of Figures 5A and 5B.

Driver stage 544 includes a PMOS load transistor 550, a pair of NMOS differential-driver transistors 552 and 554 having their gates connected to respective extended-driver input signals DX and DX/, a diode-connected PMOS transistor 556, and a PMOS transistor 558 connected as a capacitor between terminal VCCO and terminal PCOM. Transistors 550, 552, and 554 combined amplify the extended-driver signals DX and DX/ to produce an amplified output signal on output terminal TX_A. In one embodiment, transistor 556 is diode-connected between terminals PCOM and VCCO to establish the appropriate level for line PCOM, which is common to both drivers 410 and 415. Finally, transistor 558 can be sized or eliminated as desired to minimize noise on line PCOM.

Driver stage 546 is identical to driver stage 544, except that lines DX and DX/ are connected to the opposite differential driver transistors. Consequently, the signals on output terminals TX_A and TX_B are complementary. Driver stages 544 and 546 thus supplement the drive strength provided by driver stage 415.

As shown in Figure 4, the extend-differential-signaling signal X_DS is a logic one when CBIT 425 is programmed. However, programming CBIT 425 causes AND gate 430 to output a logic zero, disabling termination load 532 of Figure 5B. Thus, programming CBIT 425 substitutes termination load 548 for termination load 532, thereby increasing the termination load resistance to an appropriate level. In one embodiment, the resistance of termination load 532 is selected so that the resulting output signal conforms to the LVDS Standard.

Figure 6 depicts a multi-stage driver 600 in accordance with another embodiment of the invention. Driver 600 includes a multi-stage delay circuit 605, a first sequence of differential amplifiers 610, a second sequence of differential amplifiers 615, and a termination load 620. For illustrative purposes, the amplifiers of sequences 610 and 615 are referred to as "high-side" and "low-side" amplifiers, respectively. In different embodiments, each amplifier sequence 610 and 615 can be implemented as a portion of the IOB (not shown) associated with the respective one of terminals TX_A and TX_B. Termination load 620 can be part of either IOB, neither IOB, or can be split between the two.

Delay circuit 605 receives a pair of complementary signals D and D/ on a like-named pair of input terminals. A sequence of delay elements -- conventional buffers 625 in the depicted example -- provides a first pair of delayed complementary signals D1 and D1/ and a second pair of delayed complementary signals D2 and D2/.

Sequence 610 includes three differential amplifiers 630, 631, and 632, the output terminals of which connect to one another and to output terminal TX_A. The differential input terminals of each of these high-side amplifiers connect to respective complementary terminals from delay circuit 605. That is, the non-inverting (+) and inverting (-) terminals of differential amplifier 630 connect to respective input terminals D and D/, the non-inverting and inverting terminals of differential amplifier 631 connect to respective input terminals D1 and D1/, and the non-inverting and inverting terminals of differential amplifier 632 connect to respective input terminals D2 and D2/. When the signal on terminal D transitions from low to high, each of amplifiers 630, 631, and 632 consecutively joins in pulling the voltage level on

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terminal TX_A high as the signal edges on terminals D and D/ propagate through delay circuit 605. Conversely, when the signal on terminal D transitions from high to low, each of amplifiers 630, 631, and 632 consecutively joins in pulling the voltage level on terminal TX_A low.

Sequence 615 includes three differential amplifiers 634, 635, and 636, the output terminals of which connect to one another and to terminal TX_B. Sequence 615 is similar to sequence 610, except that the differential input terminals of the various low-side differential amplifiers are connected to opposite ones of the complementary signals from delay circuit 605. Thus, when the signal on terminal D transitions from low to high, each of amplifiers 634, 635, and 636 consecutively joins in pulling the voltage level on terminal TX_B low as the signal edges on terminals D and D/ propagate through delay circuit 605, and when the signal on terminal D transitions from high to low, each of amplifiers 634, 635, and 636 consecutively joins in pulling the voltage level on terminal TX_B high.

Driver stage 600 is similar to driver stage 415 of Figures 4 and 5A, except that driver stage 600 progressively increases the drive strength used to provide amplified signals across termination load 620, and consequently progressively reduces the output resistance of driver stage 600. Progressively reducing the output resistance of amplifier 600 reduces the amplitude of reflected signals. This effect, in turn, reduces the noise and increases the useable data rate of the LVDS circuitry. While illustrated as having three driver stages, other embodiments of amplifier 600 include more or fewer stages. Figure 7A schematically depicts a predriver 700 in which predriver 405, detailed in Figure 5A, is connected to delay circuit 605 of Figure 6 to develop the three complementary signal pairs (e.g., D and D/) of Figure 6. The various elements of predriver 405 are described above in connection with Figure 5A, like-numbed elements being identical. In one embodiment, each buffer 625 is an instance of non-inverting delay circuit 512. Figure7B schematically depicts differential-amplifier sequences 610 and 615 and termination load 620, all of Figure 6. The differential amplifiers in sequences 610 and 615 are substantially identical, except the D and D/ input terminals are reversed. The following description is limited to a single differential amplifier (630) for brevity. Differential amplifier 630 includes a PMOS load transistor 700, an NMOS load transistor 705, and a pair of active transistors 710 and 715 having their respective gates connected to data inputs D and D/. One embodiment of amplifier 400 of Figure 4 employs driver stage 600 in place of driver 415 (detailed in Figure 5B). Amplifier sequence 610 may include a capacitor 725 between PCOM and VCCO, and amplifier sequence 615 may include a capacitor 730 connected between NCOM and ground. These capacitors can be sized to minimize noise. Figures 8A and 8B schematically depict a programmable bias-voltage generator 800 in accordance with an embodiment of the invention. A key 802 in the bottom right-hand corner of Figure 8A shows the relative arrangement of Figures 8A and 8B.

The portion of generator 800 depicted in Figure 8A may be divided into three general areas: bias-enable circuitry 804, NBIAS pull-up circuitry 806, and NBIAS pull-down circuitry 808. As their respective names imply, bias-enable circuitry 804 determines whether bias generator 800 is active, NBIAS pull-up circuitry 806 can be used to raise the NBIAS voltage level, and NBIAS pull-down circuitry 808 can be used to reduce the NBIAS voltage level. The NBIAS pull-up and pull-down circuitry are programmable to allow users to vary the NBIAS voltage as desired.

Bias-enable circuitry 804 includes a configuration bit (CBIT) 810, an inverter 812, a PMOS transistor 814, and, in

Figure 8B, a PMOS transistor 815 and a pair of NMOS transistors 816 and 817. CBIT 810 is conventional, in one embodiment including an SRAM configuration memory cell 818 connected to a level-shifter 820. Level-shifter 820 is used because bias generator 800 is a portion of the output circuitry of a PLD, and operates at higher voltage (e.g., 3.3 volts) than the core circuitry (e.g., 1.5 volts) of the PLD: level-shifter 820 increases the output voltage of SRAM cell 816 to an appropriate voltage level. Some embodiments that employ lower core voltages use thicker gate insulators in the transistors of the I/O circuitry. The gate insulators of differing thickness can be formed using a conventional dual-oxide process. In one embodiment in which the circuits depicted in Figures 5A-8B are part of the output circuitry of a PLD, each of the depicted devices employs relatively thick gate insulators.

Generator 800 is activated by programming SRAM cell 818 to include a logic one, thereby causing bias-enable circuitry 804 to output a logic one on line BIAS. This logic one connects high-supply-voltage line H_SUP to supply voltage VCCO through transistor 814 and disconnects line PBIAS from VCCO to enable line PBIAS to carry an appropriate bias voltage. The inverted signal BIAS/ from inverter 812, a logic zero when active, disconnects lines NBIAS and NGATE from ground, thereby allowing those lines to carry respective bias voltages. The logic levels on lines PBIAS and NBIAS are one and zero, respectively, when SRAM cell 818 is set to logic zero.

NBIAS pull-up circuitry 806 has an input terminal VBG connected to a conventional band-gap reference, or some other suitable voltage reference. The voltage level and line VBG turns on a PMOS transistor 822 that, in combination with diode-connected transistors 824 and 826, produces bias voltage levels on lines NGATE and NBIAS. Terminal VBG also connects to a pair of transmission gates 828 and 830, each consisting of

NMOS and PMOS transistors connected in parallel. The transmission gates are controlled by configuration bits similar to CBIT 810. For example, transmission gate 828 can be turned on by programming CBIT_A to contain a logic one. The logic one produces a logic one on line A and, via an inverter 834, a logic zero on line A/. Transmission gate 828 passes the reference voltage on line VBG to the gate of a PMOS transistor 836, thereby reducing the resistance between VCCO and line NBIAS; consequently, the voltage level on line NBIAS rises. Transistor 838 can be turned on and both of transmission gate 828 and transistor 836 can be turned off by programming CBIT_A to contain a logic zero. Transmission gate 830 operates in the same manner as transmission gate 828, but is controlled by a different CBIT (CBIT_B) and an associated inverter. One or both of transmission gates 828 and 830 can be turned on to raise the voltage level on line NBIAS.

NBIAS pull-down circuitry 808 includes a pair of programmable pull-down circuits 840 and 842 that can be programmed independently or collectively to reduce the bias voltage on terminal NBIAS. Pull-down circuits 840 and 842 work the same way, so only circuit 840 is described.

Pull-down circuit 840 includes three transistors 844, 846, and 848. The gates of transistors 844 and 846 connect to terminals C and C/, respectively, from a configuration bit CBIT_C and an associated inverter 849. When CBIT_C is programmed to contain a logic zero, transistors 844 and 848 are turned off, isolating line NBIAS from ground; when CBIT_C is programmed to contain a logic one, transistors 844 and 848 are turned on and transistor 846 turned off. The reduced resistance through transistor 848 reduces the voltage on line NBIAS.

Any change in the bias voltage on line NBIAS results in a change in voltage on line NGATE via a transistor 850. A transistor 852 connected between line NBIAS and ground is an

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optional capacitor that can be sized or eliminated as desired.

The portion of bias-voltage generator 800 depicted in Figure 8A adjusts the level of NBIAS; the portion depicted in Figure 8B adjusts the level of PBIAS. Referring now to Figure 8B, the portion of Figure 8B includes PBIAS pull-up circuitry 852 and PBIAS pull-down circuitry 854. PBIAS pull-up circuitry 852 operates in the same manner as NBIAS pull-up circuitry 806 of Figure 8A to raise the level of the bias voltage on line PBIAS. A pair of configuration bits CBIT_E and CBIT_F and associated inverters control circuitry 852. A capacitor 856 can be sized or eliminated as necessary.

PBIAS pull-down circuitry 854 includes a pair of programmable pull-down circuits 858 and 860 that can be programmed independently or collectively to reduce the bias voltage on terminal PBIAS. Pull-down circuits 858 and 860 work the same way, so only circuit 858 is described.

Pull-down circuit 858 includes a transmission gate 862 and a pair of transistors 864 and 866. With CBIT_G programmed to contain a logic zero, transmission gate 862 is off, transistor 866 on, and transistor 864 off; with CBIT_G programmed to contain a logic one, transistor 866 is off, and transmission gate 862 passes the bias voltage NGATE to the gate of transistor 864, thereby turning transistor 864 on. This reduces the voltage level on line PBIAS.

The present invention can be adapted to supply complementary LVDS signals to more than one LVDS receiver. For details of one such implementation, see "Multi-Drop LVDS with Virtex-E FPGAs," XAPP231 (Version 1.0) by Jon Brunetti and Brian Von Herzen (9/23/99), which is incorporated herein by reference.

While the present invention has been described in connection with specific embodiments, variations of these embodiments will be obvious to those of ordinary skill in the art. For example, while described in the context of SRAM-based

FPGAs, the invention can also be applied to other types of PLDs that employ alternate programming technologies, and some embodiments can be used in non-programmable circuits. Moreover, the present invention can be adapted to convert typical dual-voltage logic signals to other types of differential signals, such as those specified in the Low-Voltage, Pseudo-Emitter-Coupled Logic (LVPECL) standard. Therefore, the spirit and scope of the appended claims should not be limited to the foregoing description.

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CLAIMS

What is claimed is:

1. A differential amplifier comprising:
   a. a first differential-amplifier stage having:
      i. first and second differential input terminals adapted to receive a differential input signal; and
      ii. first and second differential output terminals;
   b. a second differential-amplifier stage having:
      i. third and fourth differential input terminals adapted to receive the differential input signal;
      ii. third and fourth differential output terminals connected to the first and second differential output terminals; and
      iii. an amplifier-enable terminal; and
   c. a programmable memory cell capable of maintaining a programmed state and a deprogrammed state, the memory cell having a memory-cell output terminal connected to the amplifier-enable terminal;
   d. wherein the second differential amplifier stage amplifies the input signal when the memory cell is in the programmed state and does not amplify the input signal when the memory cell is in the deprogrammed state.

2. The differential amplifier of claim 1, wherein the memory cell stores a voltage representative of a logic one when in the programmed state.

3. The differential amplifier of claim 1, further comprising a predriver having:
   a. a data input terminal adapted to receive an input data signal; and

b. first and second complementary output terminals connected to respective ones of the first and second differential input terminals.

4. The differential amplifier of claim 3, wherein the predriver further comprises:

a. a first tri-state buffer having a first tri-state input terminal connected to the data input terminal;

b. a second tri-state buffer having a second tri-state input terminal connected to the data input terminal;

c. an inverter having an inverter input terminal connected to the data input terminal and an inverter output terminal connected to the first complementary output terminal; and

d. a non-inverting delay stage having a delay-stage input terminal connected to the data input terminal and a delay-stage output terminal connected to the second complementary output terminal.

5. The differential amplifier of claim 4, wherein the inverter exhibits a first signal propagation delay and the non-inverting delay stage exhibits a second signal propagation delay substantially equal to the first signal propagation delay.

6. The differential amplifier of claim 1, further comprising a programmable termination load connected between the first and second differential output terminals.

7. The differential amplifier of claim 6, wherein the termination load includes a termination-load enable terminal connected to the memory-cell output terminal.

8. The differential amplifier of claim 6, further comprising

a second termination load connected between the first and second differential output terminals.

9. The differential amplifier of claim 8, wherein the second termination load is programmable.

10. An amplifier comprising:

a. first and second differential input terminals adapted to receive first and second complementary input signals;

b. a first high-side differential amplifier having:

  i. a first high-side differential amplifier input terminal connected to the first differential input terminal;

  ii. a second high-side differential amplifier input terminal connected to the second differential input terminal; and

  iii. a first high-side differential-amplifier output terminal;

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c. a first low-side differential amplifier having a first low-side differential amplifier input terminal connected to the first differential input terminal and a second ~~high-side~~ low-side differential amplifier input terminal connected to the second differential input terminal;

d. a delay element having:

  i. a first delay-element input terminal connected to the first differential input terminal and a first delay-element output terminal, the delay element adapted to provide a delayed version of the first complementary input signal on the first delay-element output terminal; and

  ii. a second delay-element input terminal connected to the second differential input terminal and a second delay-element output terminal, the delay element adapted to provide a delayed version of the second complementary input signal on the second delay-element output terminal;

e. a second high-side differential amplifier having:
   i. a third high-side differential amplifier input terminal connected to the first delay-element output terminal;
   ii. a fourth high-side differential amplifier input terminal connected to the second delay-element output terminal; and
   iii. a second high-side differential-amplifier output terminal connected to the first high-side differential-amplifier output terminal; and

f. a second low-side differential amplifier having:
   i. a third low-side differential amplifier input terminal connected to the first delay-element output terminal;
   ii. a fourth low-side differential amplifier input terminal connected to the second delay-element output terminal; and
   iii. a second low-side differential-amplifier output terminal connected to the first low-side differential-amplifier output terminal.

11. The amplifier of claim 10, further comprising a termination load connected between the first high-side and first low-side differential-amplifier output terminals.

12. The amplifier of claim 11, further comprising a programmable memory cell capable of maintaining a programmed state and a deprogrammed state, the memory

cell having a memory-cell output terminal connected to the termination load.

13. The amplifier of claim 10, further comprising a second delay element having:

a. a third delay-element input terminal connected to the first delay-element output terminal of the first-mentioned delay element;

b. a fourth delay-element input terminal connected to the second delay-element output terminal of the first-mentioned delay element;

c. a third delay-element output terminal; and

d. a fourth delay-element output terminal.

14. The amplifier of claim 13, further comprising a third low-side differential amplifier and a third high-side differential amplifier, each having a pair of input terminals connected to respective ones of the third and forth delay-element output terminals.

a 15. The amplifier of claim ~~13~~ 14, wherein the third low-side differential amplifier includes a third low-side differential-amplifier output terminal connected to the first low-side differential-amplifier output terminal, and wherein the third high-side differential amplifier includes a third high-side differential-amplifier output terminal connected to the first high-side differential-amplifier output terminal.

16. The amplifier of claim 10, wherein the first high-side differential amplifier comprises:

a. an input transistor having a control terminal connected to the first high-side differential-amplifier input terminal, a first input-transistor current-handling terminal connected to the first high-side differential-amplifier output terminal, and a second input-transistor current-handling terminal; and

b. a load transistor having a control terminal connected to a bias voltage, a first load-transistor current-handling terminal connected to a power terminal, and a second load-transistor current-handling terminal connected to the second input-transistor current-handling terminal.

17. The amplifier of claim 16, further comprising a programmable bias generator adapted to provide the bias voltage on a bias-generator output terminal connected to the control terminal of the load transistor.

18. The amplifier of claim 16, wherein the first high-side differential amplifier further comprises:

a. a second input transistor having a second control terminal connected to the second high-side differential-amplifier input terminal, a first input-transistor current-handling terminal connected to the first high-side differential-amplifier output terminal, and a second input-transistor current-handling terminal; and

b. a second load transistor having a control terminal connected to a second bias voltage, a first load-transistor current-handling terminal connected to a second power terminal, and a second load-transistor current-handling terminal connected to the second input-transistor current-handling terminal.

19. The amplifier of claim 18, further comprising a programmable bias generator adapted to provide the first-

mentioned bias voltage on a first bias-generator output terminal and the second bias voltage on a second bias-generator output terminal.

20. A programmable logic device comprising:
  a. a predriver having:
    i. a data input terminal adapted to receive an input data signal; and
    ii. complementary first and second predriver output terminals;
  b. first and second input/output pins adapted to convey signals from the programmable logic device;
  c. a first programmable output block including a first differential amplifier, the first differential amplifier having a first differential-amplifier input terminal connected to the first predriver output terminal, a second differential-amplifier input terminal connected to the second predriver output terminal, and a first differential-amplifier output terminal connected to the first input/output pin; and
  d. a second programmable output block including a second differential amplifier, the second differential amplifier having a third differential-amplifier input terminal connected to the first predriver output terminal and a fourth differential-amplifier input terminal connected to the second predriver output terminal, and a second differential-amplifier output terminal connected to the second input/output pin.

21. The programmable logic device of claim 20, wherein the first pin is adjacent the second pin.

22. The programmable logic device of claim 20, further comprising:
    a. an enable terminal connected to at least one of the predriver and the first and second programmable output blocks; and
    b. a programmable memory cell connected to the enable terminal.

23. The programmable logic device of claim 20, further comprising a termination load connected between the first and second input/output pins.

CIRCUIT FOR PRODUCING LOW-VOLTAGE DIFFERENTIAL SIGNALS

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ABSTRACT OF THE DISCLOSURE

Described are systems for producing differential logic signals. These systems can be adapted for use with different loads by programming one or more programmable elements. One embodiment includes a series of driver stages, the outputs of which are connected to one another. The driver stages turn on successively to provide increasingly powerful differential amplification. This progressive increase in amplification produces a corresponding progressive decrease in output resistance, which reduces the noise associated with signal reflection. The systems can be incorporated into programmable IOBs to enable PLDs to provide differential output signals.

Docket No X-784 US

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) that is disclosed and/or claimed and for which a patent is solicited by way of the application entitled

CIRCUIT FOR PRODUCING LOW-VOLTAGE DIFFERENTIAL SIGNALS

which (check)

[X] is attached hereto.
[ ] and is amended by the Preliminary Amendment attached hereto.
[ ] was filed on ______________________ as Application Serial No.______________.
[ ] and was amended on ______________________ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified application, including the claims, including portions amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below

(Application Number(s)) (Filing Date (MM/DD/YYYY))

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as any subject matter of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

(Application Serial No.) (Filing Date) (Status-patented, pending, abandoned)

(Application Serial No.) (Filing Date) (Status-patented, pending, abandoned)

Docket No X-784 US

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected herewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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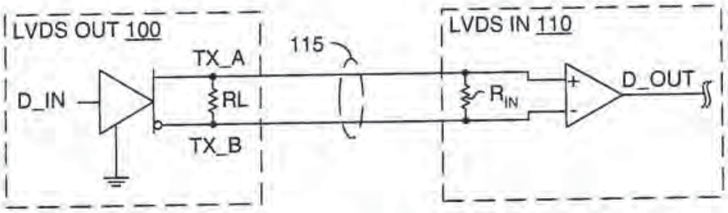

FIG. 1
(PRIOR ART)

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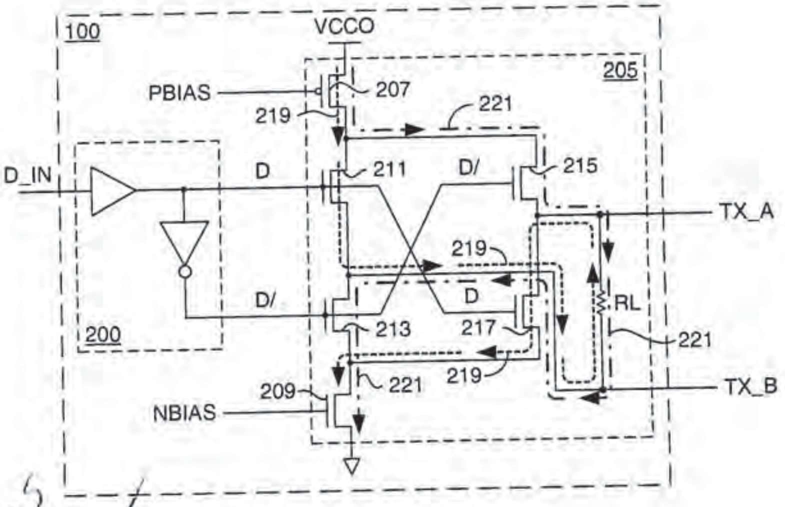


12 figs

FIG. 2
(PRIOR ART)

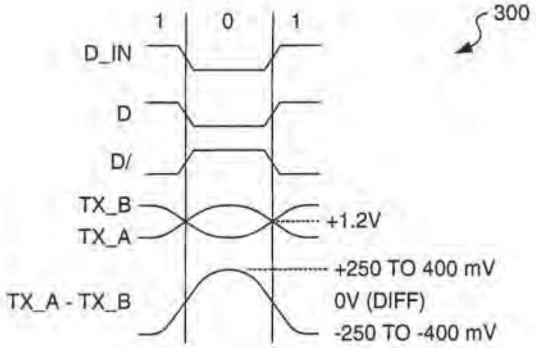


FIG. 3
(PRIOR ART)

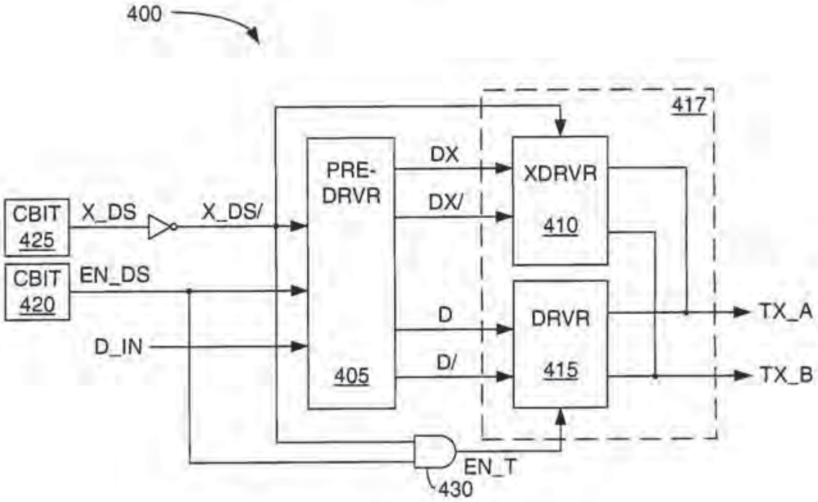
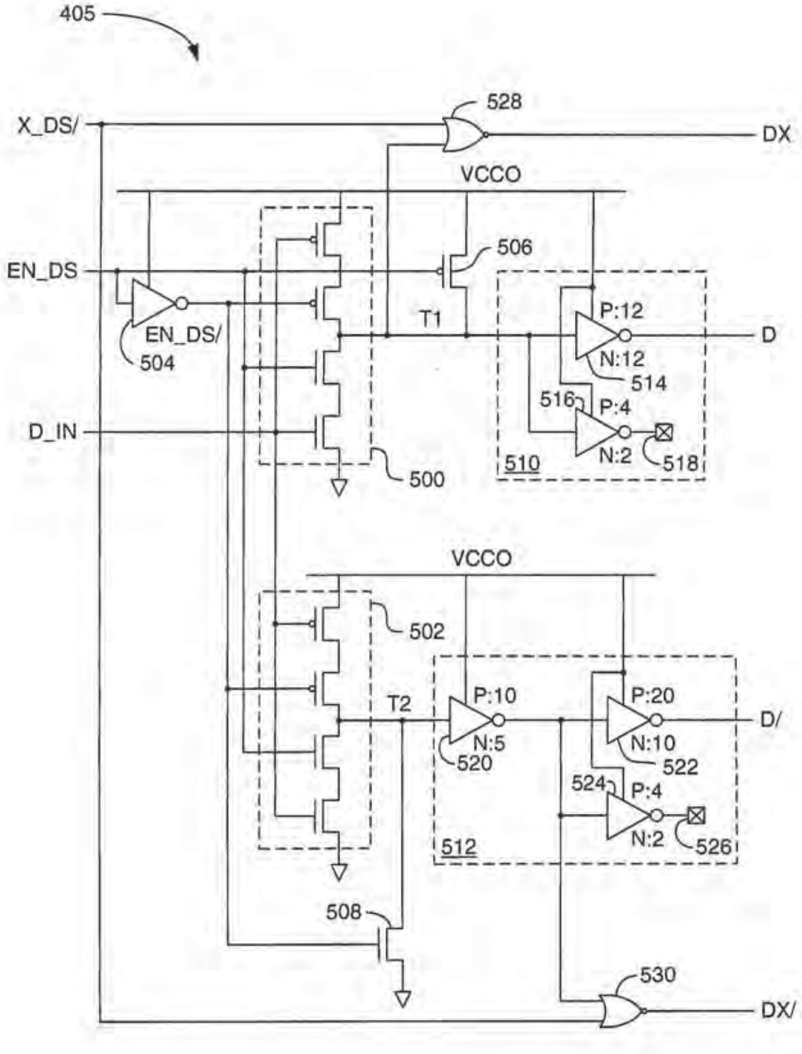


FIG. 4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D_IN
500
VCCO
502
T2
P:10
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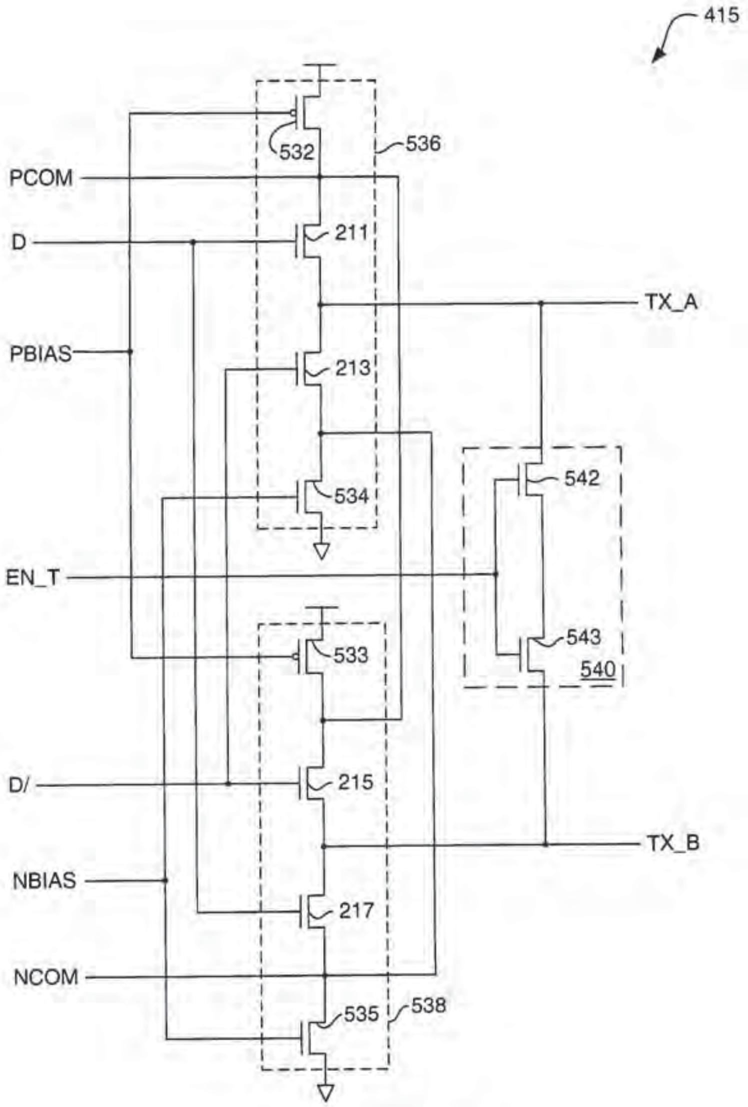
FIG. 5A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NBIAS
217
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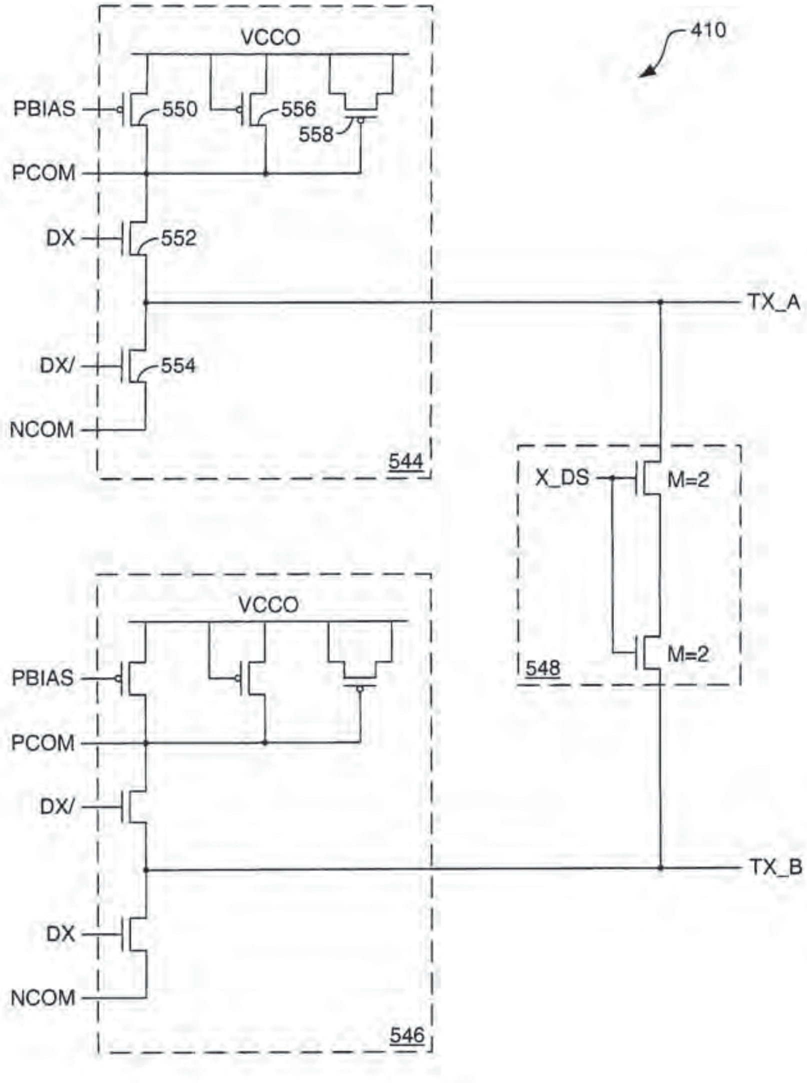
538

FIG. 5B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NCOM
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M=2
M=2
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VCCO
PBIAS
PCOM
DX/
TX_B
DX
NCOM
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FIG. 5C

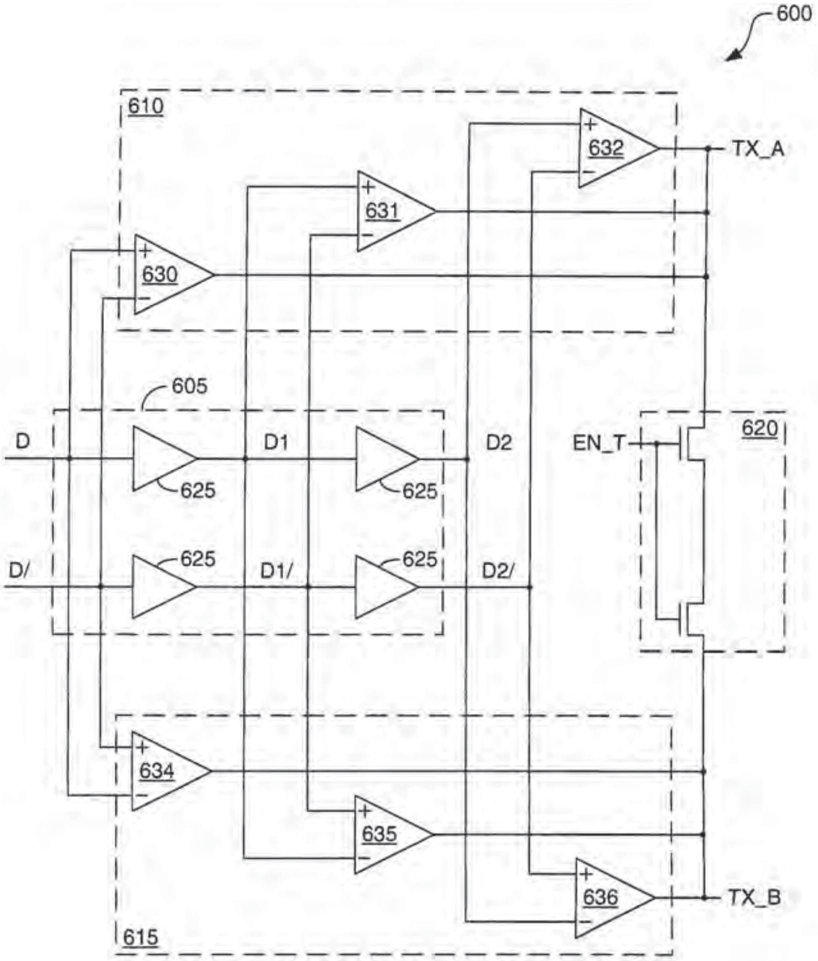
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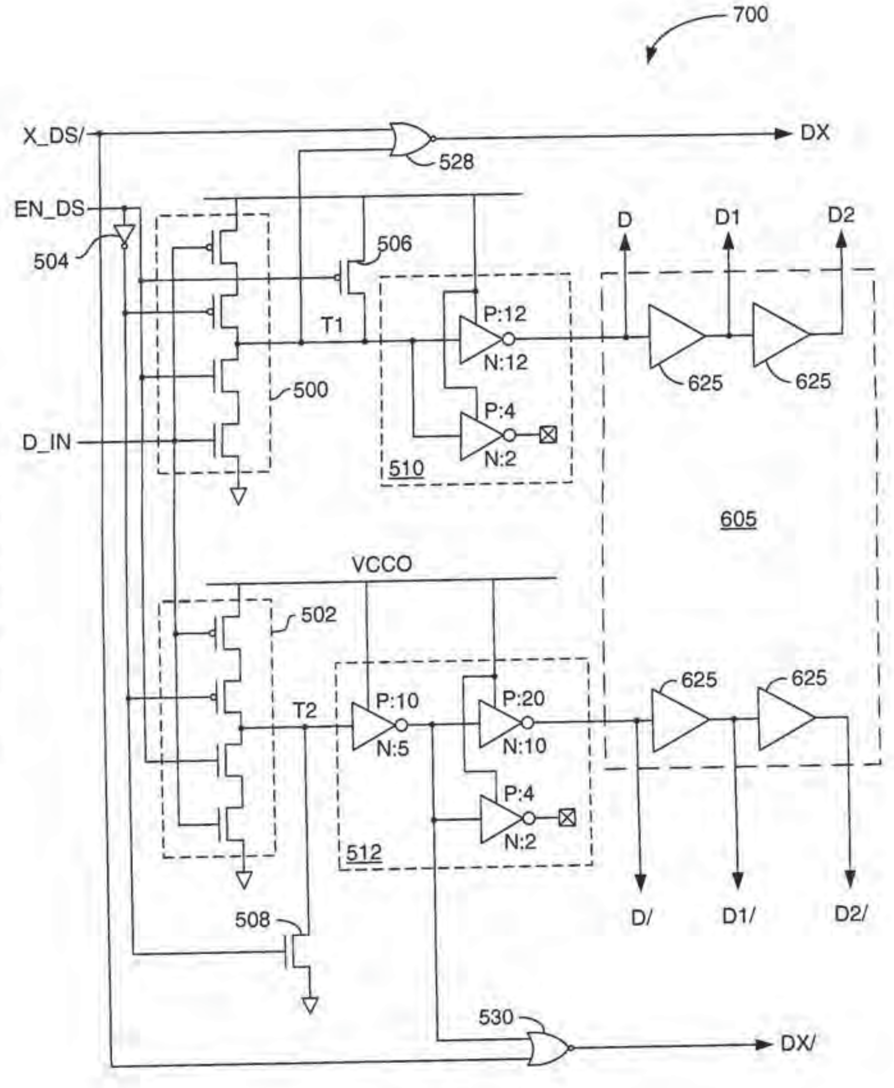
FIG. 6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D_IN
510
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VCCO
502
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625
T2
P:10
N:5
P:20
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FIG. 7A

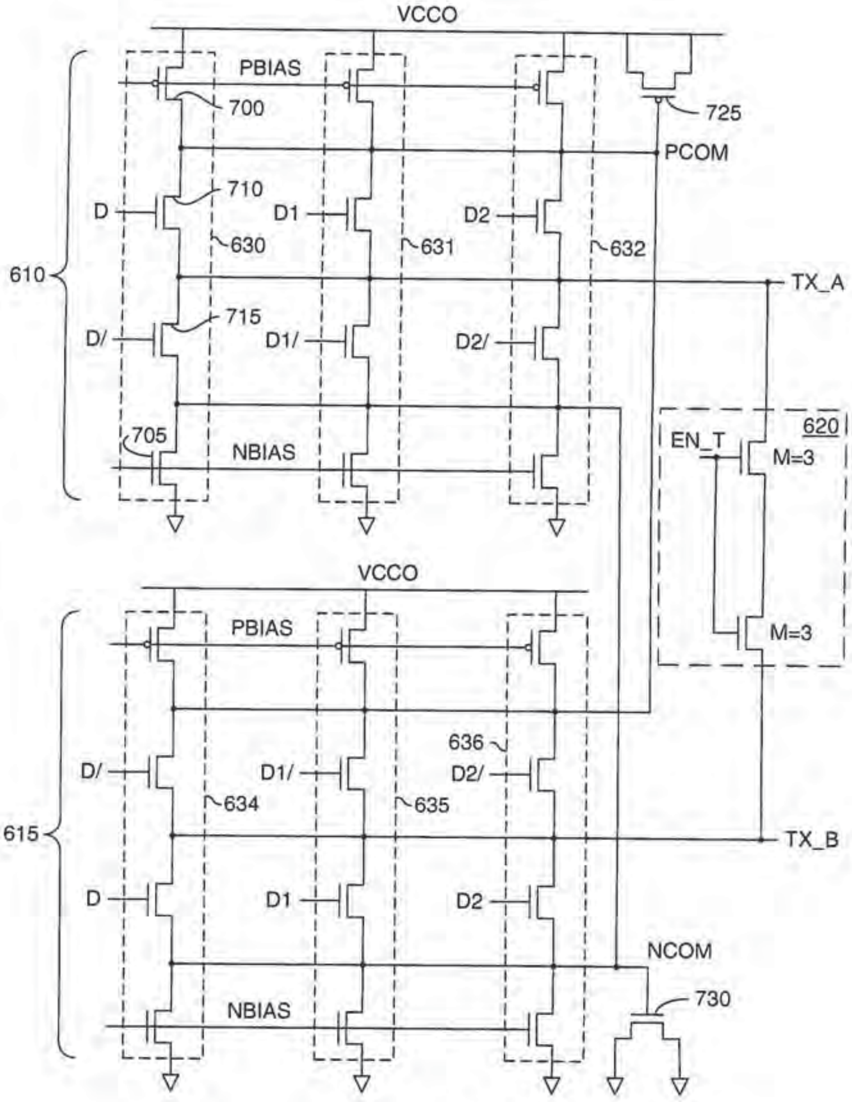
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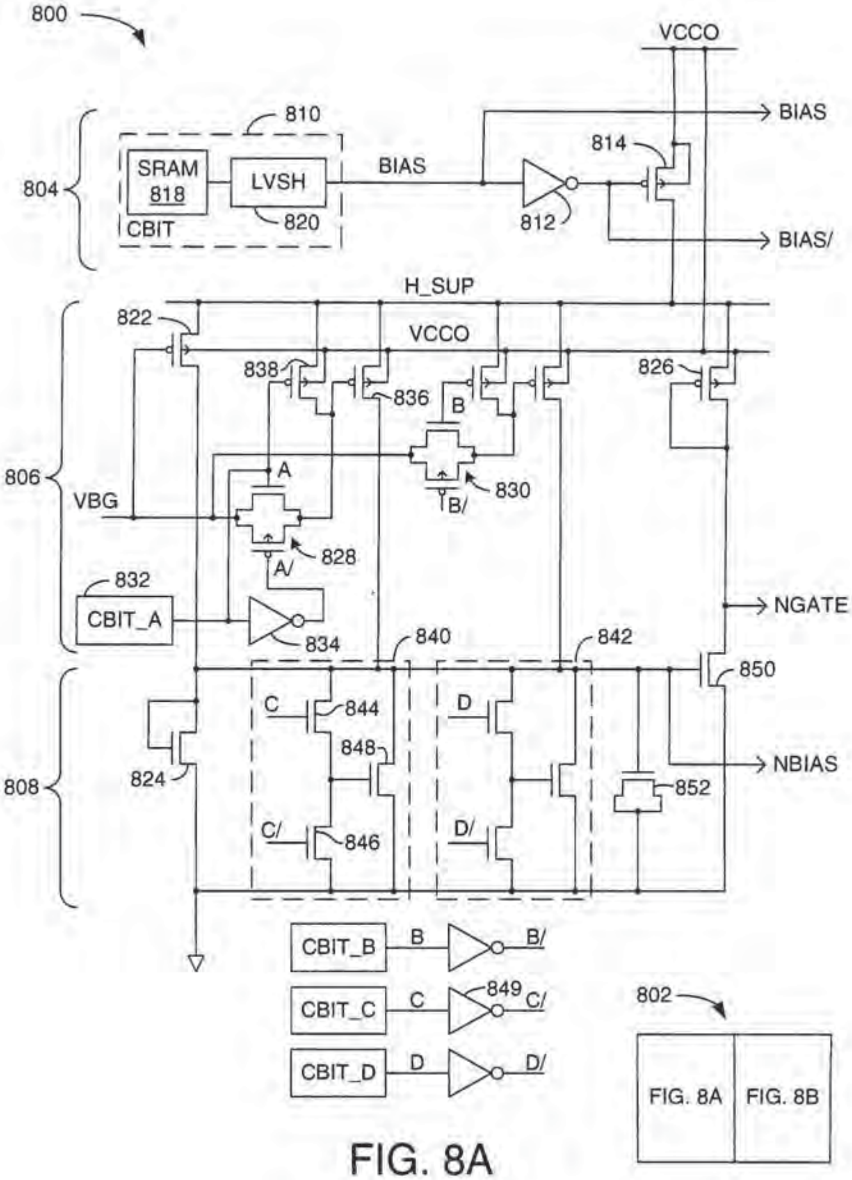
FIG. 7B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836
826
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832
CBIT_A
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FIG. 8A
FIG. 8B

FIG. 8A

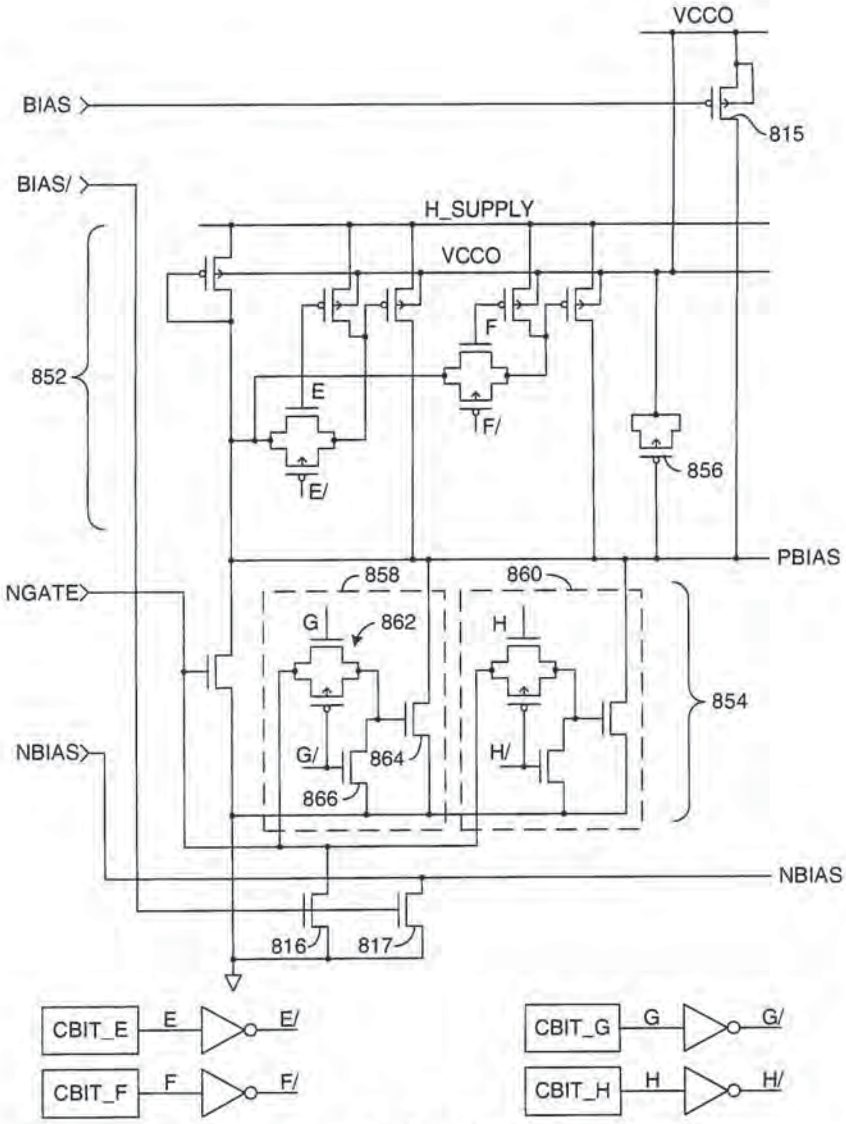
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FIG. 8B

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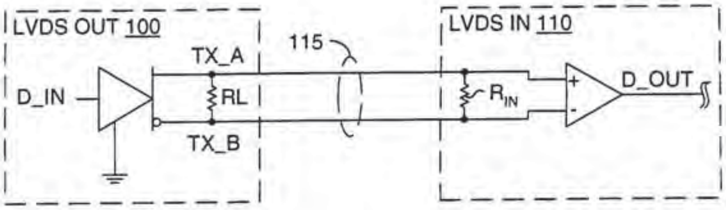

FIG. 1
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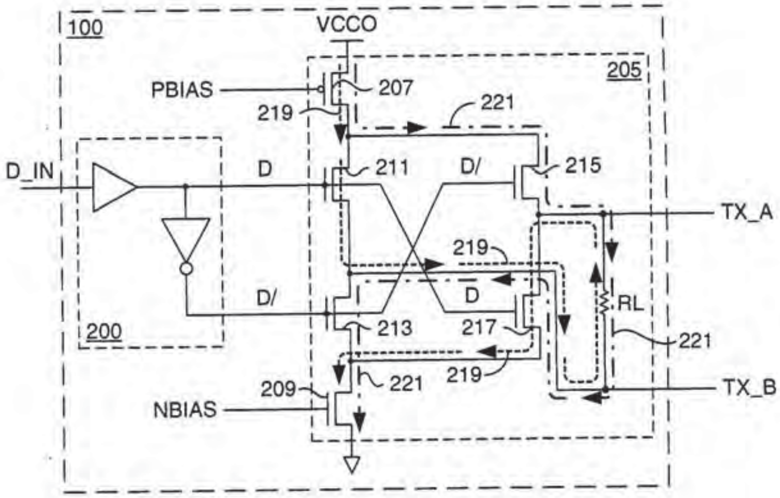

FIG. 2
(PRIOR ART)

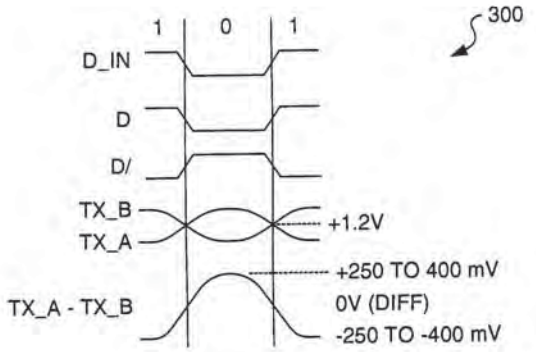

FIG. 3
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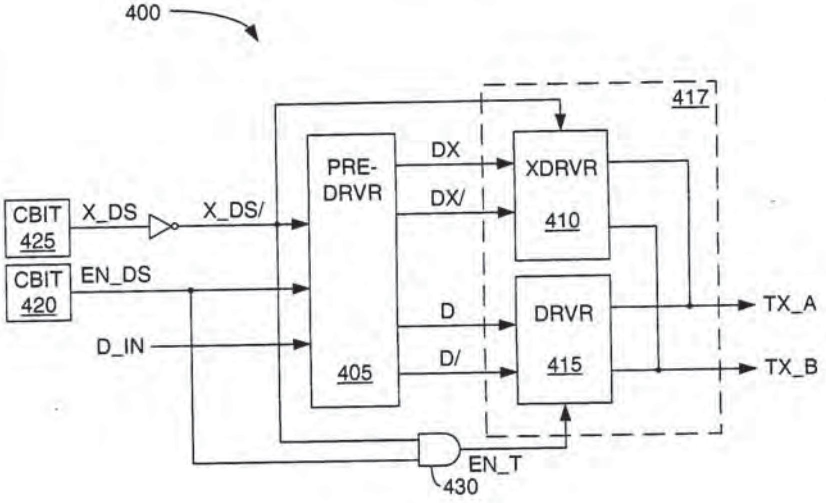

FIG. 4

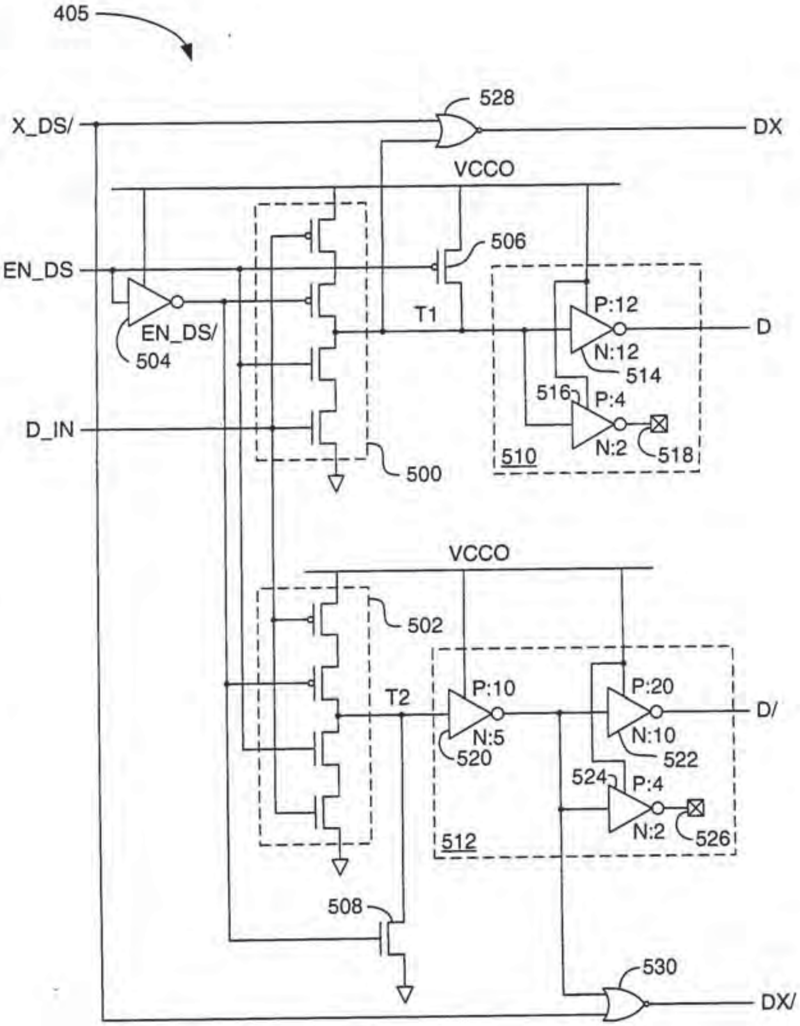
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FIG. 5A

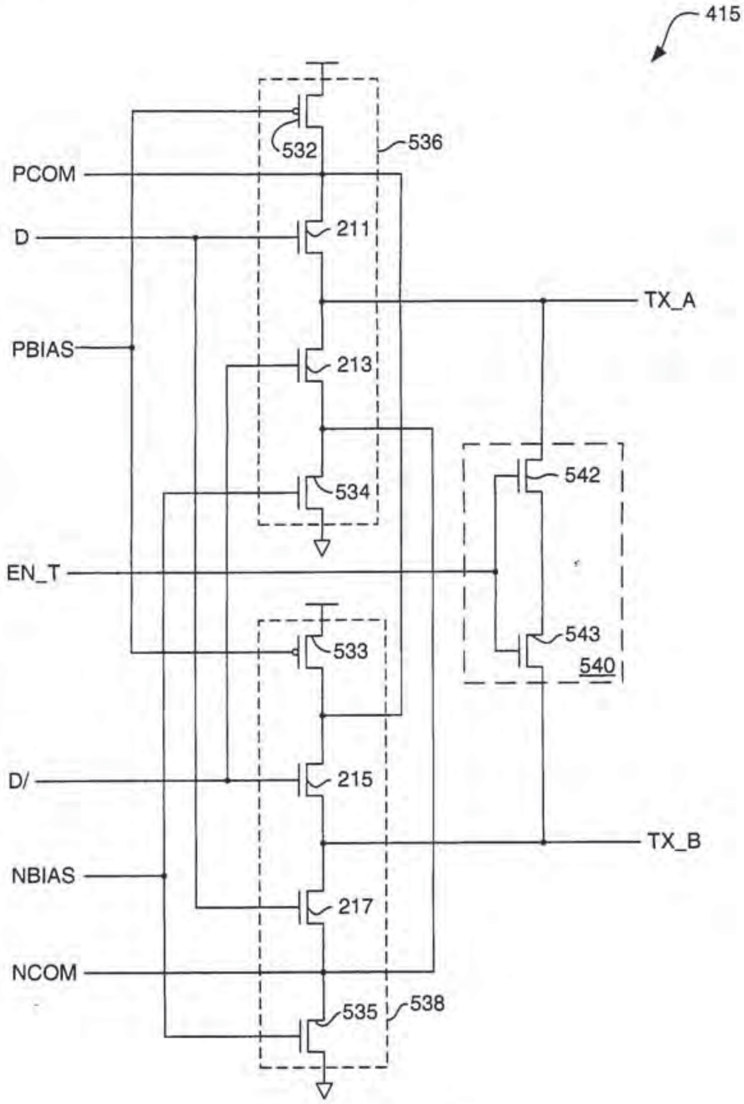
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FIG. 5B

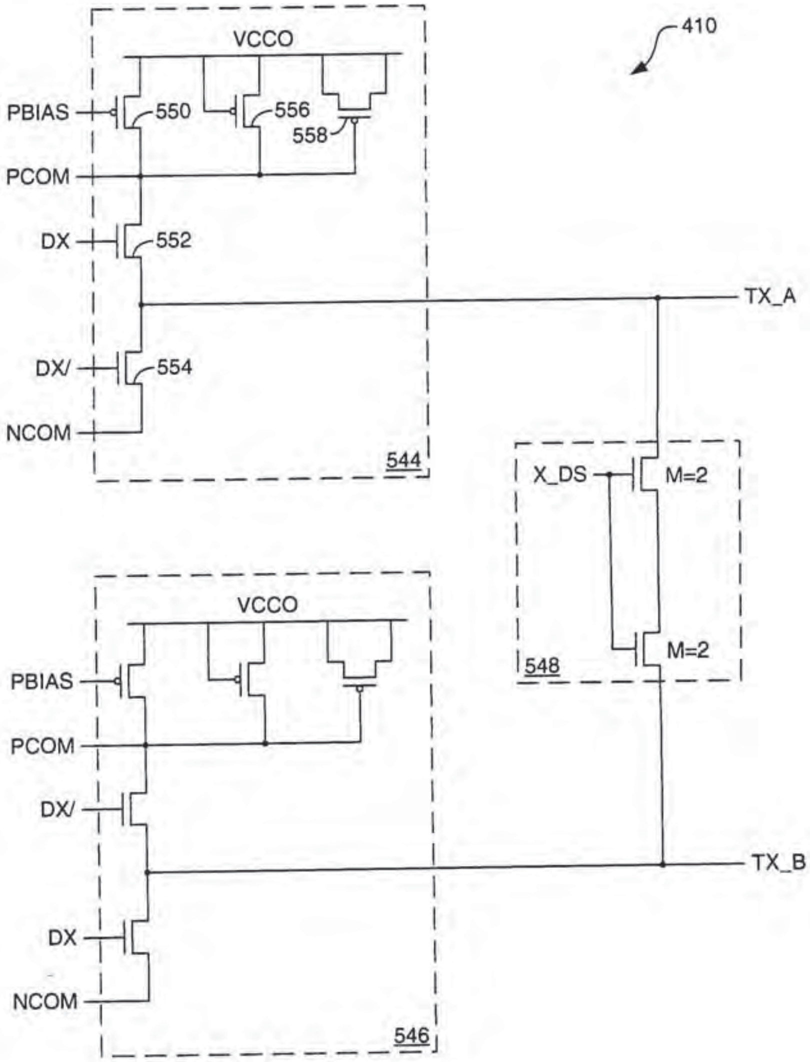
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FIG. 5C

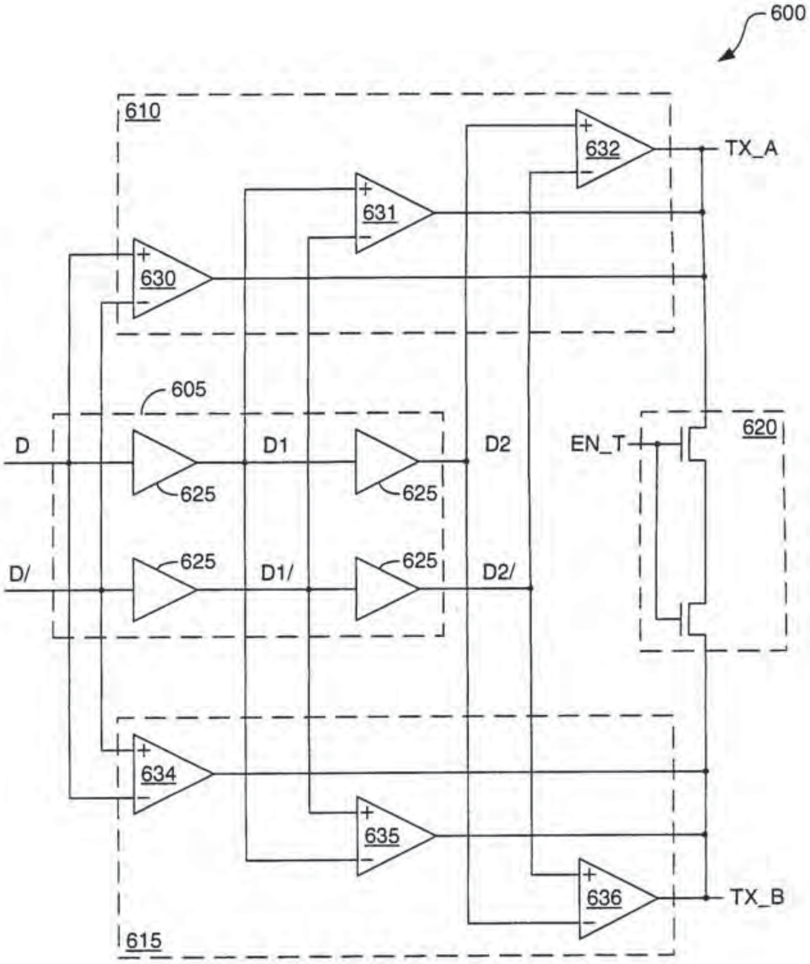
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FIG. 6

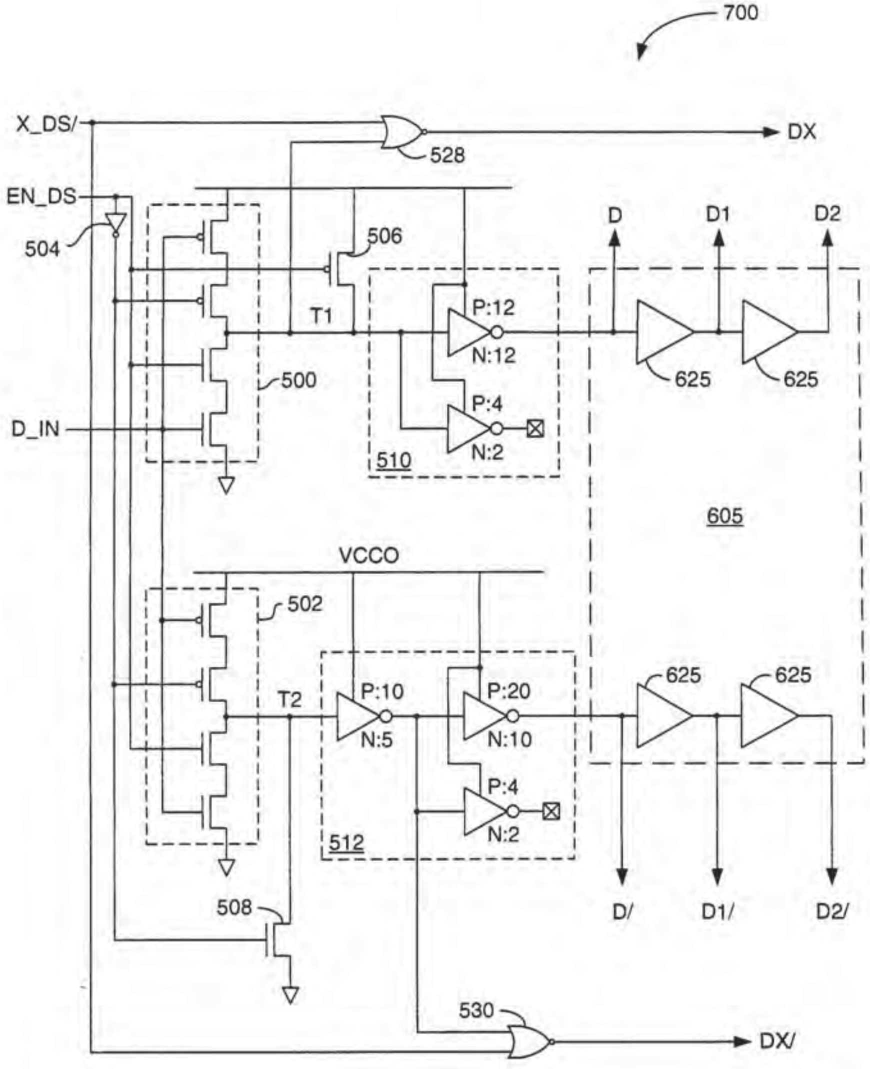
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FIG. 7A

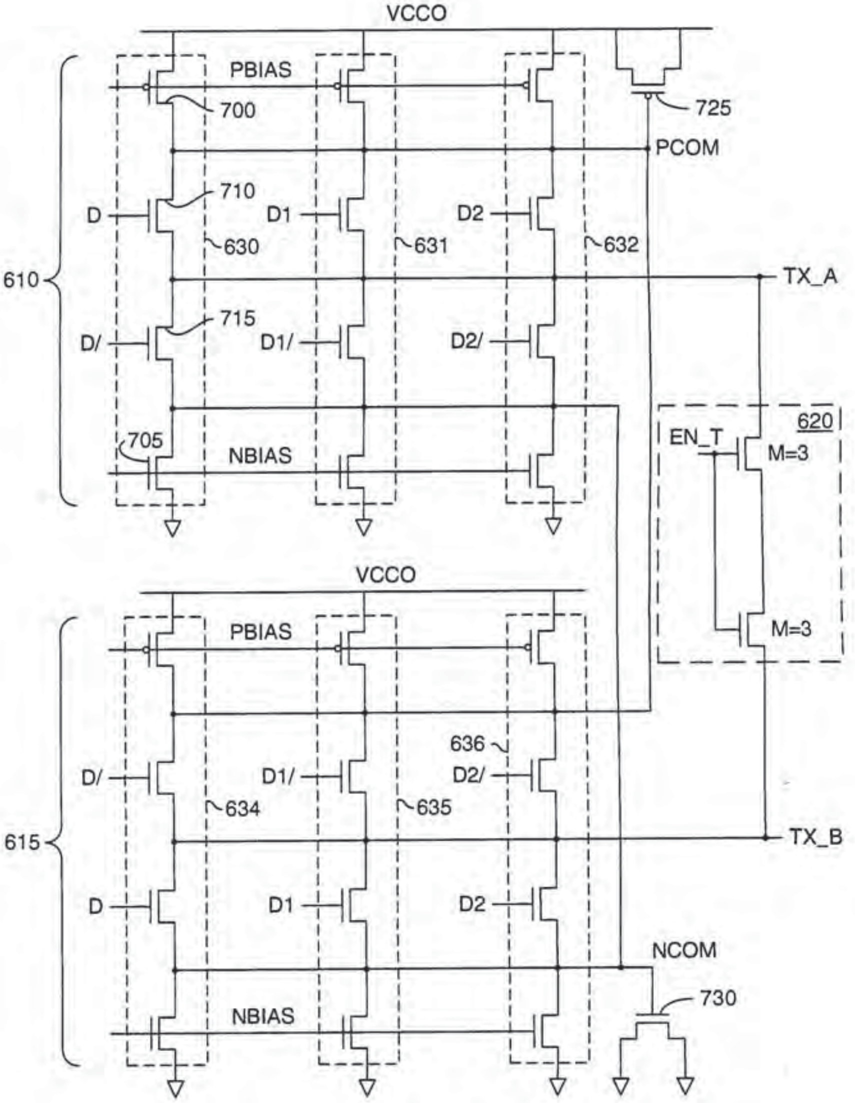
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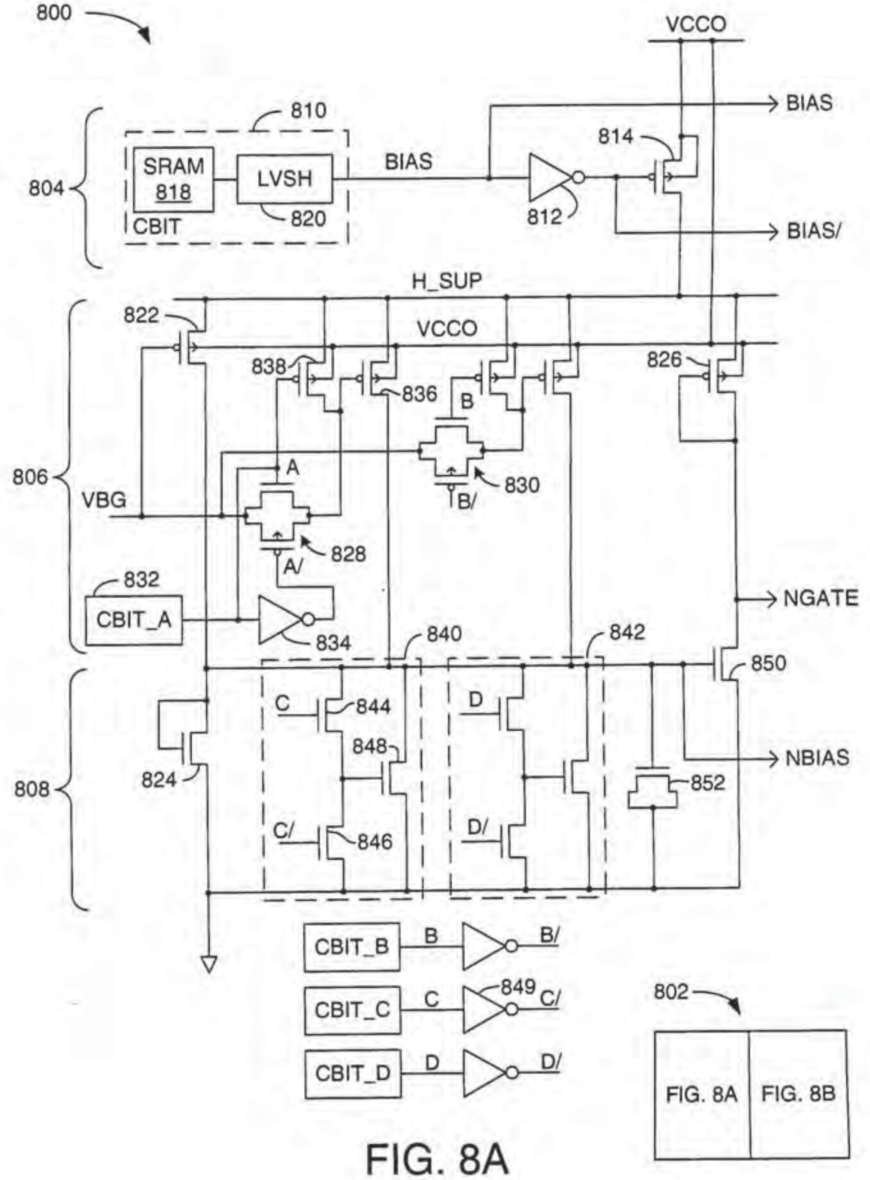
FIG. 7B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852
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846
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802
FIG. 8A
FIG. 8B

FIG. 8A

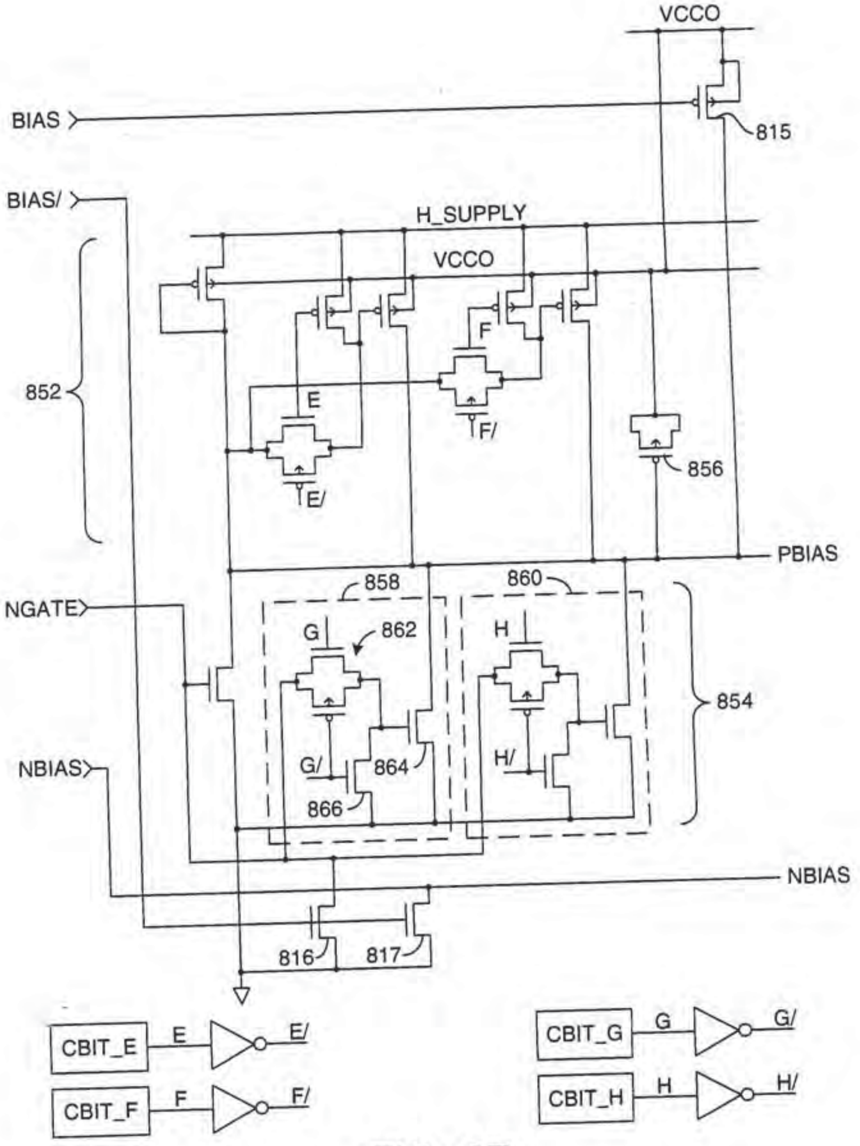
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FIG. 8B

ASmith #2

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PTO/SB/08A (10-96)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	Not Yet Known
Filing Date	September 05, 2000
First Named Inventor	Atul V. Ghia
Group Art Unit	Not Yet Known
Examiner Name	Not Yet Known
Attorney Docket Number	X-784 US

10820 U.S. PTO 09/655168 09/05/00

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.¹	U.S. Patent Document Number	Kind Code ² (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
DC		5,958,026		Goetting et al.	09-28-99	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No.¹	Foreign Patent Document Office ³	Number ⁴	Kind Code ⁵ (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶

Examiner Signature	Daniel Chang	Date Considered	8/30/01

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(use as many sheets as necessary)

Sheet 2 of 2

Complete if Known

Application Number	~~Not Yet Known~~
Filing Date	September 05, 2000
First Named Inventor	Atul V. Ghia
Group Art Unit	Not Yet Known
Examiner Name	Not Yet Known
Attorney Docket Number	X-784 US

09/655168

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials [*]	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
DC		Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits," TIA/EIA-644, March 1996	
DC		Jon Brunetti and Brian Von Herzen, "Multi-Drop LVDS with Virtex-E FPGAs," XAPP231 (Version 1.0) 09/23/99	
DC		Application Report "LVDS Multidrop Connections" published by Texas Instruments, July 1999	

Examiner Signature	Daniel Chang	Date Considered	8/30/01

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.

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#2

US005958026A

United States Patent [19]

Goetting et al.

[11] **Patent Number: 5,958,026**

[45] **Date of Patent: Sep. 28, 1999**

[54] **INPUT/OUTPUT BUFFER SUPPORTING MULTIPLE I/O STANDARDS**

[75] Inventors: **F. Erich Goetting**; **Scott O. Frake**, both of Cupertino; **Venu M. Kondapalli**, San Jose, all of Calif.

[73] Assignee: **Xilinx, Inc.**, San Jose, Calif.

[21] Appl. No.: **08/837,022**

[22] Filed: **Apr. 11, 1997**

[51] **Int. Cl.**^{6} **G06F 13/00**

[52] **U.S. Cl.** **710/52**; 710/1; 710/57; 710/58

[58] **Field of Search** 307/475, 465; 364/200, 900, 490; 365/189.05; 371/22.6; 326/39; 395/250, 872, 873, 874, 875, 876, 877, 878, 855, 866, 867, 851

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Weste, N. and Eshraghian, K. "Principles of CMOS VLSI Design—A Systems Perspective", Second Edition, Addison–Wesley, 1993, pp 84–86.

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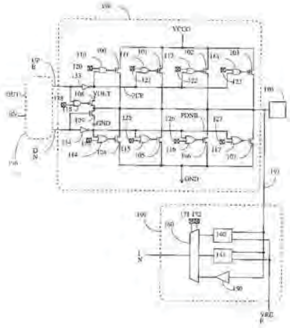
(List continued on next page.)

Primary Examiner—Hassan Kizou
Assistant Examiner—Rijue Mai
Attorney, Agent, or Firm—Lois D. Cartier

[57] **ABSTRACT**

The invention comprises a configurable input/output buffer for an FPGA that can be configured to comply with any of two or more different I/O standards. Factors such as output drive strength, receiver type, output driver type, and output signal slew rate are configurably controlled. In some embodiments, the input power supply and the output power supply can be different from the core voltage supply. In one embodiment, two or more differential amplifiers in the same configurable input buffer use different input reference voltages. According to a second aspect of the invention, the I/O pad are configurably connected to the input reference voltage line. According to a third aspect of the invention, the reference input of an I/O is configurably connected to any of two or more input reference voltage lines. According to another aspect of the invention, a single input reference voltage or a single output voltage supply is applied to each Input/Output Block (IOB), with IOBs grouped into sets. Each set of IOBs has a separate input reference voltage and/or a separate output voltage supply.

16 Claims, 9 Drawing Sheets



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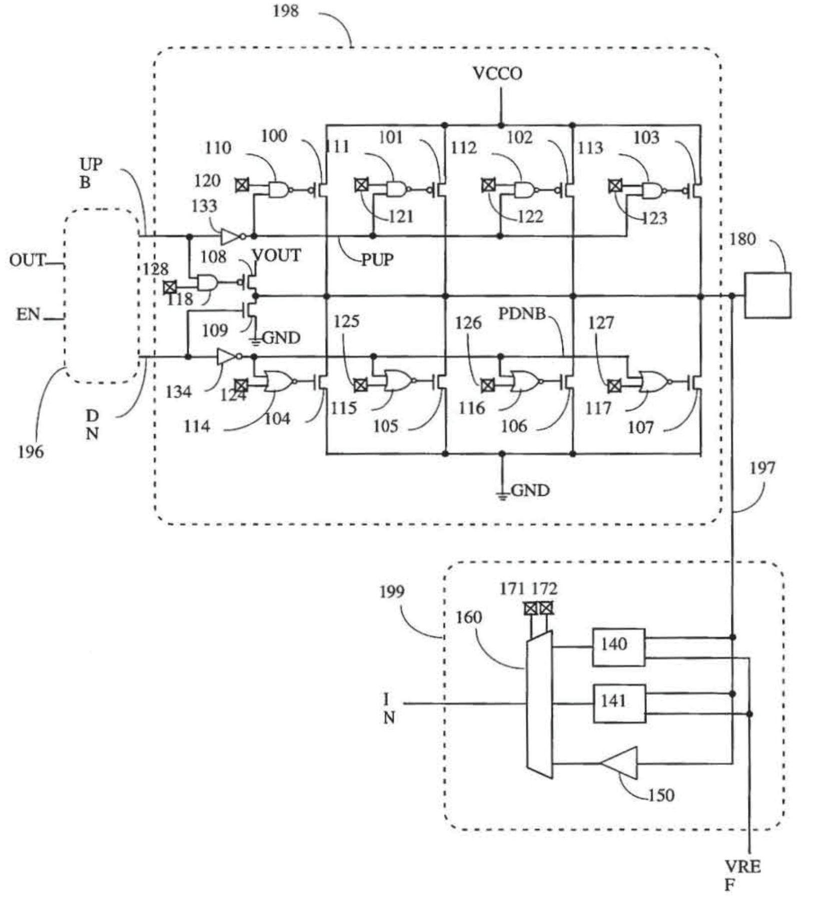
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117
114
104
105
106
107
D
N
196
GND
197
199
171 172
160
140
141
I
N
150
VRE
F

FIG. 1

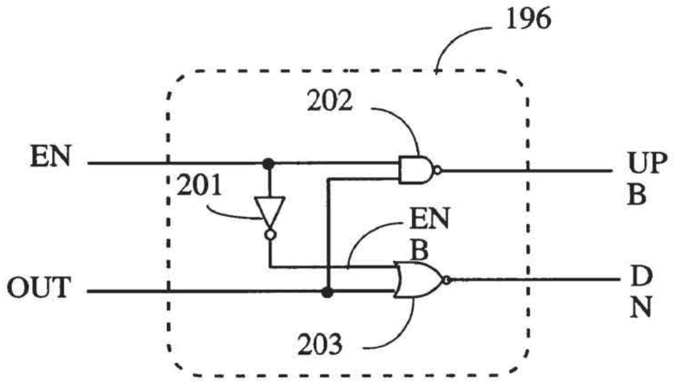

FIG. 2
(Prior Art)

OUT	EN	UPB	DN
0	0	1	0
0	1	1	1
1	0	1	0
1	1	0	0

FIG. 2A
(Prior Art)

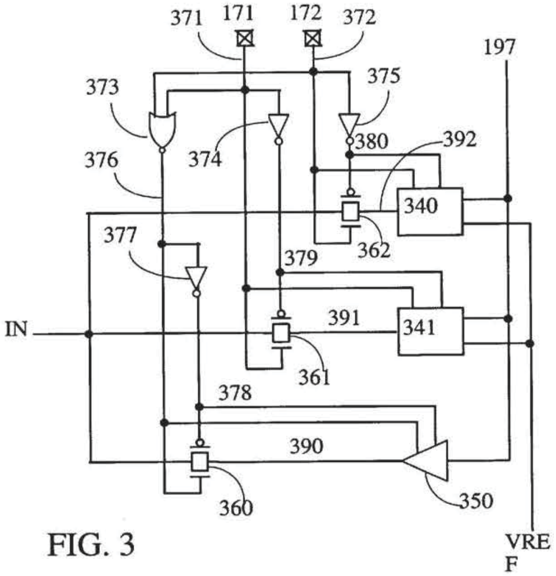
371
171
172
372
197
373
375
374
380
392
376
340
362
377
379
391
341
IN
361
378
390
350
360
VRE
F

FIG. 3

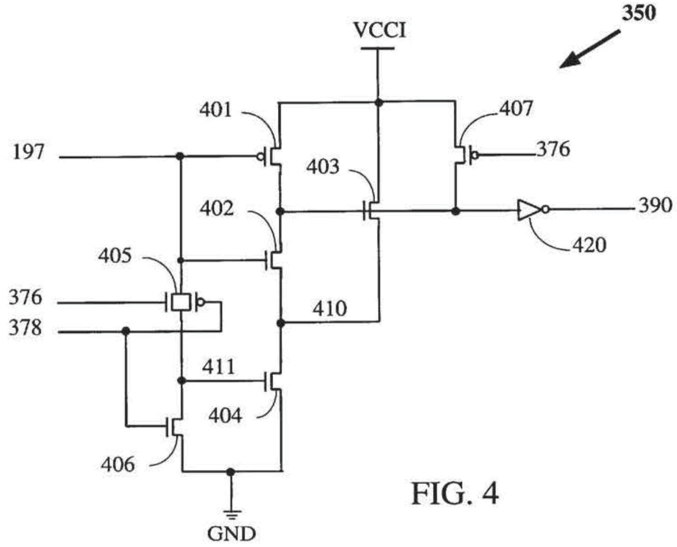
350
VCCI
401
407
197
376
403
402
390
420
405
376
378
410
411
404
406
GND

FIG. 4

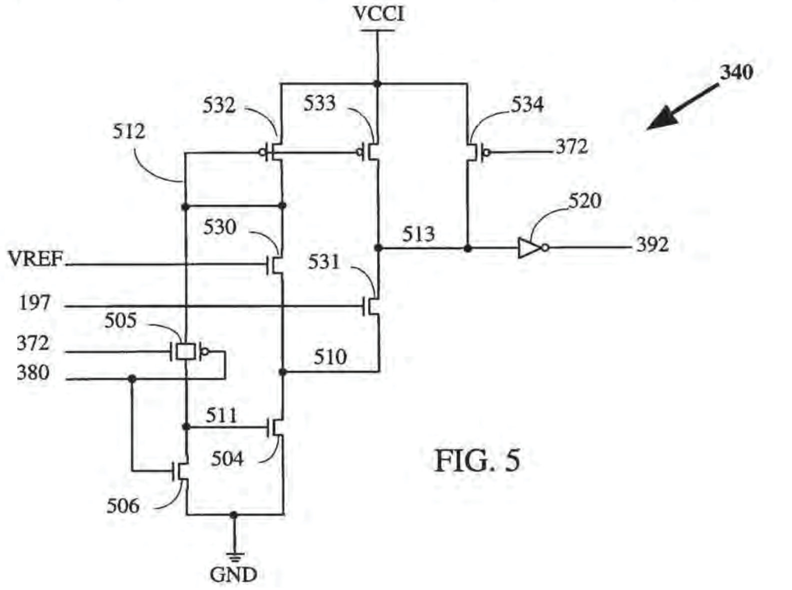
VCCI
340
532
533
534
512
372
520
530
513
VREF
531
392
197
505
372
380
510
511
504
506
GND

FIG. 5

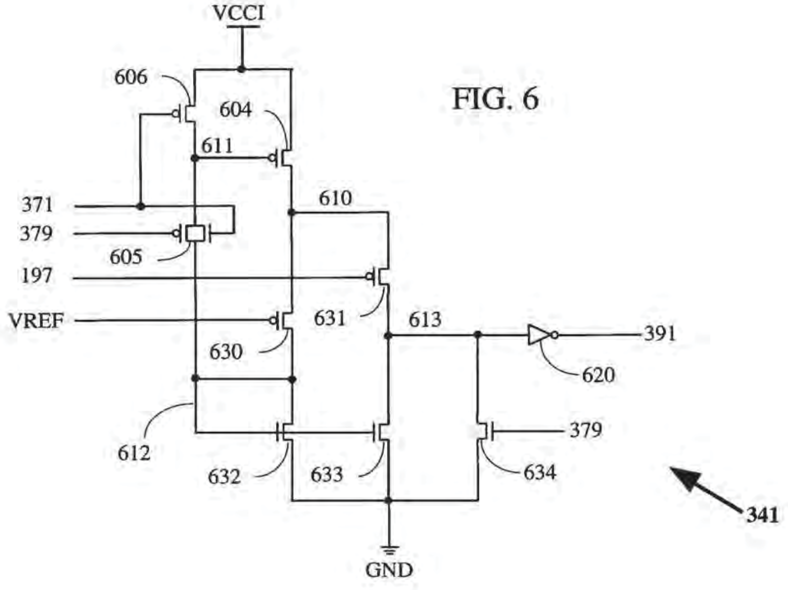
VCCI
606
604
611
371
610
379
605
197
631
613
VREF
391
630
620
612
379
632
633
634
341
GND

FIG. 6

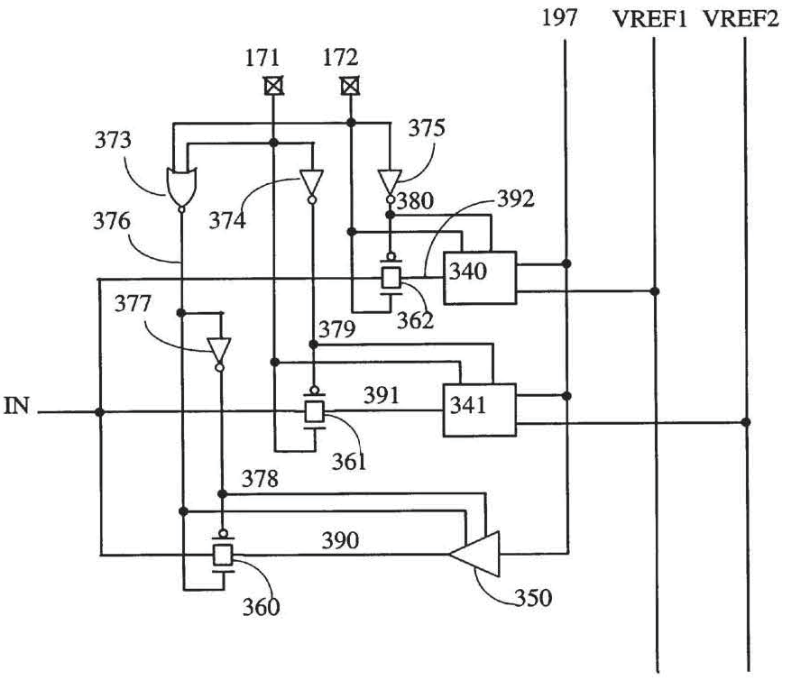
197
VREF1
VREF2
171
172
373
375
376
374
380
392
340
362
377
379
IN
391
341
361
378
390
360
350

FIG. 7

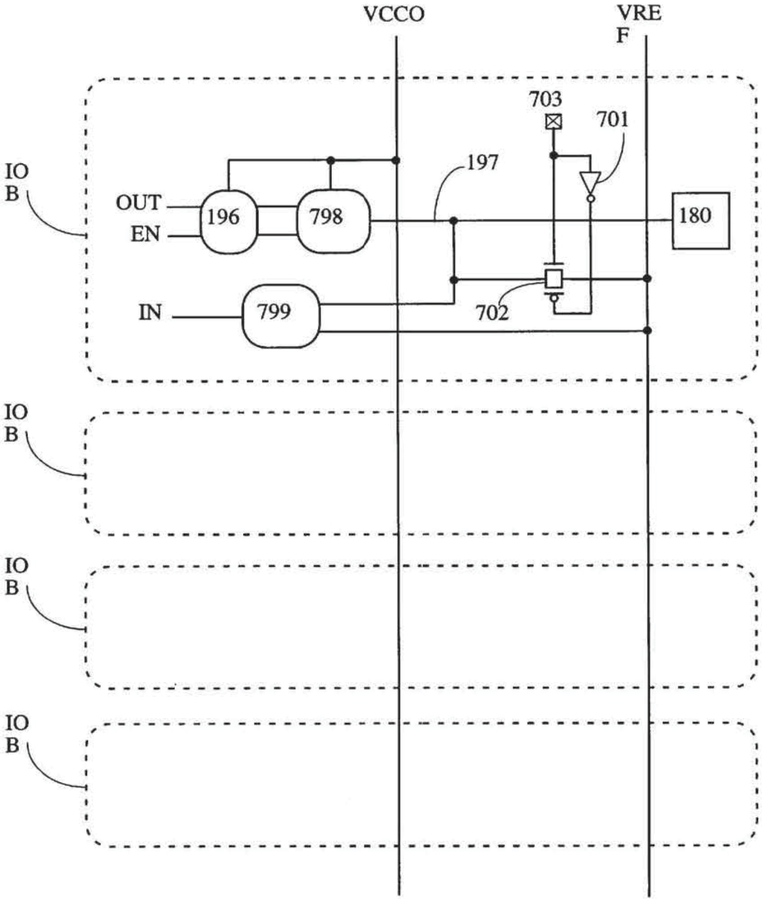
VCCO
VRE
F
703
701
197
IO
B
OUT
EN
196
798
180
IN
799
702
IO
B
IO
B
IO
B

FIG. 8

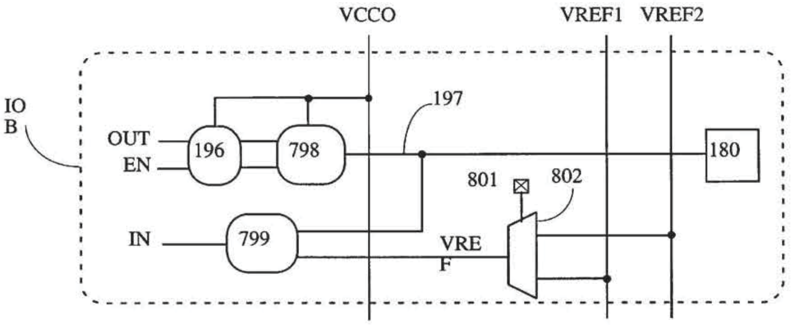
VCCO
VREF1
VREF2
IO
B
197
OUT
EN
196
798
180
801
802
IN
799
VRE
F

FIG. 9

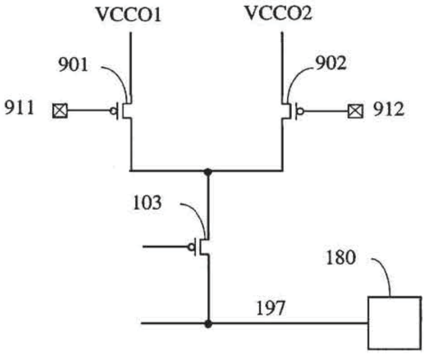
VCCO1
VCCO2
901
902
911
912
103
180
197

FIG. 9A

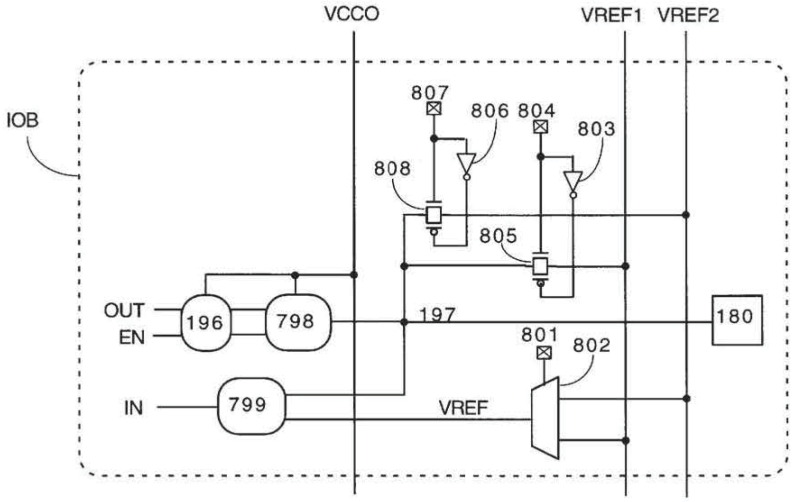
VCCO
VREF1
VREF2
IOB
807
806
804
803
808
805
OUT
EN
196
798
197
180
801
802
IN
799
VREF

FIG. 10

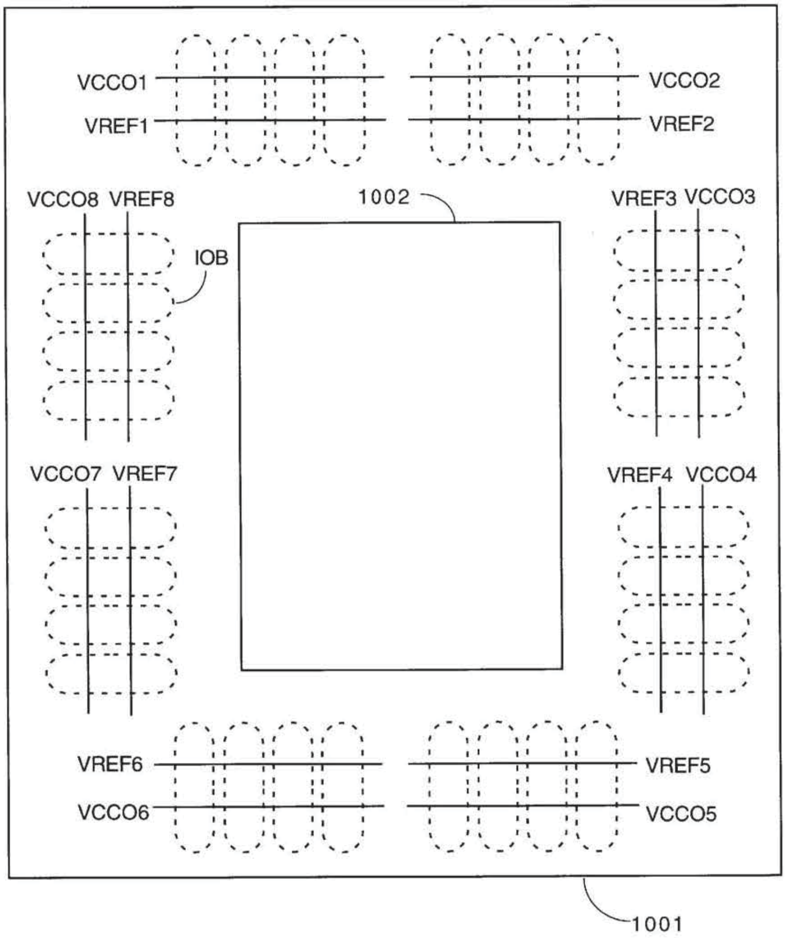
VCCO1
VREF1
VCCO2
VREF2
VCCO8
VREF8
IOB
1002
VREF3
VCCO3
VCCO7
VREF7
VREF4
VCCO4
VREF6
VCCO6
VREF5
VCCO5
1001

FIG. 11

INPUT/OUTPUT BUFFER SUPPORTING MULTIPLE I/O STANDARDS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to commonly assigned, currently-filed U.S. patent application Ser. No. 08/837,023, now U.S. Pat. No. 5,877,632, [docket X-344 US] invented by F. Erich Goetting, Scott O. Frake, Venu M. Kondapalli, and Steven P. Young entitled "FPGA WITH A PLURALITY OF I/O VOLTAGE LEVELS", which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to Field Programmable Gate Arrays (FPGAs). More particularly, the invention relates to a configurable input/output (I/O) buffer for an FPGA.

2. Description of the Background Art

Existing I/O structures for integrated circuits (ICs) are typically designed to function according to a specific I/O standard. There are several different I/O standards in use, and new standards are often introduced. These I/O standards typically include such factors as output drive strength, receiver type, output driver type, and output signal slew rate. One such I/O standard is the GTL+ standard, described in pages 46 through 50 of the Pentium Pro Processor data sheet entitled "PENTIUM PRO PROCESSOR AT 150 MHz, 166 MHz, 180 MHz and 200 Mhz", published November 1995 and available from Intel Corporation, 2200 Mission College Blvd., Santa Clara, Calif. 95052-8119, which are incorporated herein by reference. ("Pentium" is a registered trademark owned by Intel Corporation.)

A typical Input/Output Block (IOB) in an FPGA supports only one I/O standard. However, FPGAs are often used to implement "glue logic" (logic used to interface between two or more standard circuits) and therefore often interface with multiple ICs. It would be desirable for an FPGA to be able to interface with ICs that follow two or more different I/O standards.

Additionally, existing I/O structures are typically designed to function at a specific supply voltage. For example, for many years, the majority of commercially available ICs were designed to function at a supply voltage of 5 Volts. However, as the typical gate length decreases throughout the IC industry, the typical supply voltage used in FPGAs and other ICs is decreasing. Many ICs are now available that function at 3.3 Volts, and voltages of 2.5 Volts and below are commonly discussed. Therefore, it would be desirable for an FPGA to be able to interface with different ICs that function at two or more different supply voltages.

It is known in FPGA design to use one voltage for driving outputs and a different voltage in the interior (core) of the FPGA. One FPGA having a separate output voltage supply is the FLEX 10K™ FPGA from Altera Corporation, as disclosed on pages 54 to 59 of the "FLEX 10K Embedded Programmable Logic Family Data Sheet" from the Altera Digital Library 1996, available from Altera Corporation, 2610 Orchard Parkway, San Jose, Calif. 95134-2020, which are incorporated herein by reference. ("FLEX 10K" is a trademark of Altera Corporation.) In the FLEX 10K device, output voltage supply pins are provided that can be connected as a group to only one output supply voltage, either a 3.3-Volt or a 5-Volt power supply. Known FPGAs therefore typically provide for a single output supply voltage, which applies to all configurable I/O buffers on the FPGA.

Output slew rate is also programmable in known FPGAs including the XC3000 family of devices from Xilinx, Inc., as described on pages 4-292 through 4-293 of the Xilinx 1996 Data Book entitled "The Programmable Logic Data Book", available from Xilinx, Inc., 2100 Logic Drive, San Jose, Calif. 95124, which are incorporated herein by reference. (Xilinx, Inc., owner of the copyright, has no objection to copying these and other pages referenced herein but otherwise reserves all copyright rights whatsoever.) However, in such FPGAs, factors such as output drive strength, receiver type, and output driver type are not known to be configurable to meet a particular I/O standard.

Some I/O standards require that an input reference voltage be supplied. An input voltage above the input reference voltage is interpreted as a "high" voltage level; an input voltage below the input reference voltage is interpreted as a "low" voltage level. Therefore, the input reference voltage establishes a "trip point" for interpreting input signals. As far as is known, no FPGA allows a user to supply an input reference voltage.

SUMMARY OF THE INVENTION

To fully understand the invention, it is first necessary to define the several voltage levels involved in input/output buffers according to the several aspects of the invention. The "core voltage", VCCC, is the supply voltage used for the interior (non-I/O) part of the FPGA. (In one embodiment, VCCC is also used as the supply voltage for the pulldown logic in the pre-driver and output buffer.) The "input supply voltage", VCCI, is the supply voltage used for the input buffer. The "output supply voltage", VCCO, is the supply voltage used for the pullup logic in the output buffer. The terms VCCC, VCCI, and VCCO are also used to designate the power supplies supplying the corresponding voltages. Two or more of these voltages may be connected to each other; in one embodiment VCCC and VCCI are connected together and VCCO is separate. The input reference voltage required by some I/O standards is referenced herein as VREF.

A first aspect of the invention comprises a configurable input/output buffer for an FPGA that can be configured to comply with any of two or more different I/O standards. In one embodiment of the invention, input signals can be supplied to the FPGA at a voltage level with a specified switching point, where the specified switching point (the input reference voltage) is externally supplied to the FPGA. Other factors that vary from one I/O standard to another are also configurable.

One input/output buffer according to the invention comprises two configurable buffers, an input buffer and an output buffer. The two buffers may be separately or collectively configurable. In some embodiments, only the input buffer, or only the output buffer, is configurable.

In one embodiment, the input buffer can be configured to select a particular I/O standard. The input standard is selected by configuring an input multiplexer that selects between three input paths from the pad to an input signal line: 1) a Schmitt trigger such as is commonly used in FPGAs; 2) a differential amplifier for low input reference voltages (voltages below about 0.7 Volts); and 3) a differential amplifier for high input reference voltages (voltages above about 0.7 Volts). A standard input buffer can be used instead of a Schmitt trigger. The input reference voltage for the differential amplifier is dependent on the I/O standard and is supplied by the user. In one embodiment, two or more differential amplifiers in the same configurable input buffer use different input reference voltages.

In one embodiment, the output buffer can be configured to select a particular I/O standard. The I/O standard is selected by providing a series of pullups (pullup devices) and pulldowns (pulldown devices) on the output pad line (a signal line connected to the I/O pad), and by connecting the appropriate supply voltage to the output supply voltage (VCCO) pads. One or more pullups and pulldowns are enabled or disabled by configuration logic, such that the resulting total pullup and pulldown transistor widths correspond to the values needed to implement a particular I/O standard. According to the invention, for any particular standard the maximum voltage on a voltage-high output signal is set by the user by connecting the output voltage power supply to the desired voltage level.

According to a second aspect of the invention, the I/O pad line is configurably connected to the input reference voltage line driving the input reference voltage input port (hereinafter referred to as the "reference input") in the IOB. Therefore, an I/O pad can be used to supply the input reference voltage.

According to a third aspect of the invention, the reference input of an IOB is configurably connected in the IOB to any of two or more available input reference voltages. Alternatively, the output voltage supply of an IOB is configurably connected in the IOB to any of two or more available output supply voltages.

According to a fourth aspect of the invention, a single input reference voltage is applied to each IOB, with the IOBs grouped into sets. Each set of IOBs has a separate input reference voltage. In one embodiment, each input reference voltage is applied to the IOBs on one half-edge of the FPGA die. Therefore, on a rectangular die, eight separate input reference voltages are applied. These input reference voltages can be connected together outside the FPGA package, or within the FPGA package by leads or other means, or configurably connected within the FPGA.

According to a fifth aspect of the invention, the IOBs are grouped into sets and each set of IOBs has a separate output voltage supply. In one embodiment, each output voltage supply is applied to the IOBs on one half-edge of the FPGA die. Therefore, on a rectangular die, eight separate output voltage supplies are applied to eight sets of IOBS. In one embodiment, input reference voltages and output voltage supplies are each applied to one half-edge of an FPGA die. Therefore, in this embodiment eight separate input reference voltages and eight separate output voltage supplies are applied to eight sets of IOBs.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the following figures.

FIG. **1** shows a schematic representation of an input/output buffer according to a first aspect of the invention.

FIG. **2** shows a schematic representation of a prior art pre-driver that can be used in the embodiment of FIG. **1**.

FIG. **2**A shows a state table for the prior art pre-driver of FIG. **2**.

FIG. **3** shows a detailed schematic representation of the input buffer portion of FIG. **1**.

FIG. **4** shows a schematic representation of a Schmitt trigger in the input buffer of FIG. **3**.

FIG. **5** shows a schematic representation of an NMOS differential amplifier in the input buffer of FIG. **3**. (An NMOS differential amplifier is a differential amplifier wherein the input and VREF are connected to N-channel transistors.)

FIG. **6** shows a schematic representation of a PMOS differential amplifier in the input buffer of FIG. **3**. (A PMOS differential amplifier is a differential amplifier wherein the input and VREF are connected to P-channel transistors.)

FIG. **7** shows a configurable input buffer according to another embodiment of the invention in which two differential amplifiers in the same configurable input buffer use different input reference voltages.

FIG. **8** shows an FPGA IOB in which the I/O pad is configurably connected to the input reference voltage line according to a second aspect of the invention.

FIG. **9** shows an IOB in which the reference input is configurably connected to either of two available input reference voltage lines in accordance with a third aspect of the invention.

FIG. **9**A shows a structure for configurably using either of two output voltage supplies in a single IOB.

FIG. **10** shows an IOB in which the reference input is configurably connected to either of two available input reference voltages, and the I/O pad is configurably connected to either of two available input reference voltage lines.

FIG. **11** shows a simplified drawing of an FPGA I/O pad ring with eight separate input reference voltages and eight separate output voltage supplies.

DETAILED DESCRIPTION OF THE DRAWINGS

Several embodiments of the invention are described. In the following description, numerous specific details are set forth in order to provide a more thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known features have not been described in detail in order not to unnecessarily obscure the present invention.

First Aspect of the Invention

FIG. **1** shows an input/output buffer according to a first aspect of the invention. The input/output buffer of FIG. **1** comprises: 1) pre-driver **196**, driven by output signal line OUT and enable signal EN and driving signal lines UPB and DN; 2) output buffer **198**, driven by signal lines UPB and DN and driving pad line **197**; 3) pad **180** coupled to pad line **197**; and 4) input buffer **199**, driven by pad line **197** and driving input signal line IN.

In output buffer **198**, signal line UPB drives **2**-input AND-gate **118**, which drives PMOS pullup **108** connected to pad line **197**. (AND-gate **118** may be implemented as a NAND-gate followed by an inverter.) The second input to AND-gate **118** is a configuration bit in configuration memory cell **128**. (Configuration memory cells are represented in the figures herein by a box containing an "x".) Memory cell **128** can therefore be used to disable pullup **108** when an open-drain output is required. Signal line UPB further drives inverter **133** which generates active-high pullup signal PUP. Signal line DN directly drives NMOS pulldown **109** connected to pad line **197**, and further drives inverter **134** which generates active-low pulldown signal PDNB. In one embodiment, inverters **133**, **134** are designed to function as delay elements, ensuring that pullup **108** and pulldown **109** become active before any other pullups or pulldowns in output buffer **198**, thereby reducing ground bounce.

Output buffer **198** further comprises four pullups **100**, **101**, **102**, **103**. In the embodiment of FIG. **1**, pullups **100**, **101**, **102**, **103**, **108** are implemented as PMOS transistors, but NMOS transistors or resistors can be used. In this embodiment, each pullup **100**, **101**, **102**, **103** is driven by a **2**-input NAND-gate, **110**, **111**, **112**, **113**, respectively. Each NAND-gate **110**, **111**, **112**, **113** is enabled or disabled by a configuration bit in one of configuration memory cells **120**, **121**, **122**, **123**, respectively. In this embodiment, when a configuration bit in one of configuration memory cells **120**, **121**, **122**, **123**, **128** is at a high voltage level, the corresponding pullup is enabled, and pad line **197** is pulled high whenever pullup signal PUP goes high.

Using the configuration bits in configuration memory cells **120**, **121**, **122**, and **123**, one, two, three, or four pullups are configurably enabled. (However, a configurably enabled pullup does not become active until pullup signal PUP goes high.) When a different I/O standard is needed, the number of enabled pullups can be changed. A ratio of 1:2:4:8 in pullup widths is found to give a wide range of output drive capabilities, allowing the formation of total configurable pullup widths of 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, and 15 times the width of the narrowest pullup. This total configurable pullup width (made up of those of pullups **100**, **101**, **102**, **103** which are configurably enabled) is then added to the width of pullup **108** to make the total pullup width. Different types of configuration logic for enabling and disabling the pullups can be used, such as a separate configurable enabling gate in series with each pullup. Different numbers of pullups or pullups of different widths can be provided. The slew rate of a rising-edge output signal can be controlled by controlling the rate at which each pullup turns on, for example by giving each controlling NAND-gate or other circuit a different rise or fall time, or by inserting delay elements into pullup signal PUP so that the different pullups become active at different times. These and other modifications fall within the scope of the invention.

Output buffer **198** further comprises four pulldowns **104**, **105**, **106**, **107** (in addition to pulldown **109**) that can pull pad line **197** to ground voltage level GND. Pulldowns **104**, **105**, **106**, **107** are controlled in this embodiment by 2-input NOR-gates **114**, **115**, **116**, **117**, respectively. Each NOR-gate **114**, **115**, **116**, **117** is enabled or disabled by a configuration bit in one of configuration memory cells **124**, **125**, **126**, **127**, respectively. In this embodiment, when a configuration bit in one of configuration memory cells **124**, **125**, **126**, **127** is at a low voltage level, the corresponding pulldown is enabled. As with the configurable pullups, many modifications can be applied to the configurable pulldowns and these modifications fall within the scope of the invention.

In this embodiment, all logic on the pullup side of output buffer **198** (comprising pullups **100**, **101**, **102**, **103**, **108**, NAND-gates **110**, **111**, **112**, **113**, AND-gate **118**, and inverter **133**) uses output voltage supply VCCO as the positive voltage supply. All logic on the pulldown side of output buffer **198** (comprising NOR-gates **114**, **115**, **116**, **117** and inverter **134**) uses the core supply voltage VCCC (connections to VCCC not shown in FIG. **1**) as the positive voltage supply.

In one embodiment, device sizes in output buffer **198** are as follows. A single number indicates a device width in microns, and two numbers formatted as "p/n" indicate gate widths in microns of P-channel and N-channel devices, respectively, in a logic gate. All gate lengths are 0.25 microns except as otherwise noted, in which case they are given in microns. The term "N-channel" denotes an N-channel transistor. The term "P-channel" denotes a P-channel transistor.

Pullup **100**: 40
Pulldown **104**: 40
Pullup **108**: 40
Pullup **101**: 80
Pulldown **105**: 80
Pulldown **109**: 40
Pullup **102**: 160
Pulldown **106**: 160
Inverter **133**: 8/4 (gate length 0.5)
Pullup **103**: 320
Pulldown **107**: 320
Inverter **134**: 8/4 (gate length 0.5)
NAND-gate **110**: 4/4
NOR-gate **114**: 4/4
NAND-gate **111**: 8/8
NOR-gate **115**: 8/8
NAND-gate **112**: 16/16
NOR-gate **116**: 16/16
NAND-gate **113**: 32/32
NOR-gate **117**: 32/32

FIG. **1** also shows a simplified schematic drawing of configurable input buffer **199**. Input buffer **199** comprises input multiplexer **160**, which is configured by configuration bits in configuration memory cells **171**, **172** to select the input path compatible with the desired I/O standard. Multiplexer **160** passes the signal from the selected input path to input signal line IN. Input multiplexer **160** has three inputs. One input to multiplexer **160** is supplied by Schmitt trigger **150**. (Schmitt triggers are well known to persons of ordinary skill in the art of input buffer design.) When enabled, Schmitt trigger **150** passes on the signal on pad line **197**. A second input to input multiplexer **160** is supplied by differential amplifier **140**, which in one embodiment is an NMOS differential amplifier that compares the voltage level on pad line **197** to the input reference voltage on reference input VREF. If the voltage level on pad line **197** is higher than the input reference voltage on reference input VREF, the output of NMOS differential amplifier **140** is high; otherwise it is low. NMOS differential amplifier **140** only functions correctly when the input reference voltage on reference input VREF is above about 0.7 Volts. Therefore, in one embodiment NMOS differential amplifier **140** is only configured as active when following I/O standards that specify an input reference voltage above about 0.7 Volts. A third input to input multiplexer **160** is supplied by differential amplifier **141**, which in one embodiment is a PMOS differential amplifier. In one embodiment, PMOS differential amplifier **141** is only configured as active when following I/O standards that specify an input reference voltage below about 0.7 Volts. In one embodiment, the configuration logic disables the unused Schmitt trigger and/or differential amplifier(s), to reduce power consumption. However, this capability is not an essential part of the input/output buffer of the invention. The input reference voltage on reference input VREF is dependent on the I/O standard and is supplied by the user.

In this embodiment, input buffer **199** uses input supply voltage VCCI (not shown in FIG. **1**) as the positive voltage supply.

In one embodiment of the invention, each input/output buffer is separately configurable. However, two or more input/output buffers can be grouped such that they are controlled by the same configuration bits. In another embodiment of the invention, only a configurable input buffer may be provided. In yet another embodiment of the invention, only a configurable output buffer may be provided.

FIG. **2** shows prior art pre-driver **196** well-known in the art of output buffer design. Active-high enable signal EN is inverted by inverter **201** to generate active-low enable signal ENB. Active-high enable signal EN and output signal line OUT drive **2**-input NAND-gate **202**, which generates signal line UPB. Active-low enable signal ENB and output signal line OUT drive **2**-input NOR-gate **203**, which generates signal line DN. A state-table for input signals OUT, EN and output signals UPB, DN is shown in FIG. **2**A. From FIG. **2**A, it is seen that pullups **100**, **101**, **102**, **103**, **108** will only be activated (i.e., signal line UPB will only be low) when both output signal line OUT and enable signal EN are high. Configurable pulldowns **104**, **105**, **106**, **107** will only be activated (i.e., signal line DN will only be high) when output signal line OUT is low and enable signal EN is high.

In this embodiment, all logic on the pullup side of pre-driver **196** (comprising NAND-gate **202**) uses output voltage supply VCCO (not shown in FIG. **2**) as the positive voltage supply. All logic on the pulldown side of pre-driver **196** (comprising NOR-gate **203** and inverter **201**) uses the core supply voltage VCCC (not shown in FIG. **2**) as the positive voltage supply.

FIG. **3** shows a more detailed schematic of input buffer **199** of FIG. **1**. In this embodiment, multiplexer **160** of FIG. **1** is implemented as three transmission gates **360**, **361** and **362**, each comprising one N-channel transistor and one P-channel transistor. Transmission gate **362**, which configurably passes the output of NMOS differential amplifier **340** to input signal line IN, is enabled by a configuration bit in configuration memory cell **172** and its complement signal on line **380** generated by inverter **375**. Transmission gate **361**, which configurably passes the output of PMOS differential amplifier **341** to input signal line IN, is enabled by a configuration bit in configuration memory cell **171** and its complement signal on signal line **379** generated by inverter **374**. Transmission gate **360**, which configurably passes the output of Schmitt trigger **350** to input signal line IN, is enabled by the output (signal line **376**) of NOR-gate **373** and its complement signal on signal line **378** generated by inverter **377**. NOR-gate **373** is driven by the configuration bits in configuration memory cells **171**, **172**.

In one embodiment, device sizes in the input buffer of FIG. **3** are as follows:

Inverter **374**: 1/1
Inverter **375**: 1/1
Inverter **377**: 1/1
Transmission Gate **360**: 3/3
Transmission Gate **361**: 3/3
Transmission Gate **362**: 3/3
NOR-gate **373**: 1/1

FIG. **4** shows a schematic representation of Schmitt trigger **350** in the input buffer of FIG. **3**. The operation of Schmitt trigger **350** is not explained herein, as Schmitt trigger input buffers are notoriously well-known in the art. One such Schmitt trigger is described in U.S. Reissue Pat. No. Re. 34,808, "TTL/CMOS Compatible Input Buffer with Schmitt Trigger", which is incorporated herein by reference and title to which is held by the assignee hereof.

However, one feature distinguishes Schmitt trigger **350** from typical Schmitt triggers, and that is the ability to be enabled and disabled. Schmitt trigger **350** is controlled by enable signal lines **376** and **378** driving N-channel and P-channel transistors, respectively, of transmission gate **405**, by enable signal line **378** driving N-channel transistor **406**, and by enable signal line **376** driving P-channel transistor **407**. When the signal on line **376** is high, and the complementary signal on line **378** is low, Schmitt trigger **350** functions as a typical Schmitt trigger. When the signal on line **376** is low, and the complementary signal on line **378** is high, Schmitt trigger **350** is disabled to save power. When disabled, Schmitt trigger **350** no longer draws current from input power supply VCCI regardless of the voltage on pad line **197**.

In one embodiment, device sizes in the Schmitt trigger of FIG. **4** are as follows:

P-channel **401**: 20
N-channel **402**: 11
N-channel **403**: 9
Transmission Gate **405**: 2/2
N-channel **406**: 2
N-channel **404**: 11
Inverter **420**: 12/6
P-channel **407**: 2

FIG. **5** shows a schematic representation of NMOS differential amplifier **340** in the input buffer of FIG. **3**. The operation of NMOS differential amplifier **340** is not explained herein, as NMOS differential amplifiers are notoriously well-known in the art. One such NMOS differential amplifier is described in pages 84 through 86 of "Principles of CMOS VLSI Design: A Systems Perspective", Second Edition, by Neil H. E. Weste and Kamran Eshraghian, published in 1993 by the Addison-Wesley Publishing Company, which are incorporated herein by reference.

However, one feature distinguishes NMOS differential amplifier **340** from typical NMOS differential amplifiers, and that is the ability to be enabled and disabled. NMOS differential amplifier **340** is controlled by enable signal lines **372** and **380** driving N-channel and P-channel transistors, respectively, of transmission gate **505**, and by enable signal line **380** driving N-channel transistor **506**. When the signal on line **372** is high, and the complementary signal on line **380** is low, NMOS differential amplifier **340** functions as a typical NMOS differential amplifier. When the signal on line **372** is low, and the complementary signal on line **380** is high, NMOS differential amplifier **340** is disabled to save power. When disabled, NMOS differential amplifier **340** no longer draws current from input power supply VCCI regardless of the voltage on pad line **197**.

In one embodiment, device sizes in the NMOS differential amplifier of FIG. **5** are as follows:

P-channel **532**: 18
P-channel **533**: 18
P-channel **534**: 2
Transmission Gate **505**: 2/2
N-channel **530**: 55
N-channel **531**: 55
Inverter **520**: 18/6
N-channel **506**: 2
N-channel **504**: 12

FIG. **6** shows a schematic representation of PMOS differential amplifier **341** in the input buffer of FIG. **3**. The operation of PMOS differential amplifier **341** is not explained herein, as PMOS differential amplifiers are notoriously well-known in the art. PMOS differential amplifier **341** behaves the same way as NMOS differential amplifier **340**. Comparing FIGS. **5** and **6**, it is seen that the two circuits are mirror images except that ground voltage level GND and input supply voltage VCCI are reversed and N-channel and P-channel transistors are reversed. Transistor widths also differ in the two differential amplifiers, because of the differences between N-channel and P-channel devices.

One feature distinguishes PMOS differential amplifier **341** from typical PMOS differential amplifiers, and that is the ability to be enabled and disabled. PMOS differential amplifier **341** is controlled by enable signal lines **371** and **379** driving N-channel and P-channel transistors, respectively, of transmission gate **605**, and by enable signal line **371** driving P-channel transistor **606**. When the signal on line **371** is high, and the complementary signal on line **379** is low, PMOS differential amplifier **341** functions as a typical PMOS differential amplifier. When the signal on line **371** is low, and the complementary signal on line **379** is high, PMOS differential amplifier **341** is disabled to save power. When disabled, PMOS differential amplifier **341** no longer draws current from input power supply VCCI regardless of the voltage on pad line **197**.

In one embodiment, device sizes in the PMOS differential amplifier of FIG. **6** are as follows:

N-channel **632**: 22.5
N-channel **633**: 22.5
N-channel **634**: 2
Transmission Gate **605**: 2/2
P-channel **630**: 65
P-channel **631**: 65
Inverter **620**: 11.25/22.5
P-channel **606**: 2
P-channel **604**: 22.5

Second Embodiment of the Invention

FIG. **7** shows a configurable input buffer according to a second embodiment of the invention. The input buffer of FIG. **7** resembles the input buffer of FIG. **3**, except that two separate input reference voltages are supplied on input reference voltage lines VREF**1** and VREF**2**. NMOS differential amplifier **340** compares the voltage level on pad line **197** to the input reference voltage on input reference line VREF**1**. PMOS differential amplifier **341** compares the voltage level on pad line **197** to the input reference voltage on input reference line VREF**2**.

Second Aspect of the Invention

FIG. **8** shows an IOB according to a second aspect of the invention. The IOB of FIG. **8** comprises pre-driver **196**, output buffer **798**, pad **180** and input buffer **799**. In this embodiment, I/O pad **180** can either be used to supply input reference voltage VREF, or as a signal pad. Pad line **197**, which is connected to pad **180**, is configurably connected to an input reference voltage line (which in this embodiment is the same as reference input VREF) through transmission gate **702**. Transmission gate **702** is enabled by a configuration bit in configuration memory cell **703** and its complement generated by inverter **701**. The input reference voltage can go through transmission gate **702** to the input buffer in this fashion because transmission gate **702** does not cause a drop in voltage level on a signal passing therethrough. Input buffer **799** can be made configurable as with input buffer **199** of FIG. **1**, but a non-configurable buffer can also be used. Output buffer **798** can be made configurable as with output buffer **198** of FIG. **1**, but a non-configurable buffer can also be used.

This structure can be used to supply the input reference voltage from any configurable IOB.

Third Aspect of the Invention

FIG. **9** shows an IOB in which the reference input VREF is configurably connected to either of two available input reference voltages, in accordance with a third aspect of the invention. In this embodiment, multiplexer **802** selects between two input reference lines VREF**1** and VREF**2**. Multiplexer **802** is controlled by a configuration bit stored in memory cell **801**. Multiplexer **802** supplies reference input VREF to input buffer **799**. In other embodiments, more than two input reference voltages are available, and 2-input multiplexer **802** is replaced by a wider multiplexer controlled by more than one configuration bit. This and other modifications fall within the scope of the invention.

Similarly, the output voltage supply of an IOB can be configurably connected in the IOB to any of two or more available output supply voltages (VCCOs). In one embodiment, shown in FIG. **9**A, each pullup **103** on output pad line **197** is connected in series with two or more additional P-channel transistors **901**, **902**, each of which is connected to a different output supply voltage (VCCO**1**, VCCO**2**), and each of which can be configurably enabled or disabled by a configuration bit in one of memory cells **911**, **912**. In one embodiment, two output supply voltages are available to each IOB in the FPGA, and each IOB can be independently configured to use either of the two output supply voltages.

FIG. **10** shows an embodiment of the invention that combines the novel aspects of FIGS. **8** and **9**. In this embodiment, I/O pad **180** can be used either: 1) to supply one of two input reference voltages to input reference lines VREF**1** and VREF**2**; or 2) as an input pad with input buffer **799** using either of input reference lines VREF**1** and VREF**2** to supply the reference input. I/O pad **180** is configurably connected to input reference lines VREF**1** and VREF**2** through transmission gates **805** and **808**, respectively. Transmission gate **805** is enabled by a configuration bit in configuration memory cell **804** and its complement generated by inverter **803**. Transmission gate **808** is enabled by a configuration bit in configuration memory cell **807** and its complement generated by inverter **806**. Multiplexer **802**, as described with reference to FIG. **9**, programmably selects between VREF**1** and VREF**2** and generates reference input VREF. FIG. **10** shows only one of many combinations and variations that fall within the scope of the invention.

Fourth and Fifth Aspects of the Invention

FIG. **11** shows a simplified drawing of an FPGA I/O pad ring showing a plurality of IOBs along all four edges. (An FPGA will typically have many more IOBs than are shown in FIG. **11**, but only 32 IOBs are shown so as not to obscure the drawing.) The FPGA of FIG. **11** has eight sets of IOBs, with eight separate input reference voltages and eight separate output voltage supplies. Therefore, each set of IOBs has at least one associated input reference voltage pad, and at least one associated output supply voltage pad. The input reference voltage pads associated with different sets of IOBs are electrically isolated from each other, and the output supply voltage pads associated with different sets of IOBs are electrically isolated from each other. However, the different input reference voltage pads and/or the different output supply voltage pads may be connected together external to the FPGA. In one embodiment, there is a set of one or more output supply voltage pads associated with each set of IOBs. Each set of IOBs is connectable to a different one of such sets of output supply voltage pads.

In the embodiment of FIG. **11**, each edge has two separate input reference voltage lines (VREF**1** and VREF**2**, VREF**3** and VREF**4**, VREF**5** and VREF**6**, VREF**7** and VREF**8**) and two separate output voltage lines (VCCO1 and VCCO2, VCCO**3** and VCCO**4**, VCCO**5**, and VCCO**6**, VCCO7 and VCCO**8**, respectively). Therefore, the FPGA of FIG. **11** can interface with other ICs conforming to up to eight different I/O standards. The number of separate input reference voltages and output voltage supplies can be two, four, sixteen, or any other number. This aspect of the invention can further be applied to ICs other than FPGAs.

Advantages of the Invention

A configurable input/output buffer according to a first aspect of the present invention offers the advantages of compatibility with two or more different I/O standards. In one embodiment, each I/O can be separately configured. In another embodiment, several I/O are configured as a group. Therefore, a single FPGA can interface with two or more different ICs at the same time that follow two or more different I/O standards. Since the I/O standard followed by each input/output buffer can be changed by simply reconfiguring the FPGA, the resulting FPGA has a flexible input/output interface that can also adapt with the semiconductor industry to changes in I/O standards and operating voltage levels.

A configurable connection of an I/O pad to one or more input reference lines allows the I/O pad to supply the input reference voltage, in accordance with a second aspect of the present invention. This aspect of the invention offers the advantages of a flexible pinout assignment in an FPGA. according to this aspect of the invention, the input reference voltage can be applied at any configurable I/O pad.

A reference input that is configurably connected to any of two or more input reference voltage lines in accordance with a third aspect of the invention makes it possible to supply each of several input reference voltages to every input/output buffer in the FPGA.

The separation of input reference voltages and/or output voltage supplies in accordance with fourth and fifth aspects of the invention allows an FPGA to interface relatively easily with a plurality of ICs that operate at different voltage levels.

Thus it will be understood that the present invention provides an input/output interface with many novel aspects in an FPGA or a portion thereof.

Those having skill in the relevant arts of the invention will now perceive various modifications and additions which may be made as a result of the disclosure herein of preferred embodiments. Accordingly, all such modifications and additions are deemed to be within the scope of the invention, which is to be limited only by the appended claims and their equivalents.

What is claimed is:

1. An input/output buffer comprising:

an output buffer configurably driving a pad line; and

an input buffer connected to said pad line and to an input signal line, said input buffer having a plurality of input paths from said pad line to said input signal line, wherein:

said input buffer comprises means for selecting one of said plurality of input paths;

said output buffer comprises a plurality of pullups disposed in parallel between said pad line and a line at a high voltage level, and a plurality of pulldowns disposed in parallel between said pad line and a line at a low voltage level; and

said output buffer further comprises means for selectively enabling and disabling said plurality of pullups and said plurality of pulldowns.

2. The input/output buffer of claim **1** wherein said means for selecting one of said plurality of input paths comprises a multiplexer controlled by one or more configuration memory cells.

3. The input/output buffer of claim **1** wherein said means for selectively enabling and disabling said plurality of pullups and said plurality of pulldowns comprises configuration logic controlled by one or more configuration memory cells.

4. The input/output buffer of claim **1** wherein one of said plurality of input paths comprises a differential amplifier.

5. The input/output buffer of claim **4** wherein said differential amplifier comprises an NMOS differential amplifier.

6. The input/output buffer of claim **4** wherein said differential amplifier comprises a PMOS differential amplifier.

7. An input/output buffer comprising:

an input buffer driven by a pad line;

an output buffer driving said pad line, said output buffer comprising a plurality of configurable pullups disposed in parallel between said pad line and a line at a high voltage level and a plurality of pulldowns disposed in parallel between said pad line and a line at a low voltage level; and

means for configurably connecting one of a plurality of supply voltages to said high voltage level.

8. An input/output buffer in a field programmable gate array, the input/output buffer comprising:

a configurable input buffer having a plurality of input paths, said input buffer being driven by a pad line;

an output buffer configurably driving said pad line; and

configuration memory cells for configuring said input buffer to select one of said plurality of input paths.

9. A configurable input buffer, comprising:

a pad line;

an input signal line;

a plurality of input paths from said pad line to said input signal line, one such input path comprising a differential amplifier; and

means for configurably selecting one of said plurality of input paths.

10. The configurable input buffer of claim **9** wherein said means for selecting one of said plurality of input paths comprises a multiplexer controlled by one or more configuration memory cells.

11. The configurable input buffer of claim **9** wherein said means for selecting one of said plurality of input paths comprises a plurality of transistors controlled by one or more configuration memory cells.

12. The configurable input buffer of claim **9** wherein said differential amplifier comprises an NMOS differential amplifier.

13. The configurable input buffer of claim **9** wherein said differential amplifier comprises a PMOS differential amplifier.

14. A configurable output buffer, comprising:

a pad line driver by said output buffer;

a plurality of pullups disposed in parallel between said pad line and a line at a high voltage level for pulling said pad line to said high voltage level;

a plurality of pulldowns disposed in parallel between said pad line and a line at a low voltage level for pulling said pad line to said low voltage level;

means for enabling and disabling selected ones of said plurality of pullups; and

means for enabling and disabling selected ones of said plurality of pulldowns.

15. The configurable output buffer of claim **14** wherein said means for enabling and disabling selected ones of said plurality of pullups and said means for enabling and disabling selected ones of said plurality of pulldowns each comprise configuration logic controlled by one or more configuration memory cells.

16. A field programmable gate array input/output block compatible with a plurality of supply voltage levels, comprising:

a pad;

an input signal line;

an input buffer having a plurality of input paths, said input buffer supplying an input voltage to said input signal line in response to a voltage on said pad, said input buffer being configurable to select one of said plurality of input paths based on data stored in one or more configuration memory cells; and

on at least one such path, level selecting means responsive to an input reference voltage supplied from outside said IC for setting a trip point between high and low voltage levels for relating said input voltage to said voltage on said pad.

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STANDARD

Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits

MARCH 1996

TIA/EIA-644

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(From Standards Proposal No. 3357, formulated under the cognizance of the TR-30.2 Subcommittee on DTE-DCE Interfaces.)

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ELECTRICAL CHARACTERISTICS OF LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) INTERFACE CIRCUITS

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LIST OF FIGURES

LIST OF TABLES

FOREWORD

(This foreword is not part of this Standard)

This Standard was formulated under the cognizance of TIA Subcommittee TR-30.2 on Data Transmission Interfaces.

This Standard specifies low voltage differential signaling (LVDS) generators and receivers capable of operating at data signaling rates up to 655 Mbit/s, devices may be designed for data signaling rates less than 655 Mbit/s, 100 Mbit/s for example, when economically required for that application.

This Standard was developed in response to a demand from the data communications community for a general purpose high speed interface standard for use in high throughput DTE-DCE interfaces.

The voltage levels specified in this Standard were specified such that maximum flexibility would be provided, while providing a low power, high speed, differential interface. Generator output characteristics are independent of power supply, and may be designed for standard +5 V, +3.3 V or even power supplies as low as +2.5 V. Integrated circuit technology may be BiCMOS, CMOS, or GaAs technology. The low voltage (330 mV) swing limits power dissipation, while also reducing radiation of EMI signals. Differential signaling provides multiple benefits over single-ended signaling, notably common mode rejection, and magnetic canceling.

The dc electrical levels are [redacted] o electrical levels described in the IEEE 1596.3 standard, and will inter-oper ata signaling rates.

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This Standard includes two annexes, both are informative only. Annex A provides guidelines for application, addressing data signaling rate and cable length issues. Annex B provides comparison information with other interface standards, and references to this Standard.

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1 SCOPE

This Standard specifies the electrical characteristics of low voltage differential signaling interface circuits, normally implemented in integrated circuit technology, that may be employed when specified for the interchange of binary signals between:

Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE),

Data Terminal Equipment (DTE) and Data Terminal Equipment (DTE),

or in any point-to-point interconnection of binary signals between equipment.

The interface circuit includes a generator connected by a balanced interconnecting media to a load consisting of a termination impedance and a receiver(s). The interface configuration is an uncomplicated point-to-point interface. The electrical characteristics of the circuit are specified in terms of required voltage, and current values obtained from direct measurements of the generator and receiver (load) components at the interface points.

The logic function of the generator and the receiver is not defined by this Standard, as it is application dependent. The generators and receivers may be inverting, non-inverting, or may include other digital blocks such as parallel-to-serial or serial-to-parallel converters to boost the data signaling rate on the interchange circuit as required by the application.

Minimum performance requirements for the balanced interconnecting media are furnished. Guidance is given in annex A, A.2 with respect to limitations on data signaling rate imposed by the parameters of the cable length, attenuation, and crosstalk for individual installations for a typical cable media interface.

It is intended that this Standard will be referenced by other standards that specify the complete interface (i.e., connector, pin assignments, function) for applications where the electrical characteristics of a low voltage differential signaling interface circuit is required. This Standard does not specify other characteristics of the DTE-DCE interface (such as signal quality, protocol, bus structure, and/or timing) essential for proper operation across the interface.

When this Standard is referenced by other standards or specifications, it should be noted that certain options are available. The preparer of those standards and specifications must determine and specify those optional features that are required for that application.

2 NORMATIVE REFERENCES

The following Standard contains provisions which, through reference in this text, constitute provisions of this Standard. At the time of publication, the edition indicated was valid. All standards are subject to revision, and parties to agreements based on this Standard are encouraged to investigate the possibility of applying the most recent edition of the standard indicated below. ANSI and TIA maintain registers of currently valid national standards published by them.

ANSI/TIA/EIA-422-B-1994 *Electrical Characteristics of Balanced Voltage Digital Interface Circuits*

EIA-485 *Standard for Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems*

ANSI/TIA/EIA-612-1993 *Electrical Characteristics for an Interface at Data Signaling Rates up to 52 Mbit/s*

3 DEFINITIONS, SYMBOLS AND ABBREVIATIONS

For the purposes of this Standard, the following definitions, symbols and abbreviations apply:

3.1 Data signaling rate

Data signaling rate, expressed in the units bit/s (bits per second), is the significant parameter. It may be different from the equipment's data transfer rate, which employs the same units. Data signaling rate is defined as 1/tui where tui is the minimum interval between two significant instants.

3.2 DTE

Data Terminal Equipment

3.3 DCE

Data Circuit-Terminating Equipment

3.4 LVDS

Low Voltage Differential Signaling

3.5 Star (*)

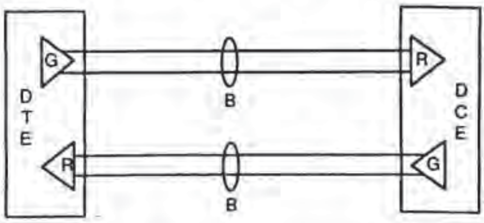
Star (*) - represents the opposite input condition for a parameter. For example, the symbol Q represents the receiver output state for one input condition, while Q* represents the output state for the opposite input state.

4 APPLICABILITY

4.1 General applicability

The provisions of this Standard may be applied to the circuits employed at the interface between equipments where information being conveyed is in the form of binary signals.

Typical points of applicability for this Standard are depicted in figure 1.



Legend:
DTE = Data Terminal Equipment
DCE = Data Circuit-termination Equipment
G = Generator
R = Receiver
B = Balanced interconnecting media

Figure 1 - Application of LVDS interface circuits

The LVDS interface is intended for use where any of the following conditions prevail:

a. The data signaling rate is too great for effective unbalanced (single-ended) operation.

b. The data signaling rate exceeds the capability of TIA/EIA-422-B, EIA-485, or TIA/EIA-612 balanced (differential) electrical interfaces.

c. The balanced interconnecting media is exposed to extraneous noise sources that may cause an unwanted voltage up to ±1 V measured differentially between the signal conductor and circuit common at the load end of the cable with a 50 Ω resistor substituted for the generator.

d. It is necessary to minimize electromagnetic emissions and interference with other signals.

e. Inversion of the signals may be required; e.g., plus MARK to minus MARK may be obtained by inverting the balanced interconnecting media.

4.2 Data signaling rate

The LVDS interface circuit will normally be utilized on data and timing, or control circuits where the data signaling rate is up to a recommended maximum limit of 655 Mbit/s. This limit is determined by the generator transition time characteristics, the media characteristics, and the distance between the generator and the load. Certain applications may impose a different (lower or higher) limit for the maximum data signaling rate. This may be accomplished by specifying a different minimum generator transition time specification, a different percentage of transition time vs. unit interval at the load, or by a different assumption of the maximum balanced interconnecting media signal distortion which is length dependent.

The theoretical maximum limit is calculated at 1.923 Gbit/s, and is derived from a calculation of signal transition time at the load assuming a loss-less balanced interconnecting media. The recommended signal transition time (tr or tf) at the load should not exceed 0.5 of the unit interval to preserve signal quality. This Standard specifies that the transition time of the generator into a test load be 260 ps or slower. Therefore, with the fastest generator transition time, and a loss-less balanced interconnecting media, and applying the 0.5 restriction, yields a minimum unit interval of 520 ps or 1.923 Gbit/s theoretical maximum data signaling rate.

NOTES

1 - 655 Mbit/s is the maximum data signaling rate for a serial channel, and employing a parallel bus structure (4, 8, 16, 32, etc. - bus width) can easily extend the obtainable equivalent bit rate into the Gbit/s range.

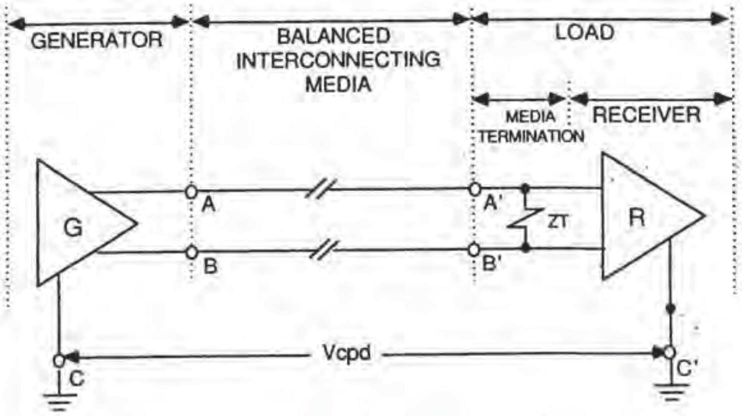
2 - The recommended maximum data signaling rate is derived from a calculation of signal transition time at the load. For example, if a cable media is selected, a maximum signal rise time degradation is assumed to be 500 ps, since cables are not loss-less (500 ps represents a typical amount of rise time distortion on 5 meters of cable media). Therefore, allowing a 500 ps degradation of the signal in the interconnecting cable yields a 760 ps (fastest) signal at the load. Therefore, with the fastest generator transition time, and a cable with only 500 ps of signal degradation (transition time), and applying the 0.5 restriction, yields a minimum unit interval of 1.520 ns or 655 Mbit/s recommended maximum data signaling rate.

Generators and receivers meeting this Standard need **not** operate over the entire data signaling rate range specified. They may be designed to operate over narrower ranges that satisfy more economically specified applications, for example at lower data signaling rates. When a generator is limited to a narrower range of data signaling rates, the transition time of the generator may be slowed accordingly to limit noise generation. For example, at 100 Mbit/s the generator's transition time should be in the range of 500 ps to 3 ns (5% to 30% of the unit interval), and the signal transition time at the load should not exceed 5 ns (50% of the unit interval).

While a restriction of maximum cable length in not specified, recommendations are given on how to determine the maximum data signaling rate for a typical cable media application (see A.2).

5 ELECTRICAL CHARACTERISTICS

The LVDS interface circuit is shown in figure 2. The circuit consists of three parts: the generator (G), the balanced interconnecting media, and the load. The load is composed of a termination impedance and a receiver(s) (R). The receiver may incorporate the termination impedance internal to the Integrated Circuit package. The electrical characteristics of the generator and receiver are specified in terms of direct electrical measurements while the balanced interconnecting media is described in terms of its electrical characteristics.



Legend:

G = Generator

A = Generator interface point

B = Generator interface point

C = Generator circuit common

ZT = Termination impedance

Vcpd = Common potential difference

R = Receiver

A' = Receiver interface point

B' = Receiver interface point

C' = Receiver circuit common

Figure 2 - LVDS interface circuit

5.1 Generator characteristics

The generator electrical characteristics are specified in accordance with the measurements illustrated in figures 4 to 8 and described in 5.1.1 through 5.1.4. The generator circuit meeting these requirements results in a balanced source that will produce a differential voltage across a test termination load of 100 Ω in the range of 250 mV to 450 mV.

The signaling sense of the voltages appearing across the termination resistor is defined in figure 3 as follows:

a. The A terminal of the generator shall be negative with respect to the B terminal for a binary 1 or OFF state.

b. The A terminal of the generator shall be positive with respect to the B terminal for a binary 0 or ON state.

The logic function of the generator and the receiver is beyond the scope of this Standard, and therefore is not defined.

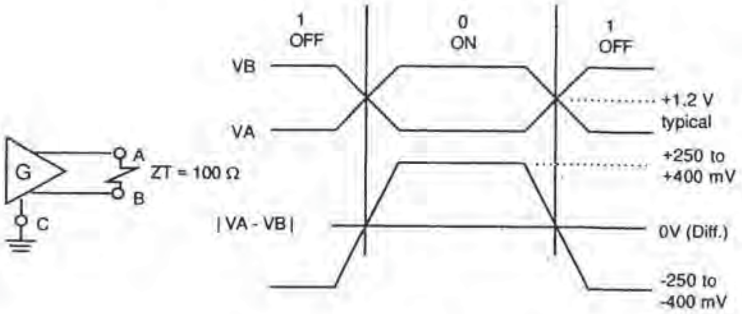


Figure 3 - Signaling sense

5.1.1 Test termination measurements (figure 4)

With a test load of two resistors, 49.9 Ω ±1% each, connected in series between the generator output terminals, the steady-state magnitude of the differential output voltage (Vt), shall be greater than or equal to 247 mV [99.8 Ω -1% (2.5 mA)] and less than or equal to 454 mV [99.8Ω +1% (4.5 mA)]. For the opposite binary state, the polarity of Vt shall be reversed (Vt*). The steady-state magnitude of the difference between Vt and Vt* shall be 50 mV or less.

$$247\text{ mV} \leq | Vt | \leq 454\text{ mV}$$

$$247\text{ mV} \leq | Vt^* | \leq 454\text{ mV}$$

$$| Vt | - | Vt^* | \leq 50\text{ mV}$$

The steady-state magnitude of the generator offset voltage (Vos), measured between the center point of the test load and the generator circuit common shall be greater than or equal to 1.125 V and less than or equal to 1.375 V for either binary state. The steady-state magnitude of the difference of Vos for one binary state and Vos* for the opposite binary state shall be 50 mV or less.

$$1.125\text{ V} \leq Vos \leq 1.375\text{ V}$$

$$1.125\text{ V} \leq Vos^* \leq 1.375\text{ V}$$

$$| Vos | - | Vos^* | \leq 50\text{ mV}$$

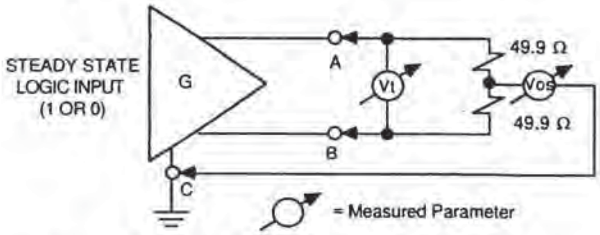


Figure 4 - Test termination measurements

5.1.2 Short-circuit measurements (figures 5, and 6)

With the generator output terminals short-circuited to the generator circuit common, the magnitudes of the currents (Isa and Isb) following through each output terminal shall not exceed 24.0 mA for either binary state (see figure 5).

$$|\,Isa\,| \leq 24.0 \text{ mA}$$
$$|\,Isb\,| \leq 24.0 \text{ mA}$$

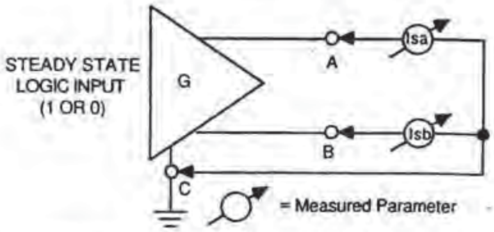


Figure 5 - Short-circuit measurements to circuit common

With the generator output terminals short-circuited to each other, the magnitude of the current (Isab) following through the output terminals shall not exceed 12.0 mA for either binary state (see figure 6).

$$|\,Isab\,| \leq 12.0 \text{ mA}$$

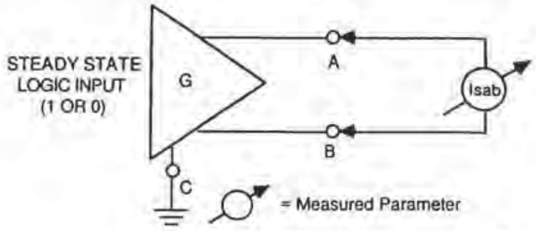


Figure 6 - Short-circuit measurements

5.1.3 Output signal waveform (figure 7)

During transitions of the generator output between alternating binary states (one-zero-one-zero, etc.), the differential voltage measured across the 99.8 Ω ±1% test load (RL) and a maximum lumped capacitance test load of 5 pF (CL) connected as shown in figure 7, shall be such that the voltage monotonically changes between 0.2 and 0.8 of Vss and is less than or equal to 0.3 of the unit interval (at the maximum data signaling rate to be employed up to 200 Mbit/s). Above 200 Mbit/s the transition time shall be greater than or equal to 260 ps and less than or equal to 1.5 ns. Thereafter, the signal voltage shall not vary more than ±20% of the steady-state value (Vring), until the next binary transition occurs. Edge rates less than 260 ps are not recommended to minimize adverse effects of switching noise. Vss is defined as the voltage difference between the two steady-state values of the generator output (Vss = 2|Vt|). Measurement equipment used for compliance testing shall provide a bandwidth of 1 GHz minimum.

For data signaling rates ≤ 200 Mbit/s (tui ≥ 5 ns):

tr ≤ 0.3 tui, tf ≤ 0.3 tui

For data signaling rates ≥ 200 Mbit/s (tui ≤ 5 ns)
and ≤ 655 Mbit/s (tui ≥ 1.526 ns):

260 ps ≤ tr ≤ 1.5 ns, 260 ps ≤ tf ≤ 1.5 ns

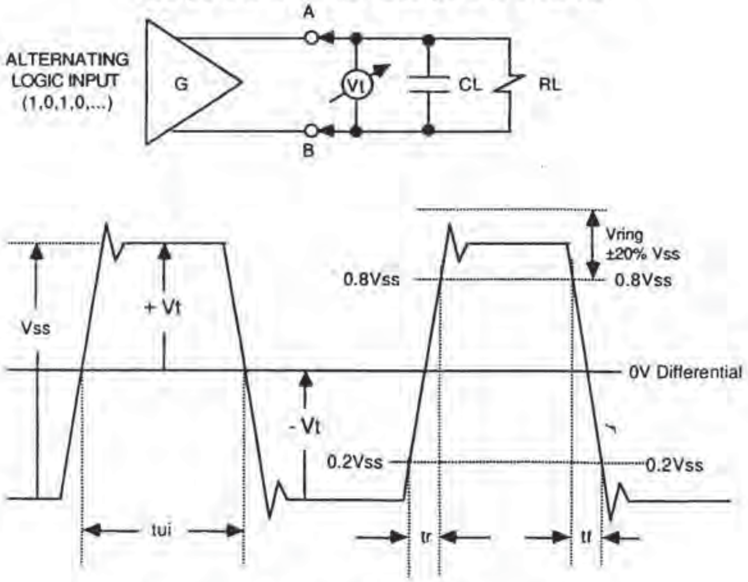


Figure 7 - Output signal waveform

5.1.4 Dynamic output signal balance (figure 8)

During transitions of the generator output between alternating binary states (one-zero-one-zero, etc.), the resulting imbalance of the offset voltage (Vos) measured between the matched 49.9 Ω ±1% test load resistors (RL) to circuit common (C) and with a maximum lumped capacitance test load of 5 pF (CL) connected as shown in figure 8, should not vary more than 150 mVpp (peak-to-peak). Measurement equipment used for compliance testing shall provide a bandwidth of 1 GHz minimum.

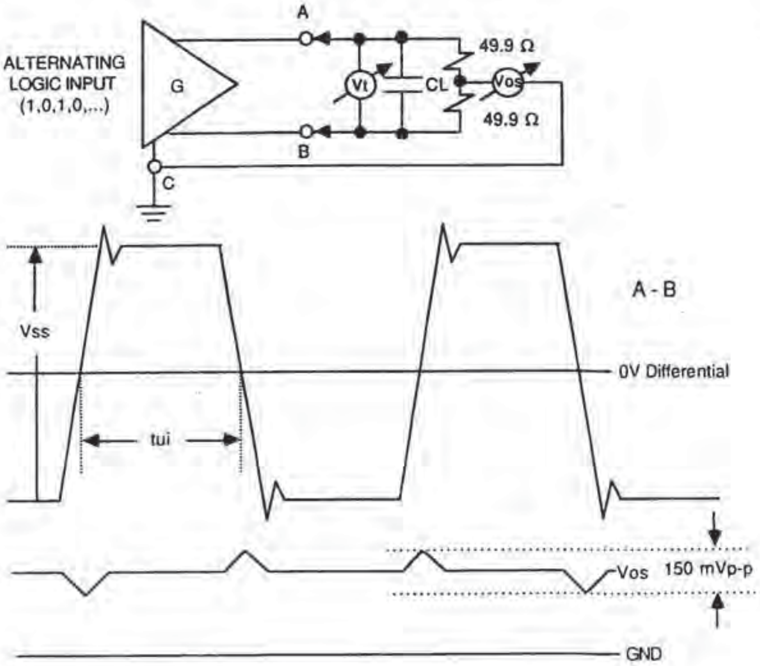


Figure 8 - Dynamic output signal balance waveform

5.2 Load characteristics

The load is defined as an impedance between A' and B' and is composed of a termination impedance and a receiver as shown in figure 2.

The electrical characteristics of a receiver without an internal termination impedance are specified in terms of measurements illustrated in figures 9, 12 and 13, and described in 5.2.1 and 5.2.3. Alternatively, the electrical characteristics of a receiver with an internal termination impedance is specified in terms of measurements illustrated in figures 10 to 13, and described in 5.2.2 through 5.2.3. A circuit meeting these requirements results in a differential receiver having a high input impedance (non-terminating receiver), and a small input threshold between ± 100 mV.

The media termination is specified in terms of measurements described in 5.2.4 and 5.2.2 for receivers that integrate the termination impedance.

The total load limit is specified in 5.4.3, and additional guidance is provided in 5.4.1 and 5.4.2 on multiple receiver operation and failsafe operation respectfully.

5.2.1 Receiver input current-voltage measurements (figure 9)

With the voltage Via (or Vib) ranging from 0 V to +2.4 V while Vib (or Via) is held at +1.2 V ± 50 mV, the resultant input current Iia (or Iib) shall be no greater than 20 μA in magnitude. These measurements apply with the receiver's power supply in both power-on and power-off conditions.

> **NOTE 3 -** Some integrated circuit manufacturers may impose additional restrictions that may be required to meet this specification under the power-off condition.

| Iia | ≤ 20 μA
| Iib | ≤ 20 μA

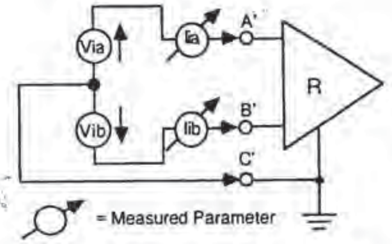


Figure 9 - Receiver input current-voltage measurements

5.2.2 Terminating receiver input current-voltage measurements and input impedance measurements (figures 10 and 11)

With the applied voltage (Vin) and forced current (Iin) listed in table 1 applied to the corresponding inputs, the resultant differential input voltage magnitude (Vid) shall be between the values listed in table 1. The test circuit is shown in figure 10 and applies only to receivers that provide an internal termination impedance. These measurements apply with the receiver's power supply in both power-on and power-off conditions.

> **NOTE 4** - Some integrated circuit manufacturers may impose additional restrictions that may be required to meet this specification under the power-off condition.

$$225 \text{ mV} \le |\text{Vid}| \le 596 \text{ mV}$$

Table 1 - Receiver input current-voltage measurements for terminating receivers

Applied Voltage Vin (V)	Forced Loop Current Iin (mA)	Switch Position S1 - S2	Resulting Input Voltage Vr (V)	Resulting Differential Input Voltage Range - Vid (mV)
2.4	- 2.5	A' - B'	2.070 to 2.175	+225 to +330
2.4	- 4.5	A' - B'	1.806 to 1.995	+405 to +596
2.4	- 2.5	B' - A'	2.070 to 2.175	-225 to -330
2.4	- 4.5	B' - A'	1.806 to 1.995	-405 to -596
0	- 2.5	A' - B'	0.225 to 0.330	-225 to -330
0	- 4.5	A' - B'	0.405 to 0.594	-405 to -596
0	- 2.5	B' - A'	0.225 to 0.330	+225 to +330
0	- 4.5	B' - A'	0.405 to 0.594	+405 to +596

NOTE 5 - Current into a terminal is positive, and current out of a terminal is negative.

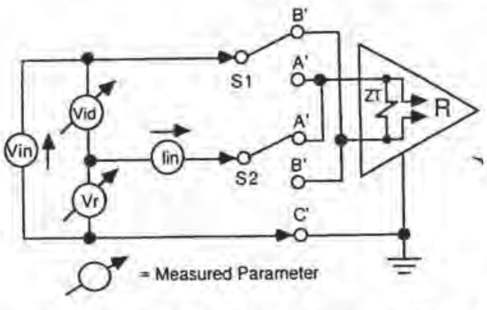


Figure 10 - Terminating receiver input current-voltage measurements

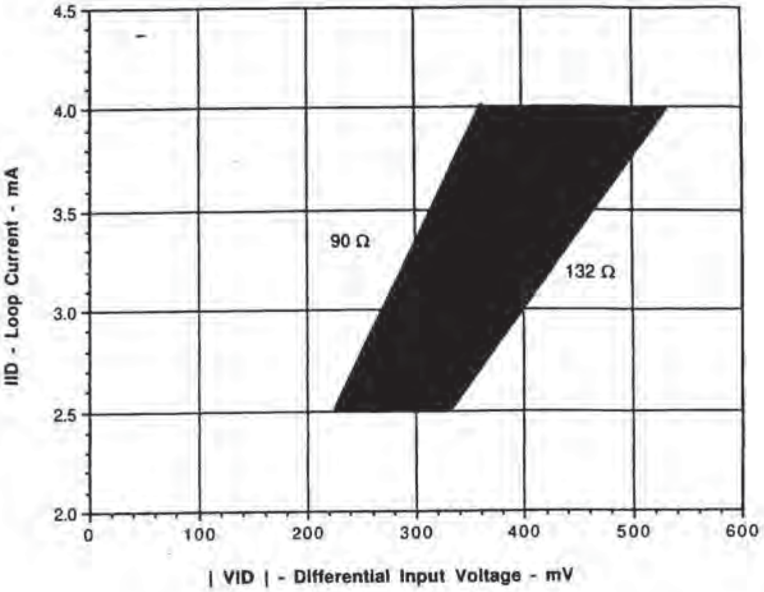


Figure 11 - Terminating receiver input current vs. input voltage range

The input impedance of the terminating receiver is dominated by the low impedance differential termination impedance (ZT). The resulting input impedance calculated from the measurements describe in table 1 shall be greater than or equal to 90 Ω, and less than or equal to 132 Ω. See 5.2.4 on media termination, and 5.4.3 on total load limit.

$$90\ \Omega \le ZT \le 132\ \Omega$$

NOTE 6 - The internal termination impedance may be a simple resistor incorporated into the package, integrated on the die, or composed of active devices on the die. The exact structure of the termination impedance is beyond the scope of this Standard.

5.2.3 Receiver input sensitivity measurements (figure 12)

Over an entire common mode voltage range of +0.050 V to +2.350 V (referenced to receiver circuit common), the receiver shall not require a differential input voltage of more than ±100 mV (threshold) to correctly assume the intended binary state. Reversing the polarity of Vi shall cause the receiver to assume the opposite binary state. The receiver is required to maintain correct operation for differential input voltages ranging between 100 mV and 600 mV in magnitude. The maximum voltage applied to either the A' or B' terminals shall not greater than +2.4 V, or be less than 0 V with respect to receiver circuit common. The maximum differential input voltage applied to the receiver is 2.4 V with no damage occurring to the receiver inputs.

Thresholds ≤ ±100 mV (differential)
100 mV ≤ Valid Differential Input Voltage Range ≤ 600 mV
0 V ≤ Valid Input Voltage (to circuit common) ≤ +2.4 V

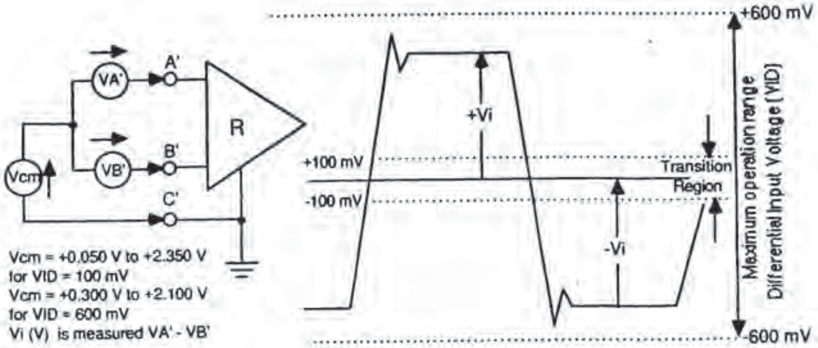


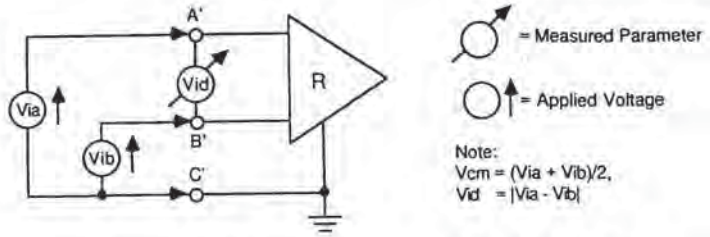
Figure 12 - Receiver input sensitivity measurements

Table 2 lists the minimum and maximum operating voltages of the receiver (input voltage, differential input voltage, and common mode input voltage), and the test circuit is shown in figure 13.

NOTE 7 - The logic function of the receiver is not defined by this Standard.

Table 2 - Receiver minimum and maximum operating voltages

Applied Voltages (Input Voltage - referenced to circuit common - C')		Resulting Differential Input Voltage VID	Resulting Common Mode Input Voltage VCM	Reason of Test
Via	Vib			
+1.250 V	+1.150 V	+100 mV	+1.200 V	To guarantee operation with minimum VID applied versus VCM range
+1.150 V	+1.250 V	-100 mV	+1.200 V	
+2.400 V	+2.300 V	+100 mV	+2.350 V	
+2.300 V	+2.400 V	-100 mV	+2.350 V	
+0.100 V	0 V	+100 mV	+0.050 V	
0 V	+0.100 V	-100 mV	+0.050 V	
+1.500 V	+0.900 V	+600 mV	+1.200 V	To guarantee operation with maximum VID applied versus VCM range
+0.900 V	+1.500 V	-600 mV	+1.200 V	
+2.400 V	+1.800 V	+600 mV	+2.100 V	
+1.800 V	+2.400 V	-600 mV	+2.100 V	
+0.600 V	0 V	+600 mV	+0.300 V	
0 V	+0.600 V	-600 mV	+0.300 V	



Note:
Vcm = (Via + Vib)/2,
Vid = |Via - Vib|

Figure 13 - Receiver input sensitivity test circuit

5.2.4 Media termination (figures 14 and 15)

All applications shall use a termination impedance. The recommended value is between 90 Ω and 132 Ω. The actual value should be selected to match the media characteristic impedance (±10%) at the application frequency. The termination impedance may be integrated onto the receiver integrated circuit, but subject to meeting the requirements of 5.2.2 instead of 5.2.1. If the termination impedance is not integrated into the receiver circuit, then it shall be located at the load end of the balanced interconnecting media, as close to the receiver input as possible to minimize the resulting stub length between the termination impedance and the receiver input.

> **NOTE 8** - Due to the high application frequency, care should be taken in choosing proper components such as the termination resistor, and in layout of the printed circuit board. The use of surface mount components is highly recommended to minimize parasitic inductance, and lead length of the termination resistor. Wire wound resistors are not recommended.

The value of this external impedance (ZT) is in the range of 90 Ω to 132 Ω. Ideally, the resistor value is equal to the characteristic impedance of the media or greater in value to minimize negative signal reflections. The media termination is shown in figures 14 and 15.

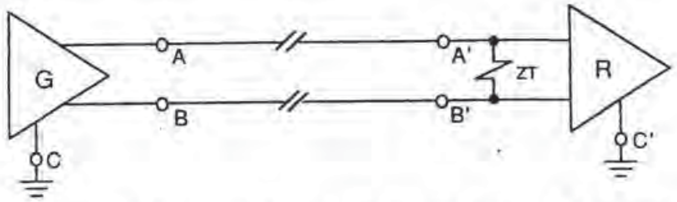


Figure 14 - Point-to-point application with external termination

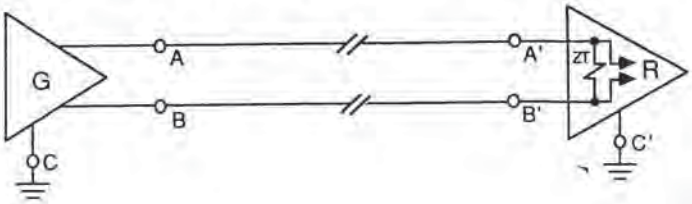


Figure 15 - Point-to-point application with internal termination

> **NOTE 9** - Matching of impedance of the PCB traces, connectors and balanced interconnect media is highly recommended. Impedance variations along the entire interconnect path should be minimized since they degrade the signal path and may cause reflections of the signal.

5.3 Interconnecting media electrical characteristics

The balanced interconnecting media shall consist of paired metallic conductors in any configuration which will maintain balanced signal transmission.

> **NOTE 10 -** The actual media of the cable is not specified and may be: twisted pair cable, twinax cable (parallel pair), flat ribbon cable, or PCB traces.

The performance of any balanced interconnecting media used shall be such to maintain the necessary signal quality for the specific application. If necessary for system consideration, shielding may be employed (see 8.2).

Annex A to this Standard provides guidance on performance and cable length versus data signaling rate and cable recommendations for typical cable applications.

5.3.1 Cable media

The cable media shall conform to the following electrical requirements:

5.3.1.1 Maximum dc loop resistance (DCR):

50 Ω is the maximum dc loop resistance of the cable. This corresponds to a voltage drop of 125 mV assuming minimum generator current of 2.5 mA.

5.3.1.2 Characteristic impedance:

110 Ω +/- 20% from 10 MHz to the application upper frequency limit.

5.3.1.3 Additional parameters

Additional parameters not specified which are application dependent (see Annex A) are: Maximum Attenuation, Maximum Propagation Delay, Maximum Propagation Delay Skew, Maximum Near End Crosstalk (NEXT), and Maximum Far End Crosstalk (FEXT). Crosstalk, skew, and related pair balance parameters may impact applications with multiple signal transmission lines.

5.3.2 PC Board trace media

The electrical requirements of PC Board traces shall also meet the requirements of 5.3.1.1 to 5.3.1.3.

5.3.3 Other media

It may be possible that other media may be employed, the definition and electrical characteristics of such media is beyond the scope of this Standard.

5.4 System parameters

5.4.1 Multiple receiver operation (figures 16 and 17)

The generator has the capability to furnish the dc signal necessary to drive multiple parallel connected receivers (without internal termination). However, the physical arrangement of the multiple receivers involves consideration of stub line lengths, location of the termination resistor, number of receivers, data signaling rate, circuit common, etc., that may degrade dynamic characteristics of the signal at the receivers if not properly implemented. It is recommended that stub lengths off the main line be as short as possible. In general, the propagation delay of the stub, should not exceed 15% of the signal transition time to prevent reflections and a severe impedance discontinuity. For applications with receivers without internal termination, the external termination resistor must be located at the far end (last receiver) of the interconnect. The actual arrangement must involve consideration of the aforementioned characteristics for the specific application and is therefore beyond the scope of this Standard. Figures 16 and 17 are provided for guidance only.

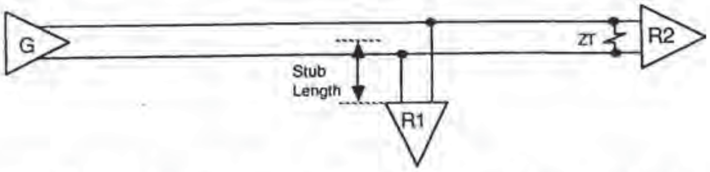


Figure 16 - Multiple receiver operation - multidrop application

NOTE 11 - If the configuration illustrated in figure 16 is employed, only the receiver at the far end of the cable may be a terminating receiver.

All receivers located between the generator and the final receiver must be non-terminating receiver(s). Multiple terminating receivers would present a low impedance load to the generator which would violate the total load limit (see 5.4.3), and adversely attenuate the signal.

The configuration shown in figure 17 is preferred over the multidrop configuration shown in figure 16. The configuration shown in figure 17 is composed of two independent uncomplicated point-to-point applications. At the expense of the second balanced interconnecting media, and termination impedance, the problem of stub lengths is eliminated, along with any impedance discontinuities that mid balanced interconnecting media connectors, and stubs may present. Signal quality is superior in an uncomplicated point-to-point configuration over a multidrop configuration.

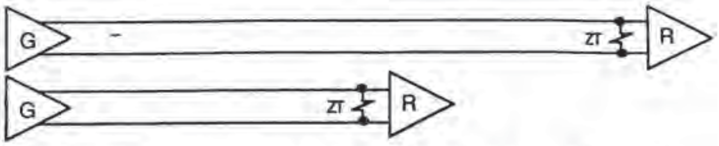


Figure 17 - Uncomplicated point-to-point application

5.4.2 Failsafe operation

Other standards and specifications using the electrical characteristics of the LVDS interface circuit may require that specific interchange circuits be made failsafe to certain fault conditions. Such fault conditions may include one or more of the following:

1) generator in power-off condition
2) receiver not connected with the generator
3) open-circuited interconnecting cable
4) short-circuited interconnecting cable
5) input signal to the load remaining within the transition region (±100 mV) for an abnormal period of time (application dependent)

When detection of one or more of the above fault conditions is required by specified applications, additional provisions are required in the load and the following items must be determined and specified:

1) which interchange circuits require fault detection
2) what faults must be detected
3) what action must be taken when a fault is detected; the binary state that the receiver assumes
4) what is done does not violate this Standard

The method of detection of fault conditions is application dependent and is therefore not further specified as it is beyond the scope of this Standard.

5.4.3 Total load limit

The total load (ZL) including multiple receivers, failsafe provisions, and media termination shall have a total impedance greater than or equal to 90 Ω and less or equal to 132 Ω between its input points A' and B', shown in figure 2. The receiver(s) shall not require a differential input voltage of more than 100 mV in magnitude for all receiver(s) to assume the intended binary state.

$$\mathbf{90\ \Omega \le ZL \le 132\ \Omega}$$

6 ENVIRONMENTAL CONSTRAINTS

A LVDS interface circuit conforming to this Standard will perform satisfactorily at data signaling rates up to 655 Mbit/s providing that the following operational constraints are simultaneously satisfied:

a. For cable applications, the cable media meets the recommended cable characteristics, the cable length is within that recommended for the applicable data signaling rate indicated in annex A, A.2 and the cable is properly terminated.

b. For PC Board traces, the traces meets the recommended characteristics for the applicable data signaling rate, and the trace is properly terminated.

c. The input voltage at the receiver (with respect to receiver circuit common) is between 0 V and +2.4 V and either input (A' or B') terminal. The input voltage is defined to be any uncompensated combination of generator-receiver common potential difference, the generator offset voltage (Vos), and longitudinally coupled peak noise voltage.

d. Maximum common potential difference between the receiver circuit common and the generator circuit common is less than ±1 V.

7 CIRCUIT PROTECTION

The LVDS interface generator and receiver devices, under either the power-on or power-off condition, complying to this Standard shall not be damaged under the following conditions:

a. Generator open circuit.

b. Short-circuit across the balanced interconnecting media.

c. Short-circuit to common.

NOTE 12 - Some integrated circuit manufacturers may impose additional restrictions that may be required to meet this specification under the power-off condition.

8 OPTIONAL GROUNDING ARRANGEMENTS

8.1 Signal common (ground)

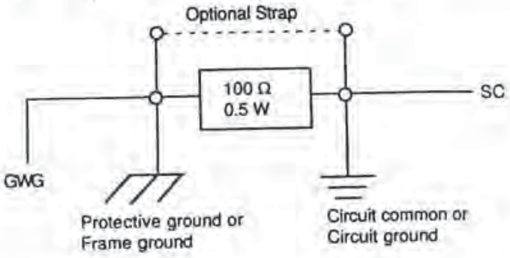
Proper operation of the LVDS interface circuits requires the presence of a signal common path between the circuit commons of the equipment at each end of the interconnection. The signal common interchange lead shall be connected to the circuit common which shall be connected to protective ground by any one of the following methods, shown in figures 18 and 19, as required by specific application.

The same configuration need not be used at both ends of an interconnection; however, care should be exercised to prevent establishment of ground loops carrying high currents.

8.1.1 Configuration "A" (figure 18)

The circuit common of the equipment is connected to protective ground, at one point only, by a 100 Ω ±20%, resistor with a power dissipation rating of 0.5 W. An additional provision may be made for the resistor to be bypassed with a strap to connect circuit common and protective ground directly together when specific installation conditions necessitate.

> **NOTE 13 -** Under certain ground fault conditions in configuration "A", high ground currents may cause the resistor to fail; therefore, a provision shall be made for inspection and replacement of the resistor.

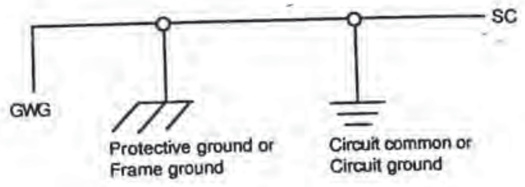


Legend:
GWG = Green wire ground of power system
SC = Signal common interchange circuit

Figure 18 - Optional grounding arrangements - configuration "A"

8.1.2 Configuration "B" (figure 19)

The circuit common shall be connected directly to protective ground.



Legend:
GWG = Green wire ground of power system
SC = Signal common interchange circuit

Figure 19 - Optional grounding arrangements - configuration "B"

8.2 Shield ground - cable applications

Some interface applications may require the use of shielded balanced interconnecting media for EMI or other purposes. When employed, the shield shall be connected only to frame ground at either or both ends depending on the specific application. The means of connection of the shield and any associated connector are beyond the scope of this Standard.

ANNEX A (informative)

GUIDELINES FOR CABLE APPLICATION

(This annex is not a formal part of the attached TIA/EIA Recommended Standard, but is included for information purposes only.)

A.1 Interconnecting cable

The following section provides further information to Section 5.3 and is additional guidance concerning operational constraints imposed by the cable media parameters of length and termination.

Generally, if more than one signal transmission line is required for an interface, twisted pairs are necessary to balance coupling reactance between individual conductors of adjacent pairs and thus reduce crosstalk.

A.1.1 Length

The length of the cable separating the generator and the load is based on a maximum loop resistance of 50 Ω, and a corresponding 125 mV loss of the signal.

The following examples given take only the dc effects into account in determining the maximum cable length. This would pertain to low speed operation only. The ac effects will limit the maximum cable length before the dc resistance for high speed applications. See A.2.

For the following cables gauges, the corresponding maximum length for a 50 mV signal loss is:

28 AWG	50 meters	(164 feet),
24 AWG	150 meters	(492 feet)

Longer lengths are possible, if the voltage attenuation is allowed to decrease the minimum generator differential output voltage to the maximum receiver threshold voltage (250 mV to 100 mV) for a 150 mV voltage attenuation or -7.9 dB. For the following cables gauges, the corresponding maximum length at a 150 mV signal loss is:

28 AWG	150 meters	(492 feet),
24 AWG	450 meters	(1,476 feet)

A.1.2 Typical cable characteristics

A.1.2.1 Parallel interface cable

The following characteristics apply to common parallel interface cable (as used for TIA/EIA-613, and other I/O interface standards) consisting of 25 twisted pairs surrounded by an overall shield:

A.1.2.1.1 Parallel cable, physical characteristics

Conductor	28 AWG, 7 strands of 36 AWG, tinned annealed copper, nominal diameter 0.38 mm (0.015 inch)
Insulation	Polyethylene or polypropylene; 0.24 mm (0.010 inch) nominal wall thickness; 0.86 mm (0.034 inch) outside diameter
Foil Shield	0.051 mm (0.002 inch) nominal thickness aluminum/polyester laminated tape helically wrapped around the core
Braid Shield	braided 36 AWG, tinned copper with 80% minimum coverage, in electrical contact with the aluminum surface of the foil shield
Diameter	nominal overall cable diameter 9.5 mm (0.375 inch)

A.1.2.1.2 Parallel cable, electrical characteristics

DC Resistance	221 Ω / km (67.5 Ω/1000 feet)
Mutual Capacitance	43 pF/m (13 pF/ft) at 1 kHz
Impedance	(characteristic, differential mode) 110 Ω nominal at 50 MHz
Propagation Delay	4.8 ns/m (1.46 ns/ft)
Attenuation	0.28 dB/m (0.085 dB/ft) at 50 MHz
Skew	(propagation delay) 0.115 ns/m (0.035 ns/ft)
Maximum Crosstalk	(Near End, NEXT) 30 dB at 50 MHz

A.1.2.2 Serial interface cable

The following characteristics apply to a common Category 5 serial interface cable (as used for TIA/EIA-422-B, and other I/O interface standards) consisting of 4 unshielded twisted pairs surrounded by an overall jacket:

A.1.2.2.1 Serial cable, physical characteristics

Conductor	24 AWG, 7 strands of 32 AWG, tinned annealed copper, nominal diameter 0.61 mm (0.024 inch)
Insulation	Polyethylene or polypropylene; 0.18 mm (0.007 inch) nominal wall thickness; 0.97 mm (0.038 inch) outside diameter
Foil Shield	optional
Braid Shield	optional
Diameter	nominal overall cable diameter 5.6 mm (0.22 inch)

A.1.2.2.2 Serial cable, electrical characteristics

DC Resistance	84.2 Ω / km (25.7 Ω/1000 feet)
Mutual Capacitance	48 pF/m (14.5 pF/ft) at 1 kHz
Impedance	(characteristic, differential mode) 100 Ω nominal at 50 MHz
Propagation Delay	4.8 ns/m (1.46 ns/ft)
Attenuation	0.17 dB/m (0.051 dB/ft) at 50 MHz
Maximum Crosstalk	(Near End, NEXT) 36.8 dB at 50 MHz

A.1.3 Cable termination

The characteristic impedance of twisted pair cable is a function of frequency, wire size and type as well as the kind of insulating materials employed. For example, the characteristic impedance of average 28 AWG, copper conductor, plastic insulated twisted pair cable, to a 50 MHz sine wave will be on the order of 110 Ω.

The range of 90 Ω to 132 Ω allows for a range of media characteristic impedance to be specified. The nominal media characteristic impedance is restricted to the range of 100 Ω to 120 Ω to allow for impedance variations within the media. Depending upon the balanced interconnecting media specified, the termination impedance should be within 10% of the nominal media characteristic impedance.

A.2 Cable length vs. data signaling rate guidelines

The maximum permissible length of cable separating the generator and the load is a function of data signaling rate and is influenced by the tolerable signal distortion, the amount of longitudinally coupled noise and common potential differences introduced between the generator and the load circuit commons as well as by cable balance. Increasing the physical separation and the interconnecting cable length between the generator and the load interface points increases exposure to common mode noise, signal distortion, and the effects of cable imbalance. Accordingly, users are advised to restrict cable length to a minimum, consistent with the generator to load physical separation requirements.

To determine the maximum data signaling rate for a particular cable length the following calculations / testing is recommended. First, the maximum DCR of the cable length (loop resistance) should be calculated, then the resulting signal attenuation should be calculated at the load. The voltage at the load must be greater than the receiver thresholds of 100 mV. For a conservative design, a maximum attenuation of 50 mV is recommended. Next eye patterns are recommended to determine the amount of jitter at the load at the application data signaling rate and comparing that to system requirements. Typically maximum allowable jitters tolerances range from 5% to 20% depending upon actual system requirements. This testing should be done in the actual application if possible, or in a test system that models the actual application as close as possible. Parameters that should be taken in account include: balanced interconnect media characteristics, termination, protocol and coding scheme, and worst case data patterns (pseudo random for example). The generator / receiver manufacturers and also the media manufacturers should provide additional guidance in predicting data signaling rate versus cable length curves for a particular generator / receiver and a particular media as this relationship is very dependent upon the actual characteristics of the selected devices and media.

When generators are supplying symmetrical signals to clock leads, the period of the clock, rather than the unit interval of the clock waveform, shall be used to determine the maximum cable lengths (e.g., though the clock rate is twice the data rate, the same maximum cable length limits apply).

A.3 Co-directional and contra-directional timing information

With co-directional (same direction as data) timing, there are minimal problems with proper clocking of the data bits since the difference between data and clock edges is mostly the result of generator and receiver skew and not the transmission line.

With contra-directional timing, the user is advised that generator and receiver skew are not the only items to be taken into account. The cable delay and skew must also be considered.

In both cases the clock should transition as close to the center of the data bit as possible.

ANNEX B (informative)

B.1 Compatibility with other interface standards

The LVDS interface circuit is not intended for direct inter-operation with other interface electrical characteristics such as TIA/EIA-422-B, EIA-485, TIA/EIA-612, ITU-T (Formerly CCITT) Recommendation V.11, emitter coupled logic (ECL) or PECL.

Under certain conditions, inter-operation with circuits of some of the above interfaces may be possible but may require modification in the interface or within the equipment, or may require limitations on certain parameters (such as common mode range); therefore, satisfactory operation is not assured, and additional provisions not specified herein may be required.

B.1.1 Generator output levels (figure B.1)

A generator complying to this Standard features a differential current source capable of delivering a loop current in the range of 2.5 mA to 4.5 mA. When loaded with a 100 Ω load, the resulting differential voltage across the resistor will be at least 250 mV and less than 450 mV (Vt). The center point is typically +1.2 V (Vos). These voltages are depicted in figure B.1.

Any balanced receiver device that guarantees and input range of at least 0V to +2.4V, and thresholds of 200 mV or less may directly inter-operate with the generator specified by this Standard and total noise is less than 50 mV.

The balanced receiver specified by this Standard may inter-operate with other balanced generators specified by other standards along as the balanced generator does not violate the maximum receiver input voltage range, and develops a differential voltage of at least 100 mV, and not greater than 600 mV. Inter-operation with generators that provide a greater differential voltage may also be possible with the use of an attenuating circuit. The actual arrangement of such circuits is beyond the scope of this annex.

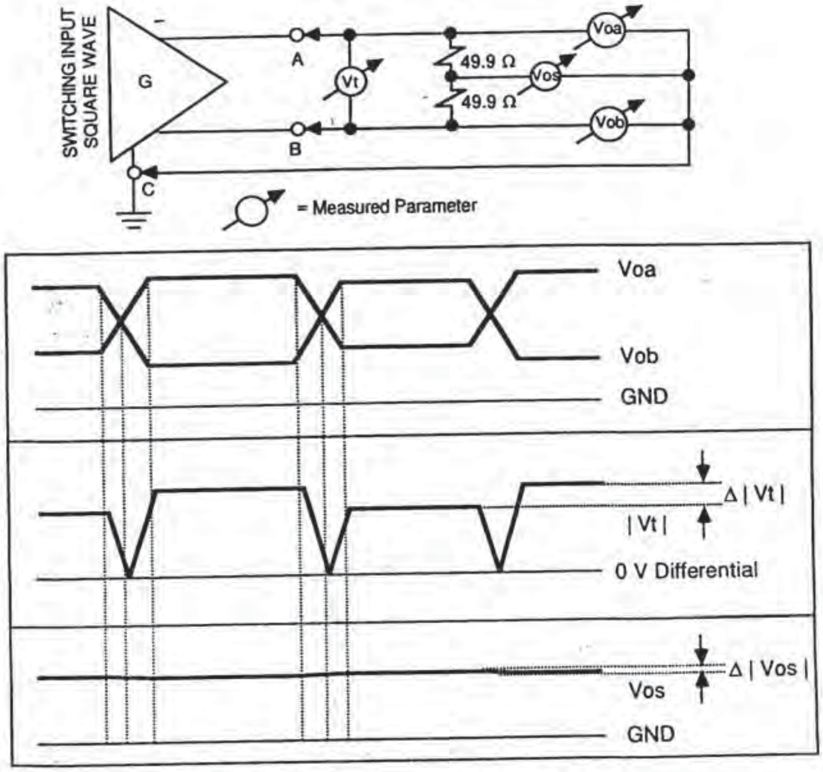


Figure B.1 - Generator output levels

B.1.2 Compatibility with IEEE 1596.3

This Standard features very similar DC electrical specifications to the IEEE 1596.3 standard titled: SCI-LVDS Low Voltage Differential Signals Specifications and Packet Encoding. Direct inter-operation should be possible at certain data signaling rates without the use of intermediate circuitry. This Standard specifies generic electrical characteristics of low voltage differential signaling interface circuits for general purpose applications.

B.1.3 Compatibility with other interface standards

To determine whether direct inter-operation is possible with other interface standards, generator output levels and the receiver input specifications must be compared. Specifically the generator's differential output voltage, and offset voltage must be within the bounds of the receiver's input ranges. Correspondingly, the receiver's input thresholds and the input voltage range must be able to accept the generator's output levels. If this is the case, direct inter-operation is possible. If differences exists, additional provisions and or precautions may be required. This may include modification or additional circuitry inserted at the interface points or imposing limitations on certain parameters such as maximum common potential difference. The exact circuitry required is beyond the scope of this annex.

B.2 Power dissipation of generators

Power dissipation is greatly reduced within the generator circuits compared to other differential standards which specify a voltage mode generator. The current mode generator can produce less spike current during transitions compared to a voltage mode generator. As data signaling rate increases, this component becomes more critical. This allows for the generator to operate into the 300 MHz region without the use of special integrated circuit packages or heat sinks. The load signal is specified between 250 mV and 450 mV typically with a 100 Ω load, with creates a small loop current of only 2.5 to 4.5 mA compared to the minimum 20 mA loop current for a differential TIA/EIA-422-B generator. Since the load current component in also reduced, this allows for highly integrated generator / receiver devices to be offered in one package or integrated with other VLSI controller integrated circuits.

B.3 Related TIA/EIA standards

TIA/EIA-422-B *Electrical Characteristics of Balanced Voltage Digital Interface Circuits*

EIA-485 *Standard for Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multipoint Systems*

TIA/EIA-612 *Electrical Characteristics for an Interface at Data Signaling Rates up to 52 Mbit/s*

B.4 Other related interface standards

IEEE 1596.3 *SCI-LVDS Low Voltage Differential Signals Specifications and Packet Encoding*

ITU-T (formerly CCITT) Recommendation V.11 *Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications*

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XILINX®

Multi-Drop LVDS with Virtex-E FPGAs

XAPP231 (Version 1.0) September 23, 1999

Application Note: Jon Brunetti & Brian Von Herzen

Summary

This application note describes how to use LVDS signaling for high-performance multi-drop applications with Virtex-E FPGAs. Multi-drop LVDS allows many receivers to be driven by one Virtex-E LVDS driver. Simulation results indicate that the reference design described here will operate from DC up to 311 Mbits/s. This application note includes DC specifications, microstrip and layout guidelines. With simple source and differential termination, Virtex-E FPGAs drive multi-drop LVDS directly, replacing costly TTL-LVDS drivers and receivers, reducing board area and skew for high-performance applications. The Virtex-E driver actually improves signal integrity over other LVDS drivers by absorbing any reflected energy at the source instead of passing it on down the line. This innovation enables 311 Mb/s signaling on multi-drop lines with as many as 20 LVDS receivers, spanning distances of over four feet in the reference design, with high signal integrity and noise immunity.

Introduction

LVDS uses differential signaling to increase noise immunity over single-ended techniques. Multi-drop LVDS allows many receivers to be driven by one Virtex-E LVDS driver. The true differential LVDS input and output capability of the Virtex-E FPGA enables this multi-drop application. Virtex-E multi-drop LVDS drivers can drive lines with fanouts of 20 to 1, making Virtex-E LVDS suitable for a broad variety of high-load applications. The Virtex-E LVDS driver eliminates costly TTL-LVDS translators, enabling the direct interface of logic to high-speed differential signaling. This integration reduces signal skew and reduces the board area needed to implement a high-performance application.

Multi-Drop LVDS Circuits

Figure 1 shows a typical multi-drop LVDS application. The Q and $\overline{Q}$ outputs of the LVDS driver on the left connect serially to the inputs of the LVDS receivers along the length of the multi-drop lines. A resistor R_T terminates the Q and $\overline{Q}$ signals in parallel at the end of the multi-drop lines. Simple microstrip lines made on standard PC boards with ground planes suffice for this application.

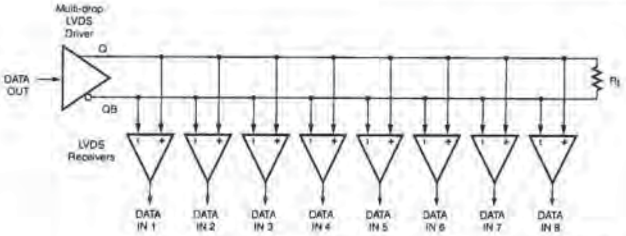

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Figure 1: Typical Multi-Drop LVDS Application

Microstrip Transmission Lines for Multi-Drop LVDS

Microstrip is a PCB (printed-circuit board) trace on the top or bottom layer of the PCB over a ground or power plane on the next inner layer. Figure 2 shows the cross-section of a microstrip transmission line. The trace width (w), trace height above ground plane (h), trace thickness (t), and the relative dielectric constant (ε_r) of the PCB determines the microstrip characteristic impedance (Z_0). Table 1 summarizes the characteristic impedance of the microstrip in Figure 2 for typical values of w and h on an FR4 PCB using 1 ounce copper.

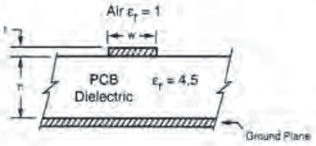

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Figure 2: Microstrip Transmission Line Cross-Section

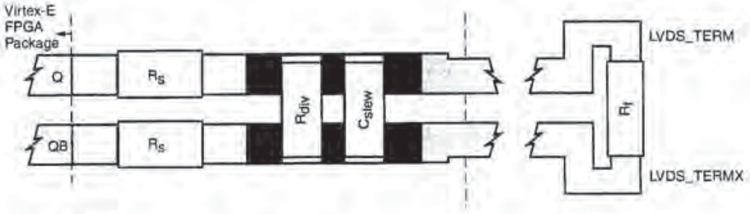
Table 1: Microstrip Impedance for Typical Values of w and h.

Trace Width (w) Mils	Height Above Plane (h) Mils	Impedance (Z_0) Ohms
4	5	70
6	5	59
8	5	51
16	10	52
16	5	34
20	5	29
40	10	30
40	5	17

Notes:
t = 1.4 mils (1 ounce copper)
ϵ_r = 4.5 (typical FR4 at high frequencies)
1000 mils = 1 inch = 25.4 mm
Impedence error = ± 2%

Trace widths and heights above the plane are rounded to the nearest mil for ease of layout and fabrication. Note the microstrip transmission line impedance is approximately constant with the w/h ratio. A w/h ratio of four, gives approximately Z_0 = 29 to 30 ohms. A w/h ratio of 1.6, gives approximately Z_0 = 51 to 52 ohms. Using the w/h ratio approximation, the characteristic impedance of a microstrip with any plane spacing can be estimated.

Figure 3 is a sample layout of the Virtex-E multi-drop LVDS driver with source resistors and capacitor on the left, and the termination resistor on the right.



Notes:
1. All PCB traces shown are 29Ω microstrip.
2. Can use higher impedance in series with R_S and R_{div}

Figure 3: Physical Layout of Virtex-E Multi-Drop LVDS Driver

Multi-Drop LVDS DC Specifications

LVDS outputs typically drive a ± 350 mV voltage swing ($Q - \overline{Q}$), and the average of Q and $\overline{Q}$, $(Q + \overline{Q})/2$, is sometimes referred to as the offset voltage or common-mode voltage. Typical LVDS output common-mode voltage is 1.25 V, and is set by the LVDS driver. For more information on multi-drop LVDS, read National Semiconductor's application note AN-1115, located at http://www.national.com/an/AN/AN-1115.pdf. Table 2 summarizes the DC specifications of LVDS.

Table 2: Standard LVDS DC Specifications

DC Parameter	Conditions	Min	Typ	Max	Units
Output High Voltage for Q and $\overline{Q}$	R_T across Q and $\overline{Q}$ signals	–	1.38	1.6	V
Output Low Voltage for Q and $\overline{Q}$	R_T across Q and $\overline{Q}$ signals	0.90	1.03	–	V
Differential Output Voltage $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, Q = Low	R_T across Q and $\overline{Q}$ signals	250	350	450	mV
Output Common-Mode Voltage $(Q + \overline{Q})/ 2$	R_T across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
Differential Input Voltage $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, Q = Low	Common-mode input voltage = 1.25V	100	350	–	mV
Input Common-Mode Voltage $(Q + \overline{Q})/ 2$	Differential input voltage = ± 350 mV	0.25	1.25	2.25	V

Driving Multi-Drop LVDS from Virtex-E Devices

Figure 4 shows the complete schematic of the Virtex-E LVDS line driver driving 20 LVDS receivers in a multi-drop configuration. The receivers are either Virtex-E receivers or other off-the-shelf LVDS receivers. The LVDS signal is driven from a Virtex-E LVDS driver on the left, and is daisy-chained with two 29-ohm transmission lines and stubs to all 20 LVDS receivers at the OUT[1:20] and $\overline{\text{OUT}[1:20]}$ nodes. Each LVDS receiver taps off the main multi-drop lines every 2.5 inches for a multi-drop line length of 50 inches. Each LVDS receiver tap line has a one inch maximum stub length with a 50-ohm transmission line impedance to ground, or a differential impedance of 100 ohms between the two stubs. A 44-ohm termination resistor R_T is placed across the LVDS_TERM and $\overline{\text{LVDS\_TERM}}$ nodes close to the final LVDS receiver, on the right. Resistors R_S and R_{DIV} attenuate the signals coming out of the Virtex-E LVDS drivers with $V_{CCO} = 2.5V$ and provide a 22-ohm source impedance (series termination) to the 29-ohm transmission lines. The design calls for a 22-ohm source impedance because the added load of the LVDS receivers brings the 29-ohm line down to an effective impedance of 22 ohms on average. The capacitor C_{SLEW} reduces the slew rate from the Virtex-E LVDS driver, resulting in smaller reflections and less ringing at the receivers.

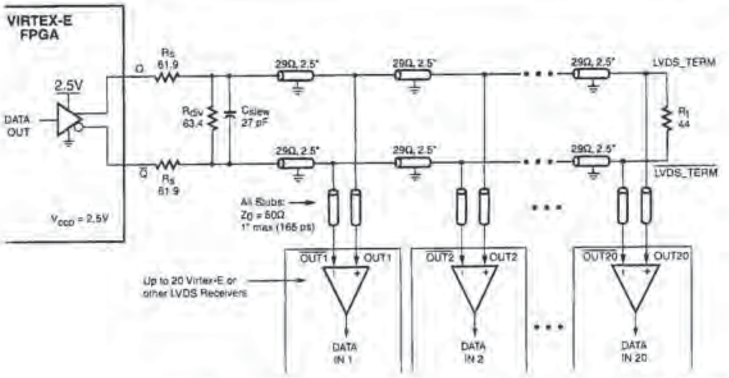


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Figure 4: Virtex-E 20-Load Multi-Drop LVDS Schematic

Why would a 29-ohm transmission line be terminated at both ends with 22 ohm terminations? The answer lies in the behavior of transmission lines. When capacitive receivers and stubs load down a transmission line, the extra capacitance reduces the effective impedance. The receivers in Figure 4 have an effective load capacitance of roughly 9 pF, including receiver capacitance, trace and stub capacitance. A 9 pF capacitor placed every 2.5 inches on a 29 ohm line brings the line down to 22 ohms. Therefore, the reflections are minimized if the line is terminated into 22 ohms. For further information on effective transmission line impedance, see Howard W. Johnson, "High-speed digital design: a handbook of black magic," 1993, pp. 172-174. The section on equally-spaced capacitive loads provides the following equations:

If $Z_0 = \sqrt{L/C}$
where L = inductance / unit length
C = capacitance / unit length
and C_L = capacitance of each load
N = number of loads
H = total length of transmission line
Then $Z_{0EFF} = \sqrt{L / [C + N^{*}C_L/H]}$

Although the transmission line uses lower impedance than the typical impedance found in the specification used in Table 2, all the voltage swings comply with the LVDS standard. This means that any LVDS receiver will work correctly on this multi-drop line. In fact, the lower impedance results in a wider trace, reducing inductance and skin-effect losses along the multi-drop lines. The two 29-ohm single-ended transmission lines can be microstrip, stripline, or the single-ended equivalent of a 58-ohm twisted pair or similar balanced differential transmission line. See Appendix A in Xilinx application note XAPP230, "The LVDS I/O Standard" for a discussion of transmission lines and terminations used in LVDS.

The multi-drop Virtex-E LVDS line driver adheres to all the standard ANSI/TIA/EIA-644 LVDS Interface Standard DC input levels as specified in Table 2. The output common-mode voltage typically averages to $V_{CCO}/2$. Component value derivations for R_S, R_{DIV}, and C_{SLEW} can be found in Appendix B on page 10. The DC performance of Virtex-E LVDS meets or exceeds the ANSI/TIA/EIA-644 LVDS Interface Standard specifications shown in Table 2.

The Virtex-E multi-drop LVDS termination in Figure 4 differs from other LVDS source terminations in that it actually absorbs reflected energy at the source. While most LVDS drivers behave like a current source with a high output impedance, the Virtex-E multi-drop LVDS line driver behaves like a current source in parallel with a 22-ohm resistor, thereby improving the source termination for reflected signals. The 22-ohm source impedance of the Virtex-E LVDS driver absorbs nearly all differential reflections from the capacitive loads distributed along the multi-drop lines, reducing standing waves, undershoot, and noise levels compared to other LVDS drivers. The voltages at LVDS_TERM and $\overline{\text{LVDS\_TERM}}$ and on the transmission lines meet or exceed all of the standard LVDS output levels shown in Table 2.

Figure 5 shows the typical step response of Virtex-E multi-drop LVDS drivers for the schematic in Figure 4. The top graph shows the single-ended waveforms at outputs 1, 10, and 20, corresponding to receivers at the beginning, middle, and end of the multi-drop line. The bottom graph shows the differential voltage at five receivers along the multi-drop line from beginning to end. All voltages are measured at the on-die differential input of the receiver. All received waveforms show similar characteristics with little undershoot or overshoot and negligible load reflections.

Figure 6 shows typical 311 Mb/s burst data (or 155.5 MHz clock) response of Virtex-E multi-drop LVDS outputs for the schematic in Figure 4. Single-ended and differential waveforms are shown for outputs 1, 10, and 20 along the multi-drop line. All received waveforms show similar characteristics with little or no undershoot/overshoot and negligible reflections. Some smoothing of the waveform occurs over the length of the multi-drop line loaded by the receivers, but the attenuation is minor. Even the last receiver sees nearly 400 mV peak at the end of the 50 inch line after 19 other receivers. The excellent performance of Virtex-E multi-drop LVDS can be attributed to its matched source impedance and the rise-time-reducing capacitor C_{SLEW} at the source.

The Virtex-E multi-drop LVDS driver is fully compatible with LVDS receivers from National Semiconductor and other companies.

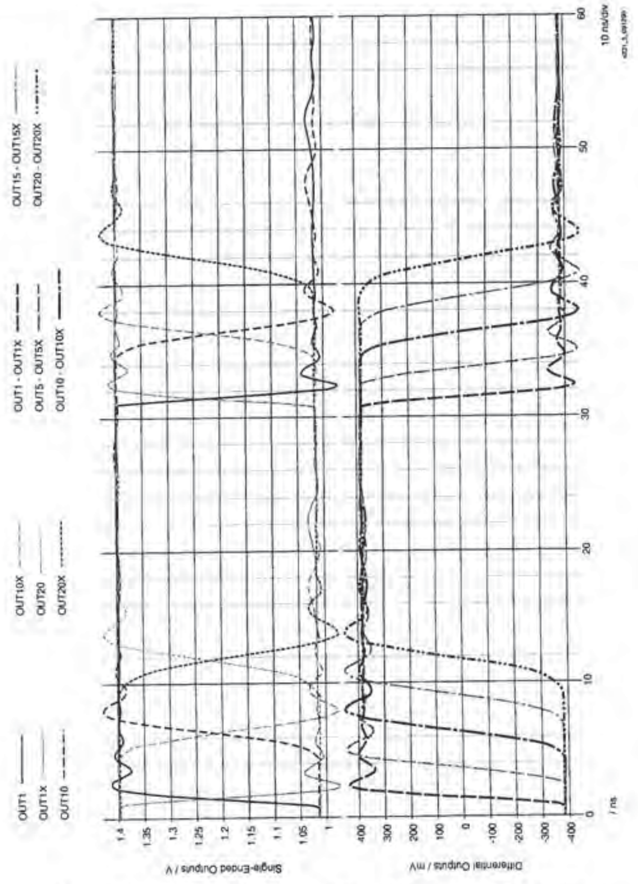

Figure 5: Typical Step Response of Virtex-E Multi-drop LVDS Drivers

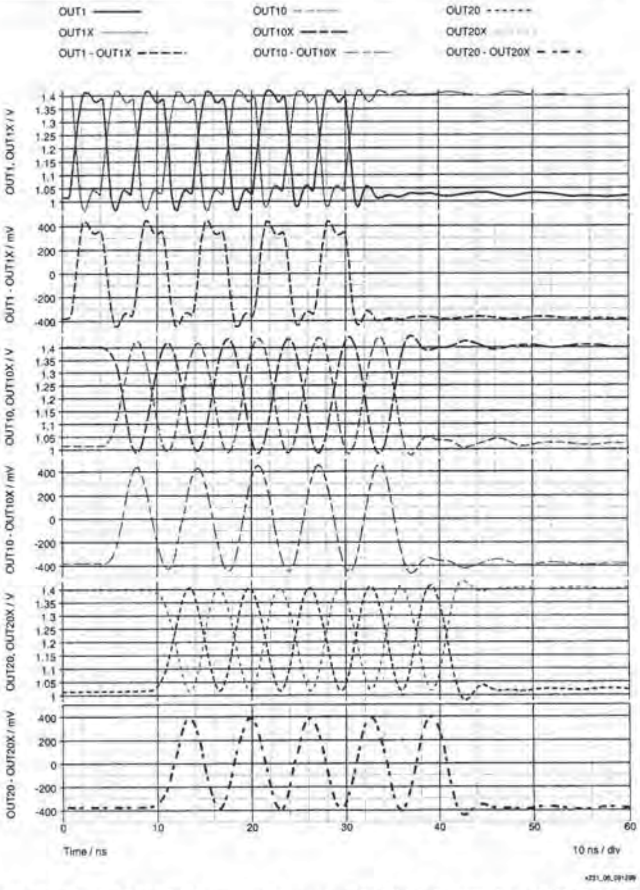

Figure 6: Typical 311 Mb/s Burst Data Response for Virtex-E Multi-drop LVDS Output for Schematic in Figure 4.

Conclusion

The Virtex-E FPGA transmits and receives multi-drop LVDS. The maximum data rate is 311 Mb/s or a clock of 155.5 MHz for the -7 Virtex-E speed grade. Virtex-E LVDS drivers provide significant improvement in signal integrity over other off-the-shelf LVDS drivers due to their matched source impedance which series terminates the transmission lines and minimizes source reflections. Reliable data transmission is possible for up to 20 LVDS receivers over electrical lengths of 8.25 ns (50 inches), limited only by skin effect losses in the PCB trace. Virtex-E FPGAs utilizing LVDS eliminate costly TTL-LVDS drivers and LVDS-TTL receivers, reduce board area, and reduce signal delay skew, while reliably transferring high-speed data and clocks over long distances between chips, boards, chassis, and peripherals.

Appendix A: PCB layout guidelines for Virtex-E multi-drop LVDS

Printed-circuit board layout guidelines for the Virtex-E multi-drop LVDS circuit in Figure 4 are as follows:

1) A multi-layer printed-circuit board with controlled transmission line impedances is required.

2) All transmission lines between LVDS drivers and receivers should be referenced to a common ground plane except when routed through a balanced differential transmission line such as twisted-pair. For twisted-pair and other balanced lines, utilize a grounded shield that connects to the ground planes at the beginning and ending of the twisted-pair cable to allow for common-mode return current. If no shield connection is available, take extra care to use symmetric and equal-length routing and ensure capacitive load balancing on the differential pair to prevent excessive common-mode to differential mode conversion. Do not split the ground plane under the signal path as this will cause large discontinuities from increased inductance.

3) The resistors R_S and R_{DIV} should be placed close to the Virtex-E outputs for the Virtex-E multi-drop LVDS line driver. Place the parallel termination resistor R_T close to the final LVDS inputs at the far end of the multi-drop line.

4) The capacitor C_{SLEW} should be placed close to resistors R_S and R_{DIV}.

5) Symmetric and equal-length routing should be used of the multi-drop LVDS signal pair between source and destinations to maximize common-mode rejection. Route the two LVDS signals with minimal spacing between the traces along the multi-drop line and the stubs. If the trace spacing is less than the dielectric thickness to the ground plane, differential impedance effects must be included to determine the effective transmission line impedance since the trace impedance will be significantly affected by the differential impedance between the two traces. Wider spacing has a smaller effect on the impedance.

6) Virtex-E provides dedicated LVDS input/output pairs for driving and receiving LVDS. The IOB registers driven from a single clock provide a convenient point to synchronize inputs and outputs.

Appendix B: Component value derivations for the Virtex-E multi-drop LVDS line driver

Referring to Figure 4, resistors R_S and R_{DIV} attenuate the signals coming out of the Virtex-E LVDS drivers and provide a matched source impedance (series termination) to the transmission lines. Values for R_S and R_{DIV} are determined by these two constraints. The equivalent source impedance R_{EQ}, including the Virtex-E driver impedance R_{DRIVER}, must equal the effective transmission line impedance, 22 ohms. Using the differential half-circuit:

$$(R_{DIV} -> R_{DIV}/2,\ R_T -> R_T/2),$$

$$R_{EQ} = (R_{DRIVER} + R_S) \mathbin{//} (R_{DIV}/2) = Z_{0EFF} \qquad (1)$$

R_S and R_{DIV} are chosen to obtain the desired attenuation of the signal path from the Virtex-E driver to the LVDS destinations. The desired signal attenuation is defined as α.

$$\alpha = V_{SWING}(LVDS) / V_{CCO} = [(R_{DIV}/2) / (R_{DIV}/2) + R_{DRIVER} + R_S)]$$
$$[R_T/2 / (R_T/2 + R_{EQ})]$$

$$R_T/2 / (R_T/2 + R_{EQ}) = 1/2, \text{ therefore,}$$
$$\alpha = V_{SWING}(LVDS) / V_{CCO} =$$
$$[(R_{DIV}/2) / (R_{DIV}/2) + R_{DRIVER} + R_S)] / 2 \qquad (2)$$

Using equations 1 and 2 and solving for R_{DIV} and R_S yields:

$$R_S = (Z_{0EFF} / 2\alpha) - R_{DRIVER} \qquad (3)$$
$$R_{DIV} = [4\alpha / (1 - 2\alpha)]\ [R_{DRIVER} + Rs] \qquad (4)$$

Substituting Z_{0EFF} = 22 ohms, R_{DRIVER} = 10 ohms, V_{CCO} = 2.5V, and $V_{SWING}(LVDS)$ = 380 mV into Equations 2 - 4 and rounding to the nearest 1% value, the values of R_S = 61.9 ohms and R_{DIV} = 63.4 ohms are found, shown in Figure 4. The typical LVDS voltage swing of 350 mV is increased to 380 mV to offset skin effect losses at 311 Mb/s data rates near the end of the 50-inch multi-drop lines.

C_{SLEW} increases the rise time out of the Virtex-E multi-drop driver. Typically, the 10-90% rise time of LVDS is 500 ps. Using C_{SLEW}, the desired rise time is increased to approximately 1 ns. Using the differential half-circuit equivalent of Figure 4, $(R_{DIV} -> R_{DIV}/2,\ C_{SLEW} -> 2C_{SLEW})$, the driving point impedance for $2C_{SLEW}$ is $R_{EQ} \mathbin{//} R_T/2 = R_{EQ}/2$. The RC time constant is:

$$(2C_{SLEW})(R_{EQ}/2) = R_{EQ}\,C_{SLEW}.$$

By setting τ, the RC time constant, equal to the original LVDS 10-90% rise time, the new 10-90% rise time will be nearly 1 ns. The value for C_{SLEW} is calculated as:

$$C_{SLEW} = \tau / R_{EQ} \qquad (5)$$

Substituting τ = 500 ps and R_{EQ} = 22 ohms into Equation 5 and rounding up to the nearest 10% value, the value of C_{SLEW} = 27 pF is obtained, shown in Figure 4.

Revision History

Date	Version	Revision
9/23/99	1.0	Initial Xilinx release

TEXAS INSTRUMENTS

LVDS Multidrop Connections

Application Report

July 1999

Mixed Signal Products

SLLA054

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LVDS Multidrop Connections

Elliott Cole, P.E.

ABSTRACT

This application report describes design considerations for low-voltage differential swing (LVDS) multidrop connections. The report describes the maximum number of receivers possible versus signaling rate, signal quality, line length, output jitter, and common mode voltage range when multidrop testing on a single LVDS line driver transmitting to numerous daisy-chained LVDS receivers.

The LVDS receivers are wired to simulate a wire-wrapped or printed circuit backplane environment. The receivers are tested to monitor system response for different signaling rates and a varied number of receivers.

1 Introduction

The most commonly used data transmission system, or topology, is known as the *Point-to-Point* application. The term *Point-to-Point* is used to describe a unidirectional system that consists of a single line driver connected to a single line receiver, that transmits data from *point A* to *point B* using one *speaker* and one *listener*. The term *multidrop*, defines a topology where one driver transmits data to more than one receiver. The *multidrop* application is the equivalent of sending data from *point A* to *point B1*, *point B2*, *point B3*, etc., since with this application, one *speaker* may have a *whole room full of listeners*.

In data transmission circuits, the output voltage transition time of a line driver is often the limiting factor in determining a maximum signal rate. This is usually due to an output stage not being fast enough to provide a *decent* pulse, however data rate limitations are also related to noise margin, crosstalk, and radiated and conducted emissions. Many conventional line drivers have a single-ended output with a long, slow voltage swing of several volts, a signaling rate may be further constrained by the increase in power dissipation as the signaling rate increases.

2 Maximum Number of Receivers

Connecting multiple LVDS receivers to a single LVDS driver works well, but at some point, increasing the number of receivers overloads a single driver, and the system fails. The maximum number of receivers possible is examined in the following discussion with *best case* and *worst case* modeling.

2.1 Best Case Analysis

2.1.1 DC Electrical Models

The effect that multiple receivers have on a driver is calculated by examining the output model of an LVDS driver and the input model of an LVDS receiver. The common mode and differential models shown in Figure 1 represent an LVDS bus consisting of an LVDS driver, the interconnection, and the LVDS receiver.

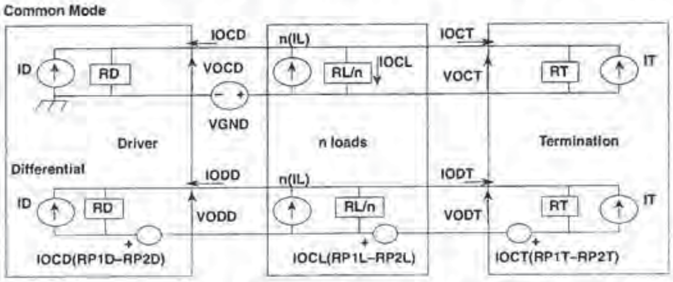

Figure 1. Common Mode and Differential LVDS Bus Model

2.1.2 Driver Analysis

Figure 2 displays an LVDS driver model from Annex C of the TIA/EIA-644 standard. The model is complex, but useful in developing a simplified differential line driver model for the examination of driver response to output load increases. For this purpose, the simple model of an SN65LVDS31 line driver is developed in Figure 3.

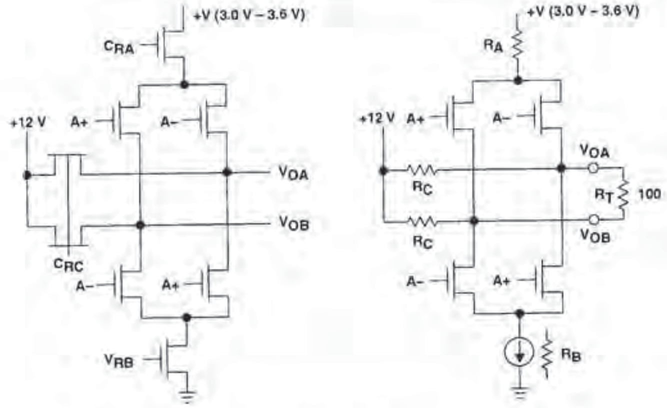

Figure 2. Differential Line Driver Model

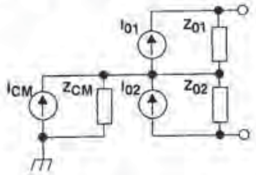

Figure 3. Simplified LVDS Driver Model

Output differential drive and common mode offset models are derived from the simplified model of Figure 3 and modeled individually in Figure 4.

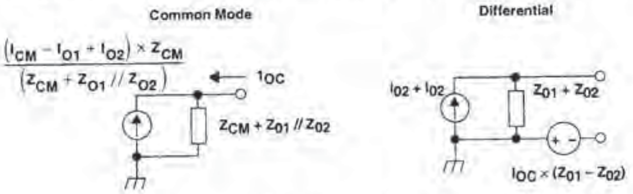

Figure 4. Common Mode and Differential Driver Models

Values are assigned to each source and impedance by using data sheet specifications and IBIS models for the SN65LVDS31. These values are obtained from a straight line approximation of the actual IBIS model and are shown in Figure 5.

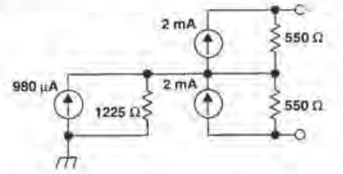

Figure 5. SN65LVDS31 Simplified Driver Model

Using the derived values in this model, individual common mode and differential models are developed in Figure 6.

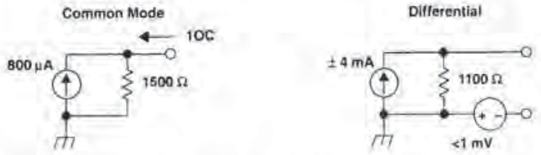

Figure 6. SN65LVDS31 Common Mode and Differential Driver Models

2.1.3 Common Mode Load

The model for the common mode output of the SN65LVDS31 shows the driver consists of a small current source and a 1500 Ω load develops a 1.2 Vdc common mode voltage. The current source is capable of maintaining the 1.2 Vdc within the limits of the 800 µA source, but loads beyond this limit will cause the common mode output to shift.

2.1.4 Differential Load

The nominal driver output is modeled differentially as a 4 mA source with an output impedance of 1100 Ω load; the resulting (nominal) current is 3.66 mA at the termination resistor, producing a differential voltage (Vod) of 366 mV across the inputs of the receiver. The LVDS standard specifies a minimum differential voltage of 250 mV, which occurs if the termination resistance decreases to 67 Ω. The differential model also contains an offset voltage modeled as a 25 mV voltage source resulting from a mismatch of the individual outputs. This mismatch can cause the output voltage levels to change differentially by 50 mV as the current source varies. The open circuit differential-output voltage of the driver without the 100 Ω termination resistor will not remain at 4.4 Vdc, but will ramp up to Vcc.

2.1.5 Receiver Input Leakage

The SN65LVDS32 simplified receiver model in Figure 7 and the common mode and differential models of the receiver in Figure 8 are developed with the same derivation technique as the SN65LVDS31 driver.

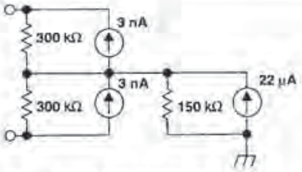

Figure 7. Simplified SN65LVDS32 Receiver Model

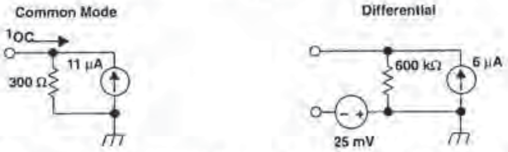

Figure 8. SN65LVDS32 Common Mode and Differential Driver Models

The receiver for the SN65LVDS32 models has an extremely high input impedance when compared to the 100 Ω termination resistor. The common mode model has very little impact on the overall system when compared to the driver. The same is true of the differential model which is the equivalent of a 6 µA source compared to the 4 mA source of the drivers. It would take a large number of receivers (over 100) before the effects would interfere with the performance of an overall system.

2.2 Worst Case Analysis

2.2.1 TIA/EIA-644 Requirements

Although both devices modeled above meet the requirements of TIA/EIA-644, there are LVDS specifications that need to be addressed.

When the standard was developed, it was specifically intended for lower signaling rates and point-to-point applications, and LVDS signal *edges* running in high-speed applications like multipoint or multidrop were clearly not envisioned. As a result, parameters that would ultimately be affected by these new applications are not completely defined in the standard.

Two of these *undefined* parameters are the common mode currents in an LVDS driver and receiver. The standard does define a common mode voltage range via the ground potential difference voltage (Vgpd) of ±1 Vdc, however the maximum allowable common mode current between a driver and receiver(s) is yet to be defined.

Another parameter that does not lend itself to multipoint or multidrop applications is the leakage current out of (or into) each receiver pin, which is modeled for the SN65LVDS32 in Figure 7 as a 3 nA current source. The standard states that leakage current *shall not exceed 20 µA*. The direction for the current is not specified. Therefore the specification is met if one receiver pin has a leakage current of −20 µA, and the other pin +20 µA.

NOTE: Current leakage can occur with another manufacturer's parts if the failsafe configuration of the receiver is based upon biasing one terminal high and the other terminal low.

Theoretically then, a resulting 40 µA *loop* current will now be working against the differential output voltage (Vod) of the driver. The nominal output of the driver model is 366 mV (4 mA across an equivalent resistance of 91.5 Ω) and the minimum allowable Vod for a driver is 247 mV, therefore a 40 µA loop current leaves an operating margin of approximately 116 mV.

Utilizing this margin, 31 receivers (116 mV/3.66 mV per receiver) can be connected to the driver before dropping below the minimum Vod; however, any desired margin lowers this number accordingly. For example, if a 50 mV noise margin and 50 mV ground potential difference margin are desired, the maximum number of receivers drops to 5. This condition, modeled with 20 theoretical LVDS receivers, is illustrated in Figure 9.

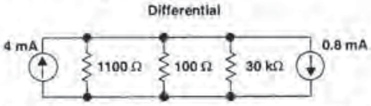

Figure 9. Spec Compliant 20 Receiver Model

The 20 receivers establish a 0.8 mA current working against the differential voltage generated by the driver. The 20 resistors in parallel develop an equivalent system impedance of approximately 90 Ω, which results in a 288 mV difference voltage across the 100 Ω termination resistor, leaving little room for a system performance margin.

NOTE: The LVDS receiver is theoretical, and the values are used to demonstrate what could happen based upon the present LVDS standard. The LVDS committee reviewing the standard should address these issues.

2.2.2 TI LVDS Characteristics

TI LVDS receivers have both inputs pulled up through 300 kΩ resistors. Since both inputs are pulled up internally, the resulting loop current is the *difference* between the input leakage currents of each pin, and not the sum of the two currents as demonstrated in the example above, where nonTI parts are modeled.

Other manufacturers employ a configuration that results in a differential *loop* current very near the 40 µA allowable limit. Although the devices meet the LVDS specification and work in point-to-point applications, they would not perform well in the multidrop application with a large number of drops.

3 Maximum Signaling Rate Obstacles

Many factors come into play when sending digital signals over copper wire at megabits-per-second rates. Signaling rates and bandwidth have increased dramatically in the last few years, and cable and connector manufacturers are struggling to keep pace with newer and faster silicon. While many of the factors affecting maximum signaling rate are nothing new, the problems they pose are a concern whether the signaling rate is kilobits-per-second or megabytes-per-second.

3.1 Driver Output Loading

The LVDS line driver converts a single-ended logic signal (LVTTL) to the differential output levels and common mode voltage specified in the LVDS standard. The voltage levels are required to drive the transmission line and termination resistor at the receiver input, but as transmission line length increases, so does its effect on the driver. The dc resistance of a CAT5 cable is specified (TIA/EIA-568-A) not to exceed 9.38 Ω/100 meters, which equates to a decrease of 35 mV in the Vod of an LVDS driver with a 100 m cable. However, the standard recommends a maximum distance for LVDS transmission of *up to 30 m*, which places the Vod loss in the range of 10 mV.

Cables also attenuate an ac signal (TIA/EIA1–568-A). The permissible attenuation allowed for a CAT5 cable may be derived with the following equation;

$$\mathit{Attenuation}\,(f) = 1.967\sqrt{f} + 0.023 \times f + \frac{0.050}{\sqrt{f}}$$

Where f is the applied frequency

Another consideration is a cable's characteristic impedance (Zo). The TIA/EIA-644 LVDS specifies the use of 90 Ω to 132 Ω transmission lines (other values may be used in nonstandard applications). Since the output impedance of an LVDS driver is significantly greater than Zo, reflections are created as signals propagate from the device, creating a trade-off between driver power dissipation and output impedance matching of the driver with the cable.

3.2 Intersymbol Interference

Maximum signaling rate is also affected by intersymbol interference (ISI). While this discussion is not restricted to the multidrop application, the effect may be more pronounced in a multidrop system due to the increased capacitive loading of multiple receivers on a transmission line. Capacitive loading induced ISI causes errors that are pattern (or data) dependent. The influence of ISI on a driver's output signal is shown in Figures 10 and 11.

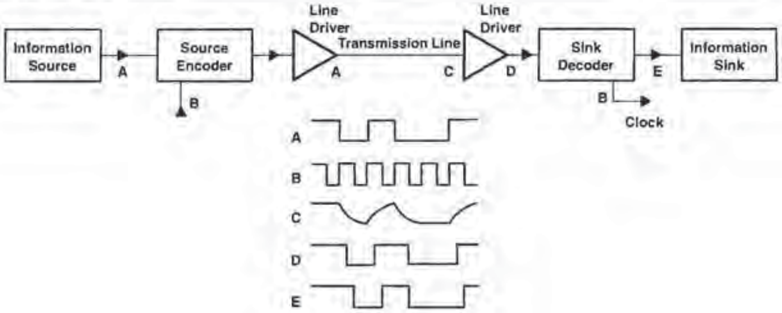

Figure 10. Loading Effects at a Receiver Input

Capacitive loading may not be as apparent at lower signaling rates because a signal has time to make the transition and settle to a steady-state level before the next transition occurs. At higher signaling rates, as shown in Figure 11, a signal may not have sufficient time to make a transition detectable by a receiver, resulting in data errors.

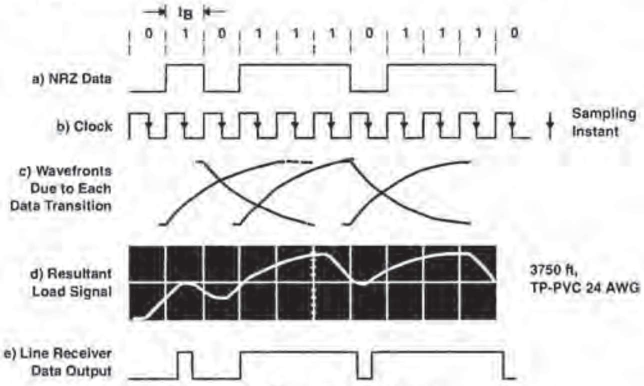

Figure 11. Data Error Pattern

3.3 Skew in Parallel Buses

The output of a SN65LVDS31 driver changes state in about 500 ps. The interconnection to a receiver greater than a few centimeters can be closely modeled as a resistive load and a time delay. Systems that use multiple LVDS drivers to form a parallel bus need the same time delay for all channels, as differences will cause a timing skew and possible data errors between channels. For example, consider a parallel bus system with a 400 Mbps signaling rate, a timing budget of 650 pS for the rising edge, 650 pS for the falling edge, and 1200 pS for the steady state level. If the propagation delay of the cable is 5 nS/meter, a 20 cm difference in cable length between two channels will cause a skew of 1 nS, or 40% of the timing budget. This problem becomes more manageable as many cable manufacturers now spec multiple twisted pair cables with a maximum skew between pairs, often listed as a difference in propagation delay between pairs of conductors per unit length of cable.

3.4 Termination

The transmission line between driver and receiver is terminated at the receiver input, with a resistance approximately equal to the line's characteristic impedance, for two reasons. First, an LVDS driver is a current mode device and the differential voltage is generated at the receiver inputs across this termination resistor. Secondly, almost all transmission systems require some type of termination to minimize reflections back into the line. Higher frequency components (fundamental and harmonic) reflect back to the source if termination resistance does not closely match the characteristic impedance of a transmission line. While allowable reflection in a system depends upon its design and tolerable noise margin, matching the nominal characteristic impedance of the cable to ±10% of the termination resistor value is generally sufficient. The TIA/EIA-644 specifies termination within the range of 90 Ω to 132 Ω, or a nominal value of 100 Ω across the inputs of an LVDS receiver.

A termination resistor is placed across the inputs of the last receiver in a multidrop application, which means that ideally, balanced driver current flows through the entire transmission line. Although other receivers connected to the line do not draw significant current, the connectors and short lines to each of the additional receivers create *stubs* on the transmission line. Each of these stubs is modeled as a small lumped capacitance attached to the line, creating a mismatch at that point on a transmission line. It is difficult to maintain the characteristic impedance of a line after the first stub, and the small mismatch increases with each successive *drop* along the line. The overall effect results in a degraded signal quality, slower signal transitions, and an increase in intermodulation products. It is therefore evident that a maximum possible signaling rate decreases as system noise and signal jitter increases with each additional drop.

3.5 Allowable Jitter

The required quality of a signal leaving a receiver is ultimately dictated by the quality of the downstream equipment in a system. Signal quality is not a major concern if the downstream equipment is high-end decoding equipment with error correction and calibration capabilities. However, if downstream equipment is low end, then the quality of the receiver output may need to be extremely *clean*.

The most common method of quantifying signal quality is by measuring jitter in the eye-pattern of a receiver's output. An eye-pattern includes all the effects of systemic and random distortion and reveals the time during which a signal may be considered valid. Figure12 portrays a typical eye-pattern with the important parameters identified.

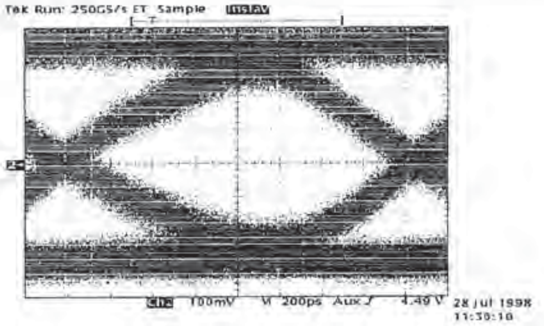

Figure 12. Typical Eye Pattern

The jitter values obtained from eye-pattern measurements are often reported as *percent jitter*, the percentage of time that jitter takes out of each bit.

$$\text{Percent Jitter} = \frac{\text{Absolute Jitter}}{\text{Time Unit Interval}} \times 100$$

The time unit interval (UI) is the reciprocal of the signaling rate, therefore percent jitter represents the portion of UI during which a logic state should be considered indeterminate.

3.6 External Noise Coupling

One of the benefits of LVDS is the superior noise immunity of the balanced differential interface between driver and receivers. This benefit outweighs the fact that two wires and connector pins are required for data transmission. The effects of noisy environments and interference from other equipment are minimized because transient noise and spikes are coupled onto both conductors at the receiver input. The receiver responds to the *difference* in signal levels across the input and this transience is present on both input conductors, it is essentially ignored and has minimal impact on system performance. While differential signaling has this advantage over single-ended signaling, both techniques are still susceptible to the other external noise sources.

3.7 Common Mode Voltage Range

Another obstacle of concern is ground potential differential voltage (Vgpd), which occasionally occurs when the driver and receiver are in different locations with separate power supplies. When the ground reference of the driver's and receiver's power supplies is not common, a dc offset between the driver and receiver may develop. The LVDS standard addresses this problem by requiring that any dc offset stay within a ±1 Vdc range, a 3.3 V LVDS system may require that a dedicated ground line or *water-pipe* ground be used between the driver's and receiver's power supplies.

4 Bench Verification

Now that the major obstacles limiting signaling rate have been addressed, the LVDS multidrop system is examined on the bench.

4.1 The Multidrop Setup

A basic multidrop system consists of one LVDS driver connected to multiple LVDS receivers. TI's LVDS evaluation module (EVM) is shown in Figure 13.

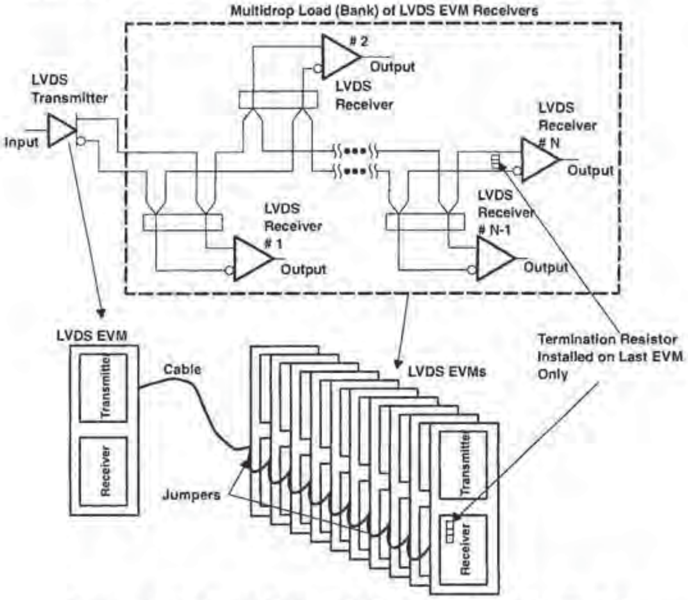

Figure 13. Multidrop System With TI LVDS Evaluation Modules

The EVM is constructed with SMA connectors on one receiver channel. The remaining channel connections lead to empty solder pads on the edge of the board. Two-wire terminal posts (Berg Sticks™) are soldered to two of the receiver's edge pads. These posts facilitate the two-wire connection to an adjacent EVM receiver channel, providing for a *daisy-chain* of 36-receiver channels. Figure 14 is a closeup of the *Berg Sticks* installed on one EVM.

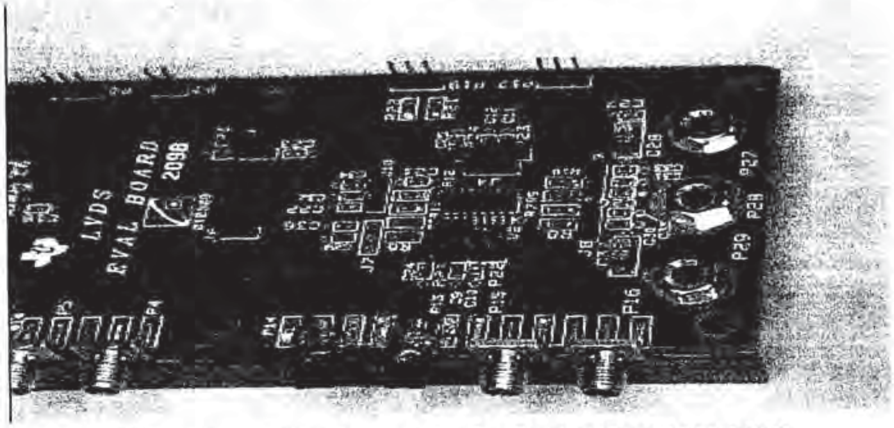

Figure 14. Berg Sticks Connected to One Receiver Channel on the EVM

The 36 EVMs are bolted together with threaded rod, slid through the banana jack connectors of each EVM, then fitted with flat washers and nuts on both sides of each EVM. This creates the equally spaced multidrop bank of 36 receivers shown in Figure 15. Power (V_{CC} and ground) is then applied to the bank by connecting a dedicated supply to the metal rods. Thirty-five 7,62 cm (3″) length twisted pair wires are used as jumpers from one receiver connection to the next. A 100 W termination resistor is installed between the inputs of the last (farthest) EVM. Another EVM is set up as the *driver*, mounted and powered separately, from the *load bank* of receivers.

Berg Sticks is a trademark of Berg Electronics.

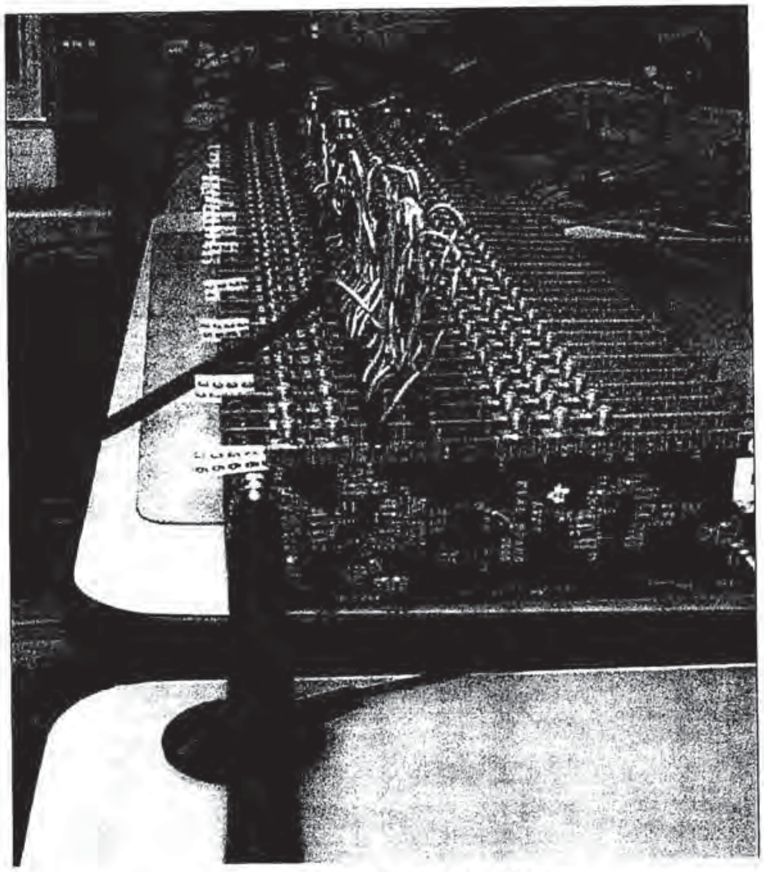

Figure 15. Multidrop Bank of 36 Receivers

4.2 Equipment Setup

The Tektronix HFS-9003 signal generator in Figure 16 (top shelf on the left), employed as the signal source for the multidrop system is adjusted as follows:

- Pattern: NRZ, pseudo-random binary sequence (PRBS)
- Input high level: 2.7 Vdc
- Input low level: 0.0 Vdc
- Slew rate: 800 ps

The Tektronix HFS-9003 signal generator is capable of generating a pseudo-random binary sequence (PRBS) data pattern at signaling rates up to 630 Mbps, with data patterns not repeated in the same sequence for $2^{16}-1$ (64K) bits. The setup is monitored with the Tektronix 784D oscilloscope on the right side of the photo, and powered with the two small Hewlett Packard power supplies on the bench behind the load bank. One of these supplies the driver, while the other supplies the load bank, with both set to 3.3 Vdc.

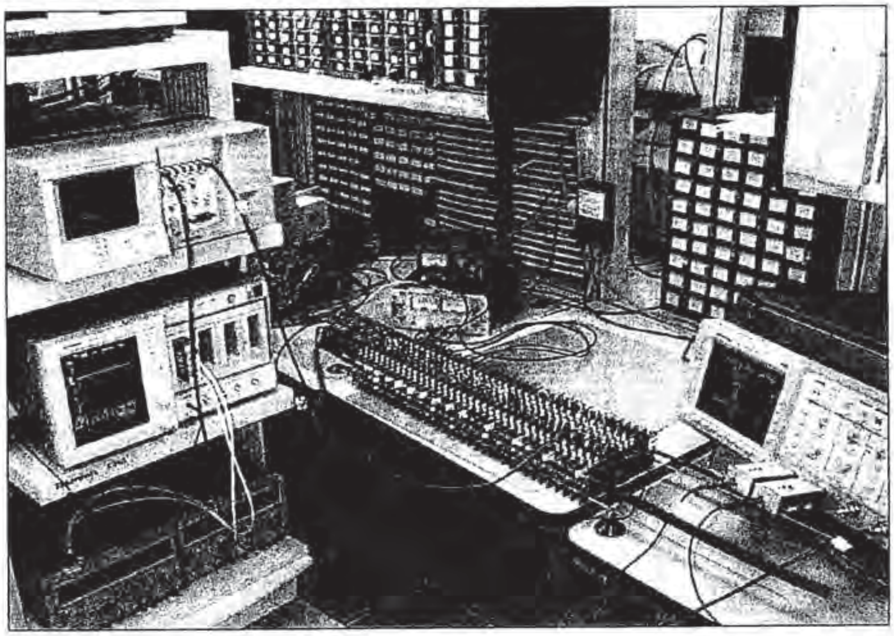

Figure 16. Test Setup With Instrumentation

At high data rates, the influence of equipment used to measure a signal of concern should be minimized, therefore probe heads should behave like a low-capacitance, high-impedance load with high bandwidth. For this test, the Tektronix 784D oscilloscope and Tektronix P6247 differential probes are used, since both scope and probe have a bandwidth of 1 GHz and a capacitive load of less than 1 pF. For signals in the range of 400 Mbps and above, an even higher bandwidth is recommended (as a rule of thumb, the fifth harmonic, i.e. 2 GHz, should be able to be detected), but at this time, no faster differential probe head is available.

The problems associated with the triggering jitter are eliminated by using a separate output channel from the HFS-9003, as the trigger source for the TDS784D oscilloscope.

The transmission cable is a Belden MediaTwist™ (CAT5) cable containing four unshielded twisted pair (UTP) conductors. The jumpers used to connect each receiver together are constructed by cutting nine 7,62 cm (3″) pieces of MediaTwist, removing the four pieces of twisted pair from each piece, then stripping about a half inch of insulation from both ends of each twisted pair.

5 Measurement Results

Four series of tests will be completed in order to determine the receiver number vs cable length and the receiver number vs signaling rate:

- Output Jitter vs Signaling at Different Cable Lengths
- Output Jitter From a Single Point-to-Point Receiver
- Output Jitter of Varied Load Conditions
- Output Jitter Percent From Every Fourth Load

5.1 Output Jitter From Receiver 36 With Different Cable Lengths

The first series of signal length (Mbps) measurements will be taken between the driver and the 36^{th} receiver load bank. The measurements will be performed using varied lengths of cable to examine the system response to all 36 of the EVM receivers.

- Insert the 100 m cable connectors into the driver EVM Berg-Stick connectors.
- Insert the 100 m cable connectors into the first driver EVM Berg-Stick connectors (Receiver 1).
- Record data from the 36^{th} EVM receiver for each signaling rate (Mbps) Figure 17.
- Shorten the cable (90 m, 80 m through 1 m) between the driver and the receiver load bank.
- Repeat the series of signal length (Mbps) measurements for each cable length and record the data.

MediaTwist is a trademark of Belden Wire and Cable Company.

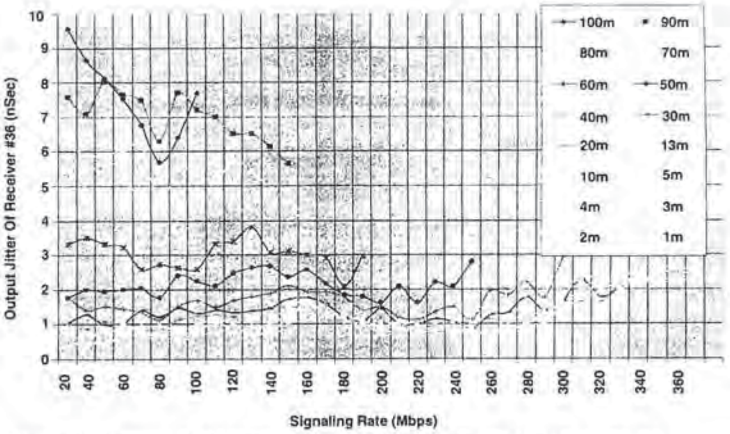

Figure 17. Output Jitter From Receiver 36 With Different Cable Lengths

The results of the tests are presented in Figure 17 and clearly show that output jitter is proportional to cable length, but the data format is not in the *conventional* format for percent jitter. In Figure 18 the same data is replotted as percent jitter.

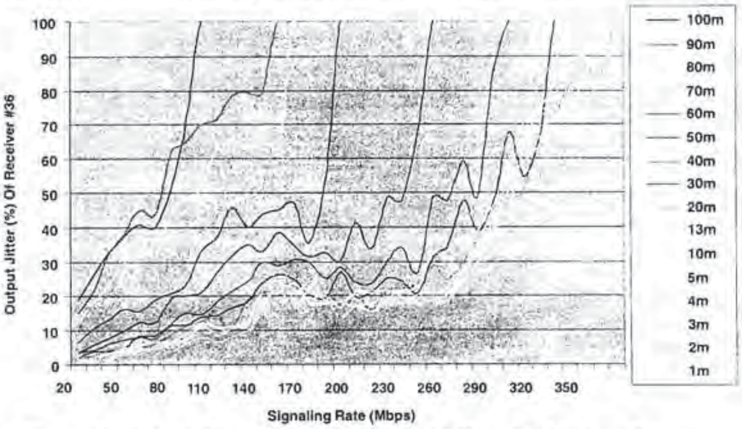

Figure 18. Output Jitter vs Signaling Rate at Different Cable Lengths

5.2 Output Jitter From a Single Point-to-Point Receiver

The second series of signal length (Mbps) measurements will be taken between the driver and the 36th EVM receiver only. The measurements will be performed using varied lengths of cable to examine the system response to the 36th EVM receiver only.

- Remove the jumper wires between the 35th and 36th EVM receivers.
- Insert the 30 m cable connectors into the driver EVM Berg-Stick connectors.
- Insert the 30 m cable connectors into the 36th EVM receiver Berg-Stick connectors.
- Record data from the 36th EVM receiver for each signaling rate (Mbps) Figure 19.
- Shorten the cable (10 m, 3 m, and 1 m) between the driver and the 36th EVM receiver.
- Repeat the series of signal length (Mbps) measurements for each cable length and record the data.

The results of the tests are presented in Figure 18.

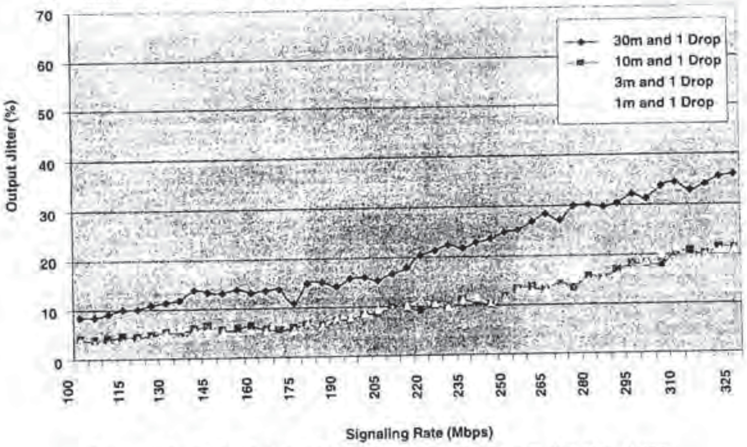

Figure 19. Output Jitter From a Single Point-to-Point Receiver

5.3 Output Jitter of Varied Load Conditions

The third series of signal length (Mbps) measurements will be taken between the driver and varied EVM receiver load drops. The measurements will be performed using varied lengths of cable to examine the system response to the varied EVM receiver load drops.

- Remove the jumper wire between the ninth and tenth EVM receivers.
- Insert the 30 m cable connectors into the driver EVM Berg-Stick connectors.
- Insert the 30 m cable connectors into the ninth EVM receiver Berg-Stick connectors.

- Record data from the ninth EVM receiver for each signaling rate (Mbps) Figure 20.
- Shorten the cable (10 m, 3 m, and 1 m) between the driver and the ninth EVM receiver.
- Repeat the series of signal length (Mbps) measurements for each cable length and record the data.
- Remove the jumper wire between the 18th and 19th EVM receivers.
- Insert the 30 m cable connectors into the driver EVM Berg-Stick connectors.
- Insert the 30 m cable connectors into the 18th EVM receiver Berg-Stick connectors.
- Record data from the 18th EVM receiver for each signaling rate (Mbps) Figure 21.
- Shorten the cable (10 m, 3 m, and 1 m) between the driver and the 18th EVM receiver.
- Repeat the series of signal length (Mbps) measurements for each cable length and record the data.
- Remove the jumper wire between the 27th and 28th EVM receivers.
- Insert the 30 m cable connectors into the driver EVM Berg-Stick connectors.
- Insert the 30 m cable connectors into the 27th EVM receiver Berg-Stick connectors.
- Record data from the 27th EVM receiver for each signaling rate (Mbps) Figure 22.
- Shorten the cable (10 m, 3 m, and 1 m) between the driver and the 27th EVM receiver.
- Repeat the series of signal length (Mbps) measurements for each cable length and record the data.

The results of the tests are presented in Figures 20, 21, and 22.

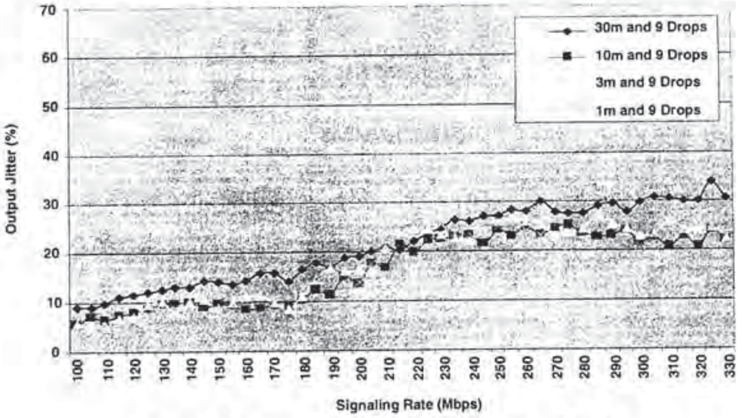

Figure 20. Output Jitter of a Nine Receiver Load Bank

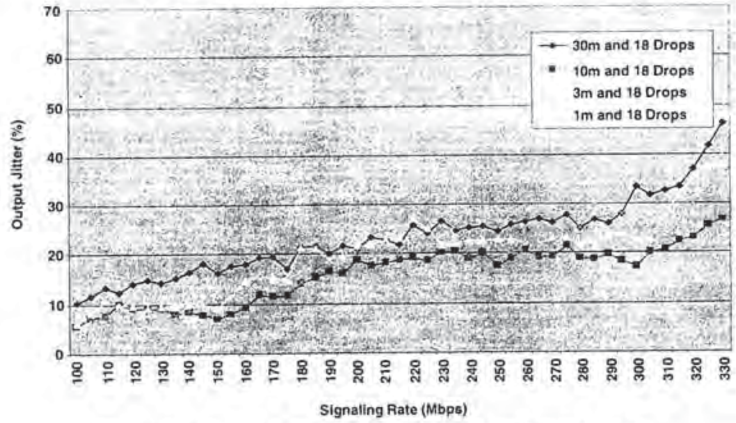

Figure 21. Output Jitter of an Eighteen Receiver Load Bank

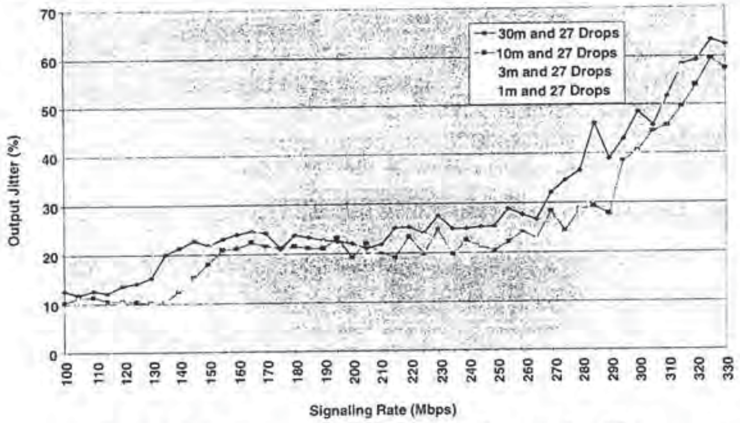

Figure 22. Output Jitter of a Twenty-Seven Receiver Load Bank

Combine the jitter data test results from all three series of tests (Figures 18 through 22). Examine the effect of an increasing number of loads at a fixed cable length Figures 23 through 26.

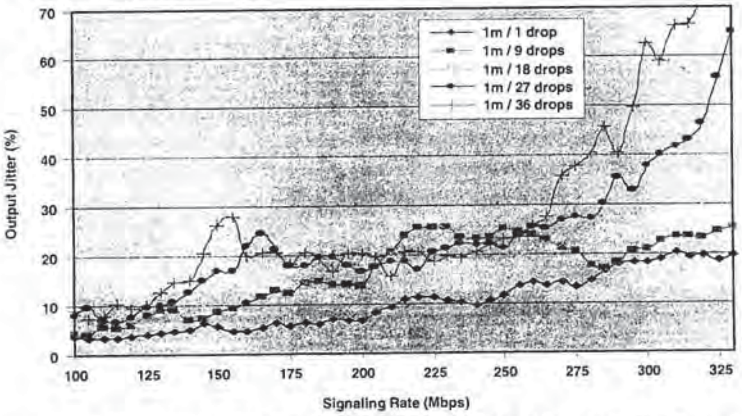

Figure 23. Output Jitter With a 1 m Cable and a Varied Number of Receivers

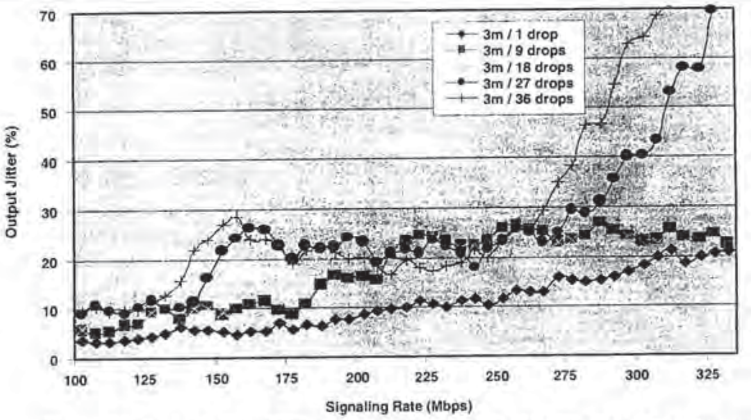

Figure 24. Output Jitter With a 3 m Cable and a Varied Number of Receivers

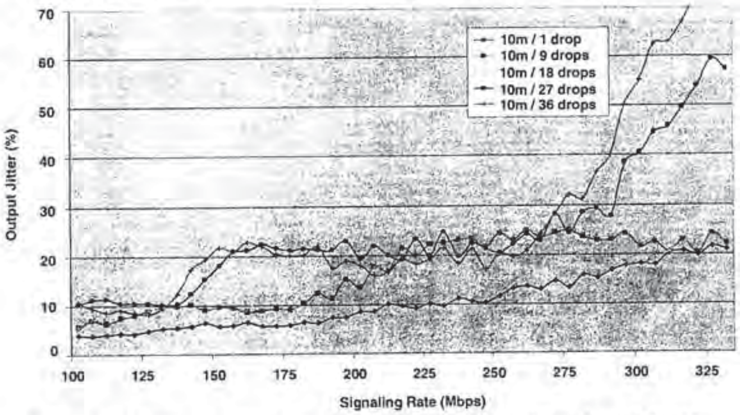

Figure 25. Output Jitter With a 10 m Cable and a Varied Number of Receivers

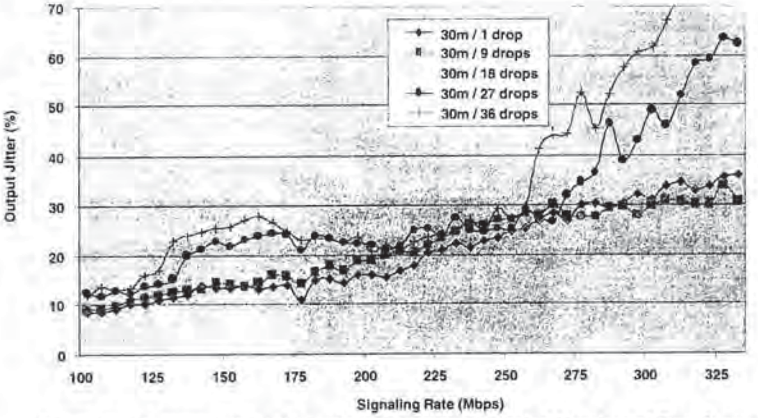

Figure 26. Output Jitter With a 30 m Cable and a Varied Number of Receivers

5.4 Percent Output Jitter From Every Fourth Load

The fourth series of signal length (Mbps) measurements will be taken first between the driver and the first EVM receiver only, then from every fourth EVM receiver in the 36 EVM receiver load bank. The measurements will be performed using a 15,24cm (6″) cable. The HFS-9003 will be adjusted for a signaling rate of 50 Mps, then incremented in 50 Mps steps to 300 Mps, measuring the output jitter at each increment.

- Remove the jumper wires between the first and second EVM receivers.
- Insert the six-inch cable connectors into the driver EVM Berg-Stick connectors.
- Insert the six-inch cable connectors into the first EVM receiver Berg-Stick connectors.
- Adjust the HFS-9003 signaling rate to 50 Mps
- Record data from the first EVM receiver for each signaling rate (Mbps) Figure 27.
- Adjust the HFS-9003 signaling rate in increments of 50 Mps, up to 300 Mps, and measure the output jitter at each increment.
- Connect the jumper wires between the first and second EVM receivers.
- Continue testing every fourth EVM receiver load in the 36 EVM receiver load bank.

The results of the tests are presented in Figure 27.

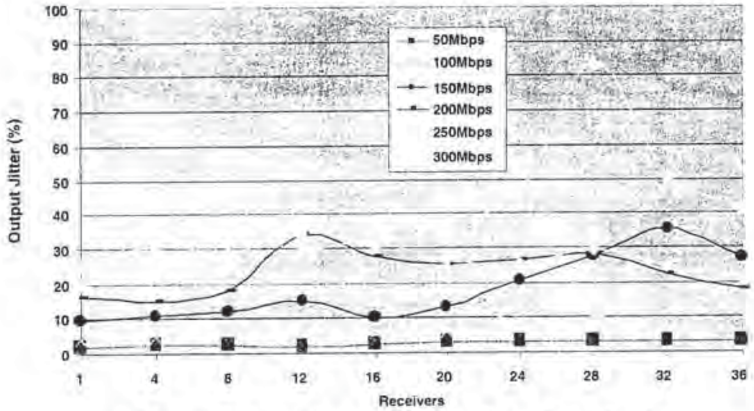

Figure 27. Percent Output Jitter From Every Fourth Load

6 Conclusion

This report provides basic design guidelines and recommendations for determining operating margins, distance between the transmitter and the receivers, and the optimal signaling rates to the number of LVDS receivers.

6.1 Receiver Number vs Cable Length

While the effect of increased cable length is apparent in Figure 18, performance of the shorter length cables (30 m) indicates that load number impacts a system as much as cable length. This is obvious when the multidrop system plots in Figure 18 are compared with the single point system plots in Figure 19. The point at which each plot crosses the 20% jitter line in Figure 20 through Figure 22 clearly demonstrates this increased loading effect.

Not as obvious in Figure 20 through Figure 22 is that the longer cables in these plots appear to both delay and attenuate reflected signals more than the shorter cables. It appears that although cable length increases jitter, length seems to reduce the high and low peaks of the output jitter caused by jumpers and stubs in the load bank. Figure 23 through Figure 26 display this unexpected characteristic with a decrease in the dramatic fluctuations of the 1 m and 3 m plots, on the 10 m and 30 m plots. The longer cables effectively smooth out the minimum and maximum peaking evident in the shorter lengths, however overall performance of the system still degrades rapidly with increased cable length.

Figure 27 illustrates the fact that data taken at the last receiver (EVM #36), does not represent the worst case jitter in the load bank. It appears that the stub lengths and connectors along the load contribute noise and jitter to the system, but the fact that the slope is negative between loads 32 and 36 implies that the termination at the last load attenuates jitter. The positive slope of the first four loads (except at 200 Mbps) indicates that the cable and driver also attenuate system jitter generated along the load bank. These effects are amplified in the higher signaling rates.

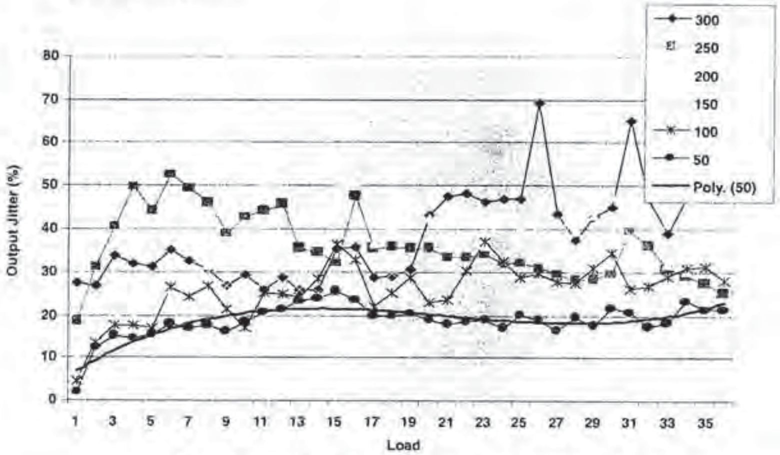

Figure 28. Percent Output Jitter From Each Multidrop Load

An examination of possible attenuation by the transmission cable and driver with a 1 m cable is recorded in Figure 28 as the output jitter from each load. These results again present a positive slope at the beginning of the load bank and a negative slope at the end. While a gradual noise increase is expected with an increase in cable length, clearly this extra noise is being generated by the stub and connectors along the load bank.

It is also apparent that jitter levels shift along the load bank as the signaling rate is changed, establishing a *characteristic wave* of the load bank. The number of loads and the propagation delays introduced by the cables between receivers directly influence this wave, which in the test setup are the 7,62 cm (3″) jumpers between EVMs. Based on these results, measurements of the propagation delay are made across the entire load bank. The fundamental and harmonic signaling rates related to this delay are examined.

A delay of 20.9 ns is measured from the output of the first receiver (#1) to the output of the last receiver (now #35 since the receiver output pins on one of the loads was damaged during the previous test). This 20.9 ns delay equates to a characteristic signaling rate of 47 Mbps (1/21 ns), and a third harmonic of 141 Mbps. If a standing wave is being generated along the load bank, then this wave should shift along the load bank as the signaling rate is changed.

Increasing the signaling rate in quarter-wave increments of 12 Mbps, the next series of tests are performed with an initial signaling rate of the third harmonic. The second test is performed with the signaling rate increased to 155 Mbps, then increased again to 167 Mbps, and finally 179 Mbps. The results are plotted with third order poly nominal trend lines in Figure 29, employed to examine the wave more clearly.

Next, the load bank is reconfigured to approximate the same characteristic wave using half the number of receivers (#19 – #36) and doubling the line length between EVMs from 7,62 cm (3″) to 15,24 cm (6″), using a 1 m cable from the driver to EVM #19. This should create a load bank of 18 receivers with a propagation delay somewhere near the original.

The delay between the output of the first load (#19) and the last load (#36) was 17.2 ns, corresponding to a characteristic rate of 58 Mbps. As done previously, the third harmonic with quarter wavelength increases in the signaling rate are now applied to the driver, with results plotted in Figure 30.

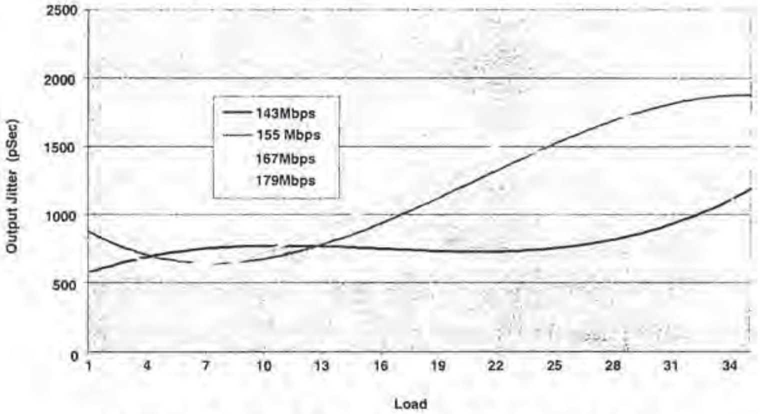

Figure 29. Percent Output Jitter From a 35 Drop 21 ns Load

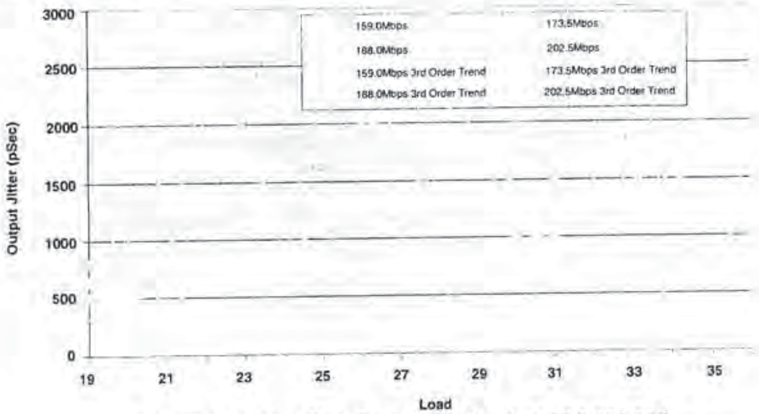

Figure 30. Output Jitter From an 18-Receiver 17.1 ns Load

The wave, generated by reflections from connectors and stubs present on each EVM, shifts along the load bank as a function of the signaling rate. The output jitter of the first load *will* not be the worst case, and the output jitter from the last load *may* not be the worst case in a system.

A closer examination of another source of jitter is made at the termination resistor, across the inputs of the last receiver in the load. As expected, the rise and fall times of the signal are much faster with this 18-receiver load bank than with the 36-receiver load bank. To analyze this apparent signal decay more closely, the short 7,62 cm (3″) jumpers are reinstalled across the 35-receiver loads and a 500 Ω series resistor is added in series with the bank on a short cable from the driver. The 100 Ω termination resistor is removed to effectively measure the time constant of the signal decay.

The HFS-9003 is adjusted for a 1 Vp-p 1 kHz pulse and applied to the driver input. The decay time of the signal is measured across the receiver inputs of the last load; this decay time divided by the 500 Ω resistance results in a total value of 640 pF for the entire bank. This breaks down to just over 18 pF (640/35) for each EVM and jumper, and it increases to 20 pF with the long 15,24 cm (6″) jumpers installed.

Increased capacitance causes slower rise and fall times, therefore the time that edges are within a receiver threshold window increases. With this effect, jitter at the input of a receiver is presented for a longer period of time, then the receiver itself increases this jitter again as a near-linear function of signaling rate (approximately 1 ps of jitter per Mbps).

6.2 Receiver Number vs Signaling Rate

Guidelines for determining the maximum allowable signaling rate that can be used with a particular number of receivers can now be established. It has already been determined that one load (EVM and jumper) adds approximately 1 ns of propagation delay and 20 pF of capacitance. Therefore, a plot of propagation delay (# of loads) versus the signaling rate that results in an output jitter of 15% becomes a practical design tool. More propagation delay measurements are needed to complete this graph.

The next series of measurements made on a 13-receiver load (#24 through #36) with 15,24 cm (6″) jumpers, yields a propagation delay of 12.3 ns. Based on the previous results, signaling rates approximately twice the fundamental period, result in jitter levels near 15%, signaling rates of 162 Mbps (2 × 1/12.3 ns) and 142.5 Mbps (1.75 × 1/21.3 ns) for the quarter wavelength shift are used with results plotted in Figure 31.

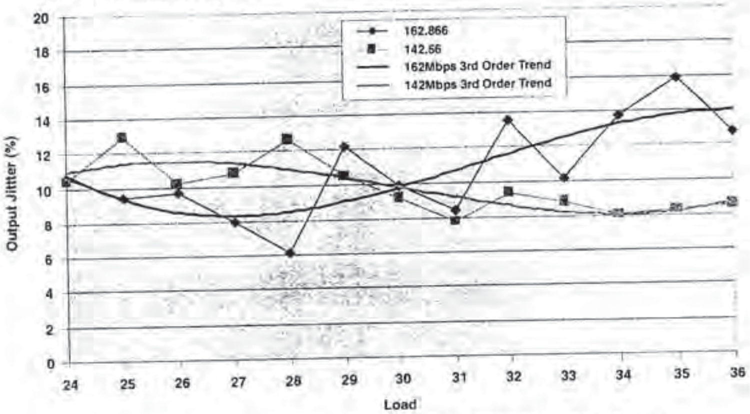

Figure 31. Output Jitter From an 13-Receiver 12.3 ns Load

The 2x signaling rate yields a peak jitter of 16%. The load bank is increased to 15 receivers and a 14.3 ns load delay is measured. Signaling rates of 140 Mbps (2 × 1/14.3 ns), 157 Mbps (2.24 × 1/14.3 ns), and 175 Mbps (2.5 × 1/14.3 ns) will be used for this test. The resulting 2.25x quarter-wave shifted rate of 157 Mbps nearly reaching the 15% jitter mark is shown in Figure 32.

Figure 32. Output Jitter From an 15-Receiver 14.3 ns Load

Remove four jumpers from the load bank to create an 11-drop, 10.4 ns load. When the value of the 2x (2 × 1/10.4 ns = 192 Mbps) was recorded, the results were already above 15% jitter. Tests were then made with *1.75x* (168 Mbps) and *1.5x* (149Mbps) signaling rates. The results are shown in Figure 33.

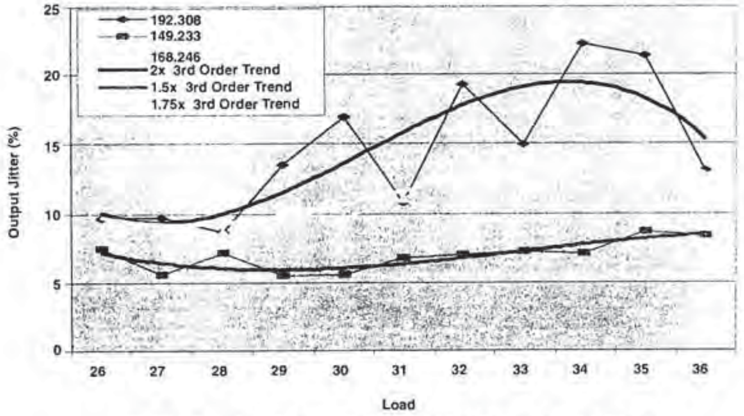

Figure 33. Output Jitter From an 11-Receiver 10.4 ns Load

Tests are repeated with loads of 30, 11, 6, and 3 receivers, and the measurements are combined with earlier results for the plot in Figure 32. The graph confirms expectations of a linear relationship between propagation delay and a 15% jitter signaling rate. (This graph could be titled *Load Capacitance vs Signaling Rate.)*

The data in Figure 34 may be useful in multidrop system development, if the same constraints utilized in the test setup are maintained. Stub lengths are 4 cm or less and the single drop capacitance is approximately 20 pF if the 15,24 cm (6″) cable length between loads is used. The transmission cable from the driver to the receiver bank is 1 m, however, this can be relaxed up to 10 m since there is very little performance difference in cables from 1 m to 10 m length (Figures 18 through 22).

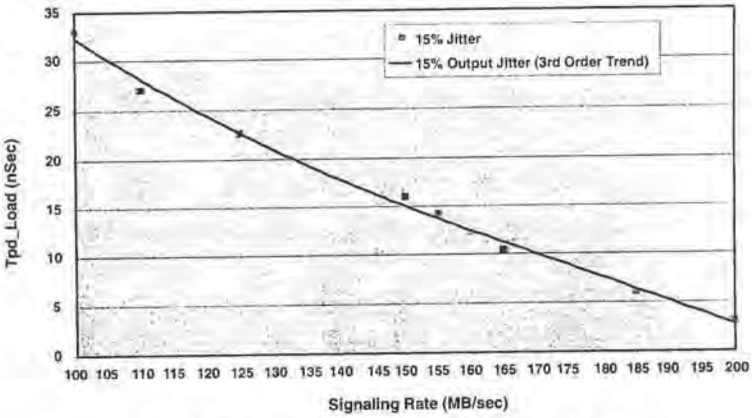

Figure 34. Load Propagation Delay vs Signaling Rate

6.3 Receiver Number vs Common Mode Voltage Range

Earlier this report mentions that the common mode output current (Ioc) of an LVDS receiver is not specified in the LVDS standard, and that as a result the ground potential difference voltage, (Vgpd) may be affected as receivers are added to the output of a single driver. Testing for this condition, a third power supply (Tekronix Model PS280) is added to the test setup for monitoring any change in Vgpd. The positive lead of the power supply is connected to the ground of the LVDS31 line driver's V_{CC} supply, and the negative lead is connected to the ground of the load bank's V_{CC} supply. With all jumpers removed from the load bank, the cable from the driver is then attached to load #36, a single receiver. The signaling rate on the HFS-9003 is set to 100 Mbps, and the output of the receiver is monitored while this common mode voltage is gradually increased.

The test is repeated with the addition of each load until all 36 receivers are connected to the single driver, then the polarity connections on the PS280 power supply are reversed and the tests repeated.

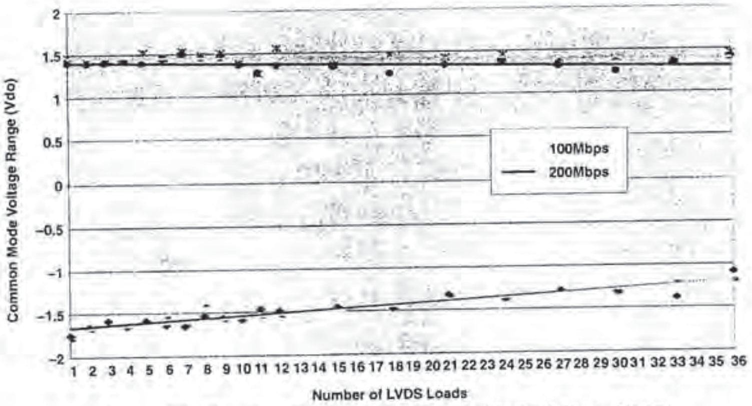

Figure 35. Receiver Number vs Common Mode Voltage Range

The results presented in Figure 35 confirm that common mode voltage is impacted by signaling rate. This is due to the gain roll off of the receiver, and is documented and reported in several point-to-point applications. Also evident in Figure 35 is the increased common mode loading of the receivers linearly loading the 1.2 V common mode voltage source of the driver, as predicted earlier in the common mode model discussion.

Clearly the common mode voltage range decreases as additional receivers are added to the output of a single LVDS driver, and as the signaling rate increases.

7 References

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Appendix A Glossary

Signaling Rate: 1/T, where T is the time allocated for one data bit. Therefore, in a transmission system with a 400 Mbps signaling rate, the width of one data bit is 2.5 ns. LVDS, as standardized in TIA/EIA-644, specifies a maximum signaling rate of 655 Mbps, where one bit has a duration of 1.5267 ns. In practice, a maximum signaling rate is determined by the quality of interconnection between line drivers and receivers, since transmission line length and line characteristics ultimately determine the maximum unusable signaling rate. However, the TIA/EIA-644 standard deals with the electrical characteristics of data interchange only, therefore mechanical specifications, bus structure, protocol, and timing are left to the referencing standard.

Data Rate: The number of data bits per second transmitted from driver to receiver. There are nondata bits, such as start bits, stop bits, parity bits, etc., used by many systems, but they are not, strictly speaking, actual data bits. If a transmission system is unformatted, and only data bits are transmitted, then the data rate is equal to the signaling rate.

Jitter: The time frame during which the logic state transition of a signal occurs. The jitter may be given either as an absolute number or as a percentage with reference to the time unit interval (UI). This UI or *bit length* equals the reciprocal value of the signaling rate, and the time during which a logic state is valid is just the UI minus the jitter. Percent jitter (the jitter time divided by the UI times 100) is more commonly used and represents the portion of UI during which a logic state should be considered indeterminate.

Eye-Pattern: A useful tool for measuring overall signal quality at the end of a transmission line. It includes all of the effects of systemic and random distortion, and displays the time during which the signal may be considered valid. A typical eye-pattern is illustrated in Figure 12 with its significant attributes identified.

Several characteristics of an eye-pattern indicate the signal quality of a transmission circuit. The height or *opening* of the eye above or below the receiver threshold level at the sampling instant is the noise margin of the system. The spread of the transitions across the receiver thresholds measures the peak-to-peak jitter of the data signal. The signal rise and fall times can be measured relative to the 0% and 100% levels provided by the series of low and high levels.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
09/555,168	09/05/00	GUTA	A	X-784 US

MM91/0910

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EXAMINER	
CHANG D	
ART UNIT	PAPER NUMBER
2819	

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09/10/01

3/a

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Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)

1- File Copy

Notice of Allowability	**Application No.** 09/655,168	**Applicant(s)** GHIA ET AL.	
	Examiner Daniel D. Chang	**Art Unit** 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Application filed 9/5/00*.
2. ☒ The allowed claim(s) is/are *1-23*.
3. ☒ The drawings filed on *05 September 2000* are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☐ CORRECTED DRAWINGS must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☒ Notice of References Cited (PTO-892)
3☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
5☒ Information Disclosure Statements (PTO-1449), Paper No. *2*.
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
2☐ Notice of Informal Patent Application (PTO-152)
4☐ Interview Summary (PTO-413), Paper No.____.
6☒ Examiner's Amendment/Comment
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other

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/9

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Ms. Edel Young on September 4, 2001.

The application has been amended as follows:

IN SPECIFICATION:

On page 9, lines 26, "??? HOW SO??????" has been deleted.

IN CLAIMS:

In Claim 10, line 17, the recitation, "high-side" has been deleted and replaced by --low-side--.

In Claim 15, line 1, the number, "13" has been deleted and replaced by --14--.

Reasons for Allowance

Claims 1-23 are allowed.

The following is an examiner's statement of reasons for allowance:

No prior art has been found to meet the limitations of claims 1-23. The prior art of record does not teach or fairly suggest a differential amplifier or a programmable logic device which comprises the following:

With respect to claim 1, in addition to other limitations in the claim, the prior art does not show two differential-amplifier stages, each having two differential input terminals and two differential output terminals and the second amplifier stage having an enable terminal, their interconnections, and a programmable memory cell connected to the enable terminal, wherein the second differential amplifier stage amplifies the input signal when the memory cell is in the programmed state and does not amplify the input signal when the memory cell is in the deprogrammed state, as set forth in the claim.

With respect to claim 10, in addition to other limitations in the claim, the prior art does not show first high and low side differential amplifiers, second high and low side differential amplifiers, a delay element, and their interconnections, as set forth in the claim.

With respect to claim 20, in addition to other limitations in the claim, the prior art does not show a pre-driver having complementary output terminals, first and second programmable output blocks, each having a differential amplifier, I/O pins, and their interconnections, as set forth in the claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Daniel D. Chang* whose telephone number is (703)306-4549.

The examiner can normally be reached between the hours of 6:30 AM to 4:00 PM Monday through Thursday and every other Friday (first Friday of the bi-week).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Daniel D. Chang
Patent Examiner, Art Unit 2819
September 4, 2001

Michael J. Tokar

	Type	Hits	Search Text	DBs
1	BRS	198	(differential adj amplifier) and (programmable adj memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
2	BRS	19	((differential adj amplifier) and (programmable adj memory)) and (326/$7.ccls. or 327/$7.ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
3	BRS	11556	(differential adj amplifier) and memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
4	BRS	2252	((differential adj amplifier) and memory) and programmable	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
5	BRS	252	(((differential adj amplifier) and memory) and programmable) and (326/$7.ccls. or 327/$7.ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
6	BRS	229	326/30.ccls. and differential	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB

Notice of References Cited	Application/Control No. 09/655,168	Applicant(s)/Patent Under Reexamination GHIA ET AL.	
	Examiner Daniel D. Chang	Art Unit 2819	Page 1 of 1

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*	A	US-5355035	10-1994	Vora et al.	327	433
*	B	US-5812461	09-1998	Komarek et al.	365	189.05
	C	US-				
	D	US-				
	E	US-				
	F	US-				
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification	
*	N	JP60260254	06-1987	JP	Taniguchi et al.	326	30
	O						
	P						
	Q						
	R						
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	T						

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office
PTO-892 (Rev. 01-2001) **Notice of References Cited** Part of Paper No. 3

US005355035A

United States Patent [19]

Vora et al.

[11] **Patent Number: 5,355,035**

[45] **Date of Patent: Oct. 11, 1994**

[54] **HIGH SPEED BICMOS SWITCHES AND MULTIPLEXERS**

[76] Inventors: **Madhukar B. Vora,** 110 Lansberry Ct., Los Gatos, Calif. 95032; **Burnell G. West,** 46750 Sentinel Dr., Freemont, Calif. 94539

[21] Appl. No.: **2,172**

[22] Filed: **Jan. 8, 1993**

[51] **Int. Cl.**^{5} **G06G 7/12;** H03K 17/56

[52] **U.S. Cl.** **307/494;** 307/495; 307/243; 307/355; 328/104; 328/154

[58] **Field of Search** 307/494, 495, 241, 242, 307/243, 355; 328/104, 154; 330/261, 252

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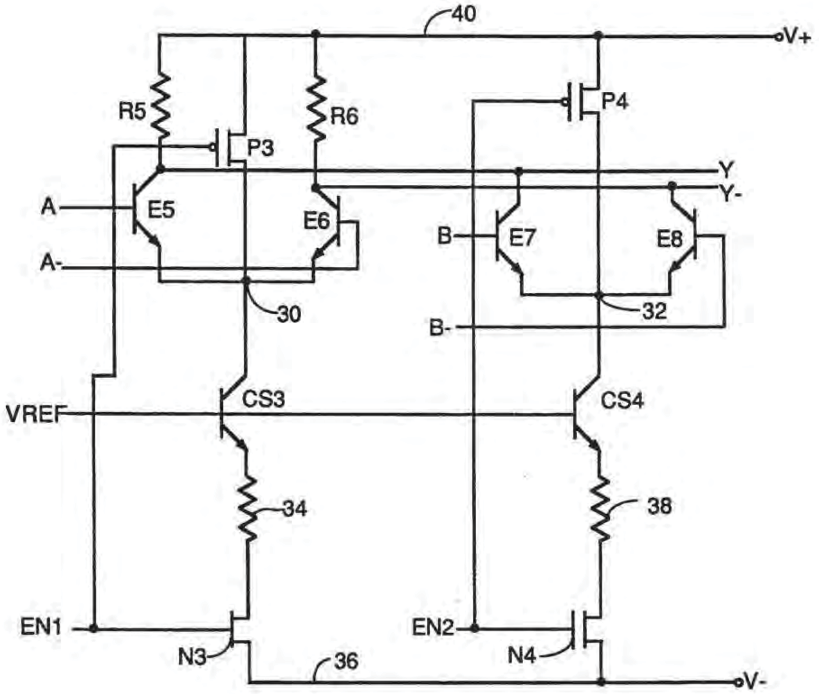
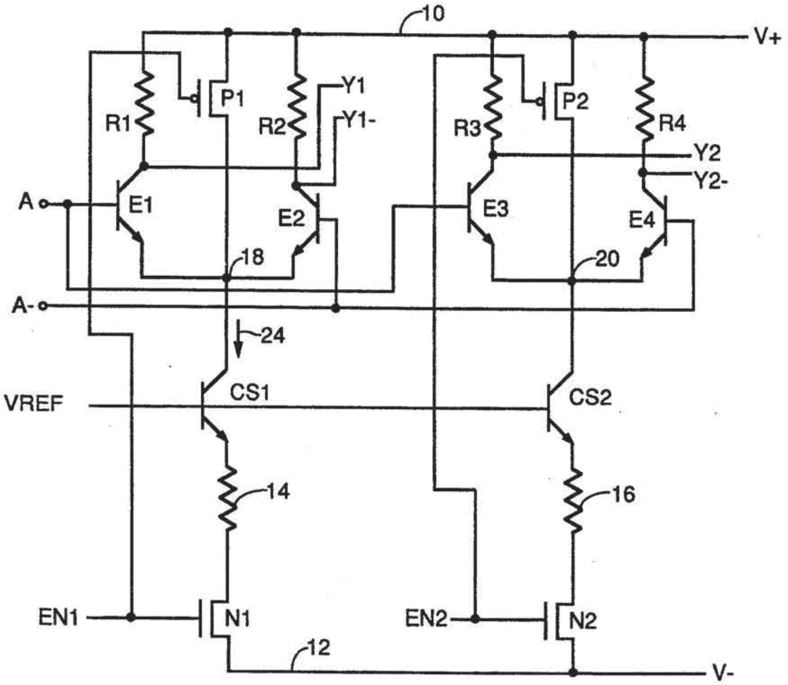
Primary Examiner—Timothy P. Callahan
Assistant Examiner—Toan Tran
Attorney, Agent, or Firm—Ronald Craig Fish

[57] **ABSTRACT**

A high speed switching technology suitable for implementing field programmable gate arrays using current mode logic in the high speed data path, and CMOS steering logic outside the high speed data path to enable the high speed switching logic and to implement multiplexer, selector and crossbar switch functions. High speed emitter follower logic compatible with the high speed switching logic for level shifting, buffering, and providing more current sink or source capacity is also disclosed.

6 Claims, 4 Drawing Sheets




10
V+
P1
Y1
R1
R2
Y1-
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R3
R4
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Y2-
A
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E3
E4
18
20
A-
24
VREF
CS1
CS2
14
16
EN1
N1
EN2
N2
12
V-

FIG. 1

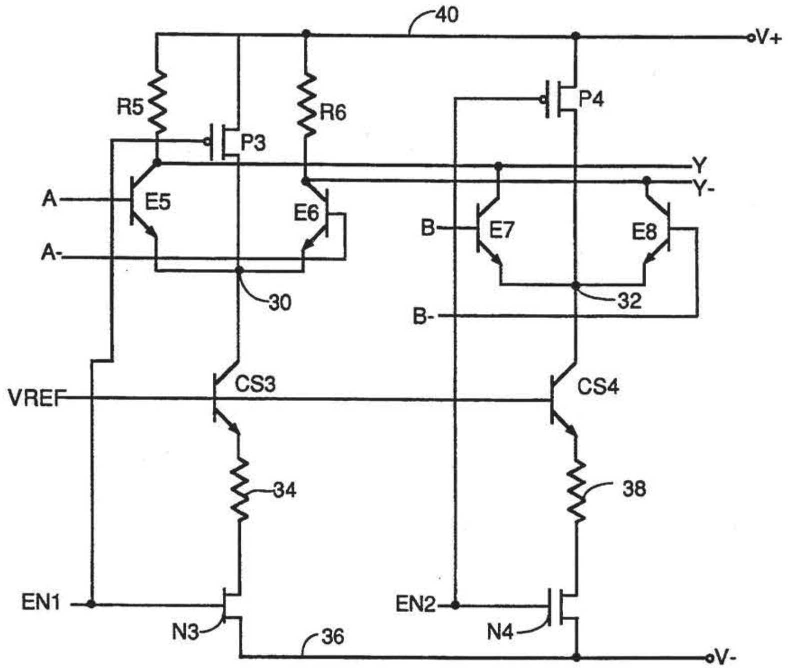
40
V+
R5
R6
P3
P4
Y
Y-
A
E5
E6
A-
B
E7
E8
30
32
B-
VREF
CS3
CS4
34
38
EN1
EN2
N3
N4
36
V-

FIG. 2

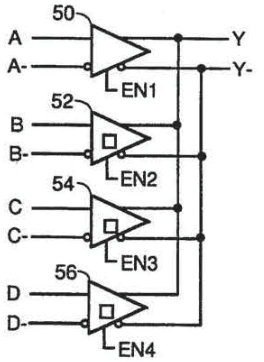

FIG. 3

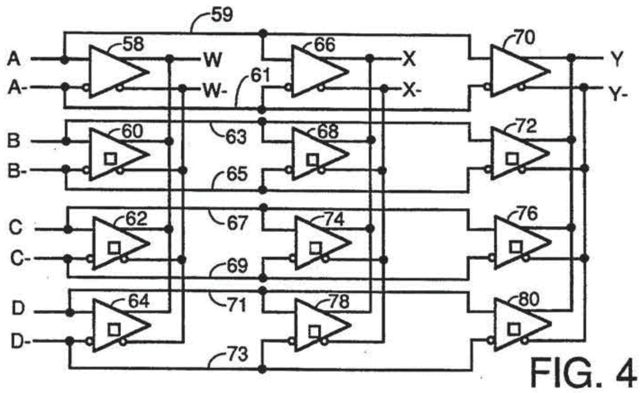

FIG. 4

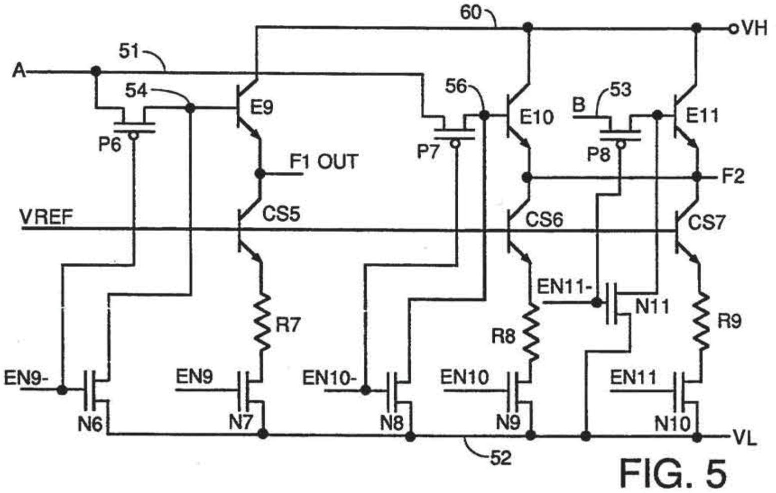

FIG. 5

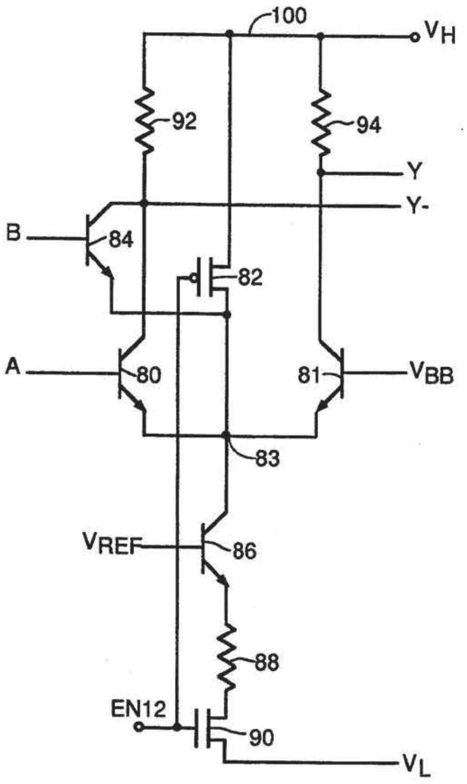

FIG. 6

HIGH SPEED BICMOS SWITCHES AND MULTIPLEXERS

BACKGROUND OF THE INVENTION

The invention pertains to the field of custom circuits, and, more particularly, to the field of components and cells from which field reprogrammable logic circuits may be constructed and field programmable logic circuits themselves.

Logic designers have long had the need for custom logic circuits to implement their designs. In the 1970's, this need gave rise to programmable logic arrays, programmable array logic and programmable read only memory. Later in the decade, custom circuits were made by customizing the metal layer of integrated circuits which had standard cells formed in the layers below the metal layer. The customized metal layer interconnected the standard cells in a manner defined by the customer of the gate array manufacturer.

Gate arrays are only a good choice where the desired function to be performed by the gate array can be determined with certainty in advance. However, gate arrays are not a good choice where the desired function can change over time with changing requirements. This can happen when a circuit design is being evaluated and testing over time reveals the need for changes in the design. Another shortcoming of gate arrays was that they could not perform the function of packet encapsulation and delivery in network settings where packet construction was subject to a variety of different protocols and where packet headers change as the packets circulate, for example in token ring networks. This function has been done in software in the prior art, but increasing network speeds demands more speed which requires that this function be done in hardware.

Another application in which fixed gate arrays had shortcomings in where data flow paths change over time as a function of changes in the process that is being emulated by a particular circuit. Thus, a need arose for more flexibility in custom circuits such that the functions thereof can be changed.

Reprogrammable gate arrays, also called field programmable gate arrays or FPGAs, were developed in response to this need. However, these gate arrays were implemented in CMOS technology. Although CMOS has significant advantages such as low power, high circuit density, good reliability and low cost, CMOS is not fast enough for very high speed custom circuits needed in applications such as supercomputers, communication systems, high speed workstations, networks, automatic test equipment, parallel processor interconnects and design emulation systems. In very fast applications such as these, having any MOS device in the signal path seriously impedes the switching speed and impairs the performance of the machine. This is because the resistivity of CMOS and MOS devices is too high, and this coupled with the junction capacitances and other capacitances intrinsic to MOS devices causes delays.

Accordingly, the need has arisen for a much faster technology that can be substituted for field programmable gate array circuits in extremely high speed applications.

SUMMARY OF THE INVENTION

According to the teachings of the invention, reprogrammable logic circuitry is implemented with multiplexer cells using high speed devices such as ECL circuitry in the data path with CMOS devices doing the function of steering the high speed signals in the data path to one or more of the high speed devices. In other words, the CMOS devices are generally kept out of the data path and only are used to program the selection of which input signals are coupled to which outputs through the high speed devices. In the preferred embodiment, the high speed devices are ECL technology devices, but in other embodiments, they may be bipolar devices or any other high speed technology.

In one embodiment of the invention, a high speed selector is implemented in differential current mode logic with CMOS steering transistors to enable the high speed switching transistors with the CMOS devices out of the high speed data path. This embodiment uses a pair of differentially coupled ECL transistors for each of a plurality of output pairs of high speed, complementary data output signals. Each of these pairs of ECL switching transistors have bases which are coupled to a shared pair of inputs for receiving a pair of high speed, complementary data inputs. Each of these pairs of ECL switching transistors also shares a common emitter node coupled selectively to the low voltage supply by a constant current source and an NMOS transistor which is part of the enabling mechanism. This enabling transistor is out of the high speed data path, and receives a steering signal which in one state turns the NMOS transistor and couples the constant current source to the low voltage supply thereby enabling the switching transistors. The other state of the steering signal turns the NMOS transistor off thereby disconnecting the constant current source from the low voltage supply and disabling the switching transistors. The other part of the enabling mechanism is a PMOS transistor which is coupled to the steering signal and selectively couples the common emitter node to the high voltage supply. When the NMOS transistor is on, the PMOS transistor is off thereby allowing the ECL transistors to operate in differential mode. When the NMOS transistor is off, the PMOS transistor is on and lifts the common emitter node to the voltage of the high voltage supply thereby turning the ECL transistors off by reverse biasing their base-emitter junctions.

In another embodiment of the teachings of the invention, a multiple-input, single-output multiplexer is disclosed. The basic ECL switching cell used in this multiplexer is the same except that one differentially coupled ECL pair is coupled to one pair of high speed data inputs and the shared pair of high speed differential outputs, and is coupled to the high voltage supply through a pair of pull up resistors. All other differential pairs coupled to high speed data input pairs are coupled to the same shared pair of high speed data outputs and share the single set of pullup resistors. Each differential pair of ECL transistors has its own constant current source and its own enabling circuitry and has a dedicated steering signal coupled to the corresponding enabling circuit. The enabling circuitry is identical to the enabling circuitry described for the selector and works the same way and has the same attributes.

In another embodiment of the invention a multiple-input, multiple-output crossbar switch can be implemented using the multiple-input, single-output multiplexer described above. In this embodiment, a first series of high speed data input pairs are coupled to a series of differentially coupled ECL switches linked together to share a common high speed data output pair in the manner just described for the multiplexer. Another series of high speed, differentially coupled ECL switches coupled together so as to share a second high speed, complementary data output pair which is common only to this second series of ECL switch pairs as described above for the multiplexer structure is then coupled so as to share the same high speed, complementary data inputs used by the first series of differentially coupled ECL switches. This structure can be repeated for a large number of series of such multiplexers sharing the same input signals to extend the number of outputs in the crossbar switch, the upper limit being more a function of how much degradation of the switching speed is tolerable under the circumstances. This switching speed degradation is a function of the number of ECL switching pairs which load each high speed data input.

Another embodiment according to the teachings of the invention is a high speed emitter follower structure which can be used in conjunction with the foregoing structures for level shifting, output buffering, increasing the output current source or sink capacity or in a stand-alone mode to implement another form of a cross-bar switch. In this embodiment, a bipolar transistor such as an ECL device is coupled as an emitter follower to a constant current source. The high speed data input is selectively coupled to the base of the emitter follower through a PMOS transistor which is part of the enabling circuitry. The constant current source is coupled to the low voltage supply selectively through an NMOS transistor which also is part of the enabling circuitry. Another NMOS transistor selectively couples the base of the emitter follower transistor to the low voltage supply. Multiple structures or "cells" like the structure just described can be used, with each such cell being coupled to one high speed data input and one high speed data output. Each cell receives two complementary steering signals which enable or disable it. When the steering signals are in a state to enable the cell, the first NMOS transistor coupled to the first steering signal couples the constant current source to the low voltage supply, and the second NMOS transistor coupled to the second steering signal decouples the base of the emitter follower from the low voltage supply. The PMOS transistor in the enabling circuitry coupled to the second steering signal, then couples the high speed data input to the base of the emitter follower. In the second, complementary state of the steering signals, the base of the emitter follower is decoupled from the high speed data input and coupled to the low voltage supply to reverse bias the base-emitter junction. Simultaneously, the constant current source is decoupled from the low voltage supply thereby disabling the emitter follower further. Multiple such cells coupled to multiple inputs and outputs can be used to implement selectors, multiplexers or crossbar switches.

The structures just described can also be implemented using single ended ECL logic, non-current mode bipolar logic or other types of high speed technologies wherein the enabling circuitry that provides field programmability can be implemented in CMOS or other switching technologies which, although slower, can be kept out of the data path. Generally, current mode logic is preferred for the switching technology because of its speed, and CMOS technology is preferred for the enabling switches because of its small size and low power consumption. Low power consumption is important especially in integrated ECL switching embodiments, because the ECL transistors dissipate large amounts of power, and this power must be dissipated which can be a problem for highly dense integrated structures. If the power is not properly dissipated and the temperature of the chip kept under control, thermal runaway problems and temperature compensation problems become a factor to be dealt with thereby complicating the design and increasing the expense and complexity thereof. Further, yield for integrated circuit production decreases when die size is increased which occurs when either more transistors are added or when the same number of transistors are implemented in technologies which are larger per transistor in terms of chip real estate consumed. Since every ECL pair and every emitter follower needs two or more enabling transistors, effectively doubling or tripling the density per switching function, it is especially useful to implement the enabling function in CMOS so as to not aggravate the power dissipation problem. Further, since MOS transistors are smaller than corresponding bipolar transistors, implementing the enabling function in CMOS uses less area and allows more switching functions to be put on the same die or allows the same number of switching functions to be put on a smaller die. Therefore, the characteristics of ECL and CMOS technologies are preferred when the circuits according to the teachings of the invention are to be fabricated as integrated circuits.

However, where chip real estate, switching speed or power consumption are not issues, bipolar or other switching enabling technology can be used to enable the switches in the high speed data path. Also, other types of architectures or other slower, cheaper, smaller or otherwise different technologies may be used for the switches in the high speed data path.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a circuit diagram of the preferred embodiment of multiplexer according to the teachings of the invention.

FIG. **2** is a circuit diagram for a multiple-input, single-output multiplexer according to one aspect of the teachings of the invention.

FIG. **3** is a circuit diagram of another notation for the multiplexer of FIG. **2** having four inputs and a single output.

FIG. **4** is a circuit diagram for a crossbar switch having four inputs and three outputs using the notation of FIG. **3**.

FIG. **5** is a circuit diagram of a typical set of high speed emitter followers for use with the circuits of FIGS. **1–4** or as a stand-alone, field-programmable switching array.

FIG. **6** is a circuit diagram of one example of how the structures of FIGS. **1–4** can be implemented in single ended ECL technology.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. **1**, there is shown a circuit diagram for a one-input-two-output multiplexer according to the teachings of the invention suitable for use in implementing programmable logic circuitry. In the embodiment shown in FIG. **1**, emitter-coupled-logic (ECL) circuitry is used in the data path, and CMOS circuitry is used for steering the input signals from the inputs to one or more of the outputs. In other embodiments, other fast technologies may be used in the data path such as bipolar, Josephson junction, ballistic effect devices etc. The data inputs for high speed data are shown at A and A-. These two inputs are coupled to two ECL differential pairs comprised of a first pair of transistors **E1** and E2 and a second pair of transistors E3 and E4. Transistors E1 and E2 have load resistors R1 and R2, respectively. Transistors E3 and E4 have load resistors R3 and R4, respectively. The first data input A is coupled to the bases of ECL transistors E1 and E3. The complementary data input A- is coupled to the bases of ECL transistors E2 and E4. The collectors of the E1 and E2 pair are coupled to the Y1 and Y1- outputs, respectively. The collectors of the E3 and E4 pair are coupled to the Y2 and Y2- outputs, respectively. Each of the ECL transistors is coupled to the high voltage supply rail **10** via a collector load resistor where R1 is the load resistor for transistor E1 and R4 is the load resistor for E4 etc.

The emitters of transistors E1 and E2 are coupled so as to share a common constant emitter current regulated by current source transistor CS1, and the emitters of transistors E3 and E4 are coupled so as to share a common constant emitter current regulated by current source transistor CS2. The bases of these two current source transistors are coupled to a reference voltage VREF, and the emitters are coupled to the low voltage supply **12** through emitter feedback resistors **14** and **16** and through NMOS steering transistors N1 and N2. The gate terminals of transistors N1 and N2 are coupled to enable signal lines EN1 and EN2, respectively. These two enable signal lines are also coupled to two PMOS steering transistors P1 and P2, respectively, which are coupled between the high voltage supply **10** and the common emitter nodes **18** and **20**.

The operation of the circuit **1** is as follows. The fundamental purpose of the circuit is to steer the signals in the data path on complementary signal lines A and A- onto one or both of the complementary output signal pairs Y1/Y1- or Y2/Y2- to implement a one-input-two-output multiplexer. This is done using the EN1 and EN2 enable or steering signals and the CMOS steering transistor pairs N1/P1 and N2/P2 outside the data path. Those skilled in the art will appreciate that the concept illustrated in the circuit of FIG. **1** can be extended to more outputs than two and can be reversed to steer input signals on one of a plurality of inputs onto a single output.

Assuming now for illustration that the EN1 enable signal is active, i.e., high. This causes the steering transistor N1 to conduct thereby connecting the steering transistor N1 to the low voltage power supply and causes the steering transistor P1 to be nonconductive. This has the effect of activating the output pair Y1 and Y1- by enabling the current source CS1 to draw the fixed current represented by arrow **24** out of node **18**. Current source transistor CS1 stabilizes the current flow out of node **24** by virtue of the negative feedback to the emitter caused by emitter resistor **14** as is well-known in the art. Because transistor P1 is nonconductive, the common emitter node **18** is not held at the voltage of the high voltage supply **10**, and the ECL transistors E1 and E2 are free to drive the outputs Y1 and Y1- as an ordinary current mode logic buffer/inverter under the influence of whatever data signals are present on the data inputs A and A- as in normal ECL differential mode operation. If the EN2 steering signal is not active, i.e., low, simultaneously with the active high state of the EN1 steering signal, the Y2 and Y2- outputs are deactivated. This results from the fact that the steering transistor N2 is not conductive thereby disabling the current source transistor CS2 from drawing current from common emitter node **20**. When steering signal EN2 is low, the PMOS steering transistor P2 is conductive thereby driving the common emitter node **20** to the voltage of the high voltage source **10**. This affirmatively reverse biases the base-emitter junctions of the ECL transistors E3 and E4 rather than leaving the common emitter node **20** floating so as to positively cut off the E3 and E4 transistors and prevent any signal leakage from the inputs A and A- to the outputs Y2 and Y2.

In some embodiments where this positive cutoff of the ECL transistors of the pair associated with whatever steering signal EN1 or EN2 is low, is not necessary and a floating common emitter node **18** or **20** provide adequate isolation between the input and output when the associated current source is not active, the PMOS transistors P1 and P2 can be eliminated.

If the enable signal EN2 is high, the NMOS steering transistor N2 is conductive and the PMOS steering transistor P2 is rendered nonconductive. This has the effect of activating the two outputs Y2 and Y2- by connecting the current source transistor CS2 to the low voltage supply thereby causing the transistors E3 and E4 to drive the outputs Y2 and Y2- in accordance with whatever data signals are on the A and A-data inputs. This is true regardless of whether steering signal EN1 is simultaneously active high. If EN1 is simultaneously low when EN2 is high, steering transistor N1 is nonconductive and steering transistor P1 is conductive. This drives common emitter node **18** to the voltage of the high voltage rail and reverse biases the emitter-base junctions of the ECL transistors E1 and E2 thereby isolating the inputs A and A- from the outputs Y1 and Y1-.

By controlling which of steering signals EN1 and/or EN2 are high, it is possible to connect the input signal pair A, A- to either or both of the output signal pairs Y1, Y1- or Y2, Y2-. Thus, by control of the states of signals EN1 and EN2, it is possible to electronically control the switching of very high speed signals at an input to any of a plurality of outputs without substantially slowing down the signals even though CMOS steering transistors are used. Because the resistivity of the NMOS steering transistors N1 and N2 is much lower than the resistance of the emitter feedback resistors **14** and **16**, the presence of the NMOS transistors N1 and N2 in the path between the emitters of the current source transistors CS1 and CS2 to the low voltage rail does not appreciably affect the speed of operation of the circuit.

The structure of FIG. **1** can be extended to more ECL differential pairs driving more output pairs, but there is a limit imposed by the loading on the input signal lines A and A- caused by the junction capacitances of the ECL transistor bases. Also, since the beta factor of the ECL pairs is not infinite, adding more ECL pairs causes the base current to exceed accepted ECL limits of no more than 10–20 bases coupled to one signal. The preferred limit of the number of bases which can be coupled to input signal lines A and A- is from 4 to 8. It is preferable for the load on A and A- signal lines to not be dependent upon the number of transistors connected thereto.

Referring to FIG. **2**, there is shown a circuit diagram for a two-input-single-output multiplexer circuit according to the teachings of the invention. A first ECL transistor pair **E5** and **E6** share a common emitter node **30**, while a second ECL transistor pair **E7** and **E8** share a common emitter node **32**. Common emitter node **30** is coupled to a constant current source comprised of transistor **CS3** and emitter feedback resistor **34**. This constant current source is turned off and on by an NMOS steering transistor **N3** which couples the current source to the low voltage supply line **36**. The transistor pair **E5** and **E6** each have a load resistor, **R5** and **R6**, respectively, which is shared with a second ECL transistor pair **E7** and **E8** via a pair of single output lines Y and Y-. The second transistor pair **E7** and **E8** share emitter node **32** and share a constant current source comprised of transistor **CS4** and emitter feedback resistor **38**. The **CS4** constant current source is selectively coupled to the low voltage supply rail **36** by an NMOS steering transistor **N4**. As in the case of the embodiment of FIG. **1**, two PMOS steering transistors **P3** and **P4** are used to positively control the voltage of common emitter nodes **30** and **32**, respectively.

The first ECL transistor pair **E5** and **E6** is enabled when the enabling signal **EN1** is high. This condition turns the NMOS transistor **N3** on and couples the current source transistor **CS3** to the low voltage supply **36**. The transistors **E5** and **E6** are coupled to a high voltage supply line **40** through their respective load resistors **R5** and **R6**. When **EN1** is high, PMOS transistor **P3** is off which releases the common emitter node **30**. Thus, transistors **E5** and **E6** are enabled to drive the output lines Y and Y- under the influence of whatever signals are on the high speed input signal lines A and A-. Note that if **EN1** is high, care must be taken to insure that **EN2** is not simultaneously high as this would cause a conflict in that ECL pair **E7** and **E8** would be simultaneously trying to drive the output lines Y and Y- at the same time transistors **E5** and **E6** were trying to drive the same lines, possibly with conflicting signal levels. This conflict is avoided if the steering signal **EN2** is low when steering signal **EN1** is high, because a low **EN2** causes PMOS transistor **P4** to be turned on which drives the shared emitter node **32** to the voltage of the high voltage supply line **40**. This disables **E7** and **E8** by reverse biasing the emitter-base junctions thereof. Likewise, when **EN1** is low, transistors **E5** and **E6** are disabled in the same way.

In alternative embodiments of the circuit of FIG. **2**, interlock circuitry is employed to prevent both **EN1** and **EN2** from being active high simultaneously. Also, in some embodiments, the PMOS transistors **P3** and **P4** can be omitted where leaving the shared emitter node floating is an acceptable way of disabling the ECL transistor pairs. The multiple input, single output arrangement of FIG. **2** can be extended to many different input pairs driving many different ECL pairs sharing a single output pair, as will be apparent to those skilled in the art. If such a circuit were to be implemented as an integrated circuit, all transistors whose collectors are connected to the same output line could share the same collector tub on the integrated circuit die thereby creating vast savings in layout area. Thus, for example, four separate input pairs could drive four ECL transistor pairs sharing a single output pair and a single pair of load (pull up) resistors. The four transistors coupled to one output line of the output pair would share the same collector tub and likewise for the four transistors coupled to the other output line. At most one of the four ECL pairs would be enabled by its corresponding steering signal while all other steering signals would be inactive.

Such an embodiment is shown symbolically in FIG. **3**. In the notation used in FIG. **3**, ECL pair **E5** and **E6** with pull up resistors **R5** and **R6** and their associated current sources and MOS steering transistors are represented by switch **50** while ECL pairs without pullup resistors such as transistors **E7** and **E8** and their associated current sources and MOS steering transistors are represented by switches **52**, **54** and **56**.

In FIG. **3**, the first ECL transistor pair is driven by high speed signal input lines A and A- in the data path, while the second ECL transistor pair is driven by high speed input signal lines B and B-. Both ECL transistor pairs drive a single pair of shared output signal lines Y and Y- and share a single pair of pull up resistors.

Referring to FIG. **4**, there is shown a symbolic diagram of a four-input-three-output crossbar switch comprised of three modules like that shown in FIG. **3** interconnected such that the data inputs of the first module comprised of switches **58**, **60**, **62** and **64** also drive the data inputs from corresponding switches in the other two modules. Specifically, the A and A- data inputs to switch **58** are coupled not only to the data inputs of switch **58**, but also to the data inputs of switches **66** and **68** via lines **59** and **61**, and the B and B- data inputs drive the data inputs of both the switch **60** and the switch **68** and **72** via lines **63** and **65**. The C and C- data inputs are similarly connected so as to drive the data inputs of switches **62**, **74** and **76** via lines **67** and **69**, and the D and D- data inputs are coupled to drive the data inputs of switches **64**, **78** and **80**. For clarity of the figure, the separate enable inputs of each switch are not shown, but each switch has an enable input coupled to receive a steering signal such as the signal **EN1** in FIGS. **1** or **2**. These steering signals are coupled to the CMOS steering transistors that control enabling of the ECL transistor pair of each switch in the manner described above for the circuits of FIGS. **1** and **2**.

Operation of the crossbar switch of FIG. **4** is a straightforward function of activating selected ones of the steering signals. For example, if it is desired to pass the D and D- signals on to only the W and W- outputs, the enable signal to switch **64** would be activated and all other enable signals to all other switches would be inactive. If the D and D- outputs were to be steered to the X and X- outputs, the enable signal for only switch **78** would be active, and all other enable signals to all other switches would be inactive.

Any input pair can be coupled to any one or more output pairs in the architecture of FIG. **4**, and two or more inputs can be coupled to two or more outputs simultaneously as long as no output is coupled to more than one input at any particular time. For example, the A and A- inputs can be coupled to the W and W- and X and X- inputs simultaneously while the D and D- inputs are simultaneously coupled to the Y and Y- inputs. Many other combinations are also possible as will be apparent to those skilled in the art.

The architecture of the crossbar switch of FIG. **4** can be extended to larger numbers of input pairs and/or output pairs.

Simulations of the operation of a 4×4 (four input pairs and four output pairs) crossbar switch having an architecture like that of the circuit of FIG. **4** has shown propagation delays of about $\frac{1}{4}$ nanosecond. This is much faster than the propagation delays of such crossbar switch circuits implemented using CMOS in the data path. That is, the time it takes for a change of level on any output pair to propagate through the circuit and cause a corresponding change in level on any one or more selected output pair is $\frac{1}{4}$ nanosecond.

The circuits shown in FIGS. **1** through **4** all use current mode logic which has a maximum output voltage swing on the order of 300 millivolts. If the output voltage swing is stretched to a value more than 300 millivolts, soft saturation or total saturation can occur in the ECL transistors. This is highly undesirable because saturation or soft saturation of current mode logic switches substantially decreases the switching speed thereof. Thus, in the preferred embodiment, emitter followers are used as output buffers so as to increase the permissible output voltage swing.

There are other reasons to use emitter followers. Specifically, emitter followers can be used to shift the voltage levels so as to drive other logic families, or they can be used to create higher current source or sink capacity for driving long lines etc.

To provide maximum flexibility, it is desirable to be able to couple the output of a current mode logic switch according to the teachings of the invention to any one or more of a number of emitter follower arrangements, some of which may have different characteristics such as different output voltage levels, logic swing or current source or sink capacity.

To provide this flexibility, the circuit of FIG. **5** may be used according to the teachings of the invention. In the circuit of FIG. **5**, a data output line A from the output of a current mode logic switch or any other type of similar logic switch circuit is coupled via line **51** to two emitter followers comprised of ECL transistors E9 and E**10** which drive output lines F**1** and F2. Each of these emitter follower transistors has an associated current source and associated CMOS enabling circuitry. Specifically, transistor **E9** drives output line **F1** and has its emitter coupled to a current source transistor **CS5** which has an emitter feedback resistor R7 and which has its base coupled to a constant reference voltage Vref as was the case with the current source transistors of the circuits of FIGS. **1**–**4**. Tile CMOS enabling circuitry for emitter follower transistor **E9** is comprised of NMOS transistors N6 and N7 and PMOS transistor P6. Likewise, emitter follower transistor E**10** has its emitter coupled to a current source transistor **CS6** having emitter feedback resistor **R8**. The base of the current source transistor **CS6** is coupled to the constant reference voltage line Vref. The enabling CMOS circuitry for the current source **E10** is comprised of NMOS transistors **N8** and N9 and PMOS transistor **P7**.

Emitter follower **E9** is enabled when the steering signal **EN9** is active high and complementary steering signal **EN9**- is active low. This state causes NMOS transistor N7 to be turned on thereby activating the current source transistor **CS5** by coupling its emitter to the low voltage supply line **52**. Because **EN9**- is active low, NMOS transistor **N6** is turned off and PMOS transistor **P6** is turned on thereby allowing the base of transistor **E9** to assume whatever voltage high speed input signal A currently has. Note that although a PMOS transistor P6 is in the high speed signal path, the load on this transistor is very light comprised of only one ECL transistor base and one NMOS transistor drain. This light load does not appreciably slow down signal propagation. It is necessary to use the **P6** transistor in the embodiment shown in FIG. **5** because it is necessary to disconnect the high speed signal A from the base of transistor **E9** when the base is coupled to the low voltage supply **52** so that the high speed data signal is not loaded down thereby slowing signal propagation.

To disable emitter follower **E9**, steering signal **EN9** is driven to its inactive low state and complementary steering signal EN9- is driven to its inactive high state. This state causes NMOS transistor N7 to turn off and NMOS transistor **N6** to turn on simultaneously with PMOS transistor **P6** turning off. This causes current source transistor **CS5** to be disconnected from the low voltage supply line **52** and become inactive thereby disabling the emitter follower transistor E9. Simultaneously, the base **54** of NPN transistor **E9** is coupled to the low voltage supply **52** to reverse bias the base-emitter junction and the base **54** is cut off from the A data input line **51** by virtue of transistor **P6** turning off. By coupling the base **54** of transistor E9 to the low voltage supply, the base-emitter junction of NPN transistor is reverse biased thereby preventing any voltage source coupled to the **F1** output from accidentally turning transistor **E9** on.

Emitter follower **E10** works in the same fashion as emitter follower E9. However, it may have a different physical geometry or emitter feedback resistor **R8** may have a different value so as to present different voltage levels on output line F2. Further, emitter follower E**10** may be designated so as to be able to source more current to output line **F2** to drive a long line. Thus, when steering signal EN**10** is active high and steering signal EN**10** is active low, NMOS transistor N9 is on enabling the current source transistor CS6 and NMOS transistor N8 is off while PMOS transistor **P7** is on thereby connecting the base **56** of NPN transistor **E10** to high speed data input A. To turn off **E10**, steering signal **EN10** is made inactive low and steering signal **EN10**- is made inactive high.

Note that the architecture of the circuit of FIG. **5** allows the high speed data signal A to drive either output F**1** or output F2, or both simultaneously or neither depending upon the states of the steering signals **EN9** and **EN10** and their complements.

Another high speed data input, B, on line **51** is coupled to the base of an NPN emitter follower transistor E**11** which also drives output F2. If level shifting of the output swing of output **F2** were desired when driven by input B, emitter follower transistor **E11** could be replaced by two transistors in series such that two base emitter drops of approximately 850 millivolts would be imposed between the high voltage supply line **60** and the output **F2** when the emitter follower **E11** is turned on. Emitter follower **E11** and its steering circuitry works the same way as emitter followers **E9** and **E10**. Specifically, when steering signal **EN11** is active high and its complement **EN11**- is active low, NMOS transistor **N10** is on and activates current source transistor CS7 by coupling the emitter thereof to low voltage supply line **52**. The base of transistor CS7 is coupled to the constant reference voltage Vref as are the bases of current source transistors CS5 and CS6. Simultaneously, NMOS transistor N**11** is turned off by the low state of EN**11**- and PMOS transistor **P8** is turned on thereby connecting the high speed data input B to the base of emitter follower transistor E**11**. This causes the changes in logic level of high speed data input signal B to be reflected on output **F2** while imposing the buffering, level shifting and current boosting benefits of the emitter follower **E11** between the high speed data input signal B and the output signal **F2** which follows it.

Thus, by driving steering signal **EN11** active high and steering signal **EN10** inactive low and the complementary steering signals to their corresponding active/inactive states, it is possible to drive output **F2** with input B. Likewise, by driving steering signal **EN10** active high and steering signal **EN11** inactive low and the complementary steering signals to their corresponding active/inactive states, it is possible to drive output **F2** with input A. It is not permitted to have both steering signals **EN10** and **EN11** active high at the same time, although it is permitted to have both inactive low simultaneously.

Note that the inputs A and B on lines **51** and **53** may be coupled to any of the outputs shown in FIG. **1–4** such as Y or Y- etc., and note that duplicate emitter follower circuitry may be used to couple to the complementary outputs. Also, the outputs **F1** and **F2** may be coupled to the inputs of the single ended circuit of FIG. **6** to provide any necessary one Vbe drop (base-emitter voltage drop) to properly bias that circuit. The number of possible permutations and combinations of the fast switching circuits and emitter follower circuitry that does not impede the switching speed according to the teachings of the invention are too numerous to draw them all, but they will be apparent to those skilled in the art. Any fast switching circuit that uses MOS enabling circuitry that is substantially removed from the data path to enable the switch or do a steering function for the high speed data signals is equivalent to what is taught herein and intended to be within the scope of the claims appended hereto.

The consequence of use of the architecture of FIG. **5** in conjunction with the architecture of any of FIGS. **1–4** is that the high speed switches of FIGS. **1–4** may be coupled to any other type of logic family regardless of the logic levels of the logic family to which the high speed switches are to be coupled. The level of the output signals at outputs F1 and F2 can be raised by raising the voltage at the high voltage supply line **60** or changing the values of emitter feedback resisters R7, R8 and **R9** and changing the characteristics of the current source transistors and/or changing the reference voltage Vref to alter the level of current flowing through the emitter feedback resisters. Likewise, output level voltages can be shifted downward by coupling more emitter follower transistors in series so that all transistors in the chain turn on or off simultaneously with changes in the input signal levels and so as to impose their base-emitter voltage drops in series between the high voltage supply line **60** and the corresponding output. This level shifting can be done without loss of the advantage of ECL speeds. This provides great flexibility to designers. For example, in well-known differential mode cascade logic, one set of data inputs coupled to the lower differential pair substituted for the normal current source must be driven between level changes which are uniformly one base-emitter voltage drop (approximately 850 millivolts) below the corresponding levels of the other set of data inputs coupled to the upper differential pair. This can be done using the emitter follower technology of FIG. **5**, for example by driving one set of inputs with the **F1** output and driving the other set of inputs coupled to the lower differential pair with output **F2** and substituting a pair of series coupled emitter followers for single emitter followers E10 and **E11**.

Those skilled in the art will appreciate that the concepts illustrated in FIG. **5** can be extended such that input A can drive more emitter followers and more outputs, and the crossbar switching capabilities of input A or B being able to drive input F2 can be extended to more inputs and outputs by modification of the circuit of FIG. **5**. Likewise, the concepts illustrated in FIGS. **1–4** may be extended to more inputs and more outputs and can be extended to single ended technology. Generally, differentially coupled current mode logic devices are preferred, because the logic swing can be reduced with adequate noise immunity and therefore great speeds can be achieved. However, where integrated circuit space is an issue, and the number of transistors is to be held down, single ended logic can also be used.

For example, a single-ended, fast OR gate employing the teachings of the invention is shown in FIG. **6**. In this circuit, a differentially coupled pair current mode NPN transistors **80**, **81** and **84** are coupled to share a common node **83**. A reference signal Vbb is coupled to the base of transistor **81**, and high speed data input signals A and B coupled to the bases of transistors **80** and **81** have logic states which swing both above and below the level of Vbb. A constant current source comprised of transistor **86** and resistor **88** selectively drives the common node **83** when NMOS transistor **90** is turned on. This occurs when steering signal **EN12** is active high. When this occurs, PMOS transistor **82** turns off and common node **83** is free to seek whatever voltage it normally assumes when the differential pair is enabled. The transistors **84**, **80** and **81** then drive the outputs Y and Y-. Pullup resistors **92** and **94** couple the outputs to the high voltage source. The voltage swings of the signals on inputs A and B can be increased to increase noise immunity, but the high level of either signal cannot be higher than one base-emitter voltage drop below the level of Vh on the **100**. Thus, an emitter follower according to the teachings of FIG. **5** could be used to drive the A and B inputs if necessary to provide the necessary one base-emitter drop. The concept of FIG. **6** can be extended to any of the other switches or arrays shown in FIGS. **1–4** as will be apparent to those skilled in the art. Further, although NPN bipolar current mode logic technology is used for illustration, PNP bipolar technology could also be used, and any differentially coupled circuit could also be single ended. Further, other high speed switching technologies either now existing or to be invented in the future could also be used to implement the teachings of the invention if the slower enabling/steering logic is kept out of the high speed data path.

What is claimed is:

1. A high speed switch, comprising:

a pair of data inputs for receiving high speed, complementary input signals; one or more pairs of high speed complementary data outputs;

a high voltage supply;

a low voltage supply;

one or more differential pairs of current mode logic transistors having base terminals coupled to said data inputs, each pair having a pair of collectors coupled to said high voltage supply and to one of said pairs of high speed complementary data outputs, and each pair having emitters coupled to a common node;

an essentially constant current source corresponding to each said differential pair of current mode logic transistors selectively coupling said common node to said low voltage supply;

one or more steering signal inputs, each steering signal input corresponding to one of said differential pairs of current mode logic transistors, each steering signal input for receiving a steering signal; and

enabling means for selectively coupling said constant current source for each said differential coupled pair of current mode transistors to said low voltage supply and for decoupling the common node of each said differential pair to said high voltage supply when the corresponding steering signal is in a first state, and for decoupling said constant current source for each said differential coupled pair of current mode logic transistors from said low voltage supply and coupling the common node of each said differential coupled pair of current mode logic transistors from said high voltage supply when the corresponding steering signal is in a second state, thereby allowing any of said differential coupled pairs of current mode logic transistors to drive the corresponding pair of high speed data outputs under the influence of the high speed data input signals received at said data inputs by control of the states of said steering signals.

2. The apparatus of claim **1** wherein said enabling means comprises for each said differential pair of current mode logic transistors, a PMOS transistor coupling said common node to said high voltage supply, and an NMOS transistor coupling said current source to said low voltage supply, each of said NMOS and PMOS transistors having their gates coupled to said steering signal.

3. A high speed switch comprising:

at least two pairs of high speed data inputs, each pair for receiving a pair of high speed, complementary data signals;

a pair of outputs for outputting a complementary pair of high speed output signals;

a high voltage supply;

a low voltage supply;

a pair of shared pullup resistors coupled to said high voltage supply;

a pair of differential current mode logic transistors, each having a collector coupled to one of said pair of pullup resistors and to one of said outputs of said output pair, and having base terminals each of which is coupled to one of the signal inputs of a selected pair of said high speed data inputs, and having a pair of emitter terminals coupled to a common node;

one or more pairs of differential coupled, current mode logic transistors, each having a collector coupled to one of said outputs of said output pair, and having base terminals each of which is coupled to one of the signal inputs of a selected pair of said high speed data inputs different from the high speed data input pairs coupled to each other said differential coupled pair of current mode logic transistors, each said differential coupled pair of current mode logic transistors having a pair of emitter terminals coupled to a common node;

one or more essentially constant current sources, each for selectively coupling one of said common nodes to said low voltage supply;

one or more steering signal inputs, each for receiving a steering signal for controlling the enabled or disabled state of a corresponding one of said differential coupled pair of current mode logic transistors; and

enabling means for selectively coupling said constant current source for each said differential coupled pair of current mode transistors to said low voltage supply and for decoupling the common node of each said differential pair to said high voltage supply when the corresponding steering signal is in a first state, and for decoupling said constant current source for each said differential coupled pair of current mode logic transistors from said low voltage supply and coupling the common node of each said differential coupled pair of current mode logic transistors from said high voltage supply when the corresponding steering signal is in a second state, thereby allowing any of said differential coupled pairs of current mode logic transistors to drive the corresponding pair of high speed data outputs under the influence of the high speed data input signals received at said data inputs by control of the states of said steering signals.

4. The apparatus of claim **3** wherein said enabling means comprises for each said differential coupled pair of current mode logic transistors, a PMOS transistor coupling said common node to said high voltage supply, and an NMOS transistor coupling said current source to said low voltage supply, each of said NMOS and PMOS transistors having their gates coupled to said steering signal.

5. A high speed, multiplexer comprising:

switching means including first and second differential inputs and a plurality of high speed differential amplifiers, each differential amplifier having a common power return node for selective connection to a low voltage supply, and each differential amplifier coupled to receive high speed data signals from said first and second differential inputs, and each differential amplifier having a pair of differential outputs, said switching means for receiving high speed data signals, and, when enabled, for coupling said high speed data signals to a selected output; and

enabling means having an enable input corresponding to each said differential amplifier including CMOS switching means corresponding to each said differential amplifier and coupled to the enable input and common power return node of the corresponding differential amplifier, said CMOS switching means for selective enabling or disabling the corresponding differential amplifier, said enabling means for enabling the corresponding differential amplifier by selective coupling of each said differential amplifier means common power return node to said low voltage supply via the corresponding CMOS switching means when the corresponding enable input receives an activated enable signal indicating the corresponding differential amplifier is to be rendered operational thereby differentially amplifying the high speed data signals at said first and second differential inputs and outputting the data signals so amplified to the corresponding pair of differential outputs, and for disabling a differential amplifier by coupling said common power return node to a high voltage supply via the corresponding CMOS switching means when the corresponding enable signal is not active.

6. A crossbar switch, comprising:

a first multiplexer having a plurality of data inputs and a shared data output comprised of a plurality of switching devices each of which is coupled to one of said plurality of data inputs and each of which can be individually enabled under the influence of a corresponding steering signal associated with that switching device so as to be able to drive said shared data output in accordance with the data received at the corresponding data input;

one or more other multiplexers each having inputs coupled to the same plurality of data inputs coupled to said first multiplexer, and each having a shared data output, and each comprised of a plurality of switching devices each of which is coupled to one of said plurality of data inputs coupled to a corresponding switching device of said first multiplexer, each of said switching devices of said one or more other multiplexers including enabling circuitry coupled to the associated switching device such that the associated switching device can be individually enabled under the influence of a corresponding steering signal so as to be able to drive the corresponding said shared data output in accordance with the data received at the corresponding data input, such that by proper manipulation of said steering signals for said first multiplexer and said one or more other multiplexers, each of the shared outputs can be driven by any of the data inputs so long as no more than one data input is used to drive any shared data output at any particular time and wherein each of said multiplexers is comprised of:

at least two pairs of high speed data inputs, each pair for receiving a pair of high speed, complementary data signals;

a pair of outputs for outputting a complementary pair of high speed output signals;

a high voltage supply;

a low voltage supply;

a pair of shared pullup resistors coupled to said high voltage supply;

a pair of differential current mode logic transistors, each having a collector coupled to one of said pair of pullup resistors and to one of said outputs of said output pair, and having base terminals each of which is coupled to one of the signal inputs of a selected pair of said high speed data inputs, and having a pair of emitter terminals coupled to a common node;

one or more pairs of different coupled, current mode logic transistors, each having a collector coupled to one of said outputs of said output pair, and having base terminals each of which is coupled to one of the signal inputs of a selected pair of said high speed data inputs different from the high speed data input pairs coupled to each other said differential coupled pair of current mode logic transistors, each said differential coupled pair of current mode logic transistors having a pair of emitter terminals coupled to a common node;

one or more essentially constant current sources, each for selectively coupling one of said common nodes to said low voltage supply;

one or more steering signal inputs, each for receiving a steering signal for controlling the enabled or disabled state of a corresponding one of said differential coupled pair of current mode logic transistors; and

enabling means for selectively coupling said constant current source for each said differential coupled pair of current mode transistors to said low voltage supply and for decoupling the common node of each said differential pair to said high voltage supply when the corresponding steering signal is in a first state, and for decoupling said constant current source for each said differential coupled pair of current mode logic transistors from said low voltage supply and coupling the common node of each said differential coupled pair of current mode logic transistors from said high voltage supply when the corresponding steering signal is in a second state, thereby allowing any of said differential coupled pairs of current mode logic transistors to drive the corresponding pair of high speed data outputs under the influence of the high speed data input signals received at said data inputs by control of the states of said steering signals.

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[54] **DRIVER CIRCUIT FOR ADDRESSING CORE MEMORY AND A METHOD FOR THE SAME**

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Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 16,811, Feb. 11, 1993, Pat. No. 5,459,693, and a division of Ser. No. 487,841, Jun. 7, 1995, Pat. No. 5,594,696, which is a continuation-in-part of Ser. No. 912,112, Jul. 19, 1992, Pat. No. 5,241,497, which is a continuation of Ser. No. 538,185, Jun. 14, 1990, abandoned.

[51] **Int. Cl.**^{6} **G11C 7/00**; H03K 19/00

[52] **U.S. Cl.** **365/189.05**; 326/58; 326/83

[58] **Field of Search** 365/189.02, 189.05; 326/58, 82, 83; 327/108, 109, 111; 368/185.16

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[57] ABSTRACT

The invention is an improved bank select read only memory in which the bit lines and virtual ground lines are precharged to ground instead of being precharged to an internal low supply voltage. Both of the two virtual ground lines are selected for the selected bit and both selected virtual ground lines are driven to ground during the precharge phase. At the top of the memory array, all virtual ground lines in the memory array are precharged to ground during the precharge phase. Next, during the sensing phase, the operation of the two virtual ground lines for the selected bit is changed to selectively hold one virtual ground line at ground and switch the second virtual ground line to a positive voltage. All bit lines are precharged to ground during the precharge phase. In the following sensing phase, the selected bit line is driven positive by the selected memory core FET if it is programmed with a low threshold voltage. If the selected memory core FET is programmed with a high threshold voltage, the bit line remains floating at the ground level, or it may be held at ground by means of the second virtual ground line, which is held at ground, and by low threshold core FETs, adjacent to the selected core FET, which are connected to the selected word line. The total diffusion capacitance on a virtual ground line is minimized when the memory cells connected to the line are programmed with more logic zeros than logic ones.

9 Claims, 12 Drawing Sheets