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BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORP., and CAVIUM, LLC
Petitioner,

v.

ALACRITECH, INC.
Patent Owner.

Case IPR. IPR2018-00234[1]
U.S. Patent No. 8,805,948
Title: INTELLIGENT NETWORK INTERFACE SYSTEM AND METHOD FOR PROTOCOL PROCESSING

INTEL CORPORATION'S UPDATED EXHIBIT LIST

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[1] Cavium, LLC, which filed a Petition in Case IPR2018-00403, has been joined as a petitioner in this proceeding.

Exhibit #	Description
Ex.1001	U.S. Patent No. 8,805,948 ("948 Patent")
Ex.1002	Excerpts from Prosecution File History of U.S. Patent No. 8,805,948 ("948 File History")
Ex.1003	Declaration of Robert Horst
Ex.1004	Curriculum Vitae of Robert Horst
Ex.1005	U.S. Patent No. 5,768,618 ("Erickson")
Ex.1006	Tanenbaum, Andrew S., *Computer Networks*, Prentice-Hall, Inc., New Jersey (1996). ("Tanenbaum96")
Ex.1007	Transmission Control Protocol, "Darpa Internet Protocol Specification", RFC: 793, Sept. 1981. ("RFC 793")
Ex.1008	Stevens, W. Richard, TCP/IP Illustrated Volume 1: The Protocols, Addison-Wesley (1994). ("Stevens1")
Ex.1009	Lilinkamp, J., Mandell. R. and Padlipsky, M., "Proposed Host-Front End Protocol", Network Working Group Request for Comments: 929, Dec. 1984. ("RFC 929")
Exs.1010	*Not Used*
Ex. 1011	Librarian Declaration of Rice Mayors regarding Andrew S. Tanenbaum, Computer Networks (3rd ed. 1996) (Ex.1006, "Tanenbaum96")
Ex. 1012	*Not Used*
Ex.1013	Stevens, W. Richard and Gary R. Wright, *TCP/IP Illustrated Volume 2: The Implementation*, Addison-Wesley (1995). ("Stevens2")
Ex.1014	*Not Used*

Exhibit #	Description
Ex.1015	Thia, Y.H., Woodside, C.M., "A Reduced Operation Protocol Engine (ROPE) for a Multiple-Layer Bypass Architecture", Protocols for High Speed Networks (Dordrecht), 1995. ("Thia and Woodside")
Ex.1016	Biersack, E. W., Rütsche E., "Demultiplexing on the ATM Adapter: Experiments with Internet Protocols in User Space", Journal on High Speed Networks, Vol. 5, No. 2, May 1996. ("Biersack")
Ex.1017	Rütsche, E., Kaiserswerth, M., "TCP/IP on the Parallel Protocol Engine", Proceedings, IFIP Conference on High Performance Networking, Liege (Belgium), Dec. 1992. ("Rütsche92")
Ex.1018	Rütsche, E., "The Architecture of a Gb/s Multimedia Protocol Adapter", Computer Communication Review, 1993. ("Rütsche93")
Ex.1019	Padlipsky, M. A., "A Proposed Protocol for Connecting Host Computers to Arpa-Like Networks Via Directly-Connected Front End Processors", Network Working Group RFC #647, Nov. 1974. ("RFC 647")
Ex.1020	U.S. Patent No. 5,619,650 ("Bach")
Ex.1021	U.S. Patent No. 5,915,124 ("Morris")
Ex.1022	Cooper, E.C., et al., "Protocol Implementation on the Nectar Communication Processor", School of Computer Science, Carnegie Mellon University, Sept. 1990. ("Cooper")
Ex.1023	Kung, H.T., et al., "A Host Interface Architecture for High-Speed Networks", School of Computer Science, Carnegie Mellon University and Network Systems Corporation. ("Kung")
Ex.1024	Exhibit D to Declaration of Dr. Gregory L. Chesson in Support of Microsoft's Opposition to Alacritech's Motion for Preliminary Injunction: "Protocol Engine Handbook", Protocol Engines Incorporated, Oct. 1990. ("Chesson")

Exhibit #	Description
Ex.1025	Kanakia, H., Cheriton, D.R., "The VMP Network Adapter Board (NAB): High-Performance Network Communication for Multiprocessors", Communications Architectures & Protocols, Stanford University, Aug. 1988. ("Kanakia")
Ex.1026	Kung, H.T., Cooper, E.C., et al., "Network-Based Multicomputers: An Emerging Parallel Architectures", School of Computer Science, Carnegie Mellon University. ("Kung and Cooper")
Ex.1027	Dalton, C., et al., "Afterburner: Architectural Support for High-Performance Protocols", Networks & Communications Laboratories, HP Laboratories Bristol, July 1993. ("Dalton")
Ex.1028	Murphy, E., Hayes, S., Enders, M., *TCP/IP Tutorial and Technical Overview Fifth Edition*, Prentice-Hall, Inc. New Jersey, (1995). ("Murphy")
Ex.1029	MacLean, A.R., Barvick, S. E., "An Outboard Processor for High Performance Implementation of Transport Layer Protocols", IEEE Globecom '91, Phoenix, AZ, Dec. 1991. ("MacLean")
Ex.1030	Clark, D.D., et al., "An Analysis of TCP Processing Overhead", IEEE Communications Magazine, June 1989. ("Clark")
Ex.1031	Provisional Application 60/061,809 ("Alacritech 1997 Provisional Application")
Ex.1032	Culler, E.C., et al., "Parallel Computing on the Berkeley NOW", Computer Science Division, University of California, Berkeley. ("Culler")
Ex.1033	"Gigabit Ethernet Technical Brief: Achieving End-to-End Performance", Alteon Networks, Inc. First Edition, Sept. 1996. ("Alteon")
Ex.1034	Smith, J.A., Primmer, M., "Tachyon: A Gigabit Fibre Channel Protocol Chip", Hewlett-Packard Journal, Article 12, Oct. 1996. ("Smith")

Exhibit #	Description
Ex.1035	Patterson, D.A., Hennessy, J.L., *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann Publishers, Inc., San Mateo, CA (1990). ("Patterson")
Exs.1036	Internet Protocol, "Darpa Internet Protocol Specification", RFC: 791, Sept. 1981. ("RFC 791")
Ex. 1037	*Not Used*
Ex.1038	Woodside, C. M., Ravindran, K., and Franks, R. G. "The protocol bypass concept for high speed OSI data transfer." IFIP Workshop on Protocols for High Speed Networks. 1990. ("Woodside")
Exs.1039-1062	*Not Used*
Ex.1063	Librarian Declaration of Pamela Stansbury regarding Gary R. Wright & W. Richard Stevens, TCP/IP Illustrated: The Implementation (1995) (Ex.1013, "Stevens2").
Ex.1064	Librarian Declaration of Lisa Rowlison de Ortiz re Y.H. Thia & C.M. Woodside, A Reduced Operation Protocol Engine (ROPE) for a Multiple-layer Bypass Architecture (1995) (Ex.1015, "Thia")
Ex.1065-1094	*Not Used*
Ex. 1095	Stevens, W. Richard and Gary R. Wright, TCP/IP Illustrated Volume 2: The Implementation, Addison-Wesley (1995) (With 1995 Copyright Page) ("Stevens2")
Ex.1096	U.S. Pat. No. 6,011,795
Ex.1097-1099	*Not Used*
Ex. 1100	Increasing TCP Throughput By Using an Extended Acknowledgement Interval (1995)

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