Paper 7 Entered: June 5, 2018

## UNITED STATES PATENT AND TRADEMARK OFFICE

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## BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INTEL CORPORATION, Petitioner,

v.

ALACRITECH, INC., Patent Owner.

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Case IPR2018-00234 Patent 8,805,948 B2

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Before STEPHEN C. SIU, DANIEL N. FISHMAN, and CHARLES BOUDREAU, *Administrative Patent Judges*.

FISHMAN, Administrative Patent Judge.

DECISION Institution of *Inter Partes* Review 35 U.S.C. § 314

### I. INTRODUCTION

Intel Corporation ("Petitioner") requests *inter partes* review of claims 1, 3, 6–8, 17, 19, 21, and 22 of U.S. Patent No. 7,337,948 B2 ("the '948



patent," Ex. 1001) pursuant to 35 U.S.C. §§ 311 *et seq*. Paper 2 ("Petition" or "Pet."). Alacritech, Inc. ("Patent Owner") filed a preliminary response. Paper 6 ("Prelim. Resp."). Institution of an *inter partes* review is authorized by statute only when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Upon consideration of the Petition and Preliminary Response, we conclude the information presented shows there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one of the challenged claims of the '948 patent.

## A. Related Matters

We are informed that the '948 patent is presently related to the following: *Alacritech, Inc. v. CenturyLink, Inc.*, Case No. 2:16-cv-00693-JRG-RSP (E.D. Tex.); *Alacritech, Inc. v. Wistron Corp.*, Case No. 2:16-cv-00692-JRG-RSP (E.D. Tex.); and *Alacritech, Inc. v. Dell Inc.*, Case No. 2:16-cv-00695-RWS-RSP (E.D. Tex.). Pet. 5; Paper 4, 1.

Petitioner identifies numerous other related patents and other petitions related to this and other related patents. Pet. 5–7. Of particular note are IPR2017-01395 ("the 1395 IPR") and IPR2017-01729 (seeking joinder with IPR2017-01395) challenging the '948 patent. Pet. 6. IPR2017-01395, filed by Intel, challenging all claims challenged in this petition and relying on essentially the same arguments, evidence, and references. We did not address the substance of the arguments in the IPR2017-01395 petition but, instead, denied institution in IPR2017-01395 due to insufficient evidence of printed publication status of one reference relied upon in the asserted grounds. *See* IPR2017-01395 Paper 8.



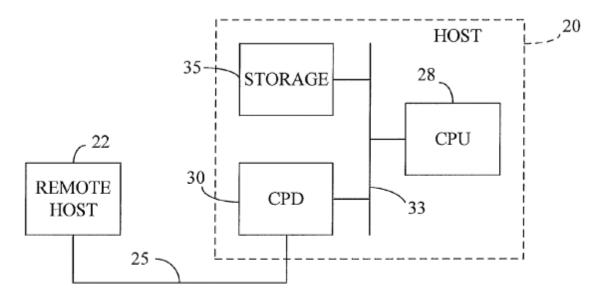
#### B. The '948 Patent

The '948 patent describes a system and method for accelerating data transfer using an intelligent network interface card ("INIC") or communication processing device ("CPD"). Ex. 1001, Abstract. The INIC or CPD provides a fast-path that avoids host protocol processing for larger messages that span multiple packets in a transmission. *Id.* According to the '948 patent, layered protocol models (such as TCP/IP or the OSI layered model) utilize header information for processing in each of the layers of the protocol stack. *See id.* at 1:33–3:19. According to the '948 patent, as complexity and popularity of such networks grew, the processing burden on a host CPU for processing these protocols grew proportionally. *Id.* at 3:20–35.

The '948 patent purports to reduce this bottleneck for processing on a host computer by providing fast-path processing in which processing for headers of a layered network protocol is offloaded from the host computer to an INIC or CPD. *See id.* at 4:65–5:6.



Figure 1 of the '948 patent is reproduced below.



# FIG. 1

Figure 1 is depicts a system including a host computer having a CPD for accelerating network communications. *Id.* at 4:9–12. Figure 1 shows host 20 connected with remote host 22 via network 25. *Id.* at 4:65–66. Host 20 includes CPU 28 and CPD 30 coupled via host bus 33. *Id.* at 5:6–7. CPD 30 processes network protocols and includes a microprocessor and memory buffers controlled by a direct memory access ("DMA") controller. *Id.* at 5:8–10. A connection context (not shown in Figure 3) stores various elements of information regarding the connection between host 20 and remote host 22 and may be stored in a communication control block ("CCB") within CPD 30 or storage 35. *Id.* at 5:22–29.



Figure 3 is reproduced below.

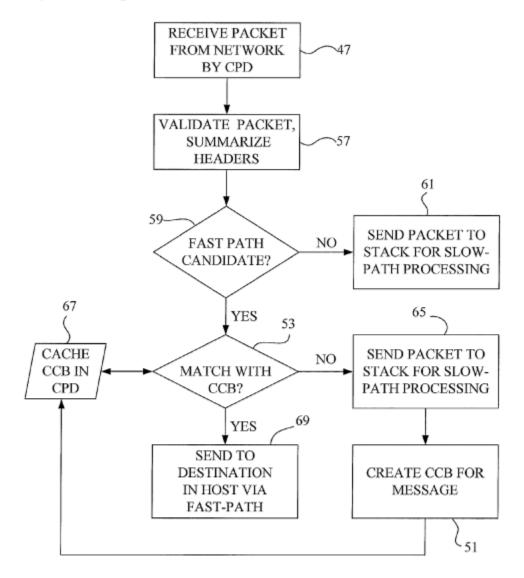


FIG. 3

Figure 3 is a flow chart describing processing of a received message. *Id.* at 4:17–18. At step 47, a packet is received in a CPD (or INIC) and, at step 57, the CPD validates various protocol headers of the received packet and summarizes the results. *Id.* at 6:30–34. The summary includes a determination as to whether the packet is a candidate for fast-path



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