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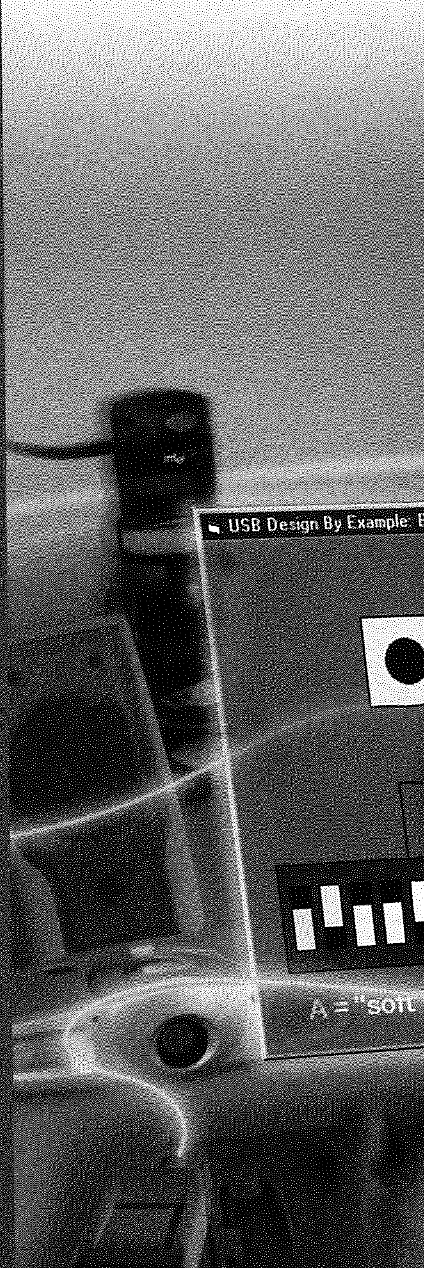
USB Desi

A Practical Guide

John Hyde



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Wiley Computer Publish

WILEY

John Wiley & Sons, Inc

New York • Chichester • Weinheim • Brisban

Publisher: Robert Ipsen (Wiley), Rich Bowles (Intel)
Acquisitions Editor: Cary Sullivan
Editor: Marcia Petty
Assistant Editor: David Spencer
Managing Editor: Frank Grazioli
New Media, Associate Editor: Mike Sosa
Text Design & Composition: Marianne Phelps
Graphic Art: Jerry Heideman (illustrations), Dan Mandish (cover)

Published by John Wiley & Sons, Inc. Published simultaneously in Canada.

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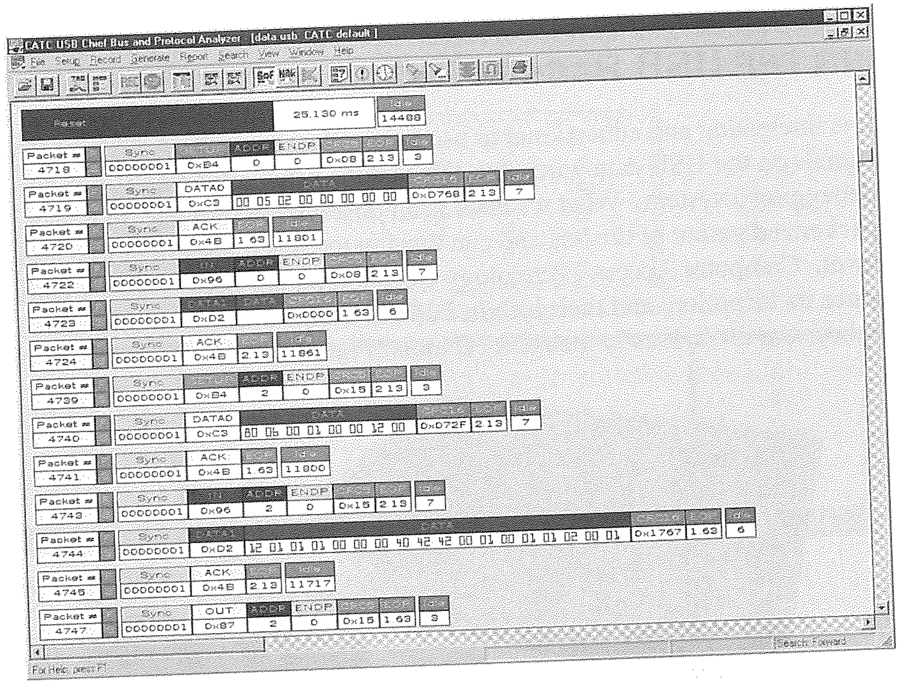
Library of Congress Cataloging in Publication Data:

Hyde, John, 1952–
USB design by example : a practical guide to building IO devices / John Hyde.
p. cm.
Includes index.
ISBN 0-471-37048-7
1. USB (Computer bus) 2. Computer input-output equipment—Design and construction. I. Title.
TK7895.B87H93 1999
004.6'4—dc21 99-35865
CIP

Printed in the United States of America

10 9 8 7 6 5 4 3 2


CATC USB Chief Bus and Protocol Analyzer - [data.usb CATC default]
File Setup Record Generate Report Search View Window Help
SoF
NAK
For Help, press F1
Search Forward

```
Reset                       25.130 ms   14488
Packet # 4718  Sync 00000001  0xB4   ADDR 0  ENDP 0  0x08  2.13  3
Packet # 4719  Sync 00000001  DATA0 0xC3  00 05 02 00 00 00 00 00  0xD768  2.13  7
Packet # 4720  Sync 00000001  ACK 0x4B  1.63  11801
Packet # 4722  Sync 00000001  0x96   ADDR 0  ENDP 0  0x08  2.13  7
Packet # 4723  Sync 00000001  0xD2          0x0000  1.63  6
Packet # 4724  Sync 00000001  ACK 0x4B  2.13  11861
Packet # 4739  Sync 00000001  0xB4   ADDR 2  ENDP 0  0x15  2.13  3
Packet # 4740  Sync 00000001  DATA0 0xC3  80 06 00 01 00 00 12 00  0x072F  2.13  7
Packet # 4741  Sync 00000001  ACK 0x4B  1.63  11800
Packet # 4743  Sync 00000001  0x96   ADDR 2  ENDP 0  0x15  2.13  7
Packet # 4744  Sync 00000001  0xD2  12 01 01 01 00 00 00 40 42 42 00 01 00 01 01 02 00 01  0x1767  1.63  6
Packet # 4745  Sync 00000001  ACK 0x4B  2.13  11717
Packet # 4747  Sync 00000001  OUT 0x87  ADDR 2  ENDP 0  0x15  1.63  3
```

Figure 2-17. USB packets displayed as packets

All of the CATC tools capture bus activity for later analysis. The use of color to display different packet types and the grouping of building-block packets into transactions allow the designer to quickly interpret what has happened on the bus. The simpler CATC tools capture all bus activity while the more elaborate tools have programmable capture and programmable triggers. Being able to isolate packets sent to a specific device or triggering after, for example, device 42 has received 58 DATA0 packets, aids the debugging of more sophisticated USB devices. The high-end CATC tools can also be used to generate bus traffic for device reliability testing and failure analysis.

HAPTER SUMMARY

This chapter provided insight into the signals on the bus, the fundamental packetized nature of the bus, and the transactions used to exchange data on the bus. The PC host uses a defined set of requests to control all of the devices attached to the bus, and these devices need to respond in a defined manner. Bus observation, or "sniffer" tools as they are called, are available to monitor and analyze these low-level bus signals.

THE ENUME

Let us assume that the PC host meets all of the
Chapter 1, is running a USB-aware operating s
port. This port could be on the PC host itself (
an external hub. Now we have a new USB I/C
running system. What actually happens betwe
to deliver the many USB features?

After understanding what the PC host is doing
general I/O device. All devices describe thems
tables. We start by looking inside the simplest
discussion to cover the general case. We then
requirements for a device.

There are many "chicken-vs.-egg" situations in
some technical discussions to keep the flow of

VICE DETECTION

Figure 3-1 shows details about the USB cable. The cable has four wires: two power wires for Vcc and Gnd and two signal wires for D+ and D–. The cable end that attaches to the hub has a Series A connector, and the cable end that attaches to the new device is either connected directly (no connector) or has a Series B connector. Both connectors have longer power and ground connector pins to ensure that the device has good voltages before signals are applied.

The hub socket supplies Vcc and Gnd. The current limiter will initially prevent more than 100 mA from being drawn, even instantaneously, from the hub. If excess current is drawn, then the hub informs the host software of this error (see "Enumeration steps," step 5), an error message is displayed on the PC screen, and the device is **not** configured.

Because we haven't plugged in the I/O device yet, it is in the **unattached** state.

In Figure 3-1, note the two biasing resistors in the hub; they ensure that D+ and D– are low when no device is plugged in. There is a single biasing resistor on the device that is attached to either D+ or D–. When the USB cable is plugged in, the biasing resistor causes D+ or D– to rise above ground, and this changed voltage difference is recognized by the hub. We have detected a cable being plugged in! By convention, if the device-biasing resistor is connected to D+, we are informing the hub that this device is full speed (12 Mbps), while a biasing resistor on D– indicates a low speed (1.5 Mbps) device. Simple and effective!

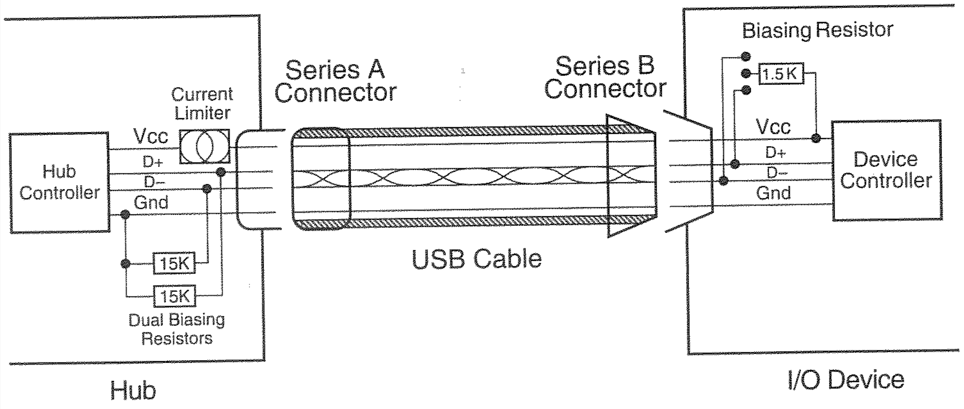


Figure 3-1. USB cable connection details

The I/O device is now in the **attached** state,
configured and operational, the device moves

The hub updates a STATUS_CHANGE regis
device and then waits to be told what to do.

The PC host controls the enumeration phase
requests to two devices. The hub that identifi
receive many requests for action, and the new
receive requests. If there are any other hubs b
they will not take part in this process. They w
bus, because that is one of their roles, but bec
by the PC host software during this process, t

The PC host software regularly polls all conn
In most cases a hub has nothing to report so w
this time the hub responds with the STATUS_
port has had a change in status—the PC host-b
begun!

ENUMERATION STEPS

In the following description the PC host is init
ToHub: prefix if the addressed device is the h
addressed device is the newly attached I/O dev

1. **ToHub:Get_Port_Status**: Host discover
2. **ToHub:Clear_Port_Feature(C_PORT_**
in the STATUS_CHANGE register that st
3. **ToHub:Set_Port_Feature(PORT_RESE**
a reset to the I/O device. The hub maintai
10 milliseconds. It then updates the RESE
PORT_CHANGE register and enables the
PORT_ENABLE bit in the PORT_STATU
register update causes an update to the ST
PC host will notice this on its next schedul
4. **ToHub:Get_Port_Status**: The PC host d

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