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United States Patent [19]

Wang et al.

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[54] **NETWORK CONTROLLER WHICH ENABLES THE LOCAL PROCESSOR TO HAVE GREATER ACCESS TO AT LEAST ONE MEMORY DEVICE THAN THE HOST COMPUTER IN RESPONSE TO A CONTROL SIGNAL**

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[73] Assignee: **Toshiba American Information Systems, Inc.**, Irvine, Calif.

[21] Appl. No.: **310,298**

[22] Filed: **Sep. 26, 1994**

[51] **Int. Cl.**[6] **G06F 13/00**

[52] **U.S. Cl.** **395/860**; 395/200.45; 395/200.59; 395/882; 395/836

[58] **Field of Search** 340/825.05; 360/69; 395/293, 500, 297, 200.43, 200.59, 860, 882; 380/3; 439/61

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Attorney, Agent, or Firm—Banner & Witcoff, Ltd.

[57] **ABSTRACT**

An application specific integrated circuit (ASIC)/field programmable gate array (FPGA) which is a component of a wireless LAN controller including a local processor and a memory enables the controller to interface with both PCMCIA™ and AT™ host computer systems. The ASIC/FPGA enables communication between a radio frequency communication module, a local processor, and the host computer. The ASIC/FPGA also includes a throttle feature that decreases the access of the host computer in comparison to access of the local processor in order to enable the local processor to rapidly generate an acknowledge signal as required by various RF LAN specifications. During operation of the controller, data to be transmitted by the host computer onto the network is written by the host to an SRAM via the ASIC/FPGA, and the host commands the local processor via the ASIC/FPGA to forward the transmitted data to the RF communication module. Under the control of the ASIC/FPGA, the local processor then forwards the transmit data from the SRAM to the RF communication module. When data is received from the RF communication module, the local processor, under the control of the ASIC/FPGA, receives the data and stores the received data in the SRAM. The received data is then forwarded to the host computer via the ASIC/FPGA.

28 Claims, 16 Drawing Sheets

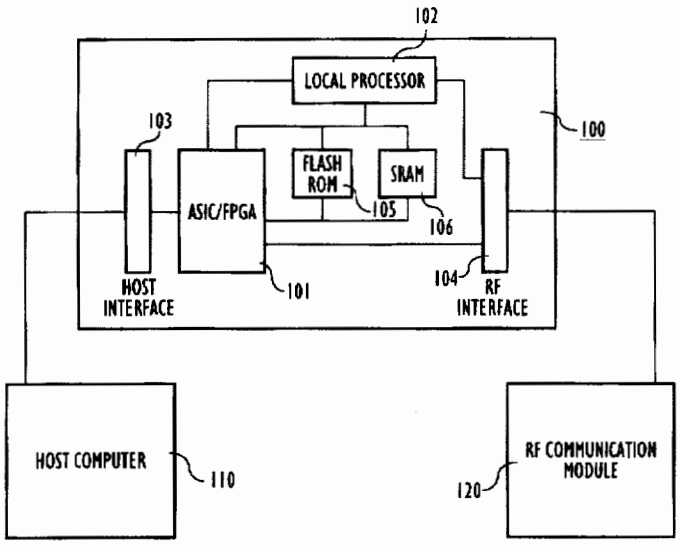

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FIG. 1

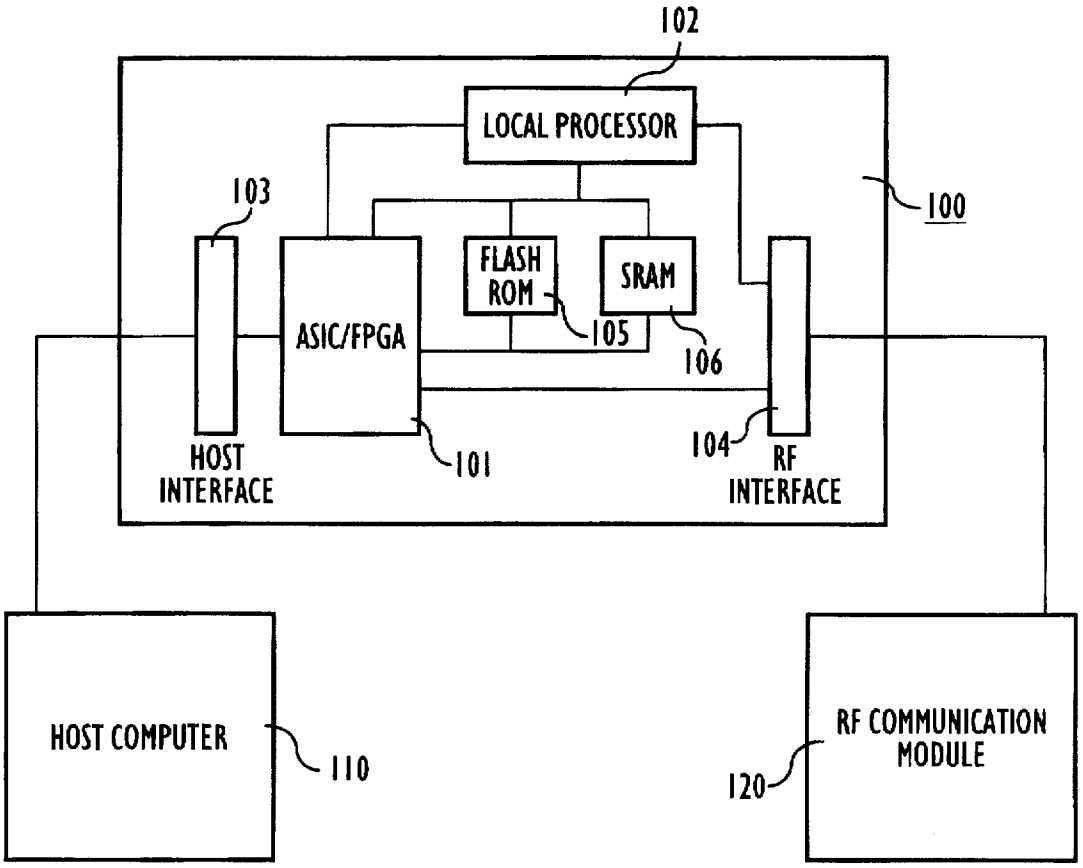

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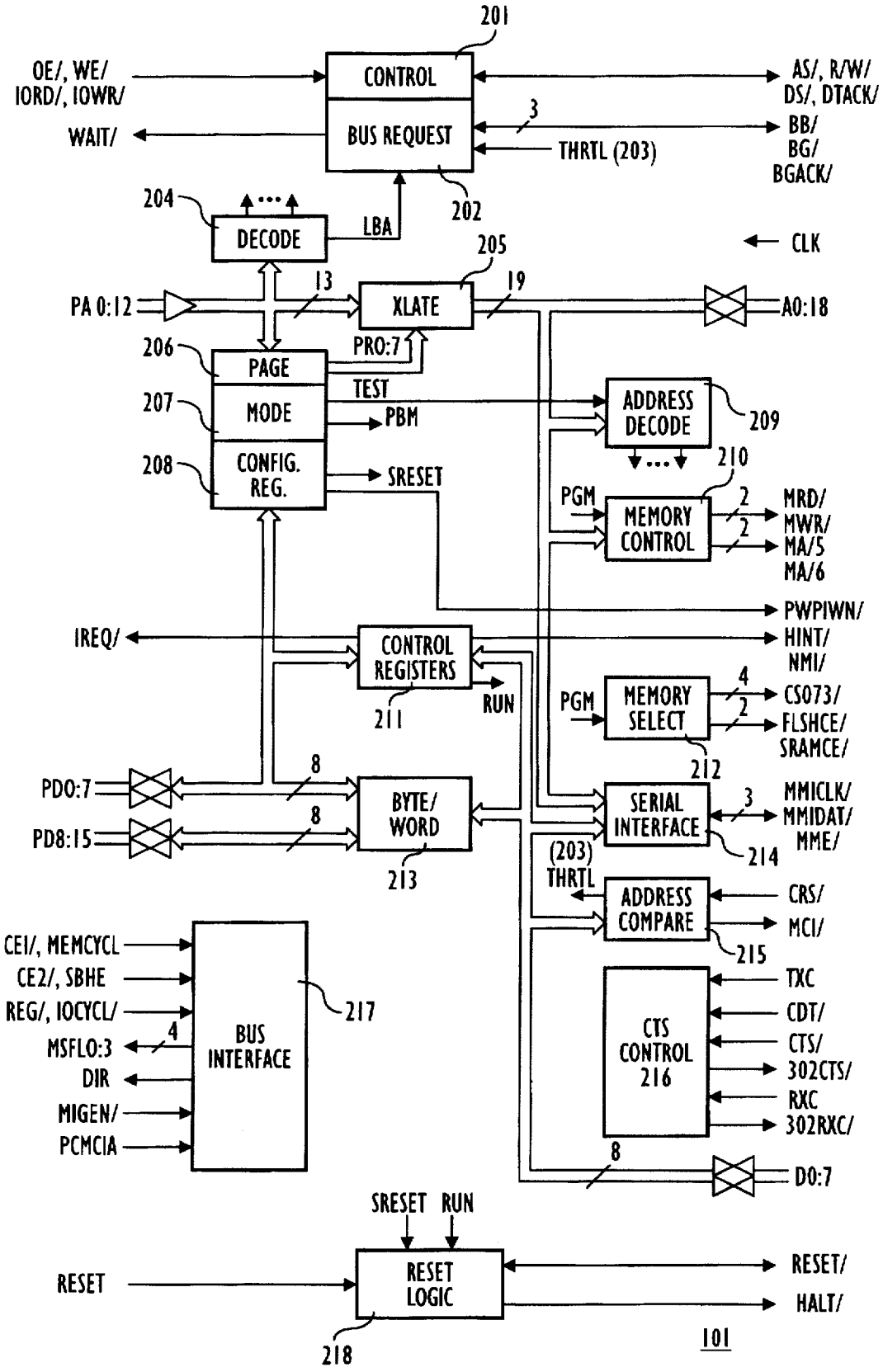
FIG. 2



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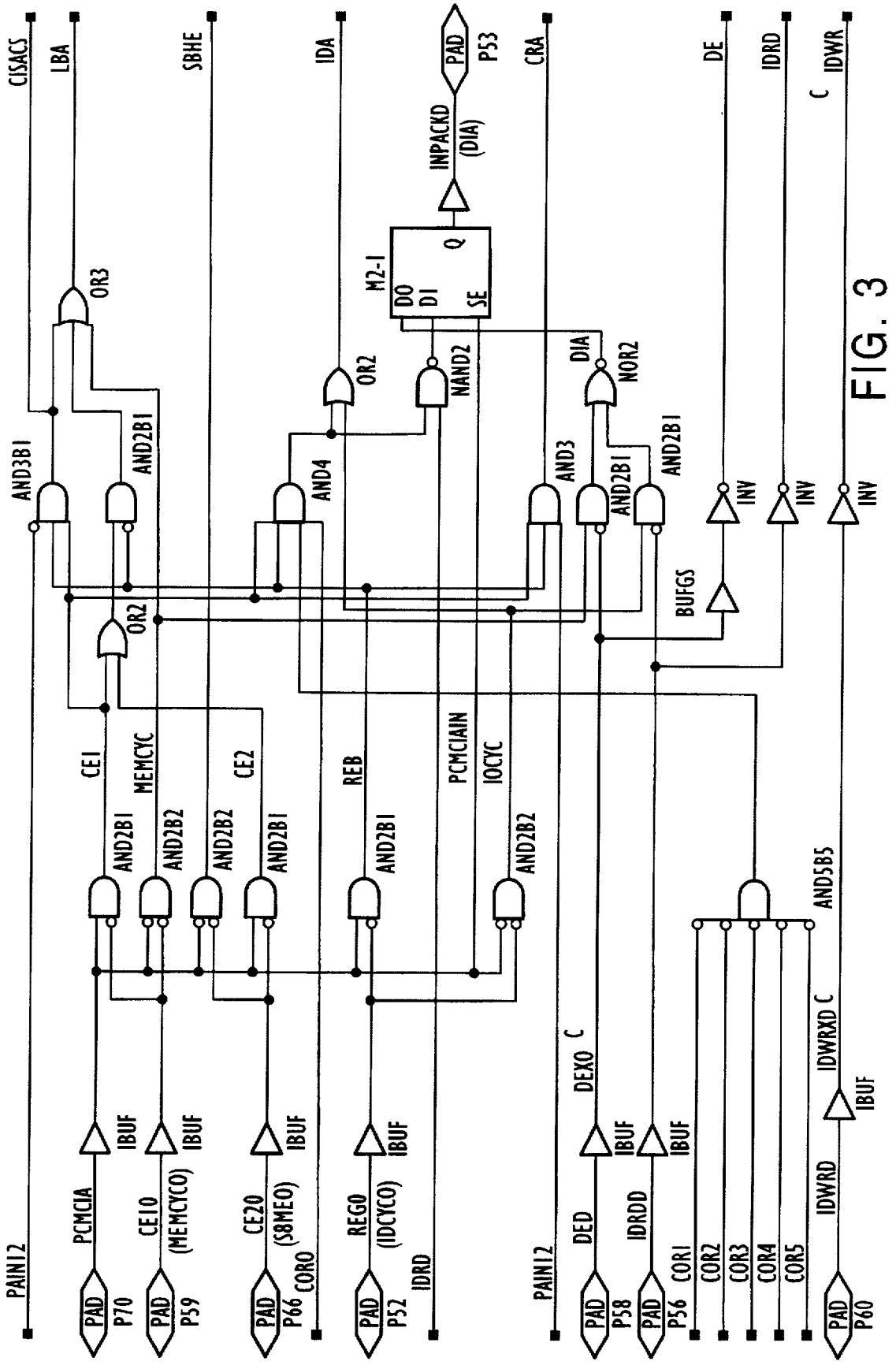

FIG. 3

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