

SYNCHRONOUS DRAM

MT48LC4M4A1/A2 S - 2 Meg x 4 x 2 banks
MT48LC2M8A1/A2 S - 1 Meg x 8 x 2 banks

FEATURES

- PC100-compliant, includes CONCURRENT AUTO PRECHARGE
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh (15.6µs/row)
- LVTTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- One- and two-clock WRITE recovery (^tWR) versions

OPTIONS

- Architectures
4 Meg x 4 **4M4**
2 Meg x 8 **2M8**
- WRITE Recovery (^tWR/^tDPL)
^tWR = 1 CLK **A1**
^tWR = 2 CLK (Contact factory for availability.) **A2**
- Plastic Package - OCPL
44-pin TSOP (400 mil) **TG**
- Timing (Cycle Time)
8ns; ^tAC = 6ns @ CL = 3 **-8B**
10ns; ^tAC = 9ns @ CL = 2 **-10**
- Part Number Example: MT48LC2M8A1TG-10 S

NOTE: The 16Mb SDRAM base number differentiates the offerings in two places: MT48LC2M8A1 S. The fourth field distinguishes the architecture offering: 4M4 designates 4 Meg x 4, and 2M8 designates 2 Meg x 8. The fifth field distinguishes the WRITE recovery offering: A1 designates one CLK and A2 designates two CLKs.

KEYTIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2*	CL = 3*		
-8B	125 MHz	-	6ns	2ns	1ns
-10	100 MHz	-	7.5ns	3ns	1ns
-8B	83 MHz	9ns	-	2ns	1ns
-10	66 MHz	9ns	-	3ns	1ns

* CL = CAS (READ) latency.

PIN ASSIGNMENT (Top View) 44-Pin TSOP

x4	x8				x8	x4
-	Vcc	□	1	44	□	Vss
NC	DQ0	□	2	43	□	DQ7
-	VssQ	□	3	42	□	VssQ
DQ0	DQ1	□	4	41	□	DQ6
-	VccQ	□	5	40	□	VccQ
NC	DQ2	□	6	39	□	DQ5
-	VssQ	□	7	38	□	VssQ
DQ1	DQ3	□	8	37	□	DQ4
-	VccQ	□	9	36	□	VccQ
-	NC	□	10	35	□	NC
-	NC	□	11	34	□	NC
-	WE#	□	12	33	□	DQM
-	CAS#	□	13	32	□	CLK
-	RAS#	□	14	31	□	CKE
-	CS#	□	15	30	□	NC
-	BA	□	16	29	□	A9
-	A10	□	17	28	□	A8
-	A0	□	18	27	□	A7
-	A1	□	19	26	□	A6
-	A2	□	20	25	□	A5
-	A3	□	21	24	□	A4
-	Vcc	□	22	23	□	Vss

Note: The # symbol indicates signal is active LOW. A dash (-) indicates x4 pin function is same as x8 pin function.

	4 MEG x 4	2 MEG x 8
Configuration	2 Meg x 4 x 2 banks	1 Meg x 8 x 2 banks
Refresh Count	4K	4K
Row Addressing	2K (A0-A10)	2K (A0-A10)
Bank Addressing	1 (BA)	1 (BA)
Column Addressing	1K (A0-A9)	512 (A0-A8)

16Mb (x4/x8) SDRAM PART NUMBERS

PART NUMBER	ARCHITECTURE
MT48LC4M4A1TG S	4 Meg x 4 (^t WR = 1 CLK)
MT48LC4M4A2TG S	4 Meg x 4 (^t WR = 2 CLK)
MT48LC2M8A1TG S	2 Meg x 8 (^t WR = 1 CLK)
MT48LC2M8A2TG S	2 Meg x 8 (^t WR = 2 CLK)

GENERAL DESCRIPTION

The Micron 16Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 16,777,216 bits. It is internally configured as a dual memory array (the 4 Meg x 4 is a dual 2 Meg x 4, and the 2 Meg x 8 is a dual 1 Meg x 8) with a synchronous interface (all signals are

GENERAL DESCRIPTION (continued)

registered on the positive edge of the clock signal, CLK). Each of the two internal banks is organized with 2,048 rows and either 1,024 columns by 4 bits (4 Meg x 4) or 512 columns by 8 bits (2 Meg x 8).

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The Micron 16Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the $2n$ rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

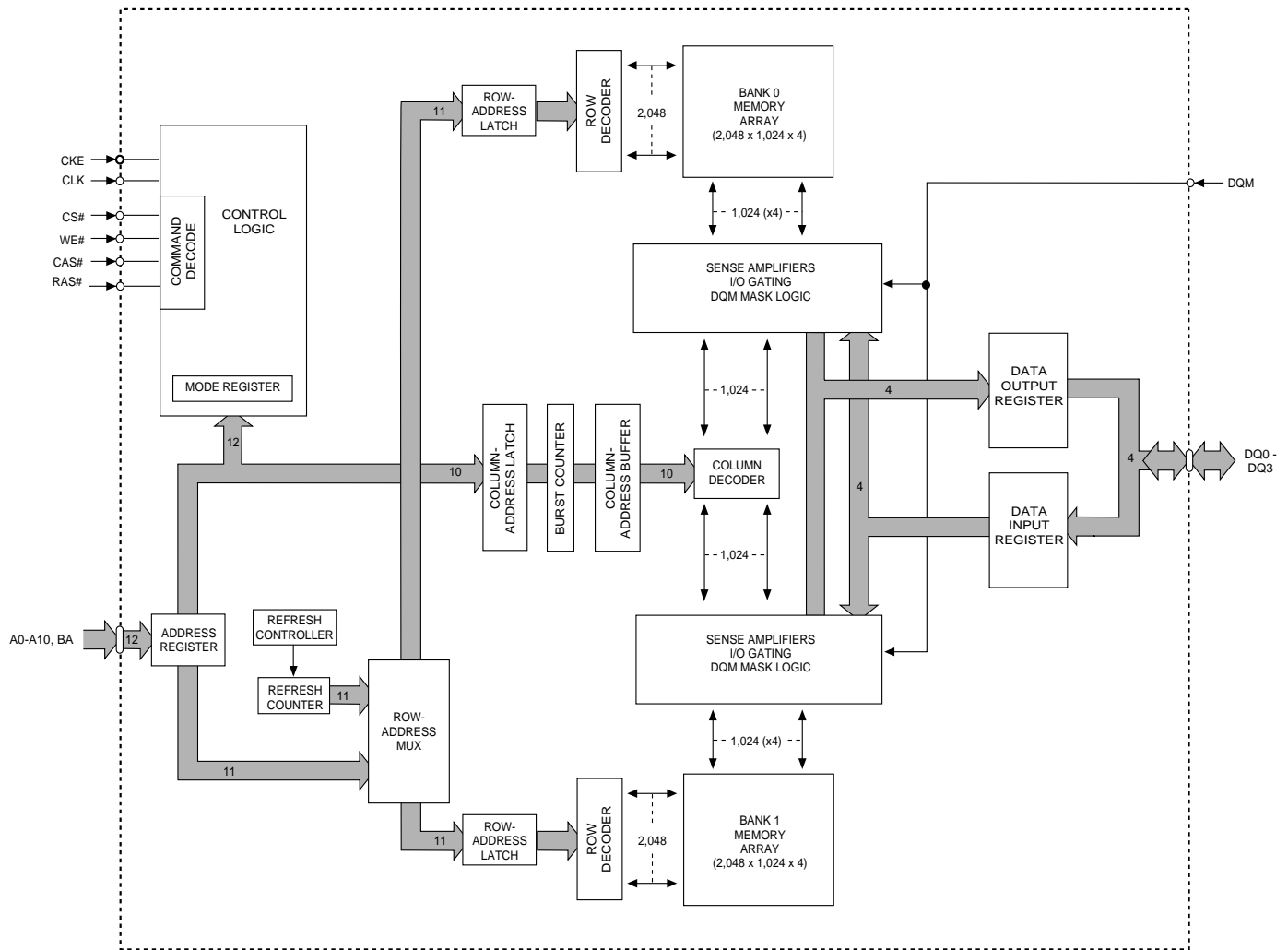
The Micron 16Mb SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

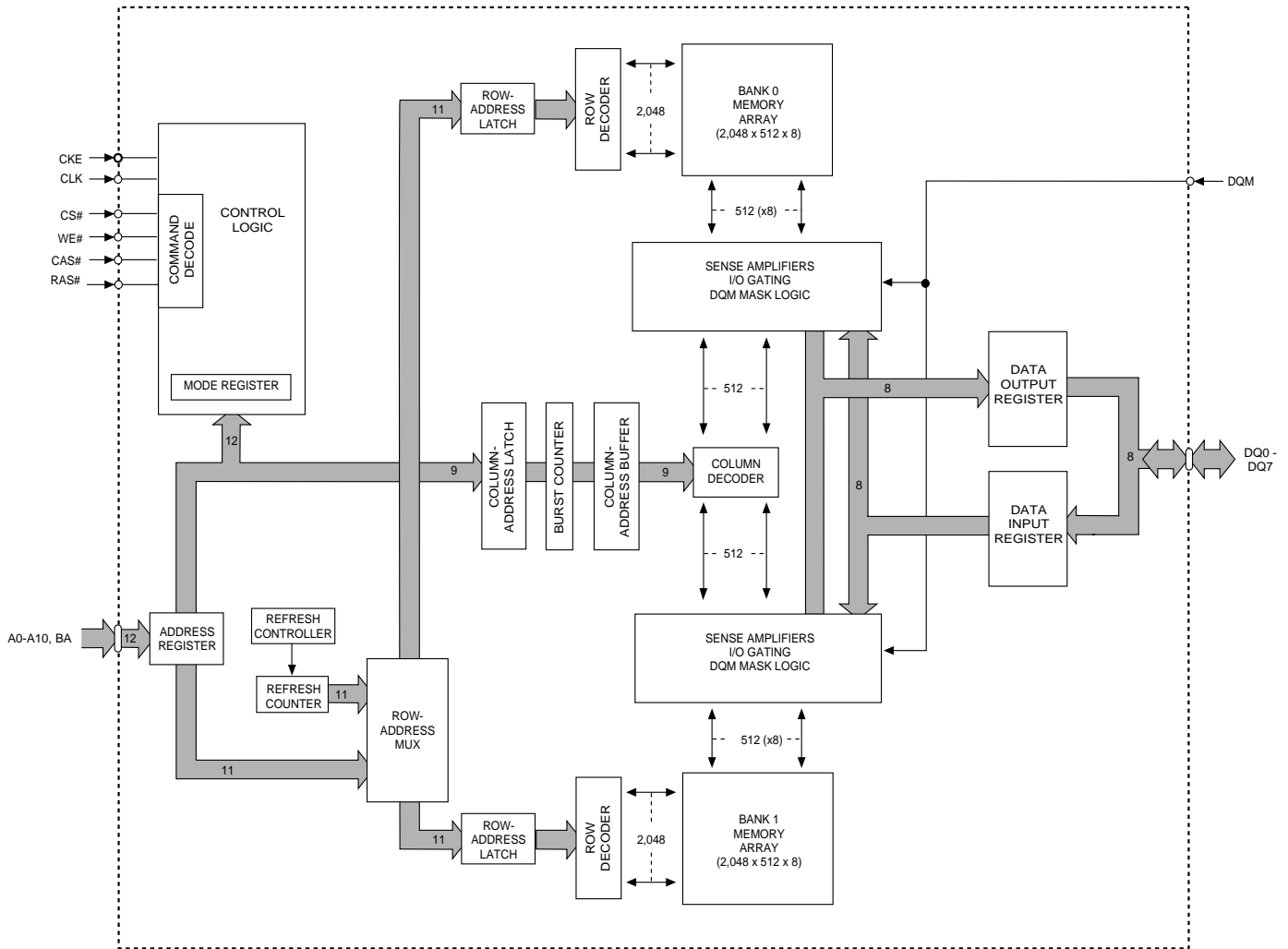
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**FUNCTIONAL BLOCK DIAGRAM
4 Meg x 4 SDRAM**



**FUNCTIONAL BLOCK DIAGRAM
2 Meg x 8 SDRAM**



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