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(54) **POWER MANAGEMENT ON A MEMORY CARD HAVING A SIGNAL PROCESSING ELEMENT**

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(52) **U.S. Cl.** **713/323**; 713/320; 713/322
(58) **Field of Search** 713/300, 320, 713/322, 323, 324, 500, 600

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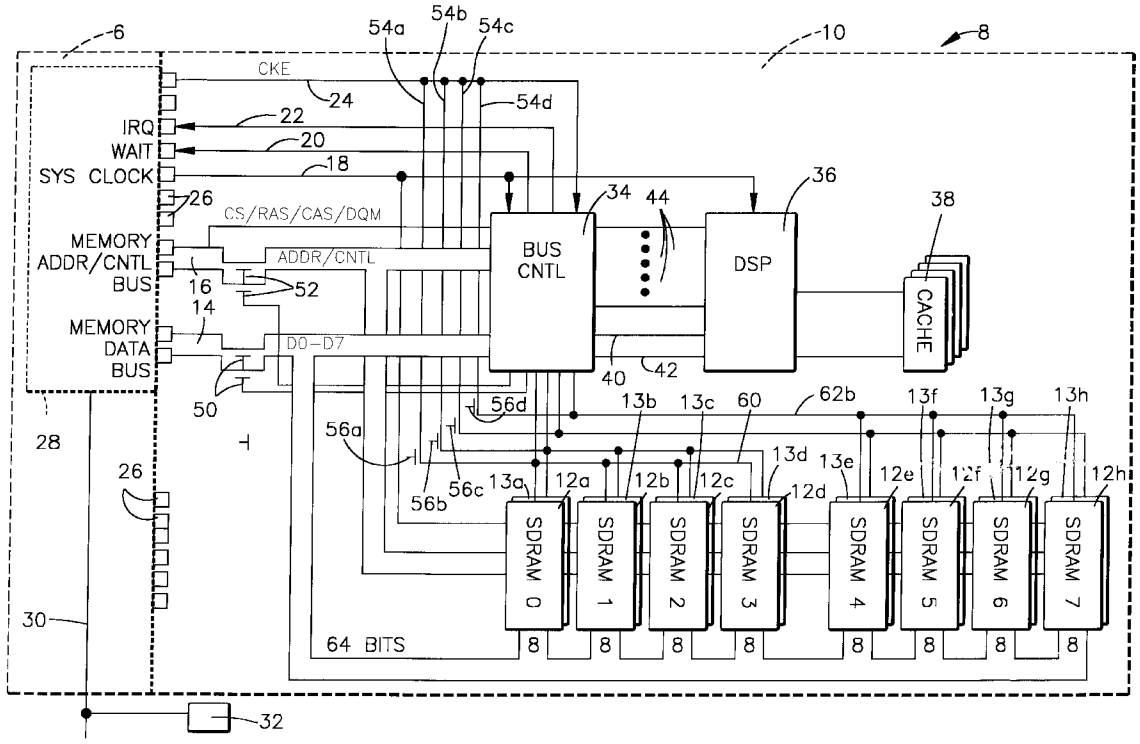
(57) **ABSTRACT**

An improved memory module and its use in a computer system is provided. The module includes a DSP first and second individually addressable banks of memory chips. The first bank is configured to function principally under the control of the signal processing element and the second bank is configured to function principally under the control of a system memory controller, although all the portions of each of the memory banks is addressable by both the signal processing element and the system memory controller. Both banks of memory chips can be placed in at least one higher power state and at least one lower power state by either the system memory controller or the DSP. The activity of each bank is sensed while in the higher power state, and the condition of each of the banks is sensed with respect to any activity during operation of the memory bank at the higher power state. The power state of each bank can be changed by either the signal processing element or the system memory controller responsive to preselected conditions of each bank. Each memory bank is returned to a predetermined known condition when changing from a lower power state to a higher power state. This is especially important when the memory bank assigned to the system controller is placed in another state by the DSP.

14 Claims, 3 Drawing Sheets



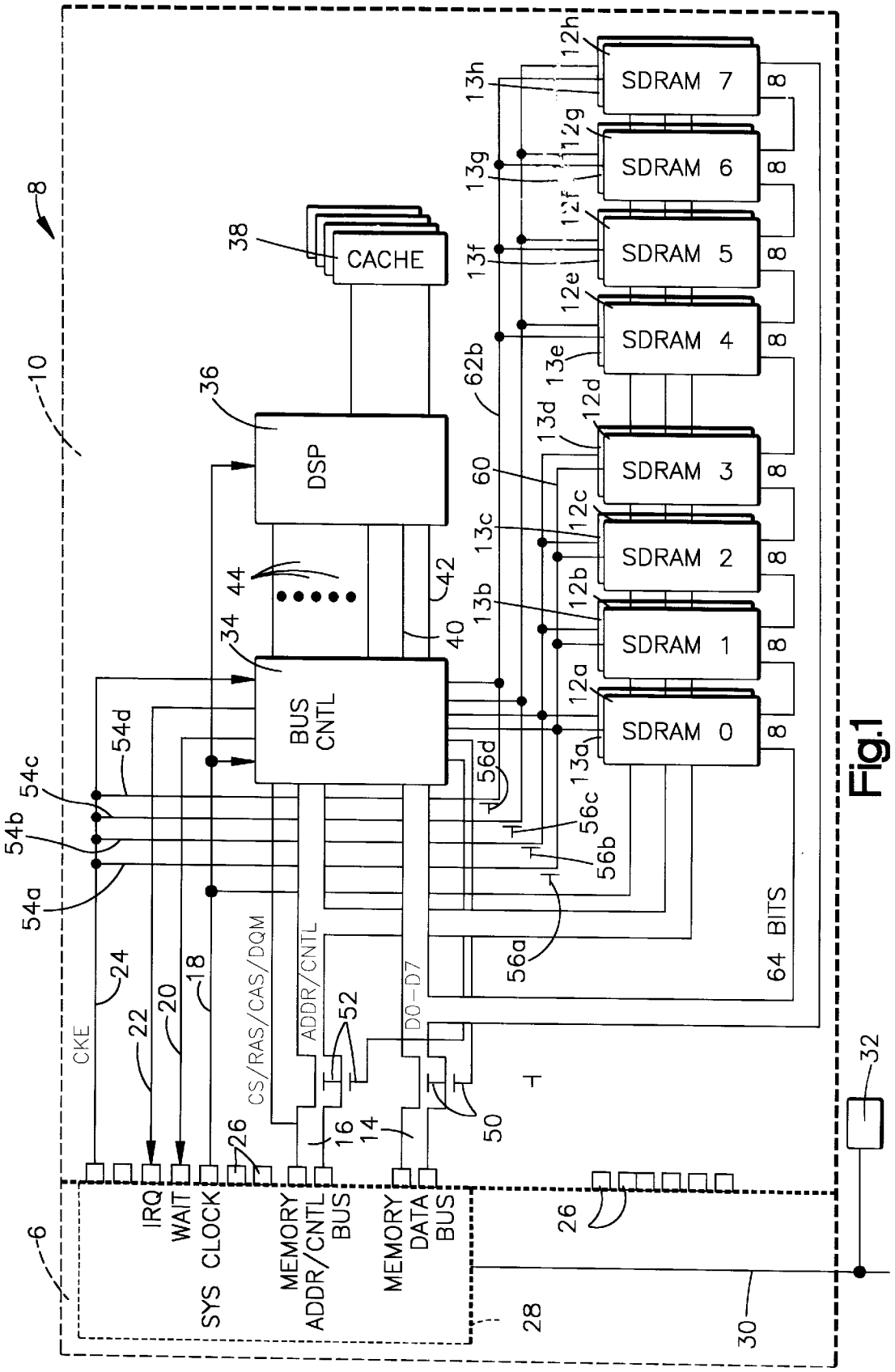


Fig.1

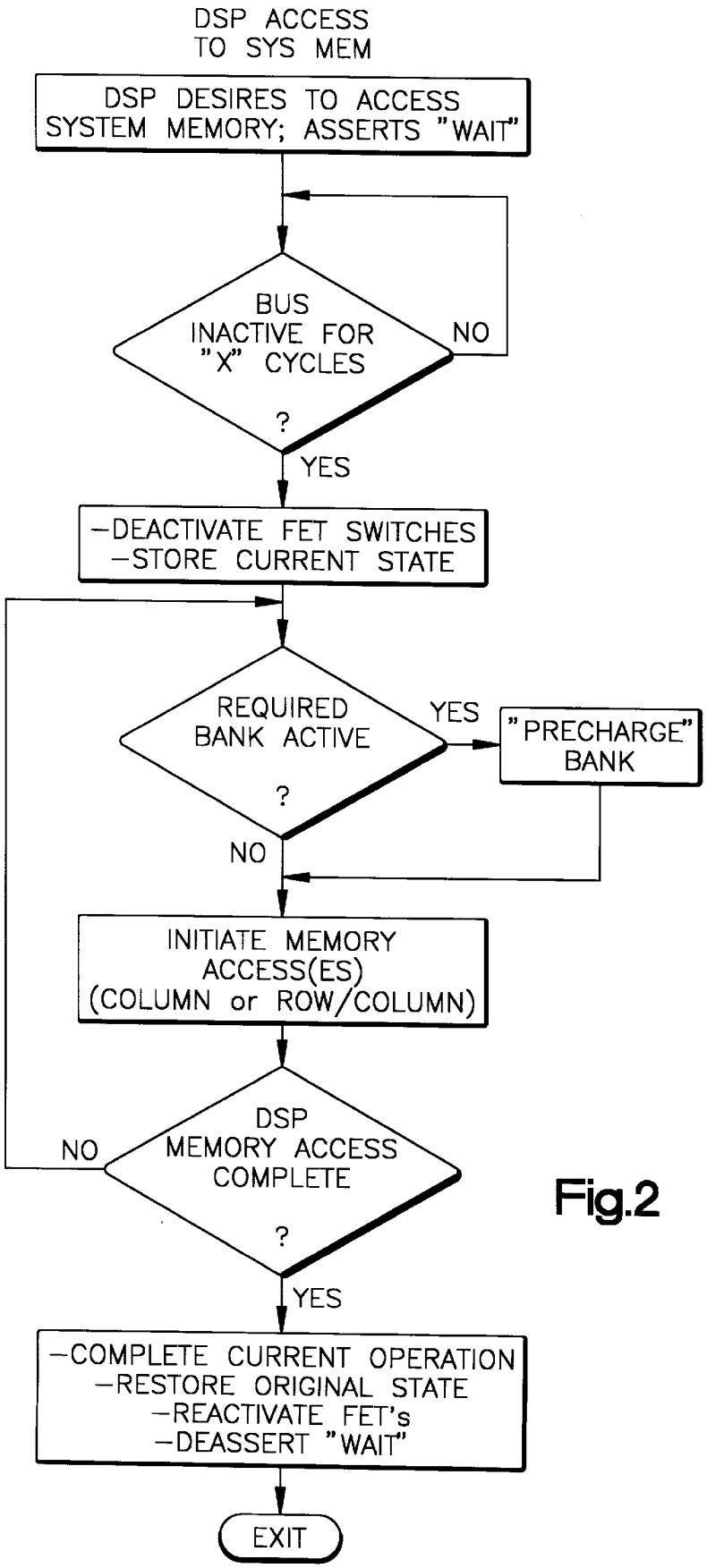


Fig.2

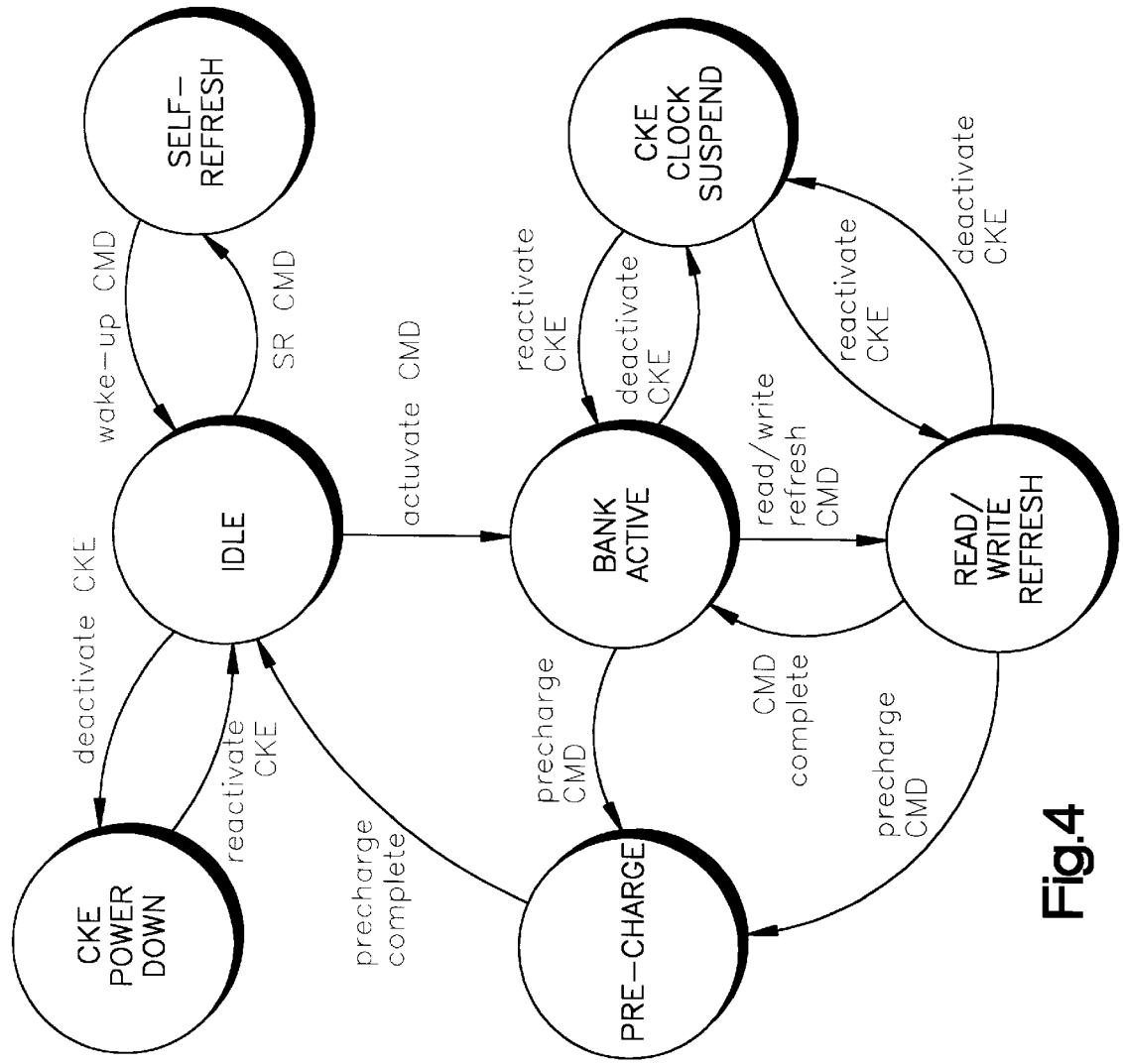


Fig.4

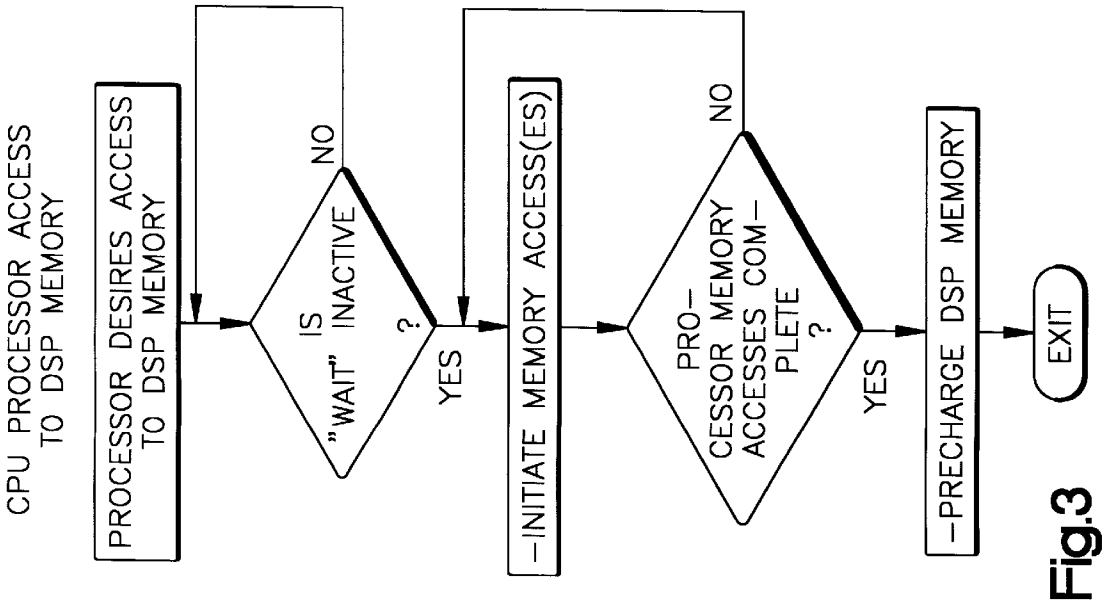


Fig.3

POWER MANAGEMENT ON A MEMORY CARD HAVING A SIGNAL PROCESSING ELEMENT

FIELD OF THE INVENTION

This invention relates generally to memory cards and their use in computer systems, and more particularly to the use in computer systems of memory cards having signal processing units on board and having at least one and preferably a plurality (i.e. at least two) of addressable banks of memory chips wherein at least a portion of at least one memory bank is individually addressable or activatable.

BACKGROUND ART

Memory cards such as SIMMs and DIMMs have increasingly more memory and more function being added thereto. Particularly, it has been proposed that signal processing elements such as digital signal processors (DSPs) be provided on board the cards to perform various functions independently of the system memory controller. These DSPs can operate on the memory when it is not being accessed by the system memory controller to perform various tasks.

This provides an inexpensive processor specific to each card to enhance the operation of the memory card. Additionally, as the amount of memory and the functions supplied on each card increase the power requirement for the card with large amounts of memory and more functions, this power requirement can be substantially increased. This is especially critical where the system is battery operated and/or the heat dissipation capability is limited. While the system memory controller generally is programmed to reduce the power level of the memory system, this is generally not a completely satisfactory solution since the memory controller operates on all of the memory cards and generally does not reduce the power state of the memory until the period of non-use amounts to a substantial period of time. Also the system memory controller is not normally programmed to operate on individual portions of memory banks. Thus there is a need for a memory card and system for the memory card to operate in a computer to selectively and expeditiously reduce power to individual banks of memory or portions thereof when the banks of memory or portion thereof are not being accessed by either the system memory controller or the DSP.

SUMMARY OF THE INVENTION

According to the present invention an improved memory card and its use in a computer system is provided. The card includes a signal processing element, preferably a DSP and at least one and preferably first and second individually addressable banks of memory chips. The first bank of chips or optionally a portion of the first bank of chips is configured to function principally under the control of the signal processing element and the second bank is configured to function principally under the control of a system memory controller in the computer system, although all the portions of each of the memory banks is addressable by both the signal processing element and the system memory controller. Both banks of memory chips or portion thereof can be placed in at least one higher power state and at least one lower power state by either the system memory controller or the DSP. The activity of each bank of memory and portion thereof is sensed while in the higher power state, and the condition of each of the banks of memory or portion thereof is sensed with respect to any activity during operation of the memory bank of memory at the higher power state. The power state of each bank of memory can be changed by either the signal processing element or the system memory controller responsive to preselected conditions of each bank. Each memory bank or portion thereof is returned to a predetermined known condition when changing from a lower power state to a higher power state. Preferably this condition is that condition, in the case of the memory bank under the control of the system memory controller that it was in following the last access by the system memory controller, and in the case of the memory bank or portion thereof under the control of the DSP, is a given preselected condition. This is especially important when the memory bank assigned to the system controller is placed in another state by the DSP.

DESCRIPTION OF THE DRAWINGS

FIG. **1** is a high level diagram of a computer system with a memory card according to this invention;

FIG. **2** is a flow diagram of the DSP access to system controller memory;

FIG. **3** is a flow diagram of the system CPU access to DSP controlled memory; and

FIG. **4** is a state diagram of the operation of the CPU memory.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawings and for the present to FIG. **1**, one embodiment of the present invention is shown as embodied in a personal computer **6**. A memory module **8** such as a DIMM or SIMM is provided which includes a printed circuit card **10** having a plurality of synchronous DRAMs (SDRAMs) **12***a*–**12***h* constituting a first bank of memory chips and **13***a*–**13***h* constituting a second bank of memory chips. The synchronous DRAMs **12***a*–**12***h* and **13***a*–**13***h*, are conventional SDRAMs. The SDRAMs of each bank **12** and **13** are divided into two sections or portions, **12***a*–**12***d* being **12** low, **12***e*–**12***h* being **12** high, **13***a*–**13***d* being **13** low and **13***e*–**13***h* being **13** high. Each of these sections is individually addressable and will be described presently.

The circuit card **10** has a memory bus which includes a memory data bus **14** and a memory address/control bus **16**. A system clock line **18**, a wait line **20**, an interrupt request line **22**, and a clock enable (CKE) line **24** are also provided. Memory data bus **14**, memory **4** address/control bus **16**, system clock **18**, wait line **20**, interrupt request line **22**, and clock enable line **14** are all connected to I/O connectors sometimes referred to as pins **26**. The I/O connectors **26** provide an interface to a system memory controller **28**, which is a part of the memory subsystem of computer **6**. The system memory controller **28** also controls a PCI bus **30** (and optionally other buses not shown). The PCI bus **30** has thereon devices such as a codec **32**.

The memory card **10** also has a memory bus controller **34** which is connected to the memory data bus **14**, the memory address/control bus **16**, the system clock **18**, the wait line **20**, the interrupt request line **22** and the clock enable line **24**. The bus controller **34** is connected to a signal processing element **36** which in the preferred embodiment is a digital signal processor (DSP). A particularly useful DSP is any one of the TMS 320C54X family manufactured by Texas Instruments, Inc. This particular DSP family includes an external cache memory **38**. The bus controller **34** and DSP **36** are interconnected by a chip address bus **40**, a chip data bus **42** and

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