

## (12) United States Patent Ooishi

(10) Patent No.:

#### (54) SEMICONDUCTOR MEMORY DEVICE WITH NORMAL MODE AND POWER DOWN MODE

- (75) Inventor: Tsukasa Ooishi, Hyogo (JP)
- (73) Assignee: Mitsubishi Denki Kabushiki Kaisha, Tokyo (JP)
- (\*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.
- (21) Appl. No.: 09/323,819
- (22) Filed: Jun. 2, 1999

#### (30) Foreign Application Priority Data

- Dec. 4, 1998 (JP) ..... 10-346051
- (51) Int. Cl.<sup>7</sup> ...... G11C 7/00

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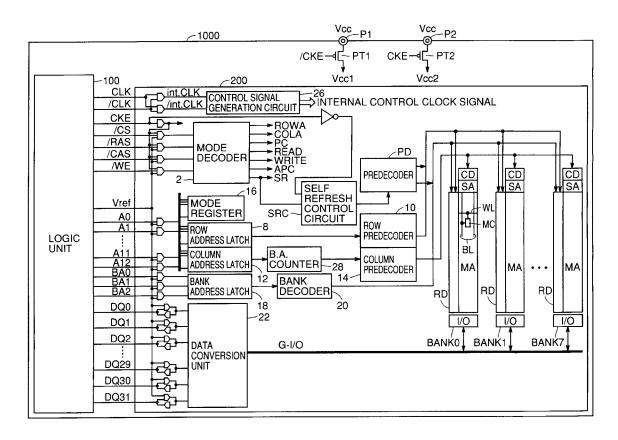
\* cited by examiner

Primary Examiner—David Nelms Assistant Examiner—Thong Le (74) Attorney, Agent, or Firm—McDermott, Will & Emery

#### (57) ABSTRACT

A semiconductor memory device includes a logic unit, a DRAM unit, and first and second PMOS transistors. In a normal mode, the first PMOS transistor is off and the second PMOS transistor is on, whereby power supply voltage is supplied to all the circuits. In a power down mode, the first PMOS transistor is on and the second PMOS transistor is off, so that power is not supplied to circuitry that is not required for a self refresh operation. Power supply voltage is provided to circuitry that is required for a self refresh operation. Thus, current consumption during self refresh can be reduced.

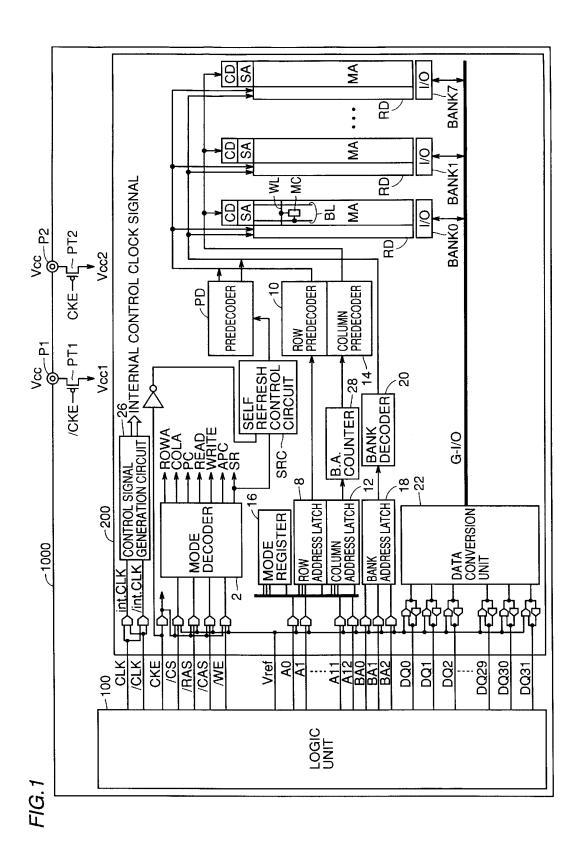
#### 16 Claims, 19 Drawing Sheets



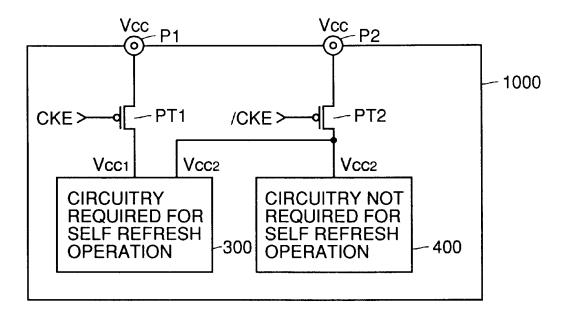
(45) Date of Patent: Jan. 9, 2001

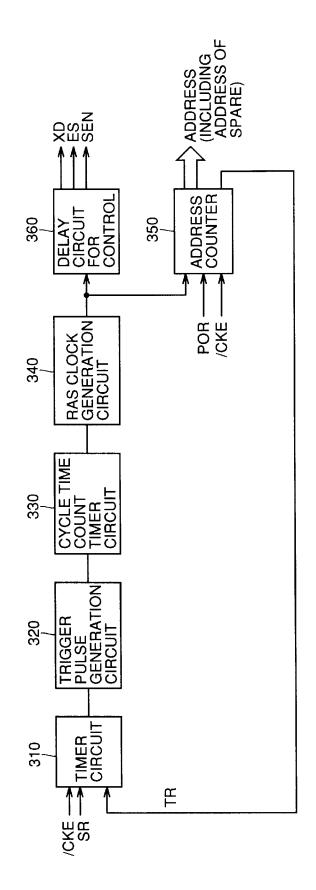
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Α



## FIG.2



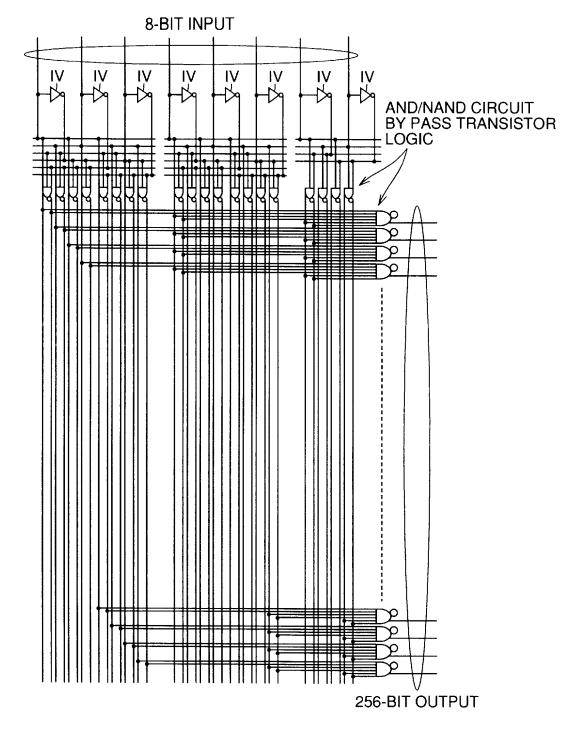


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FIG.3

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FIG.4



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