JEDEC STANDARD

CONFIGURATIONS FOR SOLID STATE MEMORIES

JEDEC Standard No. 21–C
Release 7

January 1997

ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT

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Published by

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Engineering Department
2500 Wilson Boulevard
Arlington, VA 22201

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JESD 21–C, Release 7 Insertion Instructions
Instructions for adding Release 7 to JEDEC Standard 21–C.
Inclosed with this instruction sheet are new and replacement pages for JEDEC Standard 21–C. Those pages which contain new material are labeled "Release 7" at the bottom of the page. In some cases, there will be old material on the back of the sheet containing a Release 7 page. This old material will be labeled Release 1, Release 2, Release 3, Release 4, Release 5. or Release 6 as there are no changes from the original release. All new text is marked by a "Revision Bar" in the outside margin in addition to the "Release 7" label in the inside footer of the page.

In this release, I have introduced a new feature in the Release #. In the past when an older sheet was replaced with a new one, either to make a correction, or to revise the original sheet, the new release number simply replaced the old number, thus loosing the information of the original release number. In this release, the old number will be retained followed by the letter "c" for correction, or "r" for revised, this followed by the new release number (e.f 4c7 or 6r7)

The following is a series of sheet by sheet instructions to be used to print the pages for this release. The instruction numbers correspond directly the instructions intended for the holders of the Standard. These are also included with the new originals for R–6. These instructions should be included as the first pages in Release 6. In the printing instructions, the Release # s are refered to as R#.
In the following 75 instructions, the material is arranged in 3 columns. The first column tells which sheet to remove from the 21–C binder. The second column tells which sheet to add to the binder. The third column gives an explanation of the reason for the change or addition.

REMOVE	ADD	REASON
1. Remove Cover Page	Add replacement Cover Page	Contains new Release level and date.
2. Remove Title Page;	Add replacement Title Page:	Contains revision Log for Standard.
3. Remove TOC, 8 sheets;	Add replacement TOC, 9 sheets;	Revised Table of Contents
4. Remove PP 2–3/4	Add replacement PP 2–3/4	New definitions added
5. Remove PP 2–5/6	Add replacement PP 2–5/6	
6. Remove PP 2–7/8	Add replacement PP 2–7/8	New material added.
7. Remove PP 2–9/10	Add replacement PP 2–9/10	New material added.
8. Remove P 3.5.1–3	Add replacement PP 3.5.1–3/4	New standards added
9.	Add new PP 3.5.1–33/34	New standard added
10. Remove P 3.5.2–3	Add replacement P 3.5.2–3	New standards added
11. Remove P 3.5.2–9	Add replacement PP 3.5.2–9/10	New devices added to existing standard.
12.	Add new P 3.5.2–11	New standard
13. Remove P 3.5.3–1	Add replacement P 3.5.3–1/2	Section re–orgainzed
14. Remove P 3.5.3–3/4	Add replacement PP 3.5.3–3/4	New standards added.
15. Remove P 3.5.3–5/6	Add replacement PP 3.5.3–5/6	New standard added
16. Remove P 3.5.3–7/8	Add replacement P 3.5.3–7/8	New standards added
17.	Add new P 3.5.3–9/10	New standards added
18.	Add new P 3.5.3–11/12	New standards added
19.	Add new P 3.5.3–13/14	New standards added
20.	Add new P 3.5.3–15	New standards added
21. Remove P 3.7.5–1/2	Add replacement PP 3.7.5–1/2	New standards added.
22. Remove P 3.7.5–3/4	Add replacement PP 3.7.5–3/4	New standards added.
23. Remove P 3.7.5–25/26	Add replacement PP 3.7.5–25/26	Errors corrected
24. Remove P 3.7.7–15/16	Add replacement PP 3.7.7–15/16	Errors corrected
25. Remove P 3.7.8–3	Add replacement P 3.7.8–3	Existing standard modified.

26.	Remove PP 3.7.8–9/10	Add replacement PP 3.7.8–9/10	New device added.
27.		Add new P 3.7.8–11	New standards added
28.	Remove P 3.9.1–15/16	Add replacement PP 3.9.1–15/16	New standards added.
29.	Remove P 3.9.2–3/4	Add replacement PP 3.9.2–3/4	New standards added.
30.	Remove PP 3.9.2–15/16	Add replacement PP 3.9.2–15/16	Modified drawing of existing standard.
31.	Remove PP 3.9.2–17/18	Add replacement PP 3.9.2–17/18	Modified drawing of existing standard
32.		Add new PP 3.9.2–19	New standard.
33.	Remove P 3.9.3–11/12	Add replacement P 3.9.3–11/12	Standard modified.
34.	Remove P 3.9.4–3/4	Add replacement PP 3.9.4–3/4	New standards added.
35.	Remove P 3.9.4–13/14	Add replacement PP 3.9.4–13/14	New standards added.
36.			
37.	Remove P 3.9.5–3	Add replacement P 3.9.5–3	New standards added.
38.	Remove P 3.9.5–15/16	Add replacement PP 3.9.5–15/16	New standard added.
39.	Remove P 3.10.3–1/2	Add replacement PP 3.10.3–1/2	New standards added.
40.	Remove P 3.10.3–5/6	Add replacement PP 3.10.3–5/6	Correct error.
41.		Add new PP 3.10.3–9	New standards added.
42.	Remove PP 3.10.4–3/4	Add replacement PP 3.10.4–3/4	New standards added
43.	Remove PP 3.10.4–17/18	Add replacement PP 3.10.4–17/18	New standards added
44.	Remove PP 3.10.4–19/20	Add replacement PP 3.10.4–19/20	New standards added
45.		Add new PP 3.10.4–21	New standards added
46.	Remove P 3.11.2–1	Add replacement P 3.11.2–1	New standard added.
47.	Remove P 3.11.2–3/4	Add replacement PP 3.11.2–3/4	Existing standard modified.
48.		Add new PP 3.11.2–5	New standards added
49.	Remove P 3.11.3–1	Add replacement P 3.11.3–1	New standard added.
50.	Remove P 3.11.3–3/4	Add replacement PP 3.11.3–3/4	Existing standard modified, new standard added.
51.		Add new PP 3.11.3–5	New standards added
52.	Remove P 3.11.4–1	Add replacement P 3.11.4–1/2	Standards revised.
53.	Remove P 3.11.4–3/4	Add replacement PP 3.11.4–3/4	Standards revised.
54.	Remove P 3.11.4–5/6	Add replacement PP 3.11.4–5/6	Standards revised.
55.	Remove P 3.11.4–7/8	Add replacement PP 3.11.4–7/8	Standards revised, correct error.
56.		Add new PP 3.11.4–9	New standards added.
57.	Remove PP 3.11.5–7/8	Add replacement PP 3.11.5–7/8	Correct error.
58.	Remove PP 3.11.5–9/10	Add replacement PP 3.11.5–9/10	Terminology corrections.

Section 4 on Modules has been completely re–organized. Remove and discard all of the old pages from Section 4 and replace them with the new ones supplied. No sub–dividers are supplied, but it will enhance the usability of the section by adding your own dividers. The individual sheets are not listed here as they are supplied in correct order for insertion.

CONFIGURATIONS FOR SOLID STATE MEMORIES

Formulated under the cognizance of Committees JC–42.1, PLD devices, JC–42.3, volatile memories, JC–42.4, non–volatile memories, and JC–42.5, memory modules and cards, and approved by the JEDEC Council.

Standard 21–C Revision Log.

Release 1, August 1990

Release 2, September 1991

Release 3, November 1992

Release 4, November 1993

Release 5, February 1995

Release 6, January 1996

Release 7, January 1997

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1. BACKGROUND

This standard is a compilation of all memory device standards that have been developed by the JC-42 Committee and approved by the JEDEC Council through September, 1989. Many of the standards were originally published in JEDEC Publication 102, and JEDEC Standard 21 and its addenda 21-1, 21-2, and 21-3. These documents were superseded by Standards 21-A and 21-B which combined all previous and newly approved standards, using a more coherent and consistent format designed for ease of use by the memory user. Emphasis was placed on the family compatibility and interchangeability characteristics of the various standard devices. Standard 21-A was supplemented later with an Addendum, Standard 21-A-1 that included all standards approved through June 1986. Standard 21-B, which continued with the same organization, was published in December 1988.

When the earlier standards were adopted, there were separate BIPOLAR and MOS standards and devices. In addition, the device characteristic of prime interest was the data word length. Previous issues of Std. 21 recognized these factors and were organized accordingly. Advancements in semiconductor technology and computer design needs have changed the way in which the standards are used. In recognition of these changes, Std. 21-C is substantially different from previous issues. The material is organized primarily by function (ROM, EPROM, SRAM, DRAM, etc.) rather than by technology and word length. The distinction between BIPOLAR and MOS has been eliminated. They are then arranged by interface level (TTL, ECL) and word length. Footnotes are included to identify those standards which were adopted by the BIPOLAR Committee JC-42.1.

Previous issues of Std. 21 were published as either free-standing documents or addenda to previous issues. This made it difficult to update because a new document was created for each issue. Std. 21-C has been changed from this free-standing form to a loose-leaf format. As a result new standards can be issued as supplementary sheets much earlier.

The MOS devices have evolved as several families of compatible parts. Within a family, there is a high degree of compatibility. This compatibility exists between devices of a similar function but with varying capacities as well as between devices with different functions. These compatible families fall into four categories as a function of the number of bits in the data interface. They are: (1) bit wide, (2) nibble wide, (3) byte wide, (4) word wide. In addition, a series of multi-chip modules have been introduced and standardized. These modules have capacities up to many megabits and data interface widths ranging from 1 bit up to 36 bits.

The most widely encountered family is the Byte-wide group. The Table in Figure 1 shows this group, arranged by capacity and device type. In general, the 24 pin, the 28 pin, and the 32 pin devices are compatible in the areas of pin overlap. The 28 pin family was conceived to allow the use of an orderly progression of devices in a system design from the lower capacity 24 pin devices to the higher capacity 28 pin devices without requiring that the system or circuit board be redesigned. The 32 pin devices were developed recently as a means of securing additional address pins to accommodate the larger device capacities that became technically feasible.

In addition, the various device types were configured to allow the use of a progression of devices with varying degrees of data permanence (and ease of alteration) as the system design progresses. For example, the system could be designed to initially use STATIC RAM that could be replaced later by EPROM and still later by ROM as the system firmware becomes stabilized.

A new class of memory devices has been introduced to the industry and is represented in this standard. This is the multiport DRAM (MPDRAM), also known as "Video Ram" because of the most common application for the devices.

Separately, the family compatibility concept has been applied to the Bit, Nibble, and Word wide memory devices. In several cases, there are special optional features that have been standardized. These are included in the sections with the devices to which they apply.

In this issue of Std. 21, a new family of SRAMs is introduced which addresses the increasing need for high speed. These devices use centered and multiple power pins which allow the ultimate device speed to be achieved. This family includes a wide range of device architectures including bit, nibble, and byte wide data interfaces. In addition, these pinouts have been approved for both TTL and ECL interfaces.

The standards developed by the BIPOLAR Committee, JC-42.1, have evolved in a different pattern. Numerous small families have been developed, each with a specific function, and within a specific technology group such as TTL, 10K-ECL, and 100K-ECL. The Tables in Figures 3 and 4 give a summary of the PROM and RAM standards developed by the this group.

The early standards, were for Dual-In-Line Packages (DIP). More recently, Chip Carrier (CC) standards for the same devices have been adopted. This standard now includes additional families of devices in the SOJ and ZIP packages. The Tables in Figures 1-4 show these multiple device standards. Dimensional drawings for the packages referenced in the memory device standard have been published in JEDEC Publication 95.

Many of the terms that were used in some of the earlier parts of Standard 21 are now considered obsolete. A current set of terms has been included in this revision. These terms are consistent with IEEE Standard 662/1981 which has been endorsed by the JEDEC Committee JC-42. This terminology is also consistent with JEDEC Standard 100.

The terms presented are organized in essentially the same way in which they appeared in Std. 21-B.

Standard 21-C is organized differently from Standard 21-A and 21-B. The sections of the standard are as follows:

2. Terms and Definitions
3. Single Memory Devices
4. Multi-Chip Memory Modules
5. Programmable Logic and Application Specific Devices
6. Other Applicable Documents

The standards given in section 3 are ordered using the following priorities:

1-Functionality (in order of decreasing data permanence)
2-Device word length (1, 4, 8, or 16 bits)
3-Interface level (TTL, ECL)
4-Package configuration (DIP followed by Chip Carrier, SOJ and ZIP)
5-Package size
6-Device capacity

The standards given in section 4 are ordered using the following priorities:

1-Module Functionality
2-Module pin count
3-Family relationship
4-Device word length (1 to 18 bits)

2 TERMS AND DEFINITIONS

This section contains listings and definitions of a number of terms that are needed for a clear understanding of the standards as presented. Most of these terms have been developed within the semiconductor memory industry and are not covered by JEDEC Standard 100. They are, however, not in conflict with this standard which contains all JEDEC approved definitions.

The following pin names and functional descriptions apply uniformly to all devices covered by this standard. Where a pin has a dual–function, and those functions are invoked at substantially different times, the names and symbols for the functions are separated by a slash (/)(e.g., VPP/G\). Where a pin has multiple functions which are used interspersed at essentially the same time, the slash is omitted(e.g., DQ). Where multiple pins have a similar function, a number symbolized as (n) is appended to the symbol. Where the pin function has an inverted logic sense, that is, the function is true or invoked for a low signal, the overbar or trailing reverse slash (\) is appended to the symbol. Where alternative functions are allowed by the standard, the allowed functions are listed separated by commas. Where common usage has resulted in two terms being used interchangeably, both are listed but the the order of listing indicates the order of preferred usage. For example, $\overline{CAS}$ is preferred to $\overline{CE}$.

Following the list of PIN definitions, there are a series of other terms and definitions that are required for a clear understanding of the individual device standards.

In addition to the standard terms that are commonly used in a broad range of devices, there are names that are specialized and used only with a single class of device. These terms are included in separate sections of the standard as their usage becomes commonplace. In the current release, names for MPDRAM, Memory Cards, and SRAM are included.

2.1 CONVENTIONAL DEVICE PIN NAMES

The following signal names are those that are used over a broad range of devices described in this standard. Specialized pin names that are used for a specific class of device are given is separate sections of Chapter 2 of this standard. All pin names may be either positive or negative logic as defined in the individual device standards. Logic polarity is not given here unless it is inherent in the definition.

2.1.1 – A, PORT A

In dual port memory devices, the two ports are designated port A & port B. The letter A or B is appended as a suffix to any pin that is specific to one or the other of the ports.

2.1.2 – A(n), ADDRESS INPUTS

Those inputs that select (address) a particular cell or set of cells within a memory array for presentation on the device outputs. The integer (n) serves to differentiate the address inputs, one from another. When the address numbering is significant for device operation, the addresses are numbered, beginning with 0.

2.1.3 – ADQ(n), ADDRESS DATA INPUT/OUTPUT

The pins that are multiplexed three ways to serve as address input, data input, and data output pins. When the address data input/output numbering is significant for device operation, the addresses are numbered, beginning with 0.

2.1.4 – AL, ADDRESS LATCH ENABLE

An input that when true, allows the input address to be entered into a register, and when false, causes the address state previously entered to be latched.

2.1.5 – B, PORT B

In dual port memory devices, the two ports are designated port A & port B. The letter A or B is appended as a suffix to any pin that is specific to one or the other of the ports.

2.1.6 – BA, BANK ADDRESS

In a RAM that has multiple banks in its architecture, the BANK ADDRESS is used, to select any one of the available banks.

2.1.7 – BG, BYTE MODE ENABLE

An input that when true, causes a word wide device to operate in the byte mode and to present the high or low byte on a pre–defined data pin set. Truth tables will be provided to define the details of the operation.

2.1.8 – BS, BLOCK SELECT

A group of input signals that enable individual bit blocks of the data interface.

2.1.9 – BY, BUSY

The output that, on some devices, signifies that some internal asynchronous operation is still in process, and that the device is not available for normal functions. This signal is normally implemented so that multiple devices can be OR–tied.

2.1.10 – C, OUTPUT CLOCK

The input, on some devices that contain an output data register, that causes the data to be set into the register.

2.1.11 – CA, COLUMN ADDRESS

In an address multiplexed DRAM, the address field that is captured by the COLUMN ENABLE clock CAS\. When the column address numbering is significant for device operation, the addresses are numbered, beginning with 0.

2.1.12 – CAS, (CE), COLUMN ENABLE

An enable signal that on some dynamic RAMs actuates only the column oriented internal circuits and the data input/output circuits. Most devices normally require the RAS\ signal to be present for the CAS\ signal to be effective. In some newer designs, however, special sequences of the RAS\ and CAS\ signals are used to actuate certain special device control functions. In devices that have a CAS\ per output, the CAS\s are numbered beginning with 0. In devices that have a CAS\ per byte, the CAS\s are designated LCAS\ & UCAS\ for 2 byte devices. LCAS\ affects DQ0⇒DQ7, and UCAS\ affects DQ8⇒DQ15. For devices with a CAS\ per byte, and have more than 2 bytes, the CAS\s are numbered beginning with 0. In modules that have a CAS\ per byte, the CAS\s are numbered beginning with 0. CAS0\ affects DQ0⇒DQ7, CAS1\ affects DQ8⇒DQ15, CAS2 affects DQ16⇒DQ23, and CAS4\ affects DQ24⇒DQ31.

2.1.13 – CK, INPUT AND OUTPUT CLOCK

An input that controls the activation of both input and output circuitry, normally storage registers or latches.

2.1.14 – CKE, CLOCK ENABLE

In certain synchronous memory devices, a logic level input that enables the clock input and allows it to fulfill its defined function.

2.1.15 – CL, Clear

An input that, when true, causes all cells in the memory array to be cleared to their zero state.

2.1.16 – D(n)(x), DATA INPUT

Those inputs whose state represents the value of data that is to be written into the selected address on a write cycle of an alterable memory device. When the numbering of the data inputs is significant for device operation, the data inputs are numbered beginning with 0. In devices where data bit groupings have independent control, an additional suffex "x" is applied. "x" takes the values of a, b, c, etc.

2.1.17 – DC, DIAGNOSTIC CLOCK
The input that, on some devices, invokes and controls any built–in diagnostic test features.

2.1.18 – DQ(n)(x), DATA INPUT/OUTPUT
The pins that serve as data output(s) when in the read mode and as data input(s) when in the write mode. When the device is not selected or enabled, the output(s) are in a floating state. On a devices having both serial and parallel access ports, these pins provide access to the parallel RAM port data channels. The suffix (n) is a numeric value indicating the number assignment of a particular pin with numbering starting at 0. In some situations the letters U or L are used to indicate that the pins are assigned to the upper or lower byte of a 2 byte data interface. In devices where the standard supports an optional 9th bit that may be used as a parity bit, the suffix P may be used in lieu of a numeric value. In devices where data bit groupings have independent control, an additional suffex "x" is applied. "x" takes the values of a, b, c, etc.

2.1.19 – DQM, INPUT/OUPUT DATA MASK
A control signal used primarily on SDRAMs that acts as as mask for reading and writing functions. In some instances, the DQM term will includes a prefix "U" or "L" indicating upper or lower byte control. In devices where more than two data bit groupings have a data mask applied, a "x" is applied where "x" takes the values of a, b, c, etc.

2.1.20 – E, CHIP ENABLE
The input that, when true, permits active operation including the input and/or output of data, and when false, prevents active operation and causes the memory to be in a reduced power standby mode with the outputs floating.

2.1.21 – F, REFRESH
An input that, when true, causes the device to enter a data refresh mode.

2.1.22 – G(n), OE(n), OUTPUT ENABLE
The input that, when false, disables the outputs and causes them to go to an inactive state, but that does not effect the writing function. When disabled, the inactive state is floating (Z), for MOS and TTL devices and low (L), for ECL devices. In modules that have multiple OEs, the OEs are numbered beginning with 0.

2.1.23 – GS, SYNCHRONOUS OUTPUT ENABLE
An output enable input that must be set in by a synchronizing clock signal, K (q.v.).

2.1.24 – $\overline{I}$, INITIALIZE INPUT
A control input that provides a preassigned Manufacturer or User defined code to be set into the data register. If the input is all "0", it can be called "clear", and if all "1", then "preset".

2.1.25 – ID(n), IDENTIFICATION
A group of output terminals, nominally used to convey information about the configuration or other attributes of the device when plugged into a system. The function of these outputs are similar to those of the PD(n) terminals but they often have different electrical interface chatacteristics.

2.1.26 – I/O, INPUT/OUTPUT
A generic term for otherwise undefined signal pins which can have either an input and/or an output function. This term is not used as a specific pin name, only as a generic indicatior of the nature of the function of the pin.

2.1.27 – $\overline{IS}$, INITIALIZE INPUT (SYNCHRONOUS)
A control input that provides a preassigned Manufacturer or User defined code to be presented to the data register for subsequent setting by a clock input. If the input is all "0", it can be called "clear", and if all "1", then "preset".

2.1.28 – K, INPUT CLOCK
The input that, on devices that contain input buffer registers, causes the address on the A(n), the data on the D(n) pins and/or certain control inputs to be set into the register.

2.1.29 – L, LATCH ENABLE or LOWER BYTE
An input that, on devices containing a latch register, causes the data to be latched into the register. When L is used in conjunction with a data or control term it signifies that the combined term applies to the lower byte of a two byte data interface device (e.g. $\overline{LW}$).

2.1.30 – LB, LOWER BYTE ENABLE
An input, on wordwide devices, that, when true, enables the lower byte data input/outputs, pins DQ0 through DQ7.

2.1.31 – LW, LOWER BYTE WRITE ENABLE
An input, on wordwide devices, that when true causes the data present on the lower byte input/output, terminals DQ0 through DQ7, to be written into the addressed cells of the device.

2.1.32 – M(n), M, MODE SELECT, MASK
Input signals that when true select an alternative mode of operation for the device. The alternative modes available must be defined in the applicable device standard. When M is used in conjuction with other symbols to create a new pin name, it signifies that the pin function is either MASK or MODE related.

2.1.33 – MA, MATCH
An output signal that when true indicates that there has been a match (logic compare equal) between data stored in the memory and data presented on a set of input pins as defined in the individual device standard.

2.1.34 – MCH, MUST CONNECT HIGH
A pin which must be connected to a voltage that is interpreted as logic high or "true" signal.

2.1.35 – MCL, MUST CONNECT LOW
A pin which must be connected to a voltage that is interpreted as logic low or "false" signal.

2.1.36 – NC, NO CONNECTION
A pin to which no internal electrical connection is present or allowed.

2.1.37 – NE, NON–VOLATILE ENABLE
The input, on a NVRAM, that enables the non–volatile functions ST & RC as determined by the states of S,E,G, and W.

2.1.38 – NF, NO FUNCTION
An input that is electrically connected to the device but for which the signal has no function in the device operation.

2.1.39 – NP, NO PIN
A pin position on a package where the pin has been purposely been left blank or removed after assembly. No physical pin is allowed in this position.

2.1.40 – NU, NOT USABLE
A device pin to which there may or may not be an internal connection but to which no external connections are allowed.

2.1.41 – OE,(n), G(n) OUTPUT ENABLE
The input that, when false, disables the outputs and causes them to go to an inactive state, but that does not effect the writing function. When disabled, the inactive state is floating (Z), for MOS and TTL devices and low (L), for ECL devices. In modules that have multiple OEs, the OEs are numbered beginning with 0.

2.1.42 – OP, OPTIONAL
The designation for pins on which the manufacturer has the freedom to supply a specialized function not previously defined in the standard, and still have his part meet the requirements of the standard.

2.1.43 – P, PROGRAM or PROGRAM ENABLE, PARITY
The input on a non–volatile memory device that, when true, causes the data present on the D or DQ pins to be written into the addressed cell(s) of the device. The letter P may also be used as a suffix for data pins where an optional 9th bit, that may be used for parity, is allowed by the standard (e.g. DQP)

2.1.44 – PD(n), PRESENCE DETECT
A group of output pins, normally used on modules or cards, whose state is used to convey information about the capacity, speed, configuration, or other attributes of the device when plugged into a system.

2.1.45 – PR, PAGE RESET
The input on a page select memory that, when true, unconditionally causes the page select address register to be reset to zero and the corresponding page to be selected.

2.1.46 – PS, PAGE SELECT
The input on a page select memory that, when true, causes one of the pages of memory to be selected as identified by the inputs on the DQ pins (as defined in the appropriate function table) and for this page address to be stored in an internal register.

2.1.47 – Q(n)(x), DATA OUTPUT
The outputs whose state represents the data read from the selected cells. When the device is not selected or enabled, the outputs are usually in a floating (Z, high impedance) state. When the numbering of the data outputs is significant for device operation, the data outputs are numbered beginning with 0. In devices where data bit groupings have independent control, an additional suffex "x" is applied. "x" takes the values of a, b, c, etc.

2.1.48 – RA, ROW ADDRESS INPUT
In an address multiplexed DRAM, the address field that is captured by the ROW ENABLE signal, RAS\. When the numbering of the row address numbering is significant for device operation, the RA are numbered beginning with 0

2.1.49 – RAS, (RE) ROW ENABLE INPUT
A chip enable signal that, on certain dynamic RAMs, actuates only row address oriented internal circuitry. In modules that have multiple RAS\s, the RAS\s are numbered beginning with 0.

2.1.50 – RC, RECALL
The input on a NVRAM, that transfers the non–volatile data into the RAM array.

2.1.51 – RFU, RESERVED FOR FUTURE USE
A terminal whose function is not currently defined, but which is intended to be defined in some future enhancement of this Standard. This terminal should not be used (either internally or externally) until it has been further defined.

2.1.52 – RSVD, RESERVED
In a family of standards where some devices in the family are subsets of others, terminals that are defined in some devices but not used in others. To allow for upgradeability, the unused terminals are "RESERVED" to prevent their being used. NC has often been used in similar situations.

2.1.53 – RY, READY
The output that, on some devices, signifies that no internal asynchronous operations are still in process, and that the device is available for normal functions. This signal is normally implemented so that multiple devices can be OR–tied. This signal is the inverse of BY (RY=$\overline{BY}$)

2.1.54 – S(n)(x), CHIP SELECT
The input(s) that, when any one is false, causes the device to be disabled without any significant change in the power consumption. When deselected, the outputs go to the inactive state (floating (Z) for MOS and TTL devices and low (L)

for ECL devices), and the device becomes insensitive to a write command. In devices where data bit groupings have independent control, an additional suffex "x" is applied. "x" takes the values of a, b, c, etc.

2.1.55 – ST, STORE
The input, on a NVRAM, that initiates the non–volatile data storage of the entire RAM array.

2.1.56 – Sxx, SYNCHRONOUS FUNCTION
On a synchronous memory device, any input terms that are synchronous with a clock should start with the letter S. For example: $\overline{SG}$ = Synchronous Output Enable, $\overline{SW}$ = Synchronous Write Enable.

2.1.57 – $\overline{TF}$, TEST FUNCTION
The input, on a MEMORY that, when true, causes built in on–chip test logic to be actuated and for the part to go into its test mode of operation.

2.1.58 – U, UPPER BYTE
When U is used in conjunction with a data or control term it signifies that the combined term applies to the lower byte of a two byte data interface device (e.g. UW).

2.1.59 – UB, UPPER BYTE ENABLE
An input that, on wordwide devices, when true, enables the upper byte data input/outputs, pins DQ8 through DQ15.

2.1.60 – UW, UPPER BYTE WRITE ENABLE
An input, on wordwide devices, that, when true, causes the data present on the upper byte input/output, terminals DQ8 through DQ15, to be written into the addressed cells of the device.

2.1.61 – WE, W, WRITE ENABLE
The input that, when true, causes the data present on the D or the DQ pin(s) to be written into the address cell(s) of the device. In devices that have a WE per byte, the WEs are designated LWE & UWE for 2 byte devices. In devices that have a WE per byte and more that two bytes, the WE are numbered beginning with 0. In modules that have multiple WEs, the WEs are numbered beginning with 0.

2.2 MULTIPORT DRAM PIN NAMES

The following pin names apply primarily to specialized function pins for MPDRAM. In some situations, the names may also be applicable to other types of memories such as Graphics DRAMs.

2.2.1 – DSF, SPECIAL FUNCTION ENABLE INPUT
The input on a device, that when true, actuates certain special operational functions. In devices and modules that have multiple DSFs, the DSFs are numbered beginning with 0.

2.2.2 – DT/$\overline{OE}$(n), $\overline{TRG}$(n), DATA TRANSFER/OUTPUT ENABLE INPUT
The input on a device having both serial and parallel access ports that, depending on the state of one or more of the other control lines of the device, either enables an internal data transfer between the serial and parallel port circuitry, or enables the data outputs of the parallel port.

2.2.3 – QSF, QSY, TRANSFER ACKNOWLEDGE OUTPUT
The output on a device having both serial and parallel access ports which signifies that a transfer of data from the parallel to the serial port, in certain special transfer cycles, has been completed. In devices and modules that have multiple QSFs, the QSFs are numbered beginning with 0.

2.2.4 – SC, SERIAL CLOCK
An input, on devices having a serial data access port, that actuates the serial transfer of data, either in or out.

2.2.5 – SDQ(n)(x), SERIAL DATA INPUT/OUTPUT
The pins, on a device having a serial data access port, that serve as serial data output(s) when in the read mode and as serial data inputs(s) when in the write mode. When the device or the serial port is not selected or enabled, the output(s) are in a floating (Z) state. When the numbering of the serial data input/outputs is significant for device operation, the serial data input/outputs are numbered beginning with 0. In devices where data bit groupings have independent control, an additional suffex "x" is applied. "x" takes the values of a, b, c, etc.

2.2.6 – SE, SERIAL PORT ENABLE
The input that, when true, actuates the device's serial access circuitry.

2.2.7 – SG, SERIAL PORT OUTPUT ENABLE
The input that, when true, actuates the device's serial data output circuitry.

2.2.8 – SQ(n), SERIAL DATA OUTPUT
The pins, on a device having a serial data access port, that serve as serial data output(s) when in the read mode, When the device or the serial port is not selected or enabled, the output(s) are in a floating (Z) state. When the numbering of the serial data outputs is significant for device operation, the serial data outputs are numbered beginning with 0.

2.2.9 – $\overline{TRG}$(n), DT/$\overline{OE}$(n) DATA TRANSFER/OUTPUT ENABLE INPUT
The input on a device having both serial and parallel access ports that, depending on the state of one or more of the other control lines of the device, either enables an internal data transfer between the serial and parallel port circuitry, or enables the data outputs of the parallel port.

2.3 POWER PIN NAMES

The following symbols are used to designate the power pins in a memory device. When only a single pin is provided for a given supply, the pin name is used without suffix. When multiple pins are used, a suffix may be used to designate specific pins. A numeric suffix is used to indicate the preferred order of implementation when optional redundant pins are allowed. An alphabetic suffix is used to indicate pins which have a specific power circuit or loop connection. The use of a common suffix for different supplies indicates that those pins connect to a common power loop.

2.3.1 – VBB, SUBSTRATE POWER VOLTAGE

A bias voltage that maintains the substrate at a potential which is negative with respect to GND or VSS in an NMOS or CMOS part.

2.3.2 – VCC, LOGIC POWER VOLTAGE

The most positive potential of the two logic power supply pins. This is used for the memory device power voltage when the supply voltage is nominally 5 V. VCC is also commonly used to designate the ground reference power supply voltage for ECL interface devices.

2.3.3 – VCCQ, OUTPUT STAGE LOGIC POWER VOLTAGE

See VDDQ for definition. VCCQ is restricted to 5 V applications only

2.3.4 – VDD, DRAIN POWER VOLTAGE

The primary power voltage on MOS devices that require a potential that is different from the normal system logic voltage. This is used interchangeably with VCC on devices that use 5 V.

2.3.5 – VDDQ, OUTPUT STAGE DRAIN POWER VOLTAGE

The power pin that is intended to feed power to the output transistors of the device to supply the potential and energy to drive the load applied to the data output (Q) pins or data input/output (DQ) pins. Other, non–data, output pin transistors may also be designated to be fed by this power pin. VDDQ/VCCQ may be specified to have the same or a different potential from that feeding the primary device power pins (VDD/VCC) but is DC isolated on the chip from these and any other chip power pins.

2.3.6 – VEE, EMITTER POWER VOLTAGE

For ECL interface devices, the primary and most negative power supply terminal.

2.3.7 – VHH, SPECIAL FUNCTION ENABLE VOLTAGE

A special high voltage logic level (super voltage) that enables special on–chip functions.

2.3.8 – VPP, PROGRAMMING POWER VOLTAGE

A special high voltage supply that supplies the potential and energy for altering the state of certain non–volatile memory arrays. On some devices the presence of VPP also acts as a PROGRAM ENABLE signal (see P).

2.3.9 – VREF, REFERENCE POWER SUPPLY

A power supply that acts as a reference for determining internal threshold voltages but does not supply any substantial power to the device.

2.3.10 – VSS, (GND), GROUND REFERENCE or SOURCE POWER VOLTAGE

The ground reference voltage for NMOS, CMOS, and TTL devices, commonly the reference pin for all other device pins. VSS is normally the system ground and the symbol is often used interchangeably with GND.

2.3.11 – VSSQ, (GNDQ), OUTPUT STAGE SOURCE POWER VOLTAGE or OUTPUT STAGE GROUND REFERENCE

The ground reference voltage for the data output (Q) or input/output (DQ) pins. Other, non–data, output pin transistors may also be designated to be referenced to this ground pin. Internal to the device, this pin shall be DC isolated from the primary ground reference (VSS) pin and any other ground reference pin. External to the device it must be DC common with the primary ground reference.

2.4 DEVICE TYPE NAMES

2.4.1 – ASIC, Programmable Application Specific Device
A complex array of logic elements whocs interconnection pattern can be field programmed to fill the needs of specific applications.

2.4.2 – BDRAM, Burst DRAM
A DRAM that has BURST mode data capability.

2.4.3 – Bxxx,
Device names that have the prefix "B" are devices that have a "Burst" data capability.

2.4.4 – DPM, Dual Port Memory
Any memory that has two essentially identical data ports.

2.4.5 – DPSRAM, Dual Port Static RAM
A static RAM that contains two sets of identical random access address and data ports.

2.4.6 – DRAM, Dynamic Random Access Memory
These devices are made using Dynamic RAM circuit configurations that have data storage that must be refreshed periodically.

2.4.7 – FEEPROM, Flash EEPROM
An EEPROM in which clearing can be performed only on blocks or the entire array.
Note: there are no restrictions on the block archetecture in the fefinition of FEEPROM. the blocks within a device may be of various capacities ranging from a single address to the entire memory array.

2.4.8 – EEPROM, Electrically Erasable Programmable Read Only Memory
A reprogammable ROM in which cells may be erased electrically and in which each cell may be reprogrammed electrically.

2.4.9 – EPROM, Erasable Programmable Read Only Memory
A reprogrammable ROM in which all cells may be simultaneously erased using ultraviolet light and in which each cell may be reprogrammed electrically.

2.4.10 – GRAM, Gaphics DRAM
A DRAM that contains special graphics features, similar to those contained in a MPDRAM. When the term has a prefix "S", it becomes synchronous GRAM.

2.4.11 – LPROM, Latched PROM
A PROM that contains a latch register for the output data.

2.4.12 – MPDRAM, Multiport DRAM
A dynamic RAM that contains in addition to the conventional random access data and address port, a serial access port that allows serial access to a portion of the stored data in a way which is independent of the normal RAM data terminals and in which simultaneous serial and random operations may be executed. This type of memory has been referred to as "Video RAM" because of its primary field of application.

2.4.13 – MPM, Multiport Memory
Any memory array that has two or more data ports which do not have the same architecture. The most common form of MPM is one in which there is a random access port and a serial access port.

2.4.14 – MPRAM, Multiport RAM
A RAM that has more than one port for data, address, and control, that are not identical in nature. Normally at least one port provides parallel access while one other provides serial access. When the term has a prefix "S", it becomes s synchronous MPDRAM.

2.4.15 – NVRAM, Non–Volatile Random–Access Memory
An SRAM in which provisions exist on chip for the state of the cells to be saved when power is removed.

2.4.16 – PLD, Programmable Logic Array
An array of logic elements in which the interconnection pattern can be programmed (either mask or user programmed) to perform specific logic functions.

2.4.17 – PROM, Programmable Read–Only Memory
A field programmable ROM which can have the data content of each cell altered only once.

2.4.18 – PSRAM, Pseudo Static Random–Access Memory
A combinational form of dynamic RAM that incorporates various refresh and control circuits on–chip (e.g. refresh address counter and multiplexer, interval timer, and/or arbiter). These circuits allow the PSRAM operating characteristics to closely resemble those of a SRAM.

2.4.19 – RAM, Random–Access Memory
A memory in which access to all storage data can be achieved in essentially the same time, independent of the location. In a multiport memory, this term refers to that portion of the array which contains the memory cell array and its drivers, sense amplifiers, and control circuitry and the circuitry associated with the normal random access data port.

2.4.20 – ROM, Read–Only Memory
A memory in which the contents are not intended to be altered during operation.

2.4.21 – RPROM, Registered PROM
A PROM that contains a "D" type FF register for the output data.

2.4.21 – Sxxx
The prefix "S" on a device term can mean either "Static" as in SRAM, "Serial" as in SAM, or "Synchronous" as in SDRAM and SGRAM.

2.4.22 – SAM, Serial Access Memory
A memory (or serial port in a multiport memory) in which data is accessed sequentially and the time for access depends on the location of the data desired. In a multiport memory, this term refers to that portion of the device which is related to the serial access port and its associated functions.

2.4.23 – SDRAM, Synchronous DRAM
A DRAM that has a clocked synchronous interface.

2.4.24 – SGRAM, Synchronous Graphics DRAM
A GRAM that has a synchronous interface.

2.4.25 – SMPDRAM, SVRAM, Synchronous MPDRAM (VRAM)
An MPDRAM that has a synchronous interface on all ports.

2.4.26 – SRAM, Static Random Access Memory
A read/write memory in which the data is retained in the absence of control signals generated inside or outside the integrated circuit.

2.4.27 – SSRAM, Synchronous Static RAM
An SRAM that has input and/or output buffers (either register or latch), that are controlled by an externally supplied clock (or clocks).

2.4.28 – VRAM, Video Ram
A term commonly used in the Industry to describe the device class referred to in this standard as MPDRAM. It is a multi–ported DRAM that has features keyed to the video buffer application

2.5 MISCELLANEOUS DEVICE RELATED TERMS

2.5.1 – Bit Plane
In a semiconductor memory device having a data interface that is wider than 1 bit, those storage cells and associated circuitry which are associated with a given bit in the data interface.

2.5.2 – Bit Wide
A class of memory devices that have only a single–bit data interface.

2.5.3 – Byte Wide
A class of memory devices that have a parallel 8–bit or occasionally 9–bit data interface.

2.5.4 – K
When describing the storage capacity of a memory device the quantity K=1024 is used.

2.5.5 – M
When describing the storage capacity of a memory device, the quantity M=2 exp 20 or 1024 K is used.

2.5.6 – MX, Multiplexed
A term describing a device that has pins used for different purposes at different times as a function of one or more of its control inputs. The signal groups that are multiplexed onto a common pin set are given together as in: AA MX signifying ADDRESS, ADDRESS multiplex, OR ADQ MX signifying ADDRESS, DATA IN, DATA OUT multiplex.

2.5.7 – Nibble Wide
A class of memory devices that have a parallel 4–bit data interface. This term should not be confused with "nibble mode" (see 3.1.3.2), which refers to a serial data access mode in memories.

2.5.8 – Word Wide
A class of memory devices that have a parallel 16–bit or longer data interface.

2.6 Special Operational Cycles for MPDRAM

The following terms describe a series of special operational cycles for MPDRAM. They are presented in the order of their logical relationships rather than alphabetically.

2.6.1 LOGIC SETUP, (LS)

A special non-memory cycle in which the logic state of the device is set up to actuate the desired mode of operation for future memory cycles. The selected mode is normally persistent until canceled by some subsequent special control cycle.

2.6.2 INTERNAL REFRESH, (CBR)

Defined in 3.9.2.3.

2.6.3 WRITE TRANSFER, (WT)

An operation in which the data to be written is introduced through the serial port and is then transferred internally to the memory array data bus for writing into the cells. At the same time the "Tap Pointer" is set. This is a counter that defines the starting point in the serial register into which data is entered. Data is entered serially from this point with wrap around when the end of the register is reached. The contents of the full serial register are transferred in parallel. In addition to the normal write transfer, there are numerous other types of special write transfers defined in the following paragraphs.

2.6.4 PSEUDO WRITE TRANSFER, (PWT)

This is a non-memory cycle in which the operational mode of the serial port is changed from output to input. At the same time the "Tap Pointer" is set. This is a counter that defines the starting point in the serial data register into which data is entered. Data is entered serially from this point with wrap around when the end is reached.

2.6.5 MASKED WRITE TRANSFER, (MWT)

A write transfer in which the transfer of new data from the serial register into the memory array is controlled by a "Write Mask" that is supplied on the DQ(n) terminals. This mask allows the selective writing of new data into one or more of the data bit planes of the storage array corresponding to the data bits of the parallel array. In a normal implementation, a high M value enables the writing of new data while a low M inhibits the writing and leaves the existing data unchanged. A new mask value must be supplied for each masked write cycle.

2.6.6 FLASH WRITE WITH MASK, (FWM)

A write cycle in which the contents of an entire row of the memory array can be selectively set to a stated value. The "mask" value determines which bit planes are to be altered while the "color register" (qv) contains the data value to be written. The color register is loaded in a previous "Load Color Register" cycle with a persistent value. The mask value is supplied during the cycle on the DQ(n) terminals. A new mask value must be supplied for each cycle performed. A high mask bit normally enables the write function for that bit. A low mask bit leaves the data unaltered.

2.6.7 SPECIAL WRITE TRANSFER

A write transfer in a device that has variations in the architecture of the SAM data register to allow improved performance in the internal SAM to RAM data transfers. These variations are defined in the following paragraphs.

2.6.8 SPLIT WRITE TRANSFER, (SWT)

A write transfer in which the SAM data register is split into two halves and the data is transferred to the RAM data bus separately after each half of the SAM register is filled.

2.6.9 AUTO-LOAD WRITE TRANSFER, (AWT)

A split SAM data register transfer in which the transfer from each half is automatically triggered by the state of the tap pointer counter after each half of the SAM register is filled.

2.6.10 READ TRANSFER, (RT)

A read operation in which the contents of one row of the memory array is transferred into the SAM data register in parallel.

2.6.11 SPECIAL READ TRANSFER

A read transfer in a device that has variations in the architecture of the SAM data register to allow improved performance in the internal RAM to SAM data transfers. These variations are defined in the following paragraphs.

2.6.12 SPLIT READ TRANSFER, (SRT)

A read transfer in which the SAM data register is split into two halves and the data is transferred from the RAM data bus separately into each half of the SAM register as it is needed for transfer to the SDQn terminals.

2.6.13 AUTO-LOAD READ TRANSFER, (ART)

A split SAM data register transfer in which the transfer into each half is automatically triggered by the state of the tap pointer counter after each half of the SAM register is emptied.

2.6.14 DOUBLE BUFFERED READ TRANSFER, (DRT)

A read transfer in an array that contains two full SAM data registers which are used alternately. Each one is loaded while the contents of the other is being transferred to the SDQ(n) port. The selection of the two SAM registers is automatic.

2.6.15 RAM WRITE WITH NEW MASK, (RWNM)

A RAM write cycle in which the data bits that are to be written are controlled by a write mask which is supplied at the beginning of the write cycle on the DQ(n) terminals. A high mask bit normally enables the write function for that bit. A low mask bit leaves the data unaltered.

2.6.16 RAM WRITE WITH OLD MASK, (RWOM)

A RAM write cycle in which the data bits that are to be written are controlled by a write mask register which was loaded in a previous "load write mask" cycle. A high mask bit normally enables the write function for that bit. A low mask bit leaves the data unaltered.

2.6.17 RAM READ/WRITE, NO MASK, (RR), (RW)

A normal RAM read or write access cycle with no SAM or special RAM features or functions actuated.

2.6.18 BLOCK WRITE, NO MASK, (BW)

A RAM write cycle in which four (4) bits are written into each bit plane as defined by the contents of the color register. The four (4) bits are those locations controlled by the two LSB of the column address.

2.6.19 BLOCK WRITE WITH NEW MASK, (BWNM)

A Block Write cycle in which the data written is also controlled by the write mask supplied on the DQ(n) terminals in that cycle.

2.6.20 BLOCK WRITE WITH OLD MASK, (BWOM)

A Block Write cycle in which the data written is controlled by the contents of the write mask register which was previously loaded in a "Load Write Mask" cycle.

2.6.21 LOAD WRITE MASK REGISTER, (LWR)

A non-memory cycle in which the write mask register is loaded with a new value for use in subsequent masked write cycles.

2.6.22 LOAD COLOR REGISTER, (LCR)

A non-memory cycle in which the color register is loaded with a new value for use in subsequent special cycles which utilize its contents.

2.6.23 READ WRITE MASK REGISTER, (RWR)

A non-memory cycle in which the contents of the "Write Mask Register" are interrogated with the results placed on the RAM data terminals, DQ(n).

2.6.24 READ COLOR REGISTER, (RCR)

A non-memory cycle in which the contents of the "Color Register" are interrogated with the results placed on the RAM data terminals, DQ(n).

2.7 Package-Related Terms

A series of package-related terms have been used in the Standard and are included in the glossary. The recently published JEDEC Standard JESD30, "Descriptive Designation System for Semiconductor-Device Packages" has obsoleted many of the package designations previously used. As new standaeds are published in Std. No. 21-C, the JESD30 approved term will be used or referenced. Commonly used industry package terms will be included in this section, but the reader is refered to JESD30 for definitions of the approved terms.

2.7.1 - BGA, Ball Grid Array

A package in which the external connections to the package are made via a rectangular array of ball type connections, all on a common plane.

2.7.2 - CC, Leadless or Leaded Chip Carrier

A family of device packages that can be square (SCC) or rectangular (RCC) depending on the application.

2.7.3 - DIP, Dual-In-line Package

A device package configuration that has two parallel rows of pins that are spaced nominally 0.3", 0.4", or 0.6" apart with the pins on 0.1" centers.

2.7.4 - LCC, Lateral Chip Carrier

A family of device packages that can be square (SCC) or rectangular (RCC) depending on the application and can be with or without leads.

2.7.5 - PLDCC, Plastic Leaded Chip Carrier

A chip-carrier package that has a molded plastic body and J formed leads (see CC, 2.7.1). The often used term "PLCC" is ambiguous and is deprecated in favor of this term.

2.7.6 - PP, Pin Pitch

The nominal center to center distance between adjacent pins or terminals along the side of an IC package.

2.7.7 - QFP, Quad Flat Pack

A flat pack package that has leads on all four sides (see SFP).

2.7.8 - RCC, Rectangular Chip Carrier

See LCC, par 2.7.3.

2.7.9 - SCC, Square Chip Carrier

See LCC, par. 2.7.3.

2.7.10 - SFP, Square Flat Pack

A square package body of uniform thickness with flexible, flat leads exiting, on 0.050 " centers, peripherally from the center plane of the four package sides.

2.7.11 - SIMM, Single-In-line-Memory-Module

A multichip module in which the body has a SIP form and is made up primarily of memory devices. (see SIP/SIMM and ZIP/SIMM).

2.7.12 - SIP, Single-in-line Package

A rectangular package with the leads along one side, normally one of the long sides.

2.7.13 - SIP/SIMM, SIP/SIMM Module

A multichip memory module in which the body has a SIP form, and the pins are formed into an in-line configuration.

2.7.14 - SOG, (SOP), Small Outline, Gull Wing Lead

A surface mount package that conforms to the "small outline" concept and which has the leads formed into a "gull wing" configuration.

2.7.15 - SOJ, Small Outline J Lead

A surface mount package that conforms to the "small outline" concept and which has the leads formed into a "J" configuration.

2.7.16 - TSOP, Types I and II, TSOP1, TSOP2

These are small outline packages with gull wing lead formation and whose thickness is substantially less than the standard SOG package. TSOP1 has the leads on the end or short edges of the package while TSOP2 has the leads on the sides or long edges of the package. The lead pitch is often finer than that commonly used in the standard SOG package.

2.7.17 - ZIP, Zig-Zag In-line Package

A package whose body resembles that of a DIP, except that the external leads are all along one edge of the package. The leads emerge on 0.050" centers and are formed alternately into two rows of pins that are separated by 0.100" with the individual leads on 0.100" centers along the rows. The package is mounted standing on one edge.

2.7.18 - ZIP/SIMM, ZIP/SIMM Module

A multichip memory module in which the body has a SIP form but the leads have been formed into a ZIP foot-print.

2.8 Memory Card Pin Names

The following pin names were developed for use with the 68 pin Multiple Technology Memory Card described on pages 4-24 & 4-25. Some of these terms, however, may be used on other standards to follow. The pin names used on the card but not given in this section are standard terms defined in Sec. 2.1.

2.8.1 BD(n), Battery Voltage Detect

The signals, BD1 and BD2 are generated by the memory card, as an indication of the condition of the battery on the memory card.

Both signals are kept asserted when the battery is in good condition. When BD2 is negated while BD1 is still asserted, the battery is in a warning condition and should be replaced, although data integrity on the card is still assured. If BD1 is negated with BD2 either asserted or negated, the battery is no longer serviceable and data is lost.

2.8.2 CD(n), Card Detect

The CD1\ and CD2\ signals provide for proper memory card insertion detection, and have been positioned at opposite ends of the connector to facilitate the detection process. The signals are connected to ground internally on the memory card; thus they will be forced low whenever a card is placed in a host socket. The host socket interface circuitry shall provide 10K pull-up resistors to Vcc on each of these signal pins.

2.8.3 RFU, Reserved Pins

Several pins have been identified as Reserved for Future Use. Neither memory cards, nor Host systems shall make any electrical connections to these pins.

2.8.4 RG, Attribute Memory Select

The memory card defines two planes selected by the Register (RG\) pin. When this signal is active low, the register or Attribute Memory is selected. Normal access to main memory is obtained when the RG\ signal is high (inactive). Attribute Memory is a separately accessed section of memory on the card and is generally used to record card capacity and other configuration and attribute information. Main Memory is used to store user data.

The timing of Attribute Memory may be different than that of Main Memory's; refer to manufacturers specifications for details. When Attribute Memory is accessed, only data signals DQ0-DQ7 are valid and signals DQ8-DQ15 shall be ignored. Signals E1\ and E2\ and A0 are still valid, but it is only possible to select even addresses, (a combination of E1\E2\A0 that requests an odd byte will result in invalid data on the bus.

For those PC memory cards that do not have a section reserved for Attribute Memory, all Main Memory addresses shall begin with address (hex) 0H and proceed for a minimum of 16 kilobytes of contiguous space.

2.8.5 WP, Write Protect

The WP output signal is used to reflect the status of the Write Protect switch on the memory card. If the memory card Write Protect switch is present, this signal will be asserted by the card when the switch is enabled, and deasserted when the switch is disabled. If the memory card has no Write Protect switch, the card will connect this line to ground or Vcc, depending on the condition of the card memory. If the card can always be written, the pin will be connected to Vss. If the card is permanently Write Protected, the pin will be connected to Vcc.

2.9 SRAM & SSRAM SPECIAL PIN NAMES

The following standards are applicable to SRAM AND SSRAM devices. Some of the terms are also covered in Sec 2.1 on general pin names but are repeated here for completeness.

2.9.1 – $\overline{FT}$, Flow–Through
A control input which when driven true places the RAM register into the flo–through mode; when false, the RAM register is in Register Mode.

2.9.2 – $\overline{LBO}$, Linear Burst Order
A control input which when driven true causes the Burst counter to generate addresses in sequential order; when false the Burst addresses are generated in a specified interleaved order.

2.9.3 – M, Mode Control
A control input that implements special functions. It may be a DC or active input signal, but is always intended to be tied to a logic high level or not connected by the user unless otherwise specified.

2.9.4 – SAn, SA, Sync Address
One of the clocked address inputs. In devices where the address order is significant, the SAn form is used with the values SA0 thru SAn, where "n" is the binary numeric order of the address or data bit.

2.9.5 – $\overline{SBx}$, Sync Byte "x"Write Enable
A clocked control input that enables writes to byte "x" in conjunction with the $\overline{SW}$ input. SBx has no effect on read cycles.

2.9.6 – $\overline{SE}$, Sync Enable
A clocked control input that logically selects the RAM and removes it from power–down mode.

2.9.7 – $\overline{SG}$, Sync Output Enable
A clocked control input that enables output drivers

2.9.8 – $\overline{SGW}$, Sync Global Write
A clocked control input that writes all bytes regardless of status of Sync Byte Select ($\overline{SSx}$) or Sync Byte Write Enable ($\overline{SBx}$) inputs.

2.9.9 – $\overline{SSx}$, $\overline{SS}$, Sync Byte "x"Select
A clocked control input that logically selects byte "x" for reads and writes. Where no "x" designator is given, the signal selects all bits of the device.

2.9.10 – $\overline{SW}$, Sync Write
A clocked control input that writes all bytes, or on devices with Sync Byte Select ($\overline{SSx}$), or Sync Byte Write Enable ($\overline{SBx}$) inputs, writes all selected or enabled bytes.

2.9.11 – $\overline{SWx}$, Sync Byte (Group) "x" Write
A clocked control input that writes byte (group) "x". "x" takes the values of a, b, c, d, etc. In devices where the write control is applied to bit groupings that is other than a "byte", the definition still applies.

2.9.12 – TCK, Test Port Clock
Serial Scan Test Clock Input

2.9.13 – TDI, Test Data In
Serial Scan Data Input

2.9.14 – TDO, Test Data Out
Serial Scan Test Data Output

2.9.15 – TMS, Test Mode Select
A control input that enables Scan Test Clock, and is used to select test modes.

2.9.16 – TRST, Test Port Reset
Serial Scan Test Port Reset

2.9.17 – x, Byte or Word Identifier
In the pin names in this section and their definitions, this is an alphabetic identifier for the word or byte being accessed.

2.9.18 – ZQ, Output Impedance Control
An analog signal input that sets output buffer impedance and operating mode. .

2.9.19 – ZZ Sleep Mode Enable
A control input that logically deselects RAM and places it in Sleep Mode. Devices that implement Sleep Mode may require several cycles to implement the "Go–to–Sleep" or "Wake–up"

3 MEMORY DEVICE STANDARDS

The following standards establish pin assignments, power supply potentials, and package configurations and dimensions for a series of memory devices. Only nominal voltages and dimensions are covered by the standards. Specific values and tolerances plus other specification values are left to the manufacturers and users of the parts. In some cases, special timing diagrams are included, where they are essential to the implementation and use of the standards. In the following paragraphs, only those elements unique to the device(s) covered are listed in table form. A figure reference is also given. All devices, except where specifically stated, are intended to be used in an electrical environment with logic parts which use TTL I/O signal levels. It is required that the memory devices operate with signal levels and power supply voltages that are compatible with this family. TTL uses a single primary supply voltage that is nominally 5.0 V. Devices that are approved for use in an ECL electrical environment are presented in separate subsections within the appropriate technology section.

In the following five tables are given summaries of several groups of standards contained in this document as follows:

Table 1, BYTE Wide device Standards developed by the JC-42.3 Committee
Table 2, PROM Standards developed by the JC-42.1 Committee
Table 3, SRAM and DRAM Standards developed by the JC-42.3 Committee
Table 4, SRAM Standards developed by the JC-42.3 Committee
Table 5, SRAM Standards for TTL & ECL with multiple centered power pins developed by the JC-42.3 Committee

SIZE	ROM	EPROM	EEPROM	NVRAM	SRAM	PSRAM
512X8	/32C	24D/32C	24D/28D/32C	/32C		/32C
1KX8	/32C	24D/32C	24D/28D/32C	24D/ /32C	/32C	
2KX8	24D/	/32C	/32C	24D/	/32C	/28D/32C
4KX8	24D/ /32C	24D/32C/	/28D/32C	/28D/32C	24D/28D/32C	28D/32C
8KX8	24D/28D/32C	24D/28D/32C	/28D/32C	/28D/32C	28D/32C/28S	28D/32C
16KX8	/28D/32C	/28D/32C	/28D/32C	/28D/32C	/28D/32C	/32C
32KX8	28D/28S/32C	28D/28S/32C	28D/28S/32C	/28S/32D	28D/32C/28S	/28S
64KX8	/28S/	/28S/	/32D/	/32D/	/32D/32S	
128KX8	28D/32D/32S	/32D/32S	/32D/32S	/32D/32S	/32D/32S	/32S
256KX8	/32D/32S	/32D/32S	/32D/32S	/32D/32S	/32D/32S	/32S
512KX8	/32D/32S	/32D/32S	/32D/32S			/32S
1MX8	/32D/	/32D/				

NOTE-IN THE ABOVE TABLE, SIX PACKAGES ARE REFERENCED. THEY ARE:
(1) 24D = 24 PIN DIP, 0.6" WIDE, (2) 28D = 28 PIN DIP, 0.6" WIDE, (3) 32D = 32 PIN DIP. 0.6" WIDE, (4) 32C = 32 TERMINAL RCC (5) 28S = 28 PIN SOJ, (6) 32S = 32 PIN SOJ

Table 1, BYTE-Wide Device Standards developed by JC-42.3 Committee

SIZE	BYTEWIDE			NIBBLEWIDE	
	PROM	LPROM	RPROM	PROM	LPROM
32	20C				
256	20C/24D	20C			
512	20C/24D/28C/32C	24D		20C,	
1K	24D/28C/32C	24D		20C/28C,	
2K	24D/28C/32C	24D	24D	20D//28C	20D
4K	24D/28C/32C	24D	24D	20D//28C,	
8K	24D/28C/32C			20D/ /28C	

NOTE--IN THE ABOVE TABLE, THE PACKAGES REFERENCED ARE:
(1) 20 PIN DIP, 0.3" , (2) 20 TERMINAL SCC, (3) 24 PIN DIP, 0.6" , (4) 28 TERMINAL RCC & SCC, (5) 32 TERMINAL RCC

Table 2, PROM Standards developed by JC-42.1 Committee

WORDS	STATIC			DYNAMIC	
	X1	X4	X4 W/G	X1	X4
4K	18D	20D/20C/	22D		
16K	20D/20C/24S	22D/22C/28C	24D	16D/18C	18D/20D
64K	22D/22C/24S	24D/ /28C	28D	16D/18C/16Z	18D/22C/20Z
256K	24D/ /28S	/28C	28D	16D/18C/16Z	20D/20S/20Z
1M	28D/28S	32D/32S		18D/20S/20Z	20D/20S/20Z
2M	28D/28S				
4M				18D/20S/20Z	22D/
16M				20D	22D/
64M				20D	

NOTE–IN THE ABOVE TABLE THE PACKAGES REFERENCED ARE:
(1) 16, 18, 20, 22, & 24 PIN DIP, 0.3", (2) 16 & 20 PIN ZIP, (3) 20, 22, 28, & 32 TERMINAL RCC, (4) 26/20 PIN SOJ, (5) 24 & 28 PIN SOJ

Table 3, SRAM and DRAM Standards developed by JC-42.3 Committee

SIZE	X1		X4		
	ECL	TTL	100K ECL	ECL	TTL
256		16D/20C	24F/24D	24D	22D/28C
1K	16D	16D/ 20C	24F/24D	24D	
4K	18D		28D	28D	
16K	20D			28D	
64K	22D				
256K	24D				

NOTE–IN THE ABOVE TABLE THE PACKAGES REFERENCED ARE:
(1) 16, 18, 20, 24 PIN DIP, 0.3", (2) 24, 28 PIN DIP, O.4", (3) 24 PIN S FP (4) 20 TERMINAL SCC, (5) 28 TERMINAL RCC

Table 4, SRAM Standards developed by JC-42.1 Committee

# WORDS	SRAM							SSRAM
	X1		X4				X8	X4
	W/ $\overline{G}$	W/O $\overline{G}$	W/ $\overline{G}$	W/O $\overline{G}$	SEP I/O W/$\overline{G}$	SEP I/O W/O $\overline{G}$	W/ $\overline{G}$	W/ $\overline{G}$
32K							32D/32S	
64K			28D/28S		32D/32S			32D/32S
128K							32D/32S	
256K	28D/28S		32D/32S	28D/28S	36D/36S	32D/32S		36D/36S
512K							36D/36S	
1M	32D/32S	28D/28S	32D/32S		36D/36S			36D/36S
2M							36D/36S	
4M	32D/32S		36D/36S	32D/32S	40D/40S	36D/36S		40D/40S
16M	36D/36S	32D/32S						

Table 5, SRAM Standards for TTL & ECL with multiple centered power pins developed by JC-42.3 Committee

3.1 General Standards

The following standards are applicable to multiple technologies and functionalities but are presented as a single families of devices.

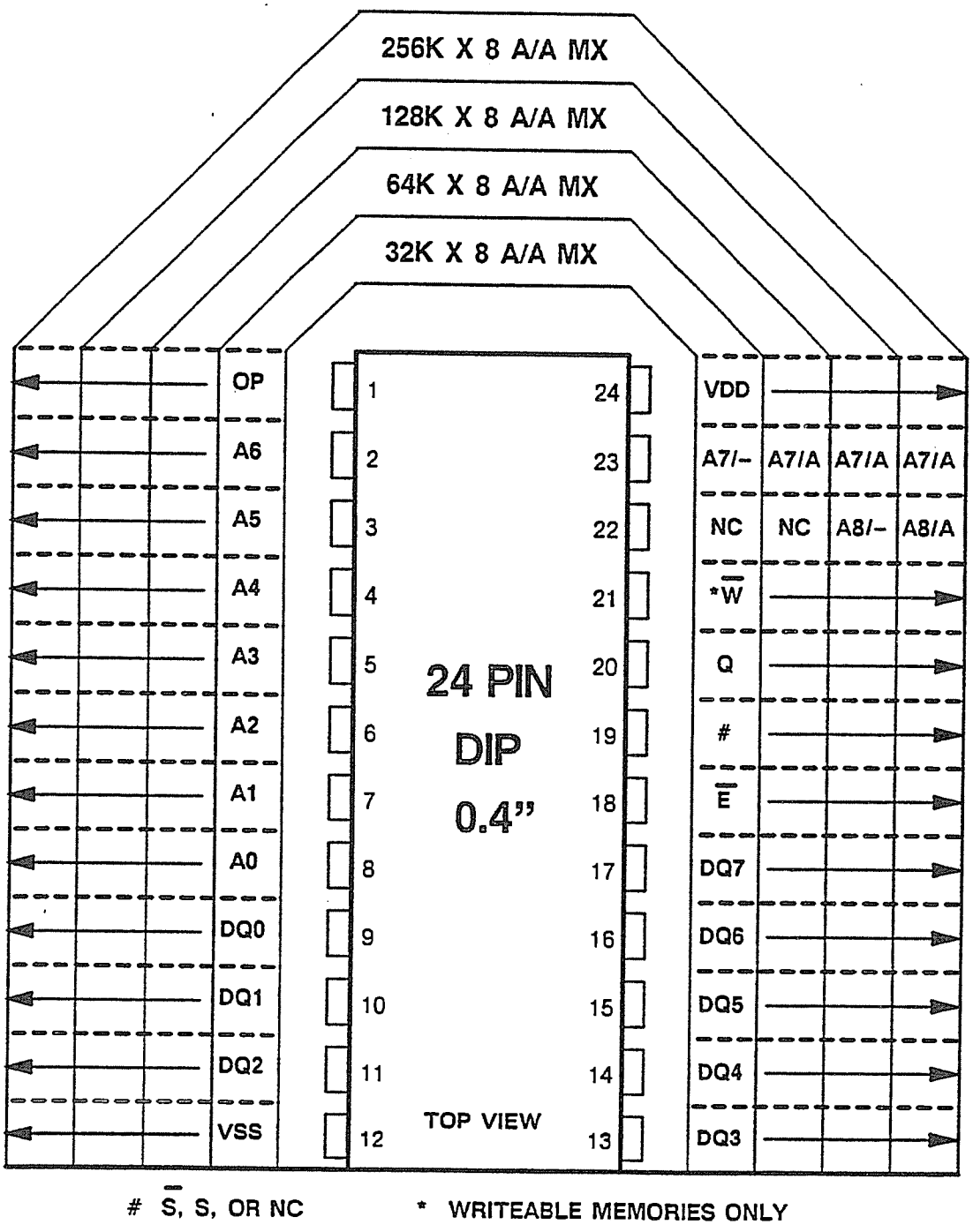
3.1.1 Byte Wide

The devices in the following sections have an 8 bit (byte) wide data interface. All devices are Type B, unless otherwise stated.

3.1.1.1 32K TO 256K BY 8 A/A MULTIPLEXED FAMILY IN DIP

CAPACITY–32K, 64K, 128K, 256K WORDS OF 8 BITS
LOGIC FEATURES–Multiplexed Address
PACKAGE–24 PIN DIP, 0.4" WIDE
PIN ASSIGNMENT–Fig. 3.1-1

This standard defines the generalized pin assignments for a family of address multiplexed byte wide memory devices. Specific pinout variations for different technologies will be defined at a later time.



32K TO 256K BY 8 A/A MULTIPLEXED FAMILY IN DIP
FIGURE 3.1-1

3.1 General Standards

The following standards are applicable to multiple technologies and functionalities but are presented as a single families of devices.

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The devices in the following sections have an 8 bit (byte) wide data interface. All devices are Type B, unless otherwise stated.

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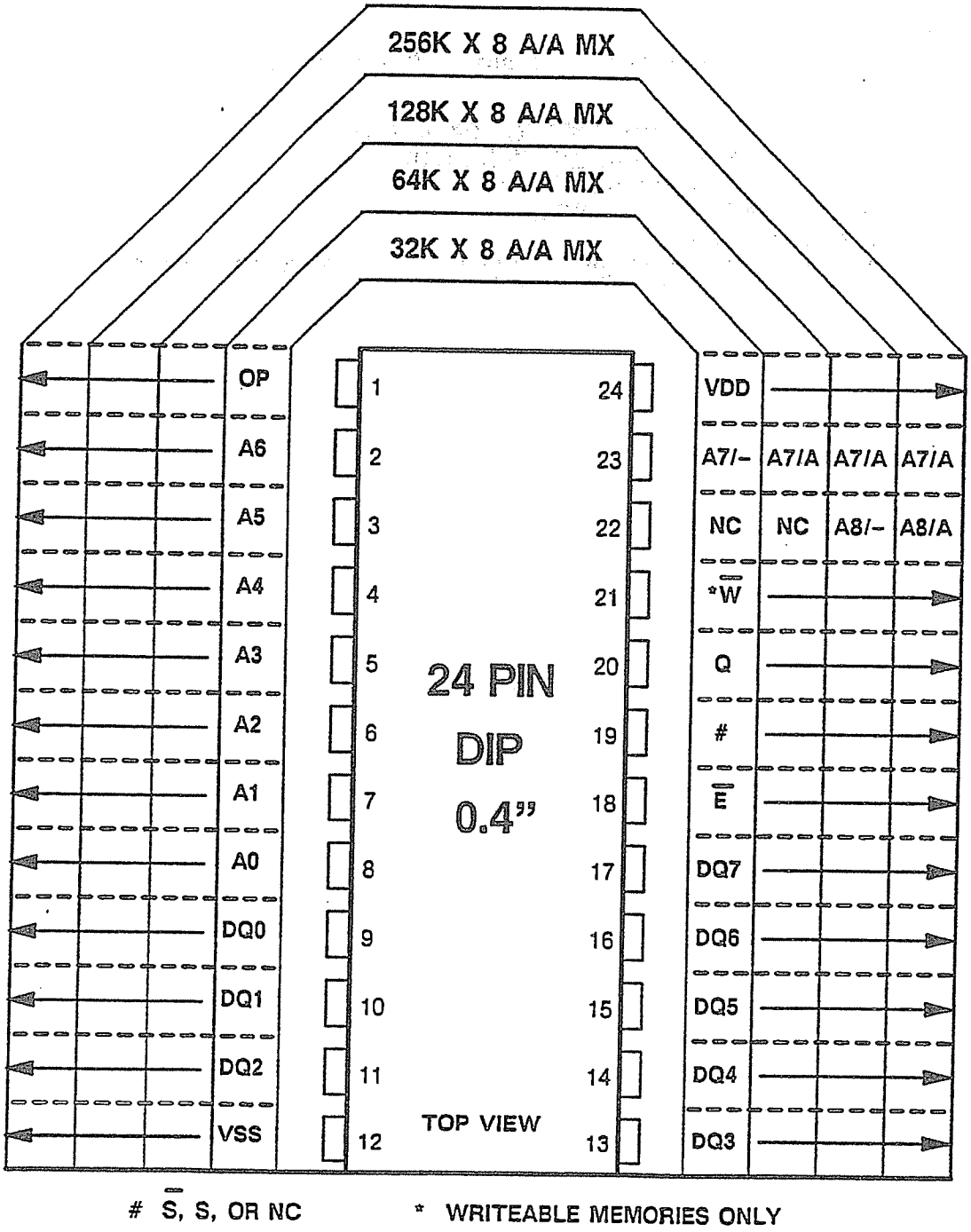
LOGIC FEATURES–Multiplexed Address
PACKAGE–24 PIN DIP, 0.4" WIDE
PIN ASSIGNMENT–Fig. 3.1-1

This standard defines the generalized pin assignments for a family of address multiplexed byte wide memory devices. Specific pinout variations for different technologies will be defined at a later time.



32K TO 256K BY 8 A/A MULTIPLEXED FAMILY IN DIP
FIGURE 3.1-1

3.2 Read Only Memory (ROM)

The following ROM standards were developed by the MOS Committee and have been implemented primarily using MOS technology.

3.2.0 ROM General Standards

The following standards are applicable to all ROM configurationas as specifically defined in the standards.

3.2.0.1 MASK ROM FAST ADDRESS MODE DEFINITION

This standard defines the minimum requirements for the location and quantity of the address bits that must be used for the "Fast Addresses" for certain Mask ROMs that have been designed using the "Fast Address Mode" architecture and circuit design to improve the access time.

1. This standard covers 4M, 8M, 16M, and 32M density Fast Address Mode Mask ROMs.
2. The fast address field (FAx) is the group of address bits, that when changed, result in faster access time than is experienced when the other address bits are changed. It is required to be the field of contiguous address bits starting at the LSB (A0) with a number of bits required to implement the fast address mode design as follows:
   4M & 8M – Minimum, 2 Fast Addresses. (A0 & A1)
   16M & 32M – Minimum 3 Fast Addresses. (A0, A1, & A2)
3. Fast Address Mode is required to provide the faster random access time only when no addresses bits outside the FAx field are changed.
4. The pinout options are the same as the current JEDEC Mask ROM standards except that the fast addresses (FAx) replace the corresponding addresses (Ax).

3.2.1 ROM, Byte Wide

3.2.1.1 2K TO 8K BY 8 ROM FAMILY IN DIP, TYPE A
CAPACITY--2K, 4K, 8K WORDS OF 8 BITS, TYPE A
PACKAGE--24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.2.1-1

3.2.1.2 4K BY 8 ROM IN DIP, Type B
CAPACITY--4K WORDS OF 8 BITS
PACKAGE--24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.2.1-1

3.2.1.3 8K TO 128K BY 8 ROM FAMILY IN DIP,
CAPACITY--8K, 16K, 32K, 128K WORDS OF 8 BITS,
PACKAGE--28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.2.1-2

3.2.1.4 2K TO 32K BY 8 ROM FAMILY IN RCC
CAPACITY--2K, 4K, 8K, 16K, 32K WORDS OF 8 BITS,
PACKAGE--32 PAD (PIN) RCC, 0.450" X 0.550"
PIN ASSIGNMENT--Fig. 3.2.1-3

3.2.1.5 32K TO 512K BY 8 ROM FAMILY IN SOJ,
CAPACITY--32K, 64K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE--28 OR 32 PIN SOJ, 0.4" WIDE OR NOT DEFINED
PIN ASSIGNMENT--Fig. 3.2.1-4

3.2.1.6 128K TO 1M BY 8 ROM IN DIP,
CAPACITY--128K, 256K, 512K, 1M WORDS OF 8 BITS,
PACKAGE--32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.2.1-5

3.2.1.7 64K TO 512K BY 9 ROM IN DIP,
CAPACITY--64K, 128K, 256K, 512K WORDS OF 9 BITS,
PACKAGE--32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.2.1-6

3.2.1.8 2 TO 64 X 16K BY 8 PAGE SELECT ROM IN DIP,
CAPACITY--32K, 64K, 128K, 256K, 512K, 1M WORDS OF 8 BITS,
--2, 4, 8, 16, 32, 64 PAGES OF 16K WORDS OF 8 BITS,
LOGIC FEATURES--Selectable pages of 16K words
PACKAGE--28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.2.1-7
This device contains multiple pages of 16K words which can be selected and the address for which is stored in an internal register.

3.2.1.9 512K and 1M BY 8 ROM IN QFP,
CAPACITY--512K, 1M WORDS OF 8 BITS,
LOGIC FEATURES--These devices can be used with either an 8 or a 16 bit data interface by the appropriate logic control (also see Par. 3.2.2.5).
PACKAGE--44 PIN QFP, 14 mm square with a 1 mm pin pitch
PIN ASSIGNMENT--Fig. 3.2.1-8

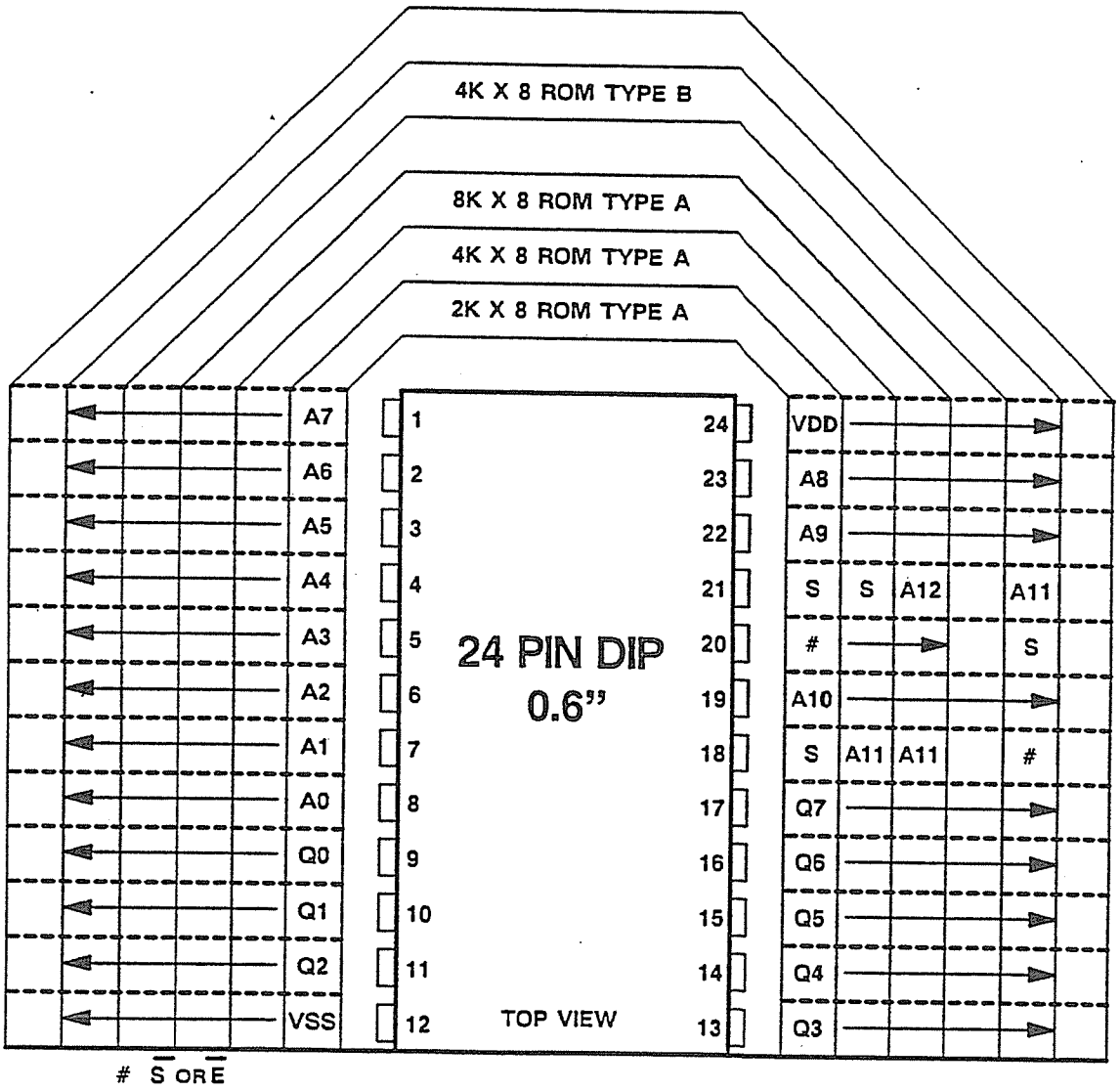


FIGURE 3.2.1-1
2K TO 8K BY 8 ROM IN DIP, TYPES A & B

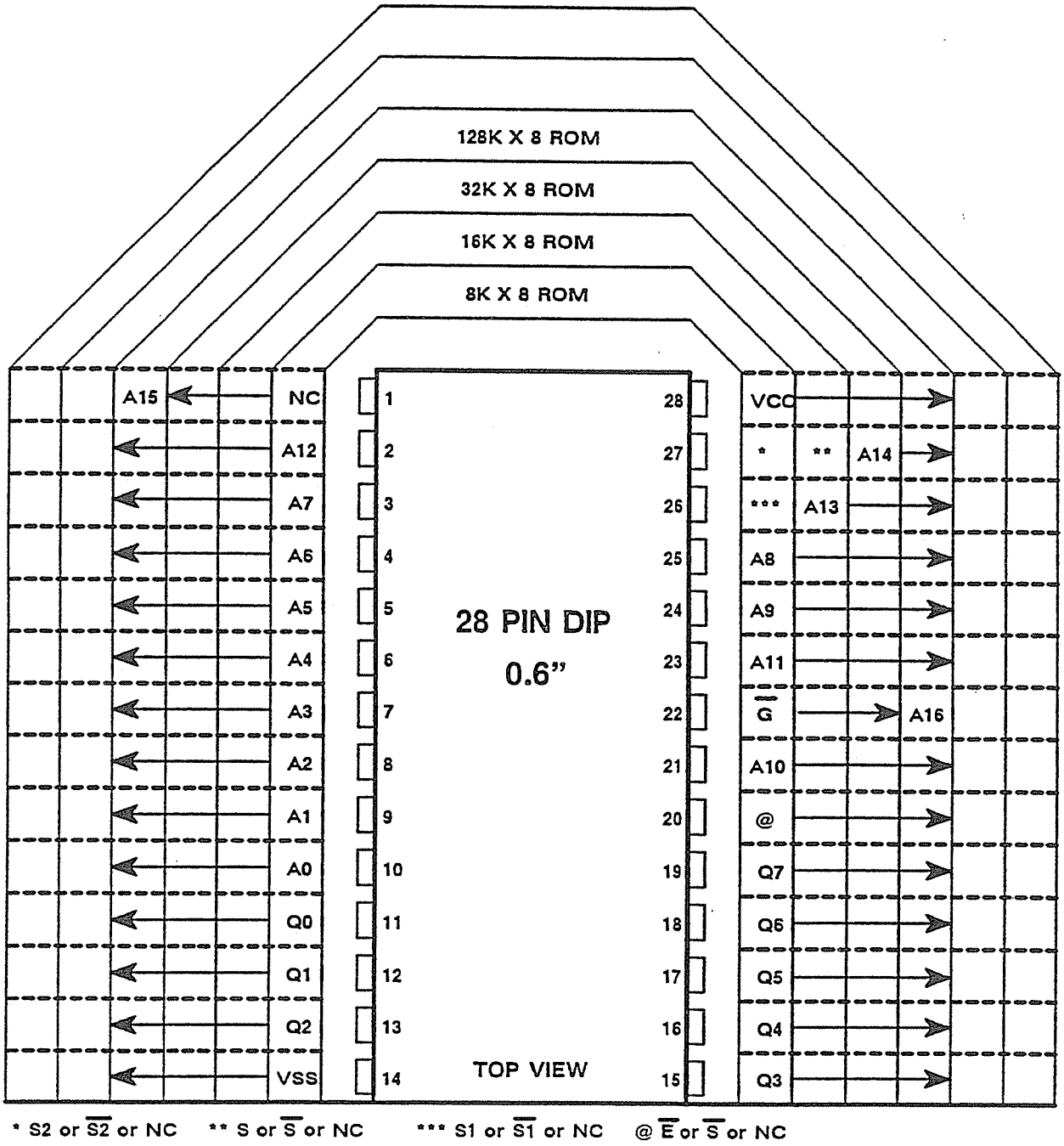


FIGURE 3.2.1-2
8K TO 128K BY 8 ROM IN DIP

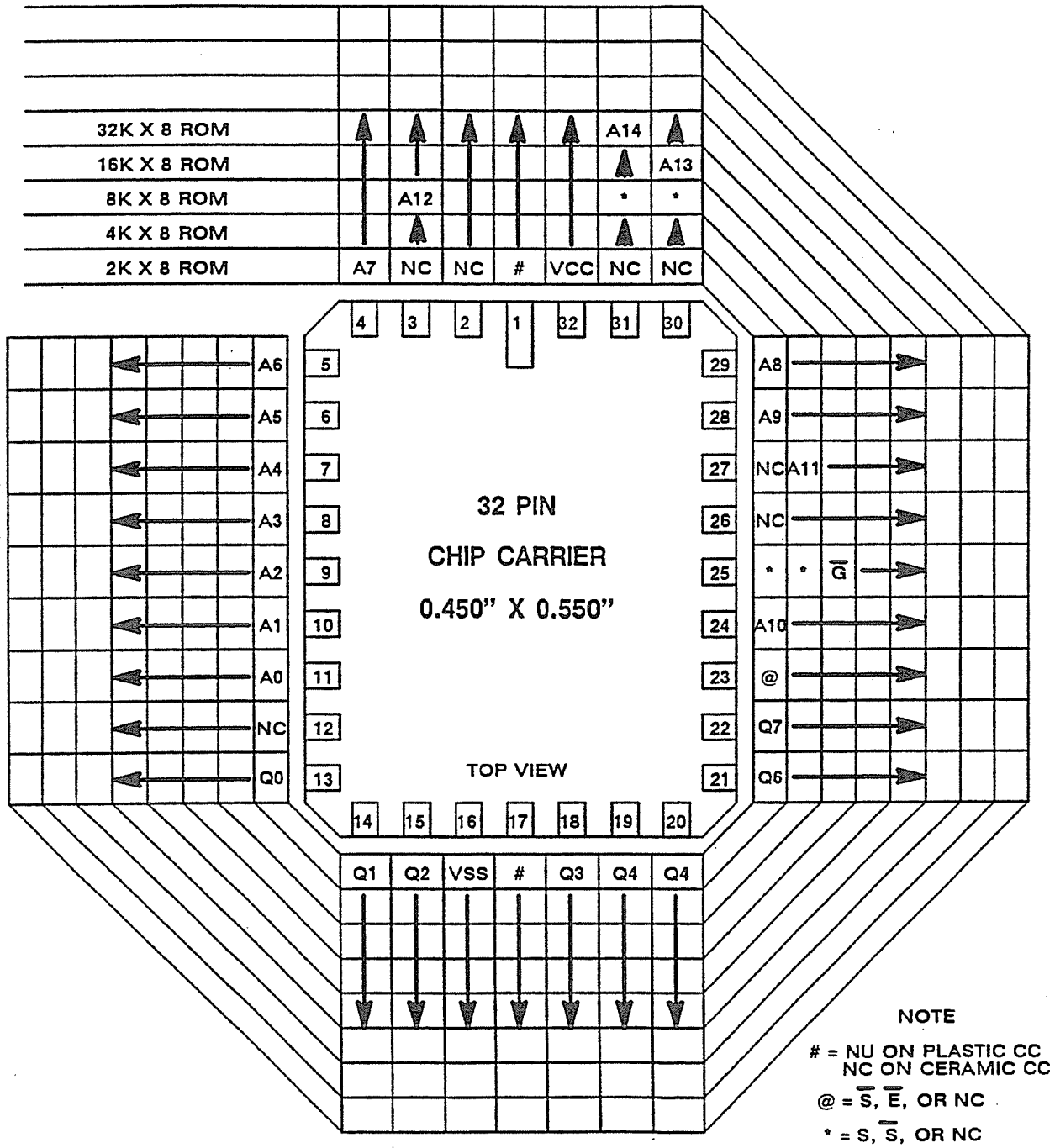


FIGURE 3.2.1-3
2K TO 32K BY 8 ROM IN CC

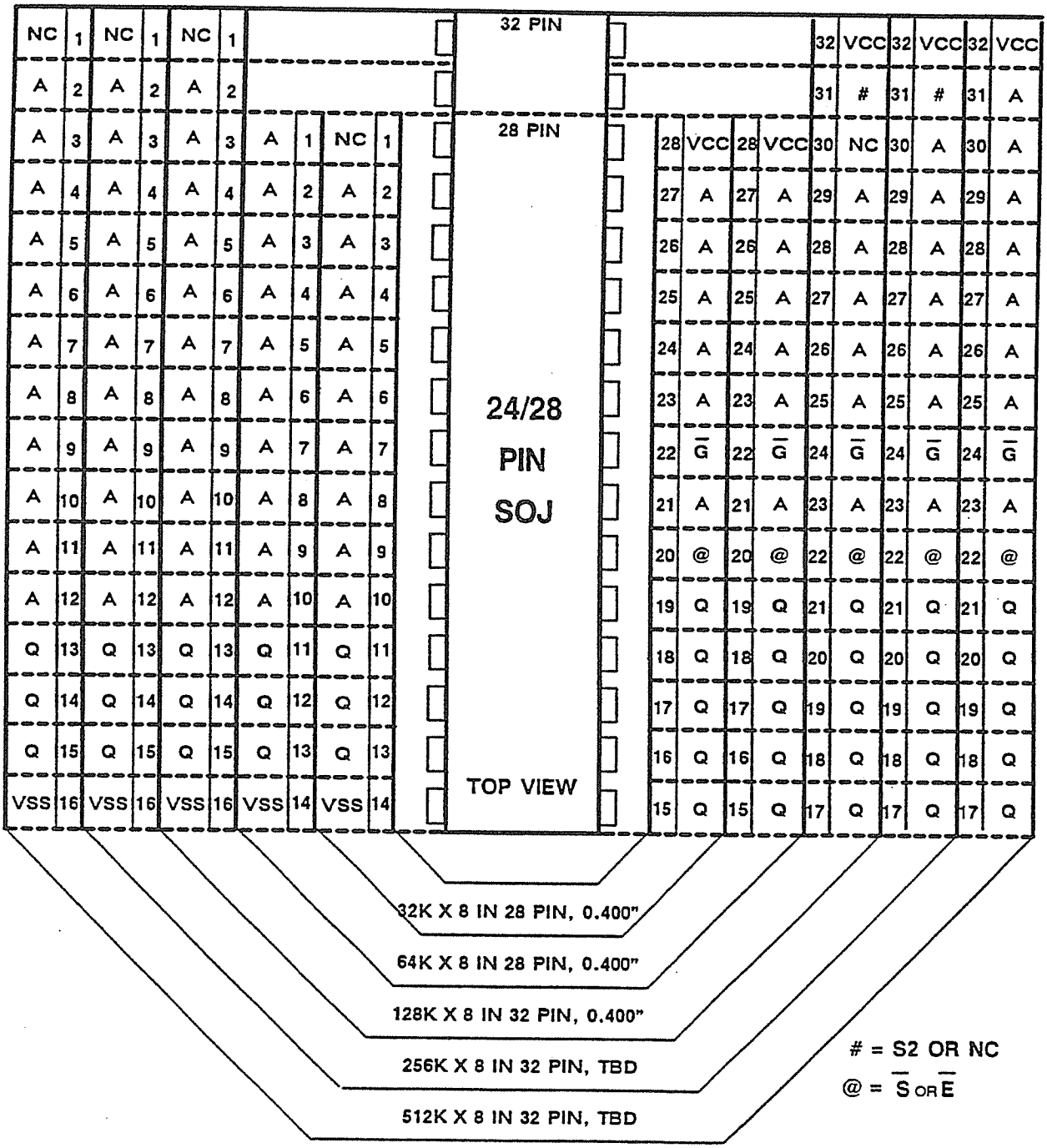


FIGURE 3.2.1-4
32K TO 512K BY 8 ROM IN SOJ

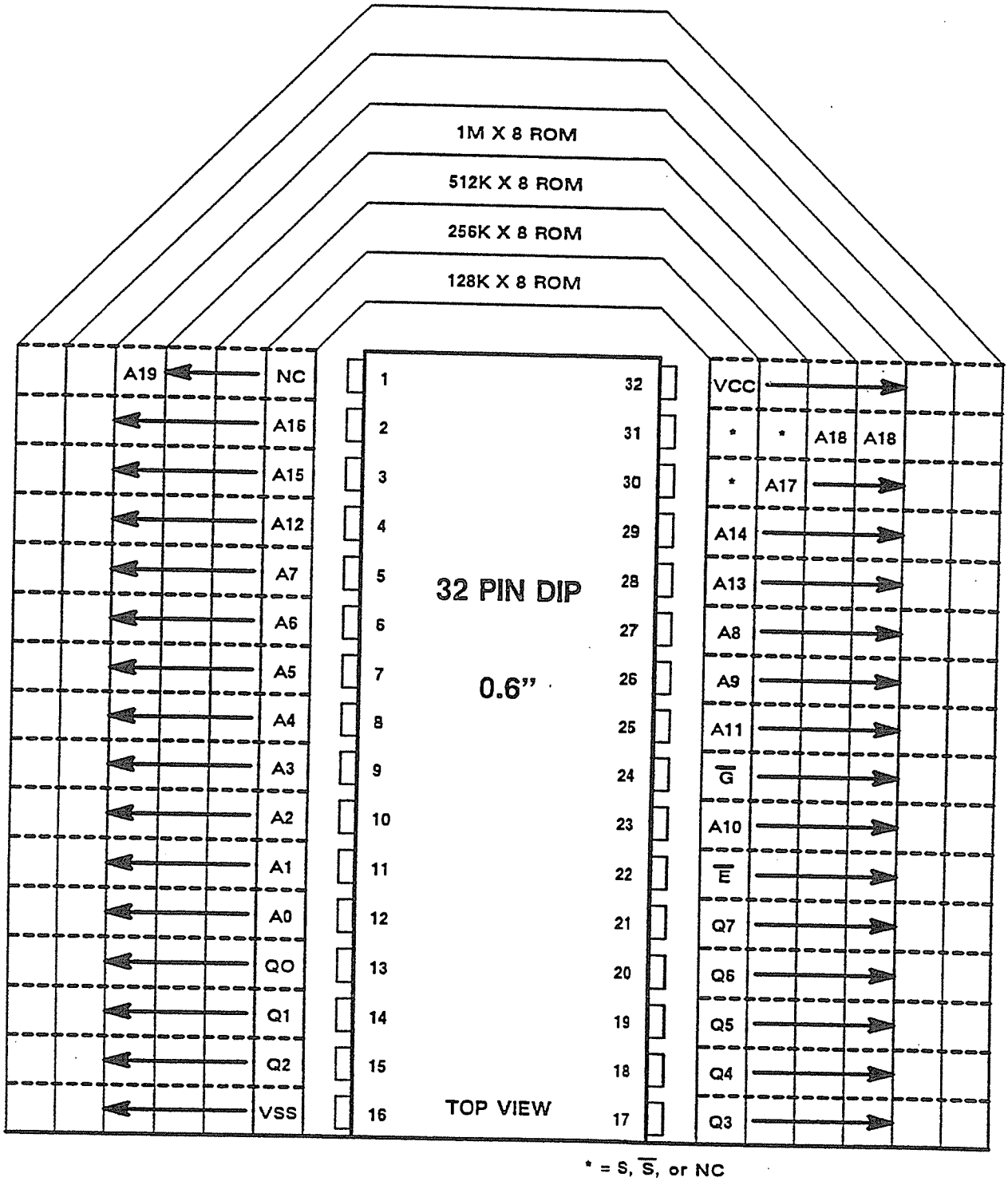


FIGURE 3.2.1-5
128K TO 1M BY 8 ROM IN DIP

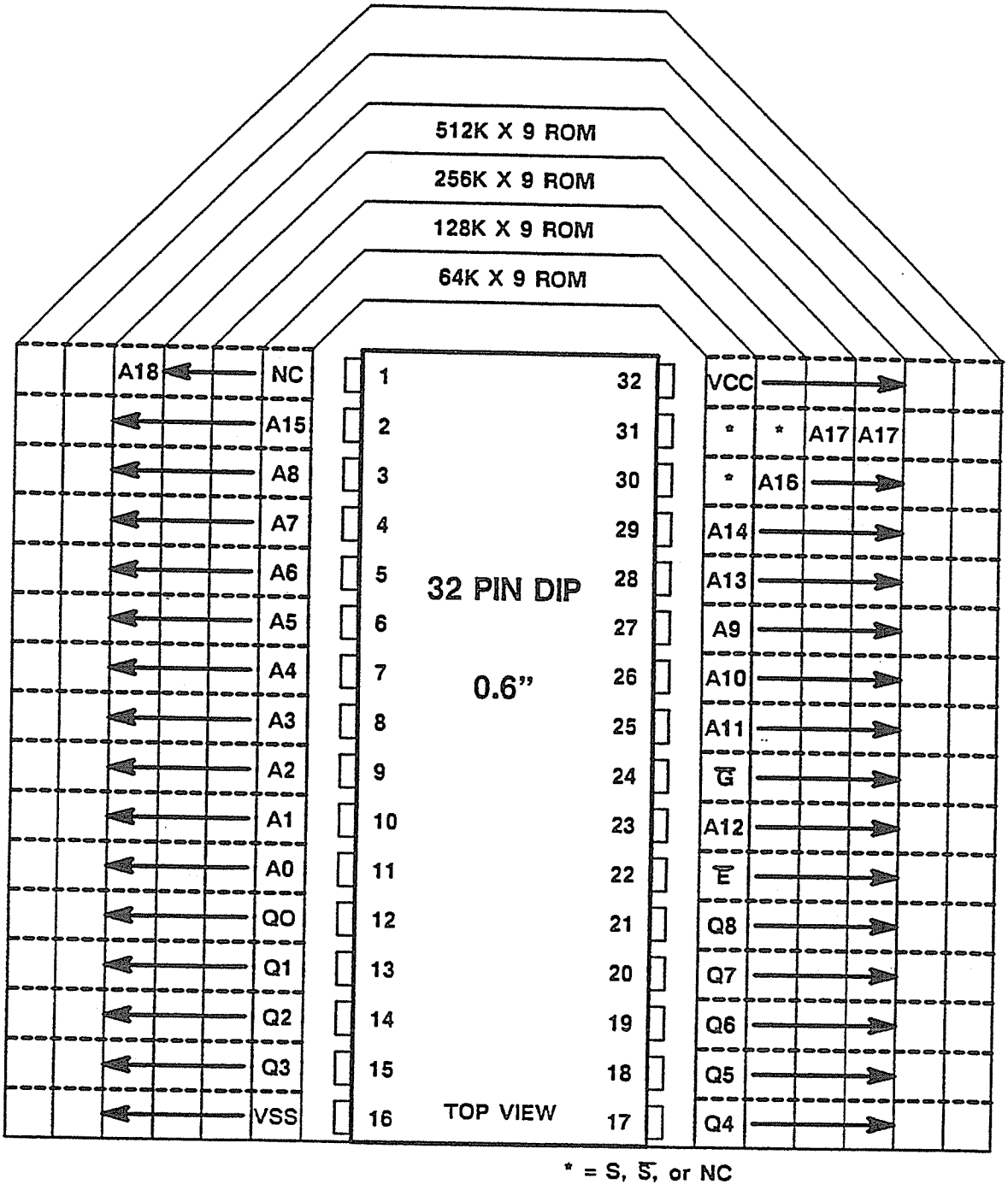
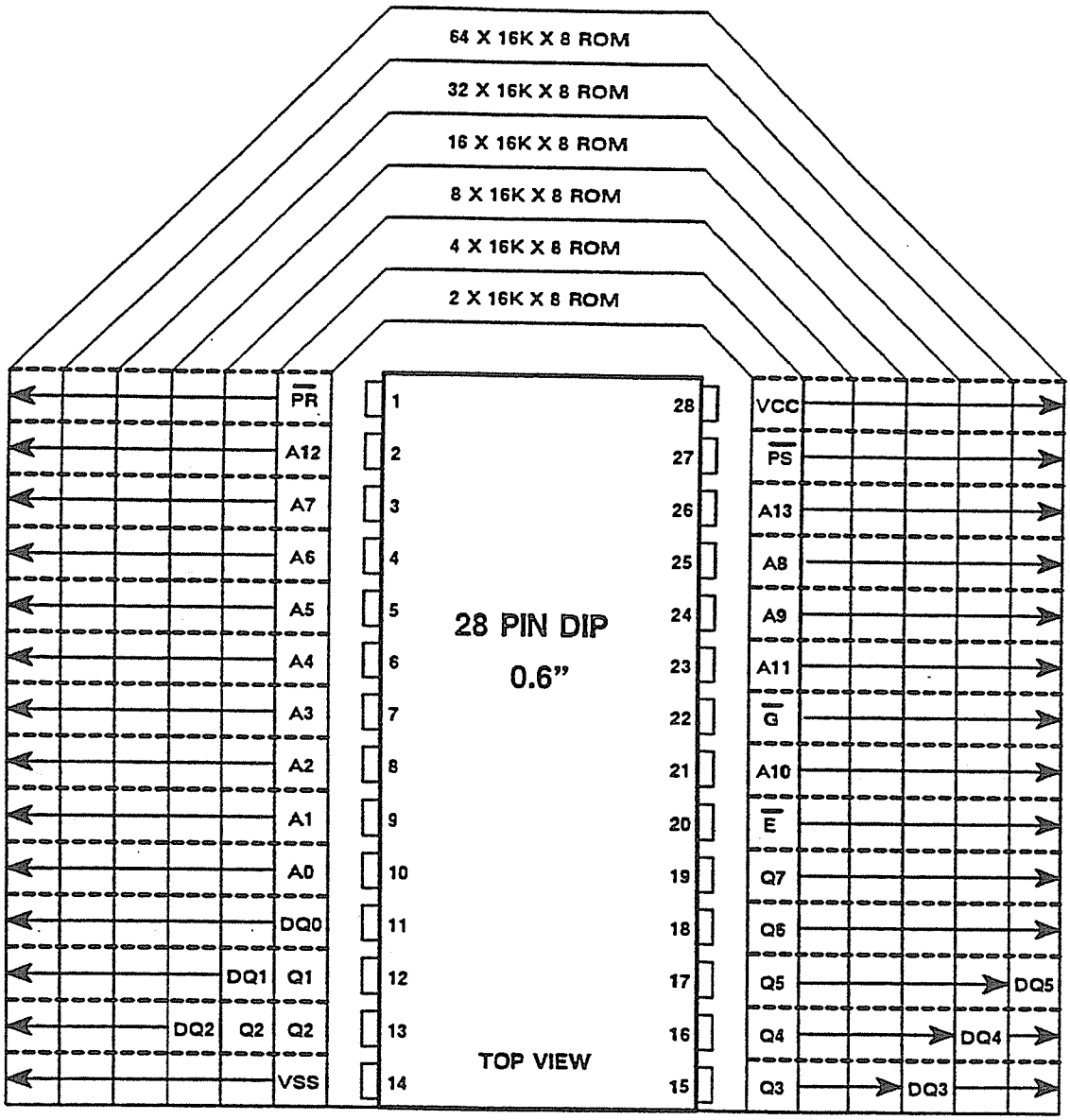


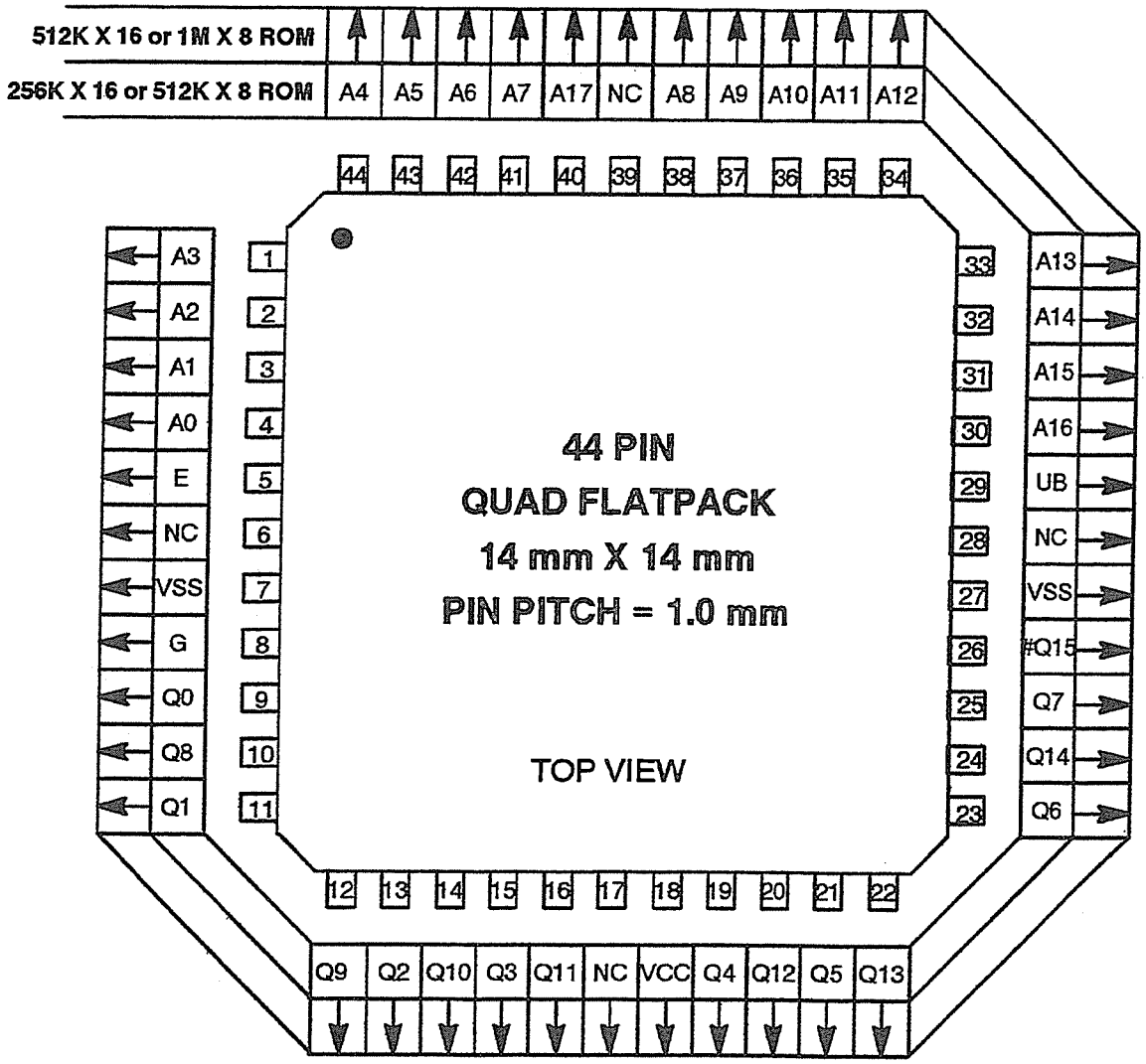
FIGURE 3.2.1-6
64K TO 512K BY 9 ROM IN DIP



FUNCTION TABLE

MODE \ PIN	$\overline{PS}$	$\overline{PR}$	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
ASYN. RESET (PAGE 0)	H	L	X	X	X	X	X	X
PAGE 0	L	H	L	L	L	L	L	L
PAGE 1	L	H	L	L	L	L	L	H
PAGE 2	L	H	L	L	L	L	H	L
PAGE 3	L	H	L	L	L	L	H	H
PAGE 4	L	H	L	L	L	H	L	L
PAGE 5	L	H	L	L	L	H	L	H
PAGE 6	L	H	L	L	L	H	H	L
PAGE 7	L	H	L	L	L	H	H	H
PAGE n	OUTPUTS = n (BINARY) ACTIVE HIGH							
PAGE 63	L	H	H	H	H	H	H	H

FIGURE 3.2.1-7
2 TO 64 X 16K BY 8 PAGE SELECT ROM IN DIP



= Pin 26 is Q15 when UB is true and a full 16 bit word is present on Q0 through Q15. When BH is false, either the upper or lower byte is present on pins Q0 to Q7 as determined by the A(–1) address presented on pin 26

FIGURE 3.2.1–8
256K X 16/512K X 8 AND 512K X 16/1M X 8 ROM IN QFP

3.2.2 ROM, Word Wide

3.2.2.1 – 32K TO 256K BY 16 ROM IN DIP

CAPACITY—32K TO 256K WORDS OF 16 BITS,
PACKAGE—40 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Fig. 3.2.2–1

3.2.2.2 – 32K TO 256K BY 16 ROM IN SCC

CAPACITY—32K TO 256K WORDS OF 16 BITS,
PACKAGE—44 PAD (PIN) RCC, 0.650" X 0.650"
PIN ASSIGNMENTS—Fig. 3.2.2–2

3.2.2.3 – 16K TO 256K BY 16 ADDRESS/DATA MX ROM IN DIP

CAPACITY—16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES—Address and Data MULTIPLEXED onto common pins.
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Figs. 3.2.2–3

3.2.2.4 – 16K TO 256K BY 16 ADDRESS/DATA MX ROM IN RCC

CAPACITY—16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES—Address and Data MULTIPLEXED onto common pins.
PACKAGE—32 PIN (PAD) RCC, 0.450" X 0.550"
PIN ASSIGNMENTS—Figs. 3.2.2–4

3.2.2.5 – 256K and 512K BY 16 ROM IN QFP

CAPACITY—256K & 512K WORDS OF 16 BITS,
LOGIC FEATURES—These devices can be used with either an 8 or a 16 bit data interface by the appropriate logic control (also see Par. 3.2.2.5).
PACKAGE—44 PIN QFP, 14 mm square with a 1 mm pin pitch
PIN ASSIGNMENT—Fig. 3.2.2–5

3.2.2.6 – 512K TO 128M BY 16 ROM IN DIP AND SOP

CAPACITY—512K, 1M, 2M, 4M, 8M, 16M, 32M, 64M, & 128M WORDS OF 16 BITS
PACKAGE—42, 44, 48 or 52 PIN DIP or SOP, 0.600" WIDE
PIN ASSIGNMENTS—512K TO 2M, Fig. 3.2.2–8
PIN ASSIGNMENTS—4M TO 128M, Fig. 3.2.2–6

3.2.2.7 – 512K and 1M BY 16 ROM IN SCC

CAPACITY—512K & 1M WORDS OF 16 BITS
PACKAGE—44TERMINAL SCC, 0.650" X 0.650"
PIN ASSIGNMENTS—Fig. 3.2.2–7

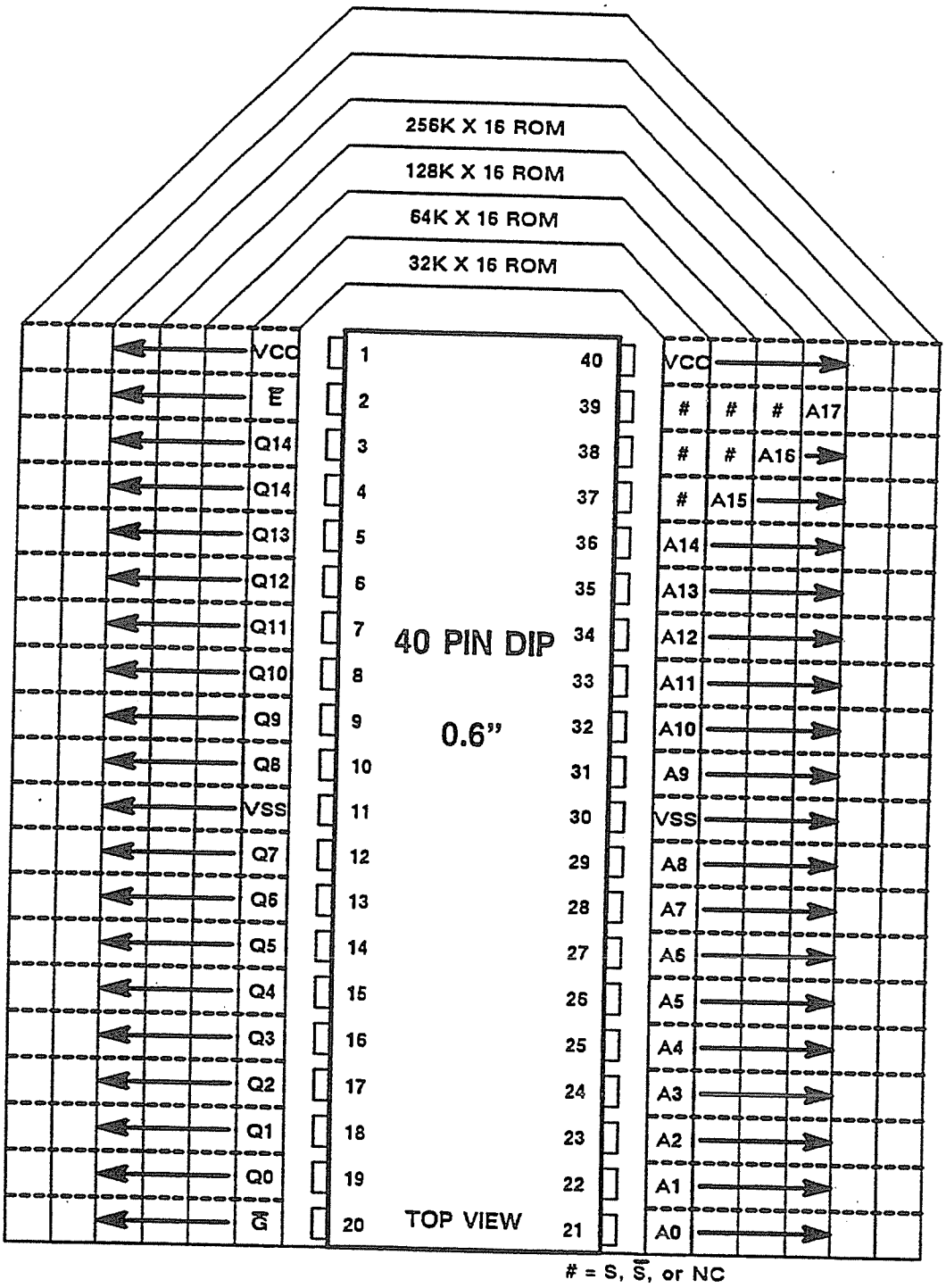


FIGURE 3.2.2-1
32K TO 256K BY 16 ROM IN DIP

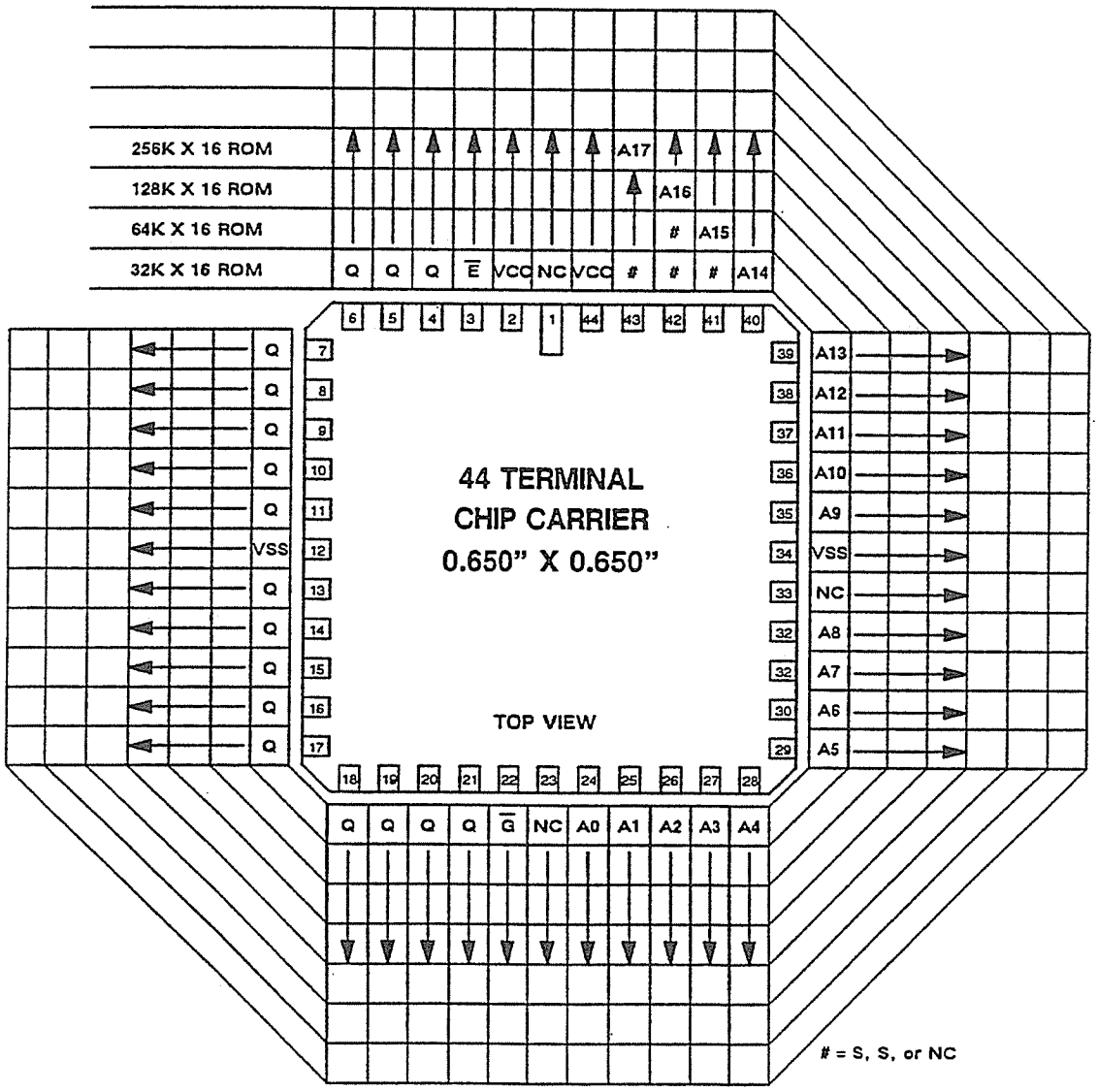


FIGURE 3.2.2-2
32K TO 256K BY 16 ROM IN CC

$\overline{BG}$	A0	D0–D7	D8–D15	OPERATION
L	L	LOWER BYTE	UPPER BYTE	WORD
L	H		UPPER BYTE	
H	L	LOWER BYTE		BYTE
H	H	UPPER BYTE		BYTE

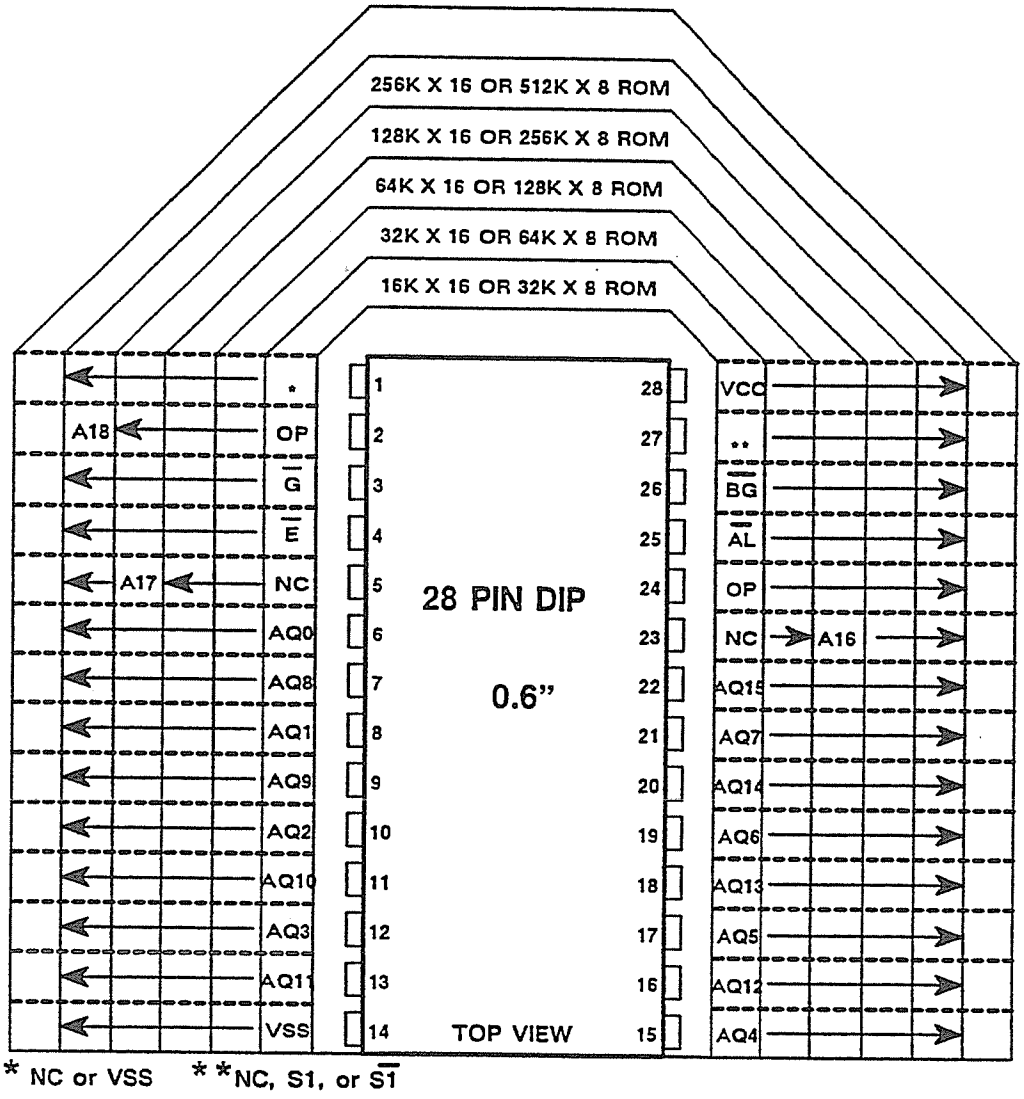


FIGURE 3.2.2-3
16K TO 256K BY 16 AQ MX ROM IN DIP

$\overline{BG}$	A0	D0-D7	D8-D15	OPERATION
L	L	LOWER BYTE	UPPER BYTE	WORD
L	H		UPPER BYTE	
H	L	LOWER BYTE		BYTE
H	H	UPPER BYTE		BYTE

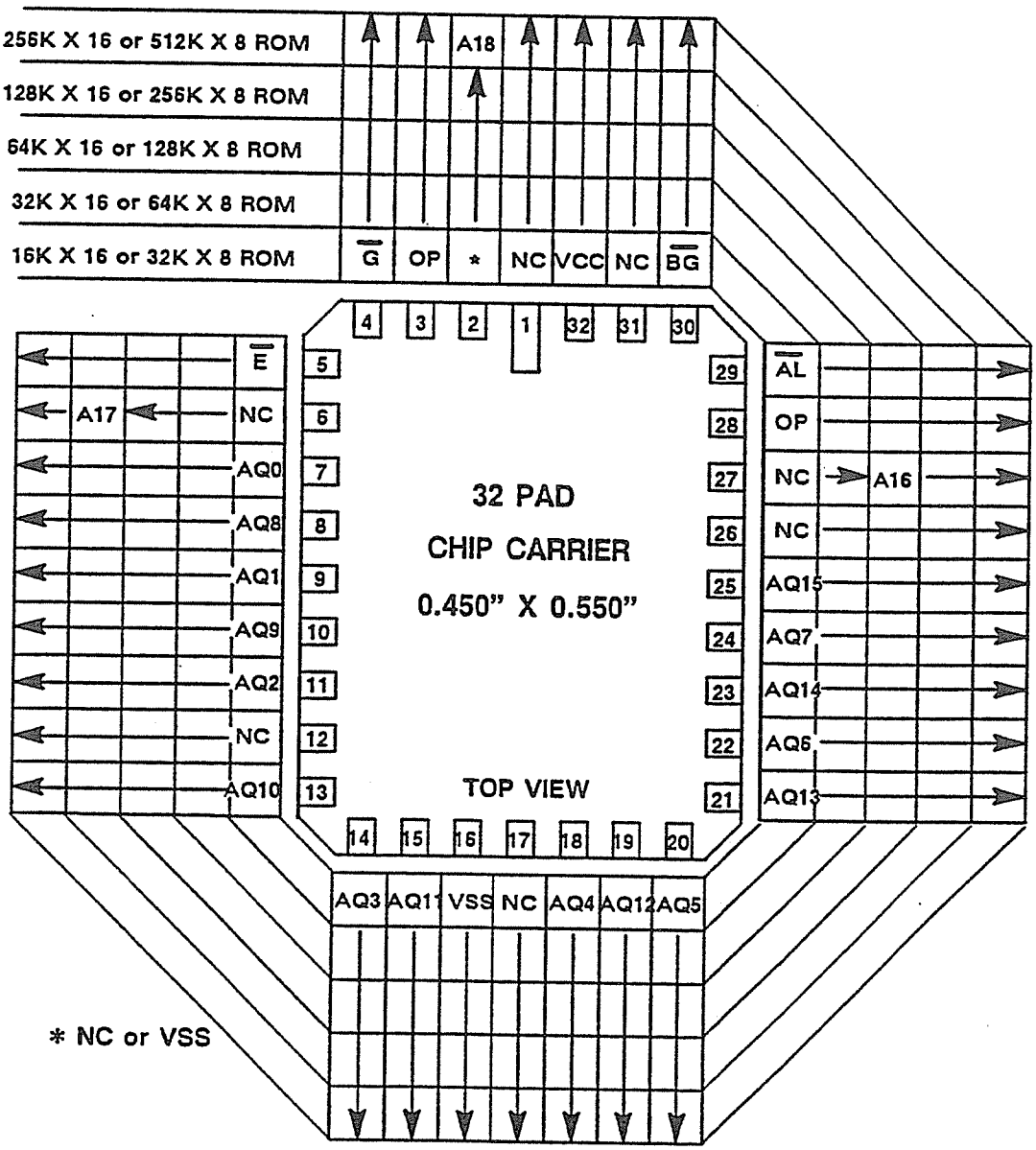
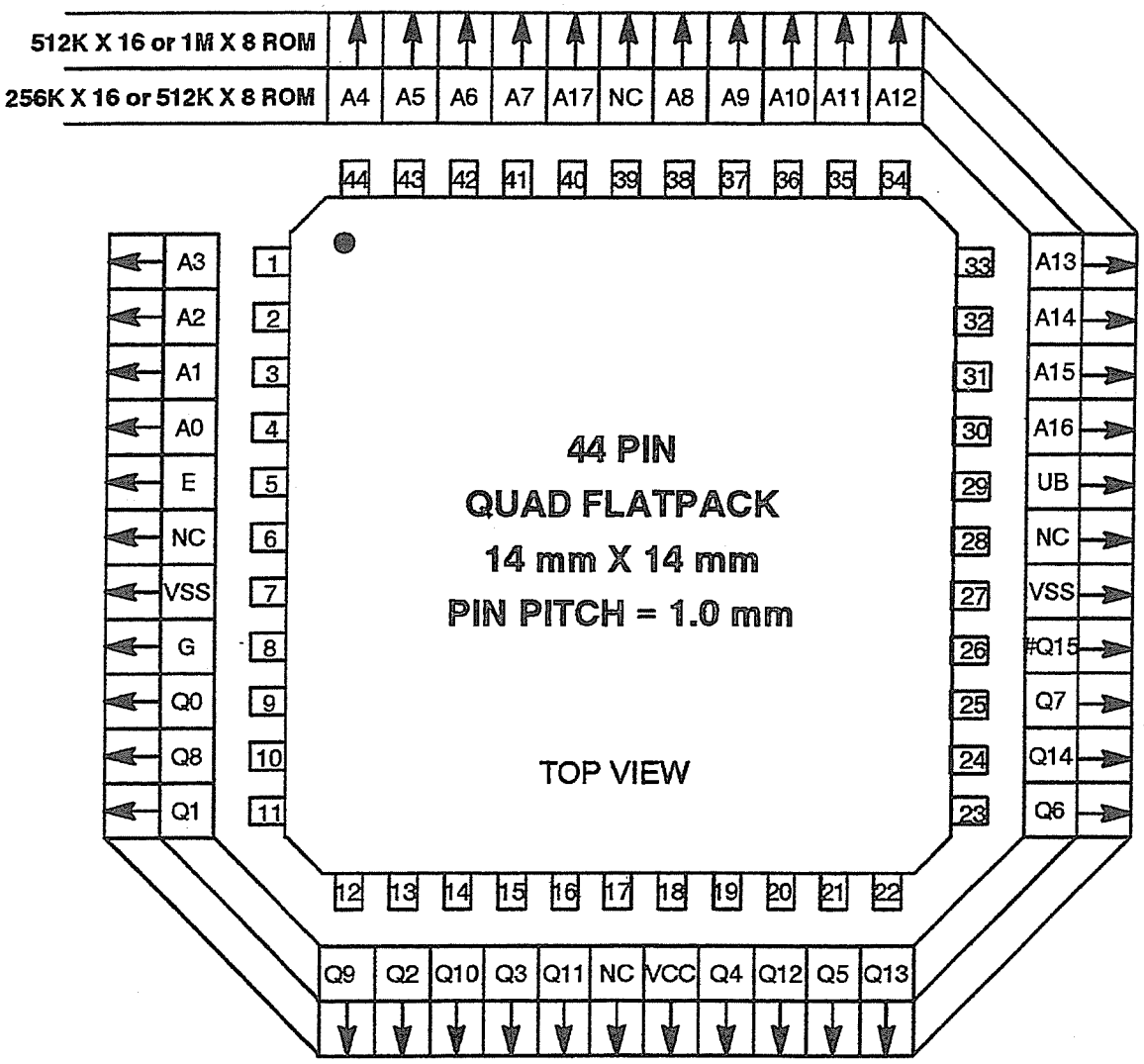


FIGURE 3.2.2-4
16K TO 256K BY 16 AQ MX ROM IN CC



= Pin 26 is Q15 when UB is true and a full 16 bit word is present on Q0 through Q15. When BH is false, either the upper or lower byte is present on pins Q0 to Q7 as determined by the A(–1) address presented on pin 26

FIGURE 3.2.2–5
256K X 16/512K X 8 AND 512K X 16/1M X 8 ROM IN QFP

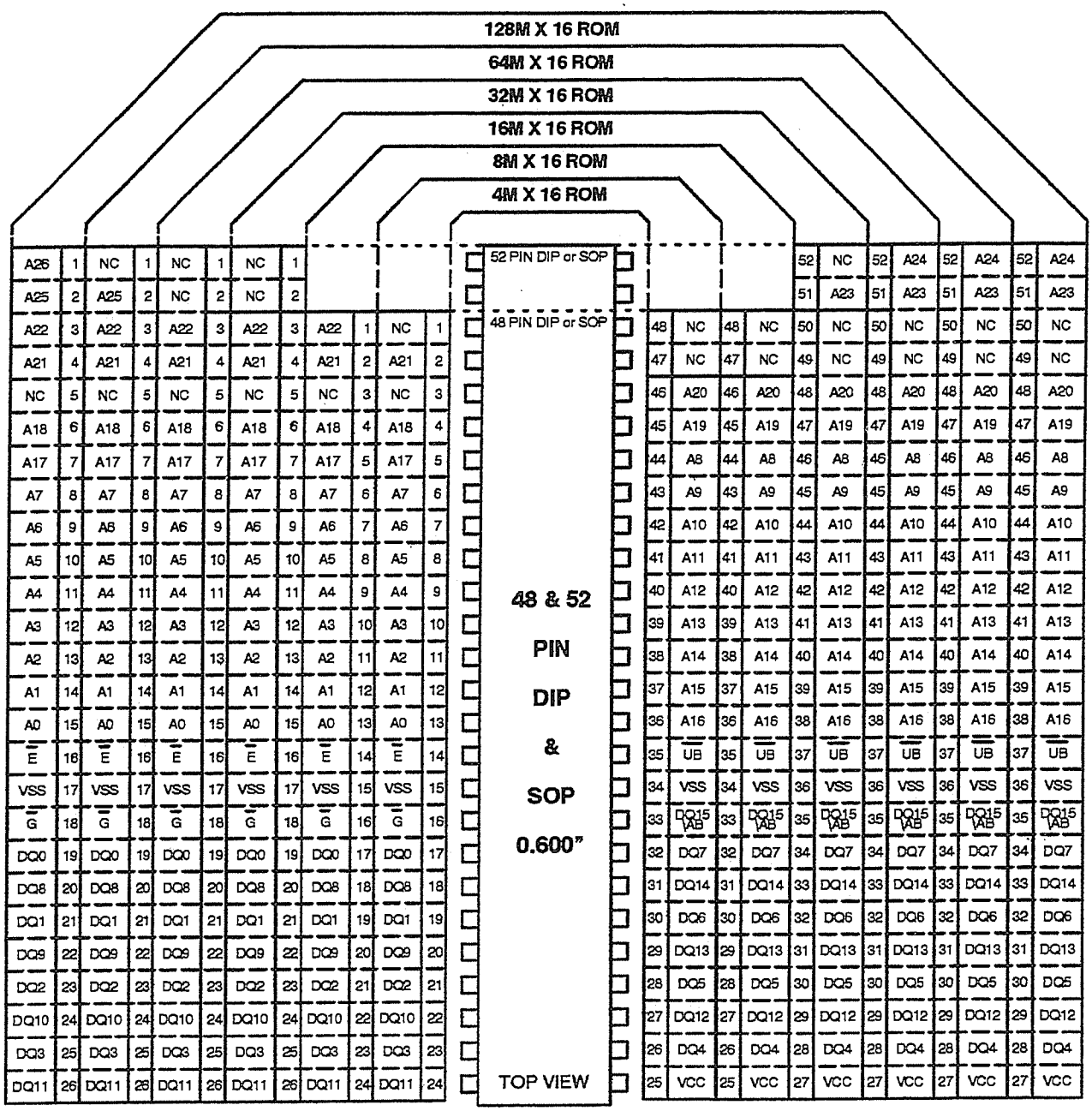
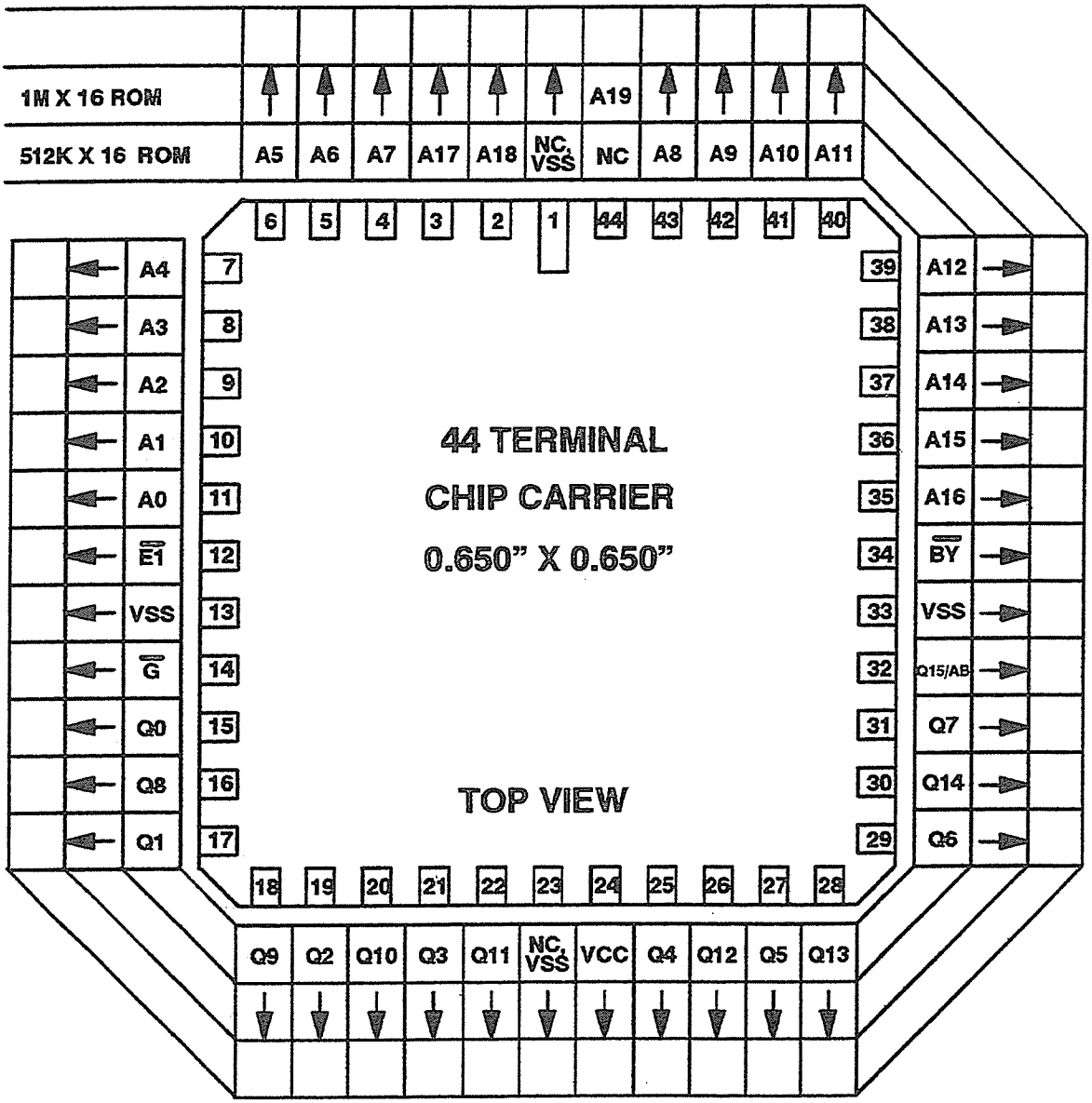


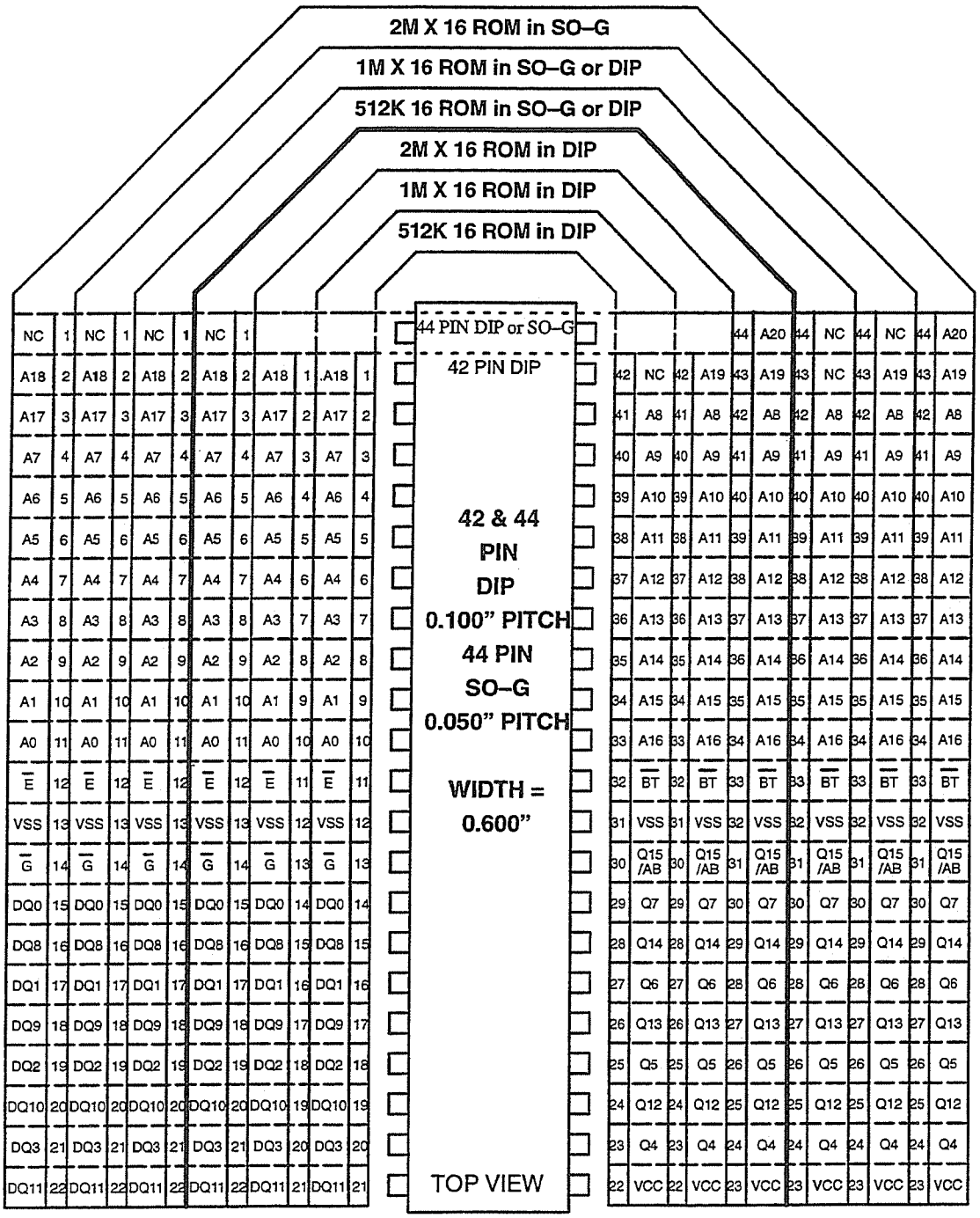
FIGURE 3.2.2–6
4M TO 128M BY 16 ROM IN DIP AND SOP



The device is x8/x16 programmable via BY (pin 34)
X8 configuration when BY = VIL
X16 configuration when BY = VIH
AB is the least significant address bit for X8 operation

FIGURE 3.2.2–7

512K & 1M BY 16 ROM FAMILY IN CC



AB: ADDRESS INPUT, UPPER/
LOWER BYTE SELECT
BT: BYTE MODE ENABLE

FIGURE 3.2.2–8
512K TO 2M BY 16 ROM IN DIP AND SO–G

Release 6

3.3 Programmable Read Only Memory (PROM)

The following PROM standards were developed by the BIPOLAR Committee and in the past have been implemented primarily using BIPOLAR technology. In recent years, however, some of the standards have been implemented using MOS technology.

3.3.1 PROM, Nibble Wide

3.3.1.1 .25K & .5K BY 4 TTL PROM IN DIP
CAPACITY--.25K, .5K WORDS OF 4 BITS
FAMILY--TTL
PACKAGE--16 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT--Fig. 3.3.1-1

3.3.1.2 .25K BY 4 ECL PROM IN DIP
CAPACITY--.25K WORDS OF 4 BITS
FAMILY--10K ECL
PACKAGE--16 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT--Fig. 3.3.1-2

3.3.1.3 1K & 2K BY 4 TTL PROM IN DIP
CAPACITY--1K, 2K WORDS OF 4 BITS
FAMILY--TTL
PACKAGE--18 PIN DIP, 0..3 WIDE
PIN ASSIGNMENT--Fig. 3.3.1-1

3.3.1.4 1K & 2K BY 4 TTL PROM IN SOP
CAPACITY--1K, 2K WORDS OF 4 BITS
FAMILY--TTL
PACKAGE--20 PIN SOG, 0.3" WIDE
PIN ASSIGNMENT--Fig. 3.3.1-3

3.3.1.5 4K TO 8K BY 4 TTL PROM IN DIP
CAPACITY--4K, & 8K WORDS OF 4 BITS
FAMILY--TTL
PACKAGE--20 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT--Fig. 3.3.1-4
NOTE--The 2K devices previously in this group have been deleted from the standard.

3.3.1.6 .25K TO 2K BY 4 TTL PROM FAMILY IN RCC
CAPACITY--256, 512, 1K, 2K WORDS OF 4 BITS
FAMILY--TTL
PACKAGE--20 PAD (PIN) SCC, 0.35" BY 0.35"
PIN ASSIGNMENT--Fig. 3.3.1-5

3.3.1.7 4K BY 4 TTL PROM, 4K BY 4 TTL RPROM IN SCC
CAPACITY--4K WORDS OF 4 BITS, NON-REGISTERED
--4K WORDS OF 4 BITS, REGISTERED
FAMILY--TTL
PACKAGE--20 PAD (PIN) SCC, 0.350" X 0.350"
PIN ASSIGNMENT--Fig. 3.3.1-5

3.3.1.8 1K TO 8K TTL BY 4 PROM FAMILY IN RCC
CAPACITY--1K, 2K, 4K, 8K WORDS OF 4 BITS
FAMILY--TTL
PACKAGE--28 PAD (PIN) RCC, 0.350" BY 0.550"
PIN ASSIGNMENT--Fig. 3.3.1-6

3.3.1.9 1K TO 8K TTL BY 4 PROM FAMILY IN SCC
CAPACITY--1K, 2K, 8K WORDS OF 4 BITS
FAMILY--TTL
PACKAGE--28 PAD (PIN) SCC, 0.450" BY 0.450"
PIN ASSIGNMENT--Fig. 3.3.1-7

3.3.1.10 1K TO 4K BY 4 DPROM FAMILIES IN DIP & SCC

CAPACITY--1K, 2K, 4K WORDS OF 4 BITS
FAMILY--TTL
LOGIC FEATURES--These parts have built in diagnostic features as defined individually by the manufacturer.

There are two versions of these parts: one in DIP and the other in SCC.

PACKAGE--24 PIN DIP, 0.300" WIDE
PIN ASSIGNMENT--Fig. 3.3.1-8
PACKAGE--28 PAD (PIN) SCC, 0.450" BY 0.450"
PIN ASSIGNMENT--Fig. 3.3.1-9

3.3.1.11 1K TO 16K BY 4 ECL PROM FAMILY IN DIP

CAPACITY--1K, 2K, 4K, 8K, 16K WORDS OF 4 BITS
FAMILY--10K ECL
PACKAGE--1K, 2K, 4K IN 20 PIN DIP, 0.3" WIDE
--8K, 16K IN 24 PIN DIP, WIDTH UNDEFINED
PIN ASSIGNMENT--Fig. 3.3.1-10

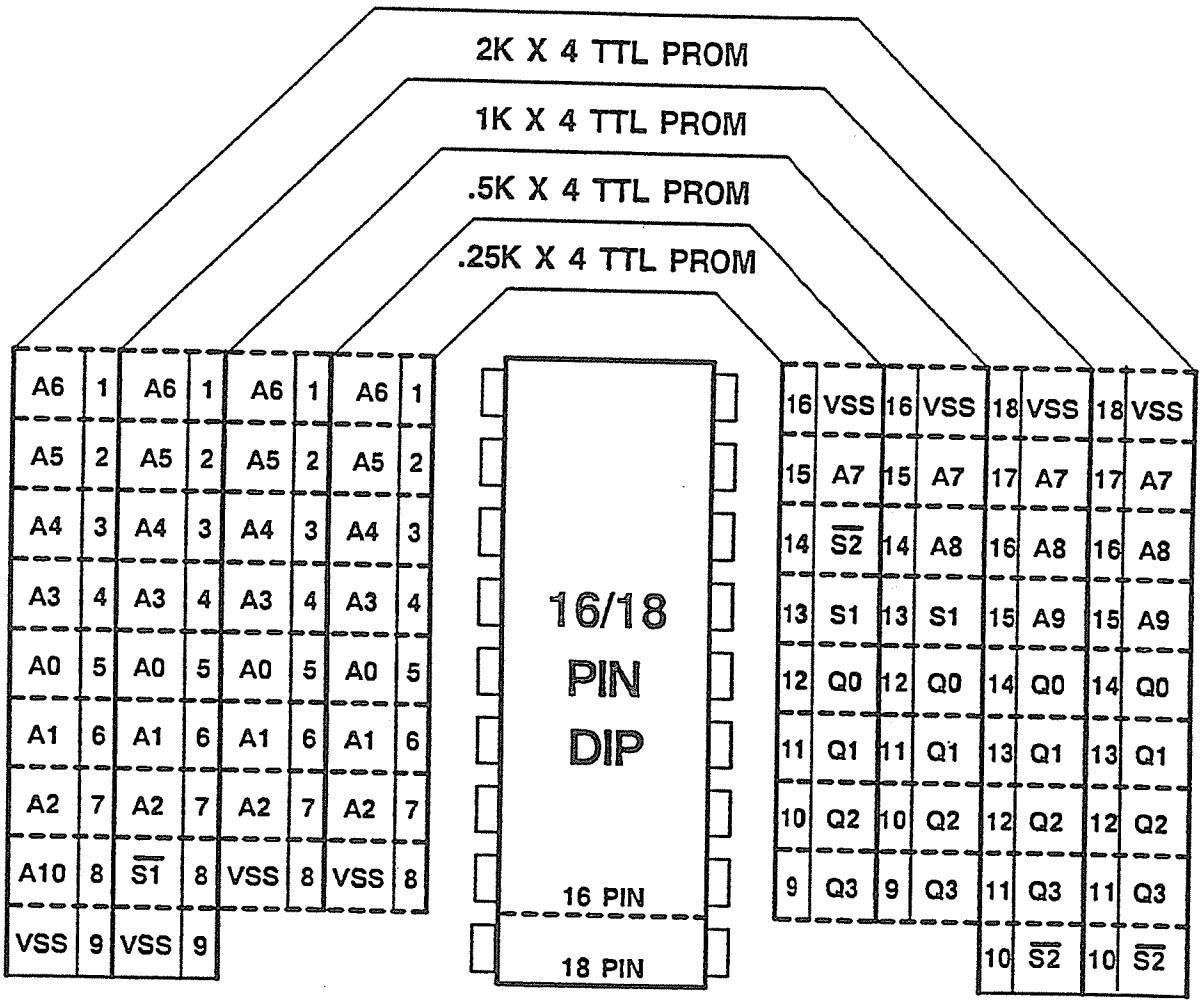


FIGURE 3.3.1-1
.25K TO 2K BY 4 TTL PROM IN DIP

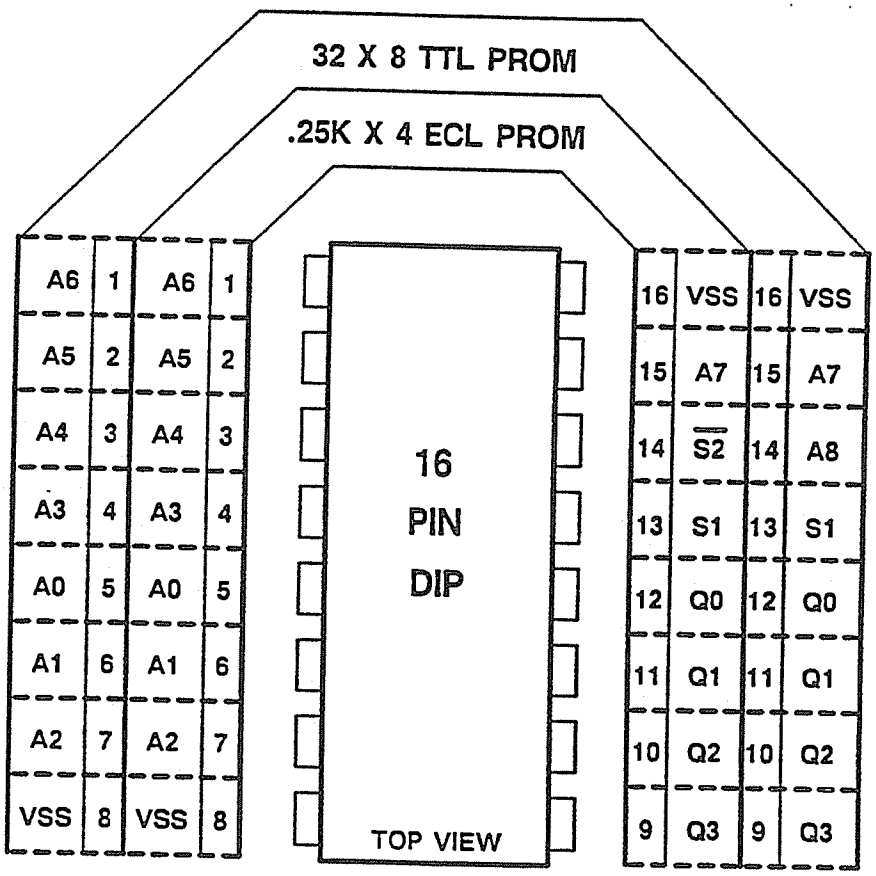


FIGURE 3.3.1-2
256 BY 4 ECL PROM IN DIP

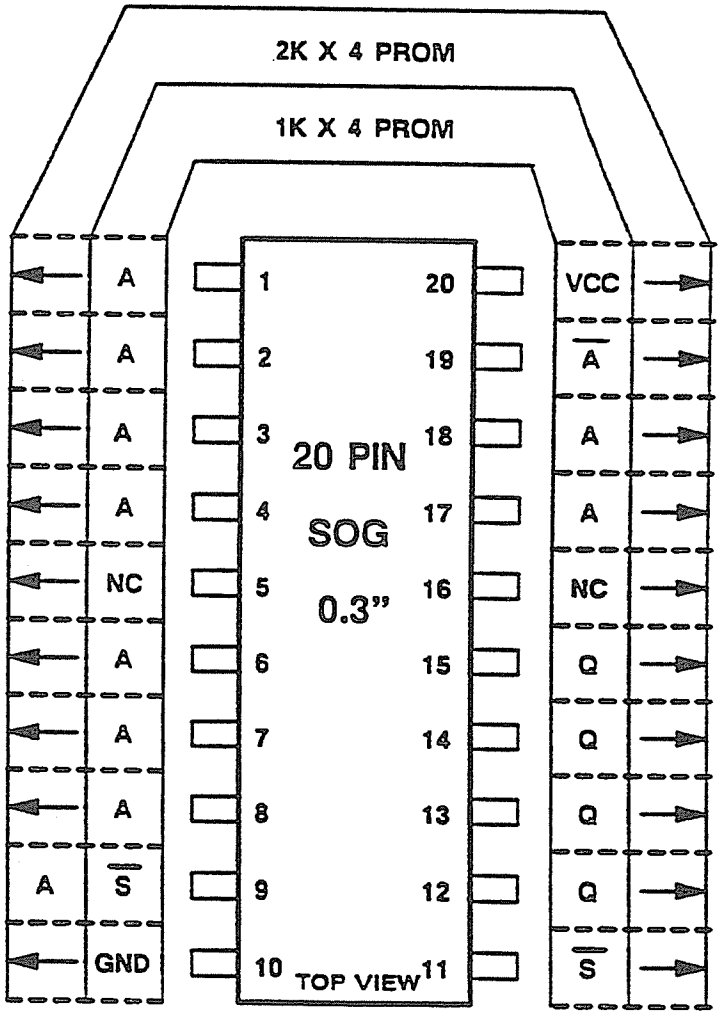


FIGURE 3.3.1-3
1K & 2K BY 4 TTL PROM IN SOG

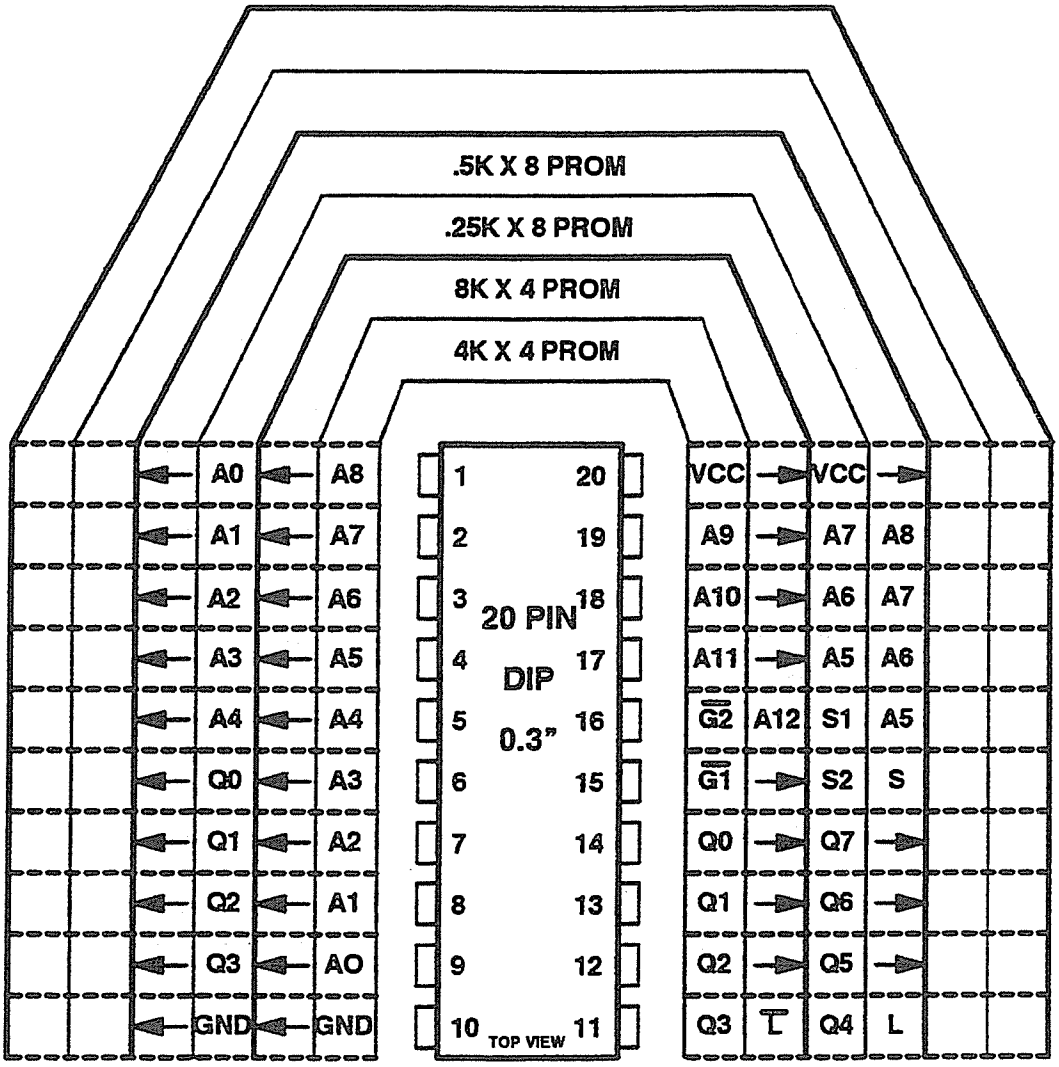


FIGURE 3.3.1–4
4K & 8K BY 4 TTL PROM IN DIP

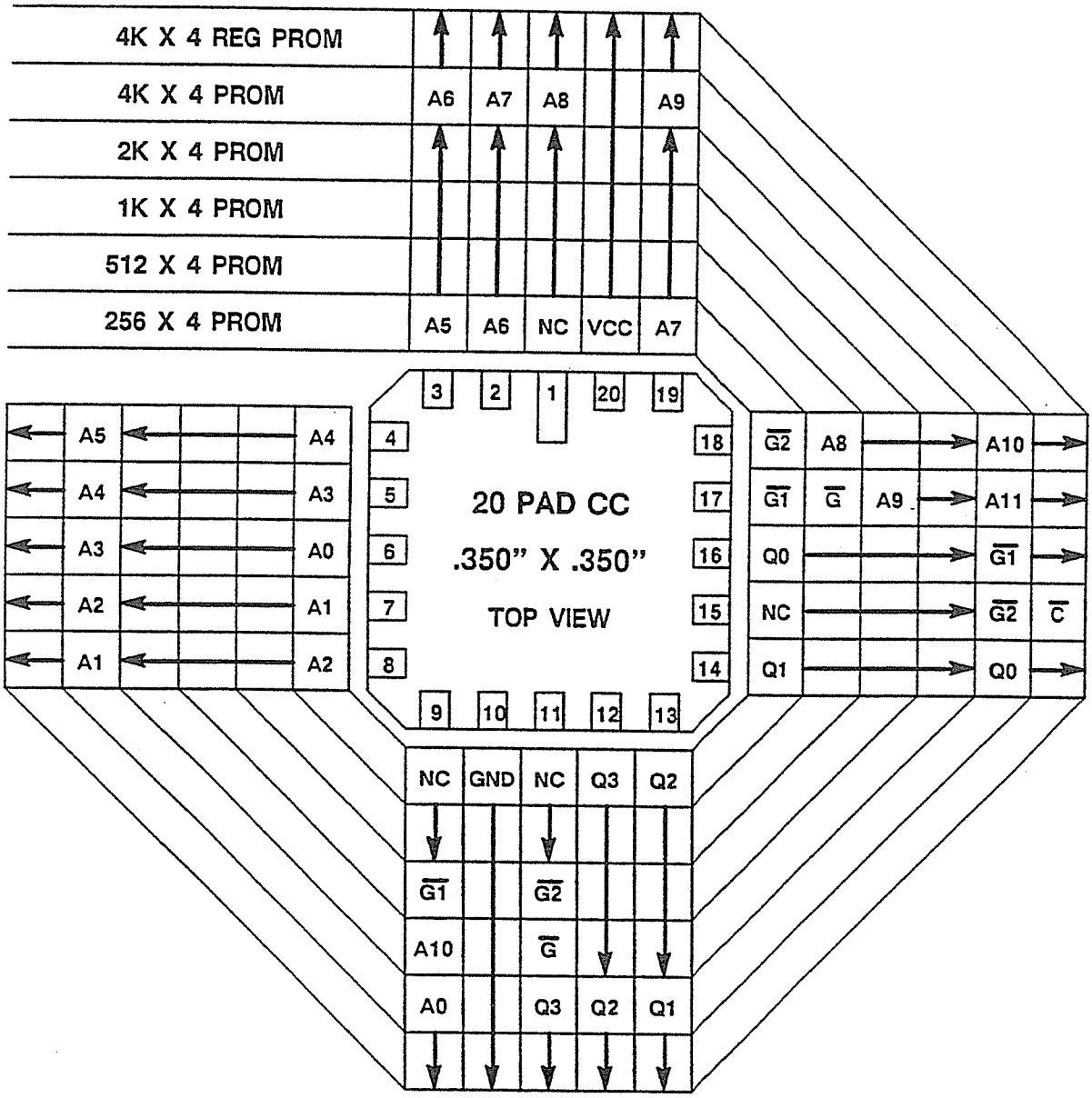


FIGURE 3.3.1-5
.25K TO 4K BY 4 TTL PROM FAMILY IN CC

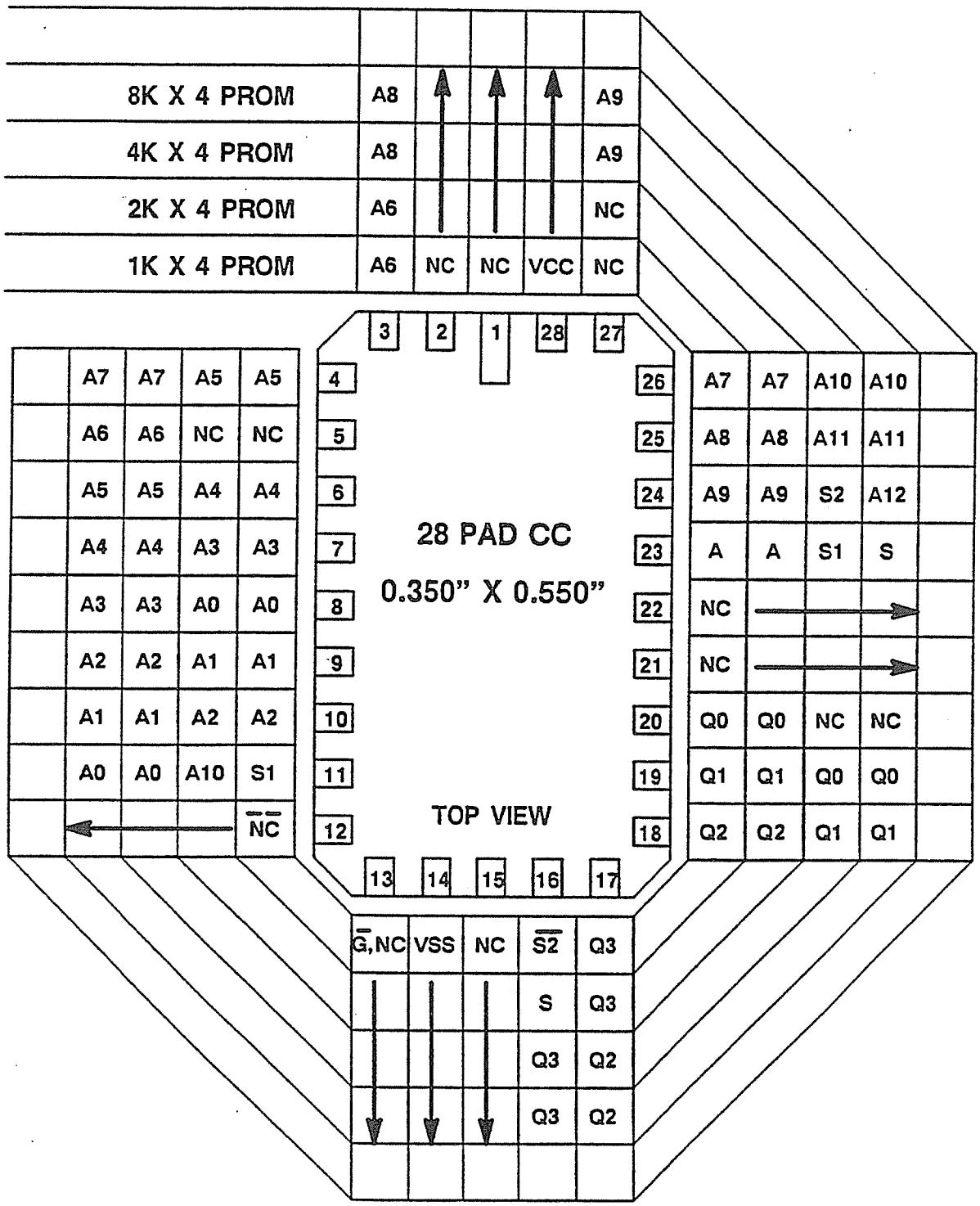


FIGURE 3.3.1-6
1K TO 8K BY 4 TTL PROM IN RCC

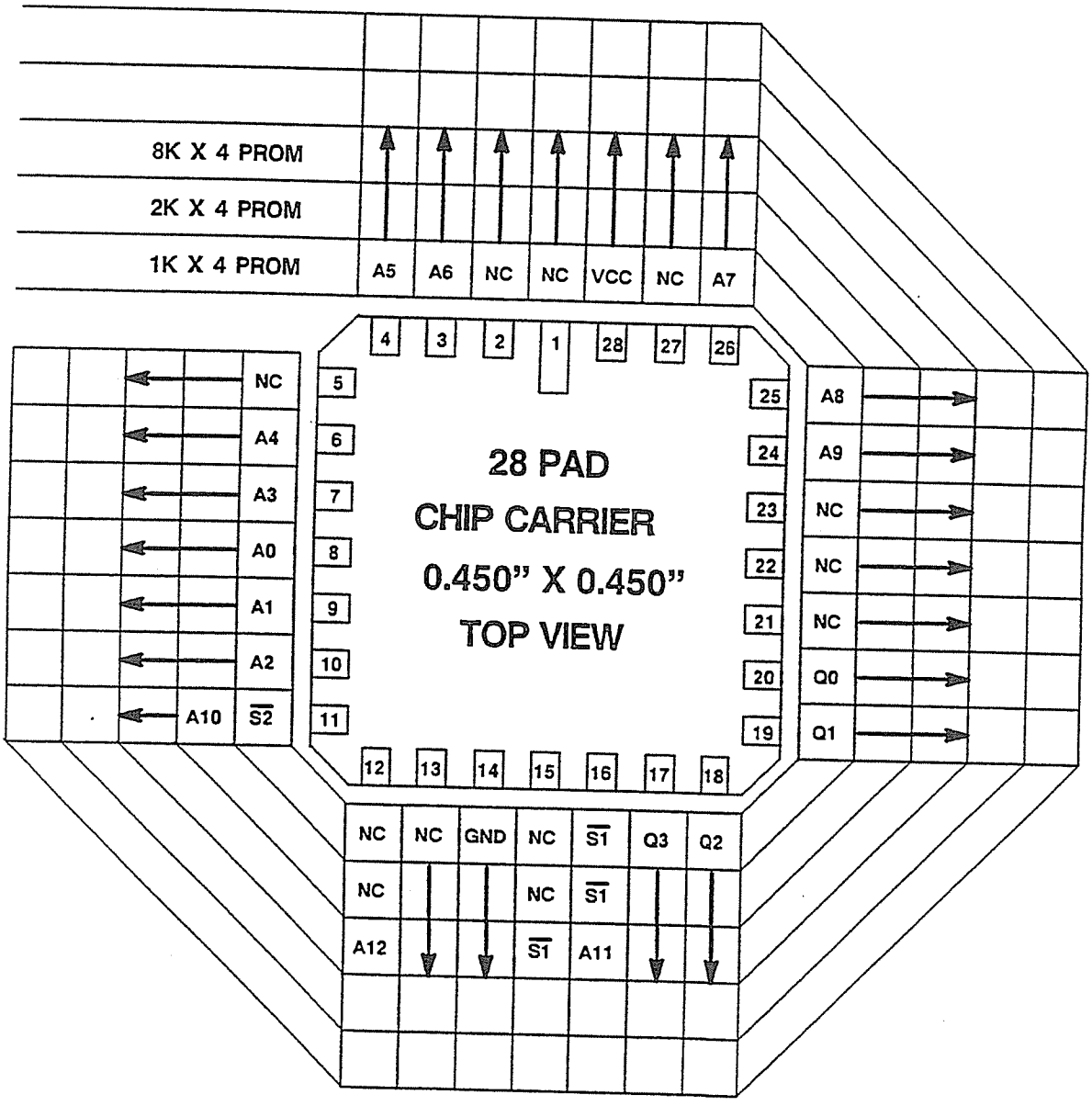


FIGURE 3.3.1-7
1K TO 8K BY 4 TTL PROM IN SCC

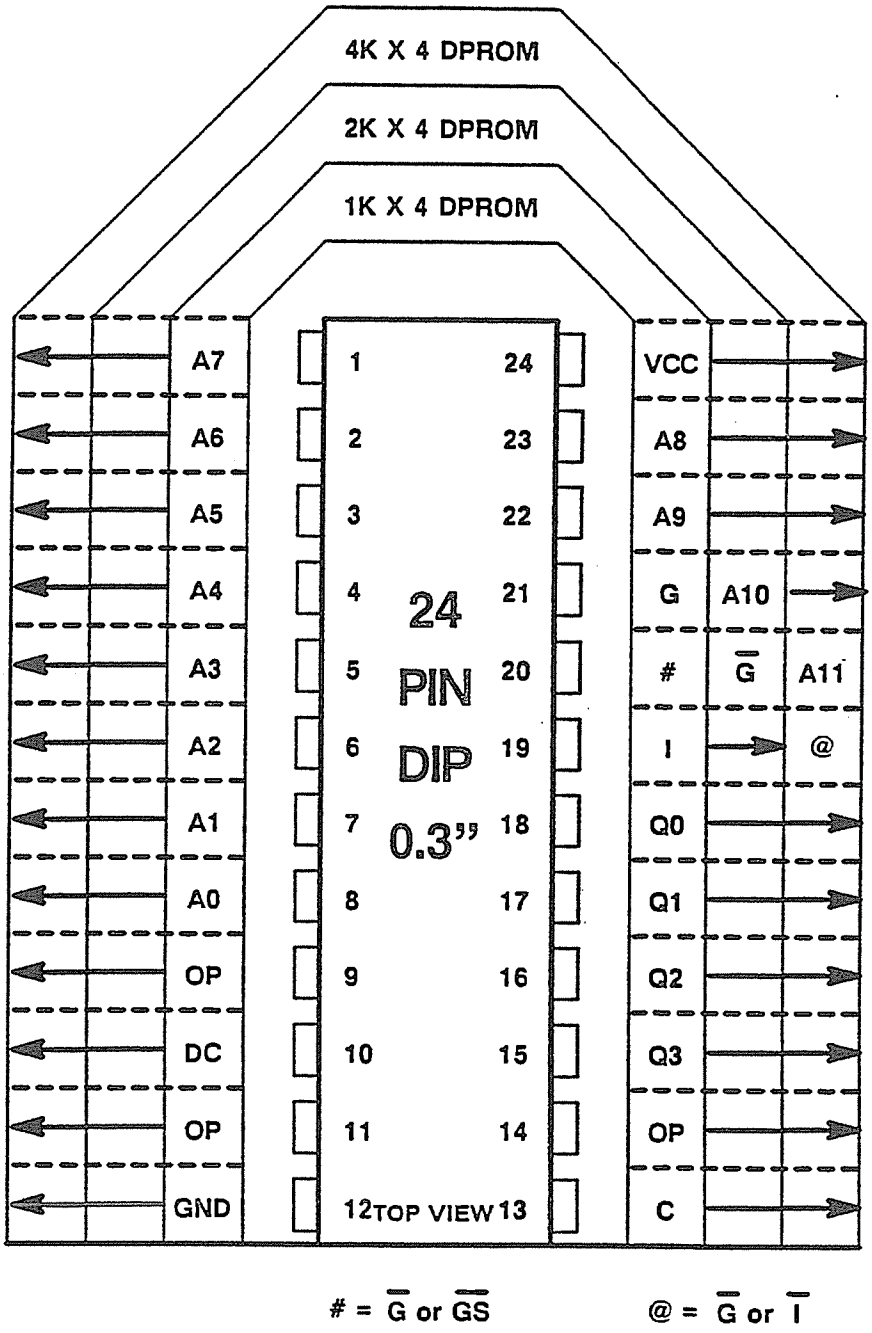


FIGURE 3.3.1-8
1K TO 4K BY 4 TTL DPROM IN DIP

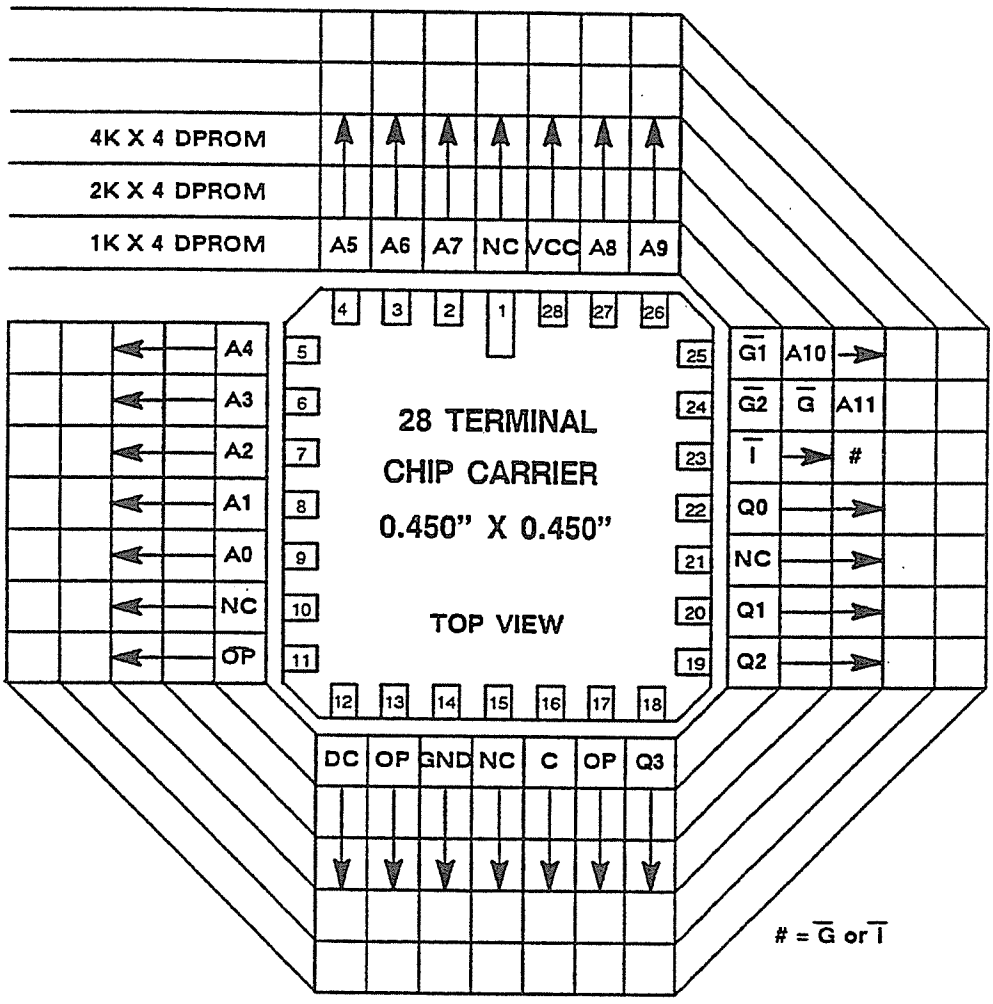
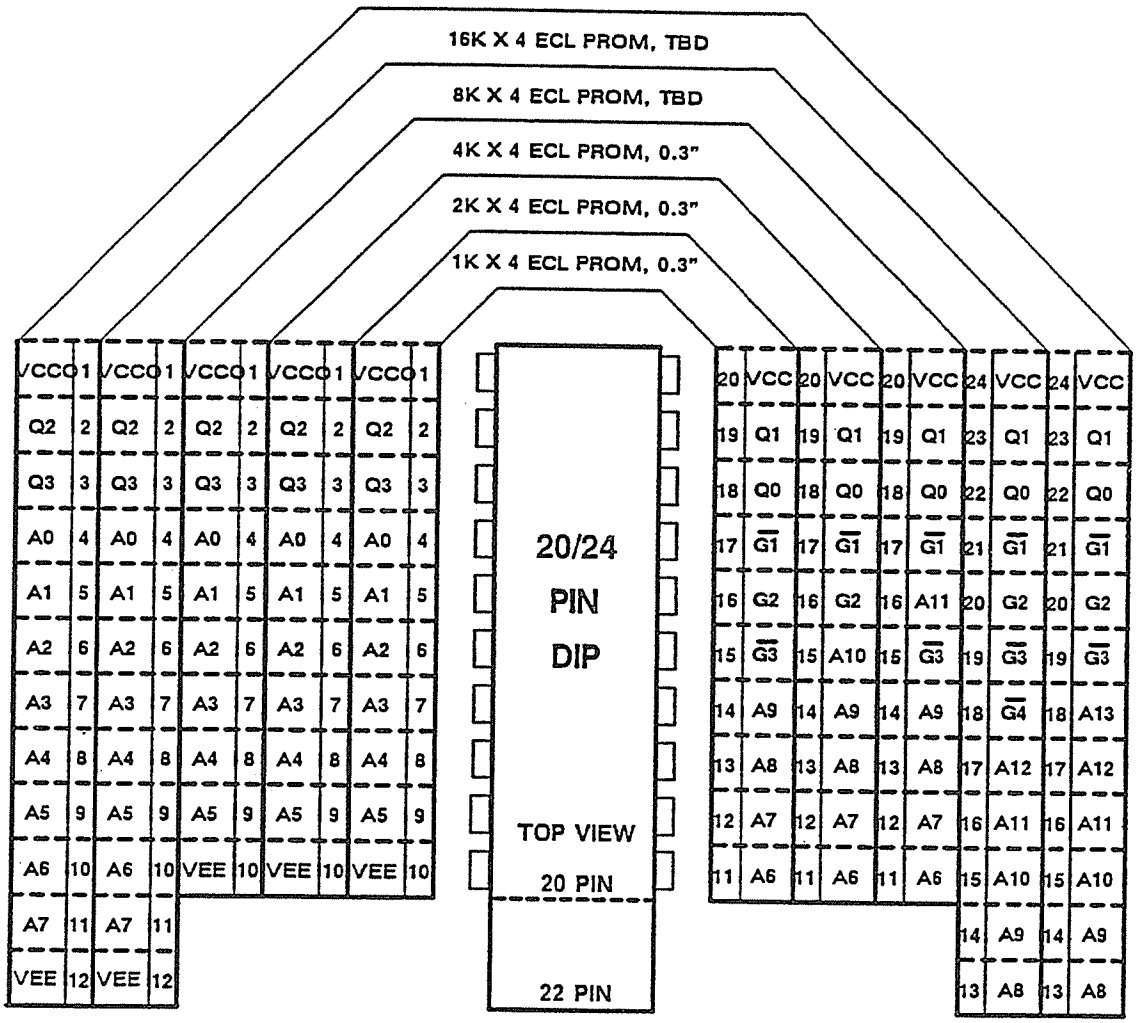


FIGURE 3.3.1-9
1K TO 4K BY 4 DPROM IN CC



NOTE: THESE STANDARDS ARE APPROVED FOR 10K ECL ONLY

FIGURE 3.3.1-10
1K TO 16K BY 4 ECL PROM IN DIP

3.3.2 PROM, Bytewide

3.3.2.1 32 BY 8 TTL PROM IN DIP & SCC

CAPACITY--32 WORDS OF 8 BITS
FAMILY--TTL

There are two versions of this part: one in DIP and the other in SCC

PACKAGE--16 PIN DIP, 0.300" WIDE
PIN ASSIGNMENT--Fig. 3.3.2-1
PACKAGE--20 PAD (PIN) SCC, 0.350" BY 0.350"
PIN ASSIGNMENT--Fig. 3.3.2-2

3.3.2.2 32 BY 8 ECL PROM IN DIP & SCC

CAPACITY--32 WORDS OF 8 BITS
FAMILY--ECL

There are two versions of this part: one in DIP and the other in SCC

PACKAGE--18 PIN DIP, 0.300" WIDE
PIN ASSIGNMENT--Fig. 3.3.2-1
PACKAGE--20 PAD (PIN) SCC, 0.350" BY 0.350"
PIN ASSIGNMENT--Fig. 3.3.2-2

3.3.2.3 .25K & .5K BY 8 TTL PROM IN DIP & SCC

CAPACITY--.25K, .5K WORDS OF 8 BITS
FAMILY--TTL

There are two versions of these parts: one in DIP and the other in SCC

PACKAGE--16 PIN DIP, 0.300" WIDE
PIN ASSIGNMENT--Fig. 3.3.2-3
PACKAGE--20 PAD (PIN) SCC, 0.350" BY 0.350"
PIN ASSIGNMENT--Fig. 3.3.2-2

3.3.2.4 .25K TO 8K BY 8 TTL PROM FAMILY IN DIP

CAPACITY--.25K, .5K, 1K, 2K, 4K, 8K WORDS OF 8 BITS
FAMILY--TTL
PACKAGE--24 PIN DIP, 0.3" or 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.3.2-4

3.3.2.5 .5K TO 4K BY 8 TTL LPROM FAMILY IN DIP

CAPACITY--.5K, 1K, 2K, 4K WORDS OF 8 BITS
FAMILY--TTL
PACKAGE--24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.3.2-5

3.3.2.6 .5K TO 4K BY 8 TTL RPROM FAMILY IN DIP

CAPACITY--.5K, 1K, 2K, 4K WORDS OF 8 BITS
FAMILY--TTL
PACKAGE--24 PIN DIP, 0.3 OR 0.6" WIDE
--Both package widths are approved for the 2K and 4K devices by this standard.
PIN ASSIGNMENT--Fig. 3.3.2-6

3.3.2.7 .5K TO 8K BY 8 TTL PROM FAMILIES IN RCC & SCC

CAPACITY--.5K, 1K, 2K, 4K, 8K WORDS OF 8 BITS
FAMILY--TTL

There are two versions of these parts: one in SCC and the other in RCC

PACKAGE--28 PAD (PIN) SCC, 0.450" BY 0.450"
PIN ASSIGNMENT--Fig. 3.3.2-7
PACKAGE--32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT--Fig. 3.3.2-8

3.3.2.8 .5K TO 2K BY 8 TTL RPROM FAMILY IN SCC

CAPACITY--.5K, 1K, 2K WORDS OF 8 BITS
LOGIC FEATURES--The data out is stored in an output register
PACKAGE--28 PAD (PIN) SCC, 0.450" X 0.450"
PIN ASSIGNMENT--Fig. 3.3.2-9

3.3.2.9 16K TO 64K BY 8 TTL PROM FAMILY IN DIP

CAPACITY--16K, 32K, 64K WORDS OF 8 BITS
FAMILY--TTL
PACKAGE--28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS--Fig. 3.3.2-10

3.3.2.10 512 BY 8 ECL RPROM IN DIP & SCC

CAPACITY--512 WORDS OF 8 BITS
FAMILY--10K and 100K ECL
There are two versions of this part: one in DIP and the other in SCC
PACKAGE--24 PIN DIP, 0.300" WIDE
PIN ASSIGNMENT--Fig. 3.3.2-11
PACKAGE--28 TERMINAL SCC, 0.450" BY 0.450"
PIN ASSIGNMENT--Fig. 3.3.2-11

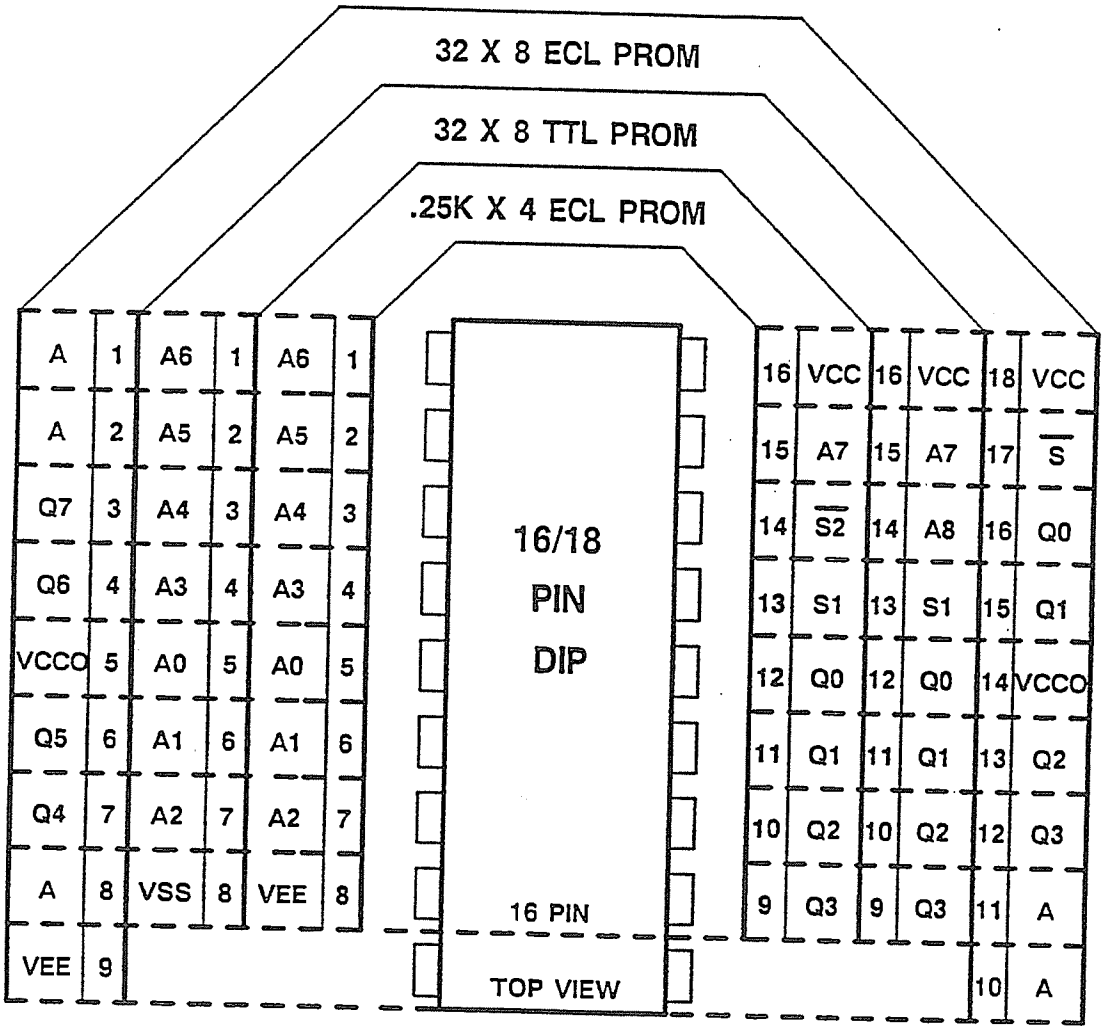


FIGURE 3.3.2-1
32 BY 8 TTL PROM IN DIP
32 BY 8 ECL PROM IN DIP

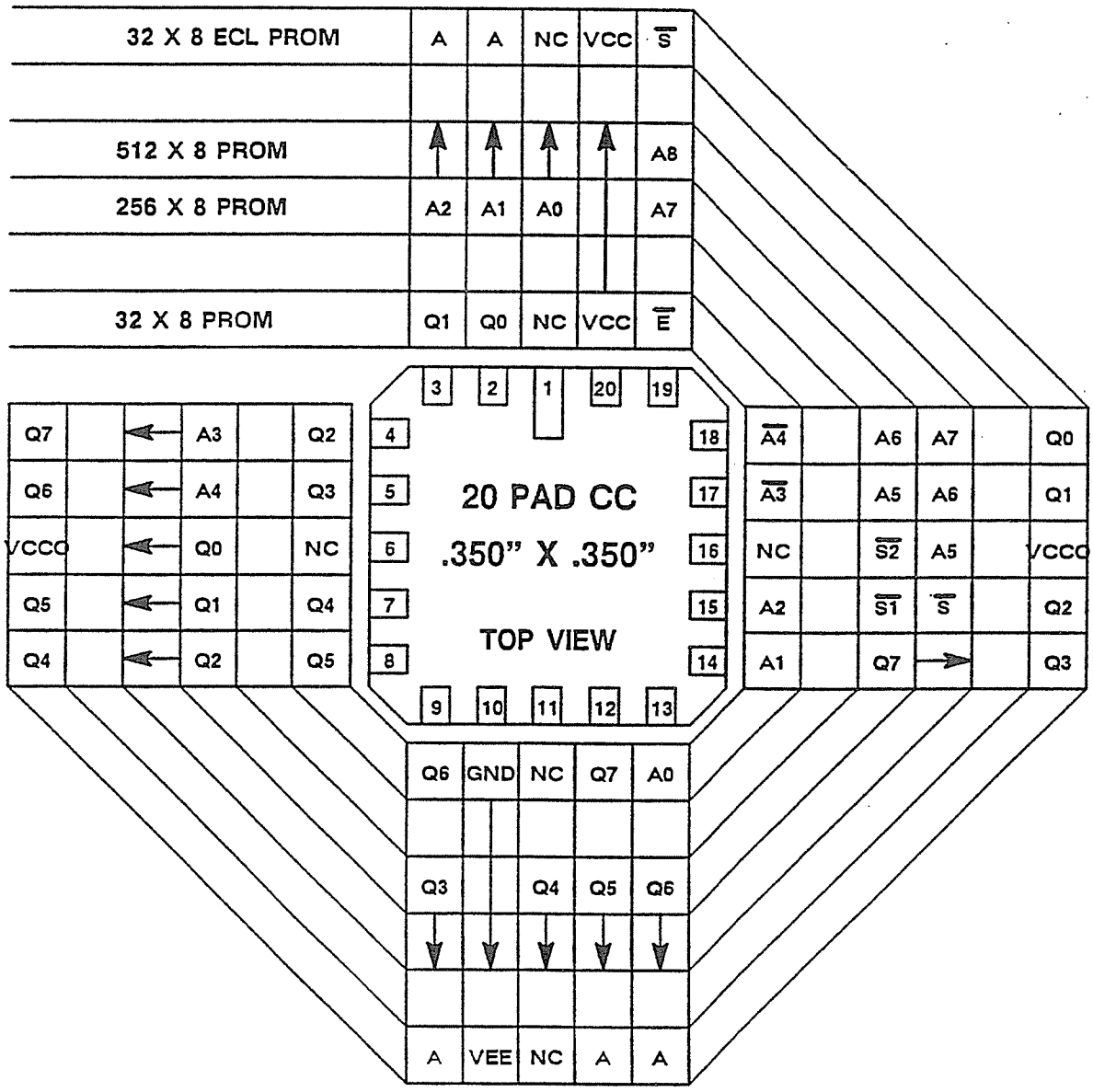


FIGURE 3.3.2-2
32, 256, & 512 BY 8 TTL PROM IN CC
32 BY 8 ECL PROM IN CC

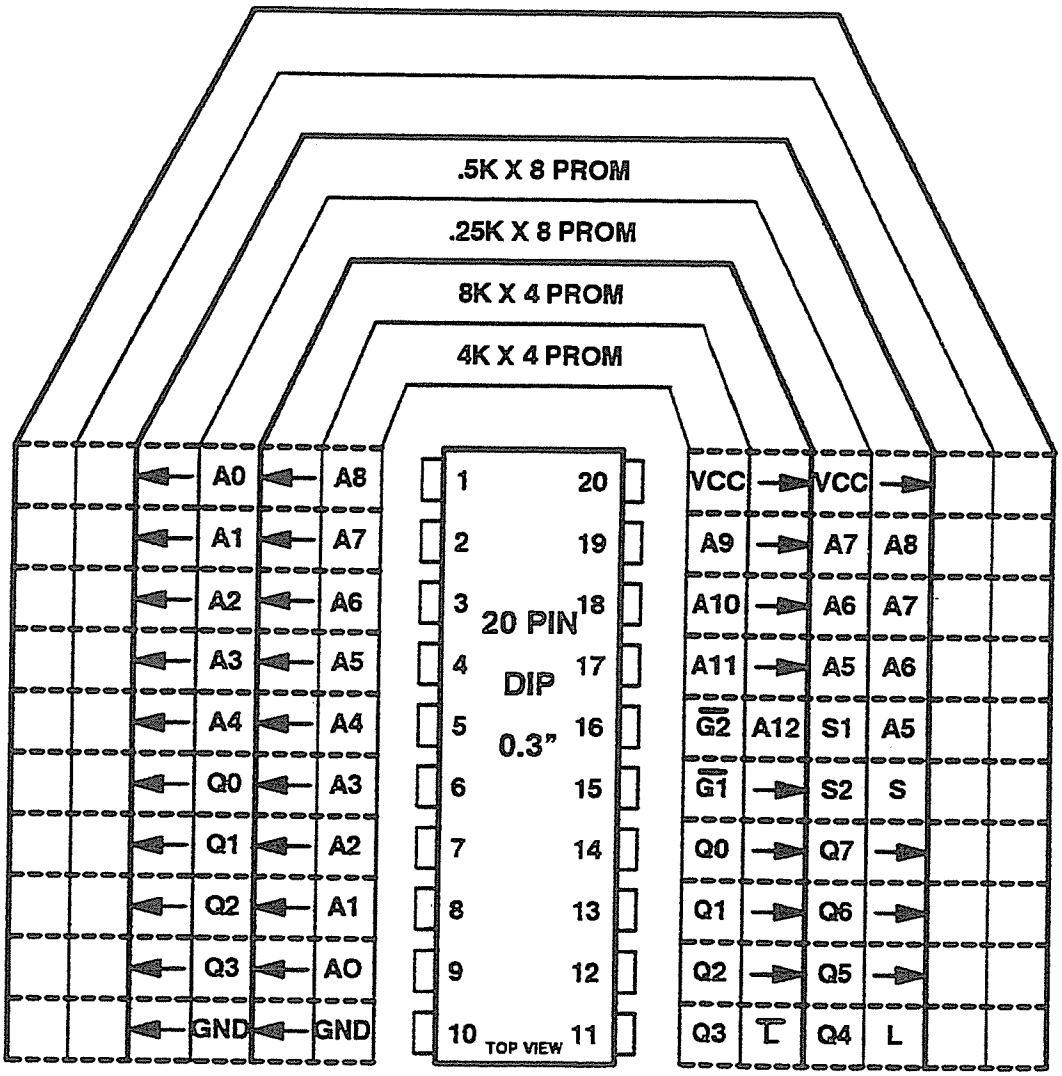
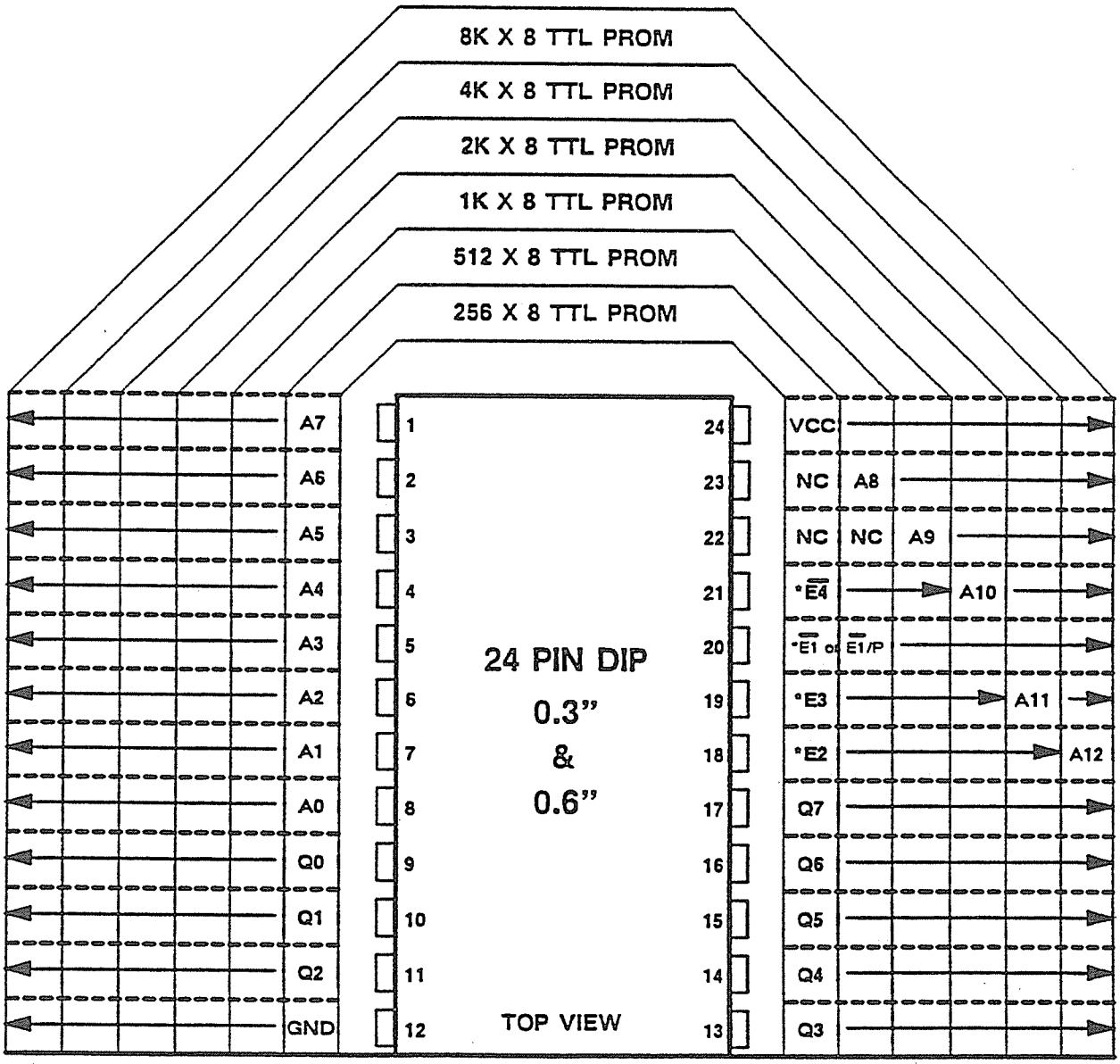
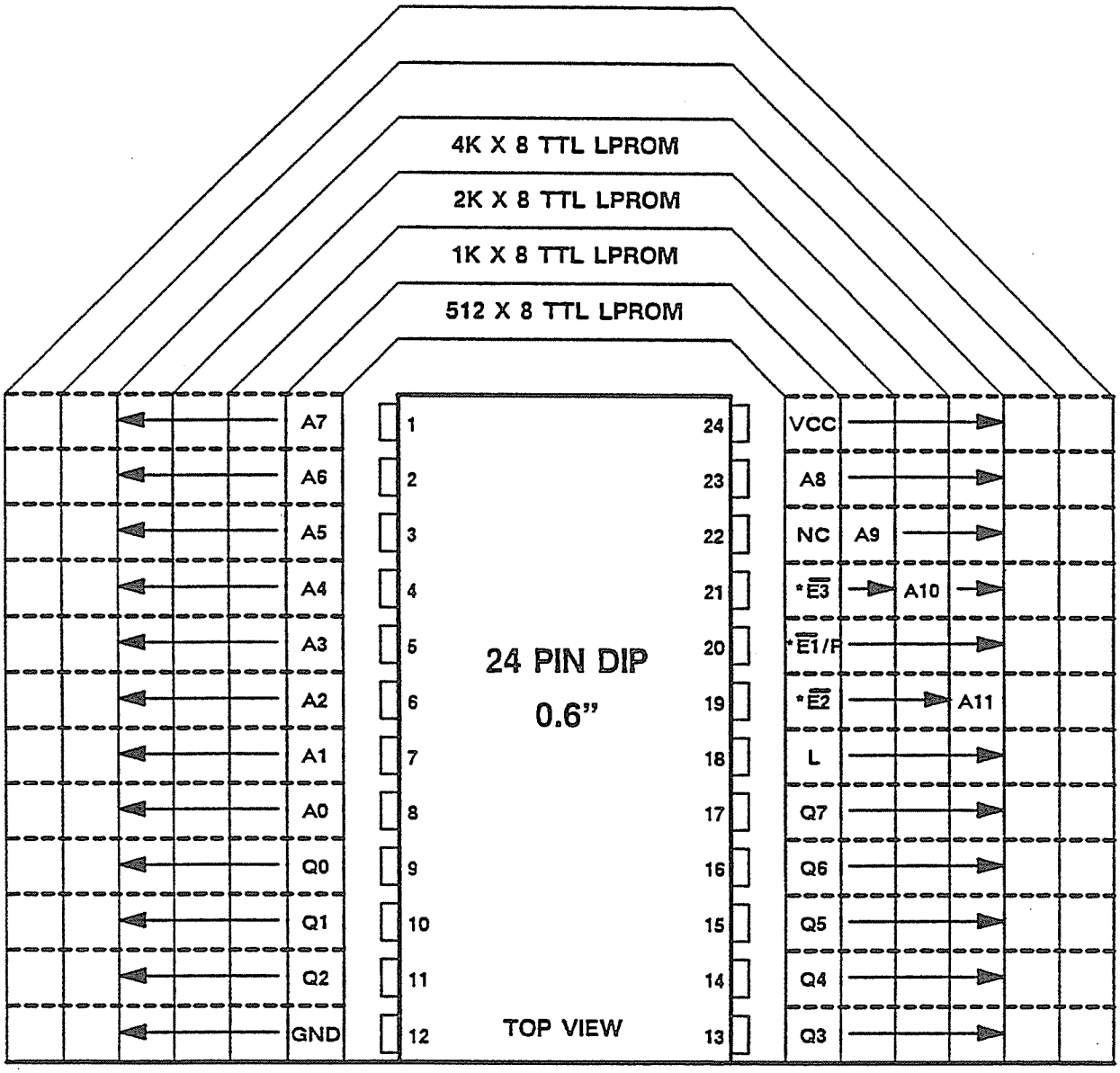


FIGURE 3.3.2–3
.25K & .5K BY 8 TTL PROM IN DIP



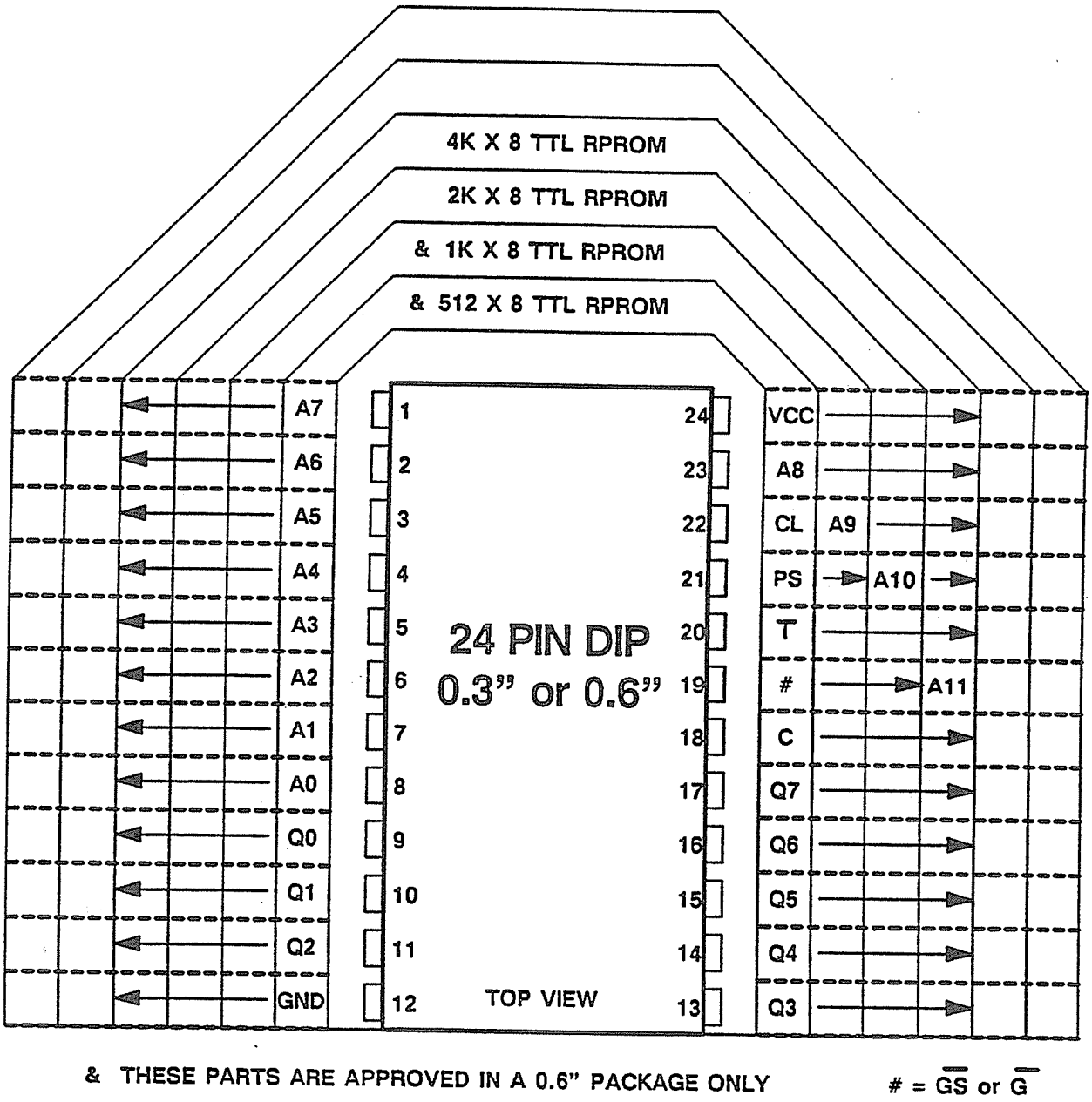
* $\overline{G}$ or G CAN BE SUBSTITUTED FOR $\overline{E}$ or E ON PARTS WITHOUT POWER DOWN

FIGURE 3.3.2-4
.25K TO 8K BY 8 TTL PROM IN DIP



* $\overline{G}$ CAN BE SUBSTITUTED FOR $\overline{E}$ ON DEVICES WITHOUT POWER DOWN

FIGURE 3.3.2-5
.5K TO 4K BY 8 TTL LPROM IN DIP



& THESE PARTS ARE APPROVED IN A 0.6" PACKAGE ONLY

= $\overline{GS}$ or $\overline{G}$

FIGURE 3.3.2-6
.5K TO 4K BY 8 TTL RPROM IN DIP

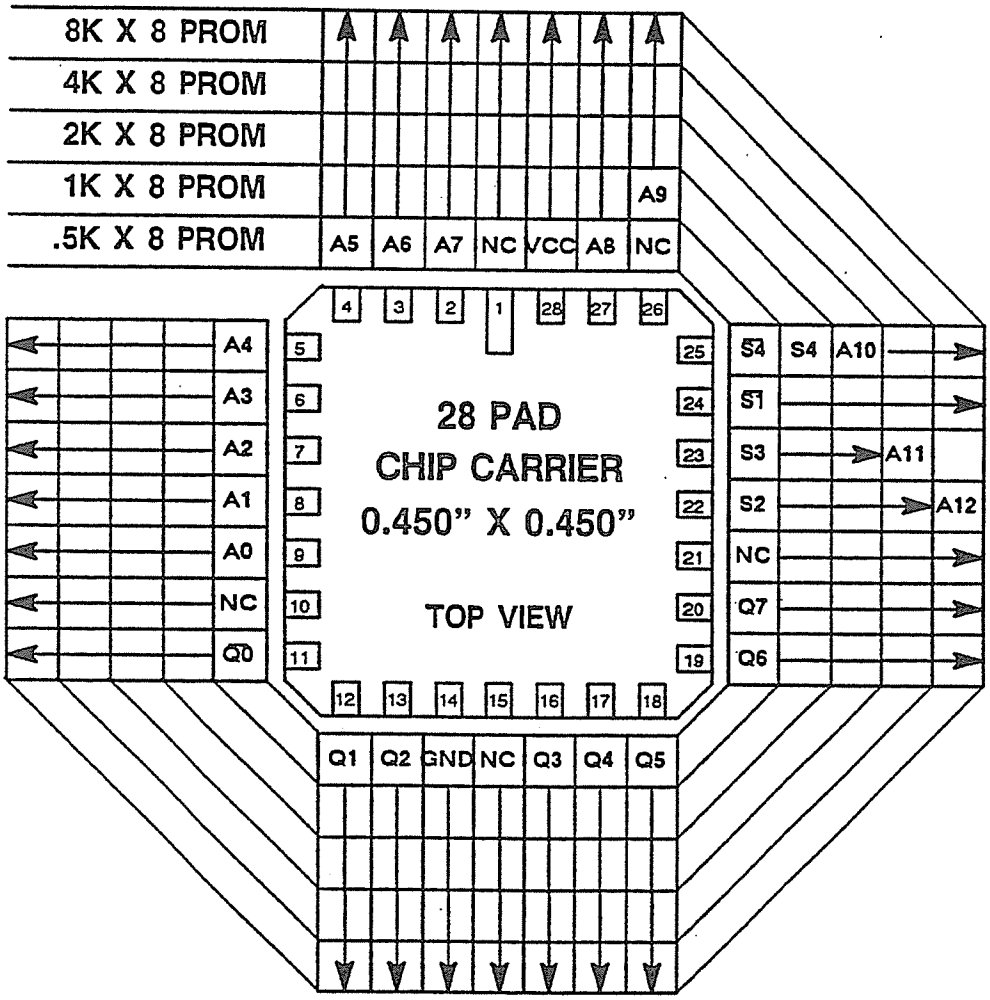


FIGURE 3.3.2-7
.5K TO 8K BY 8 TTL PROM IN SCC

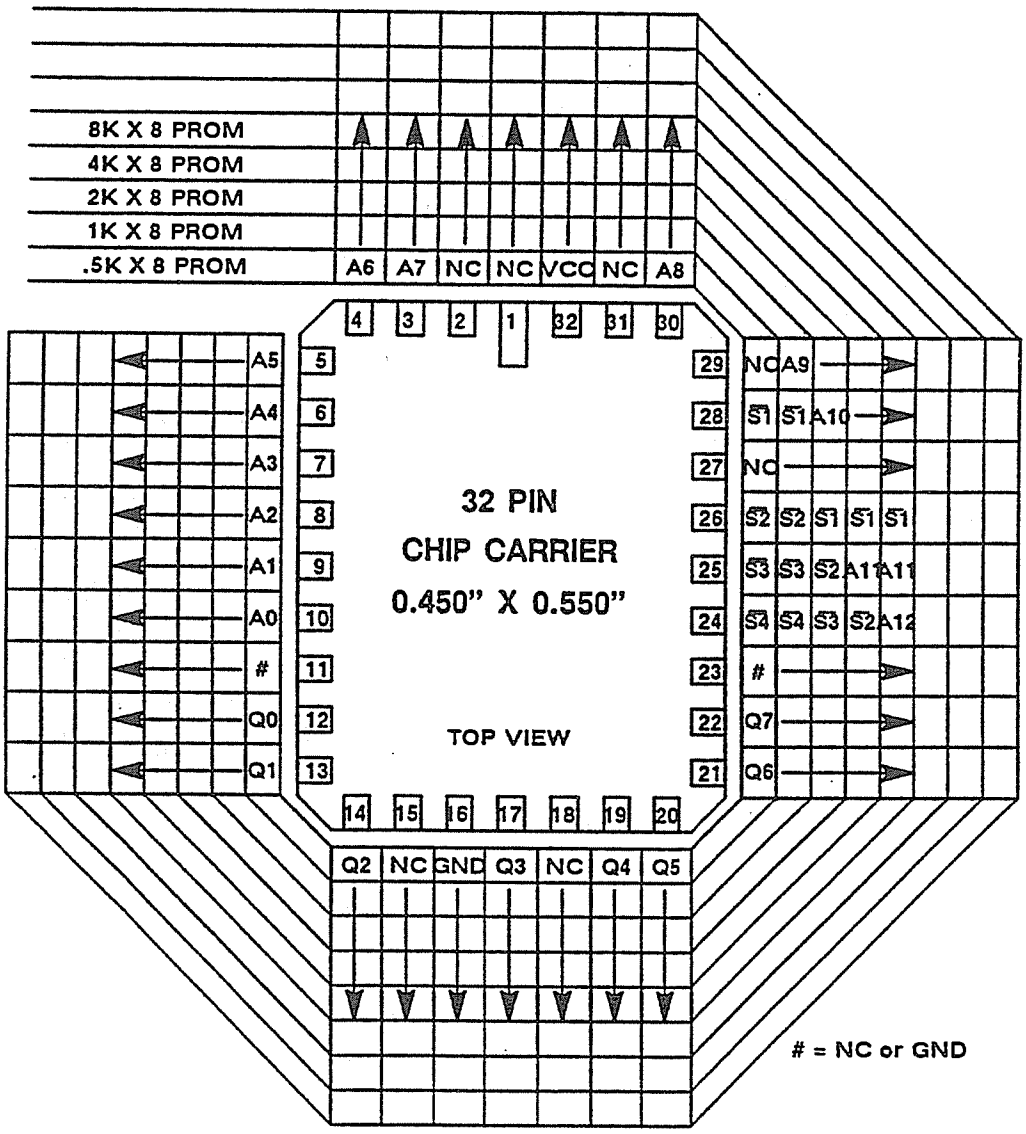
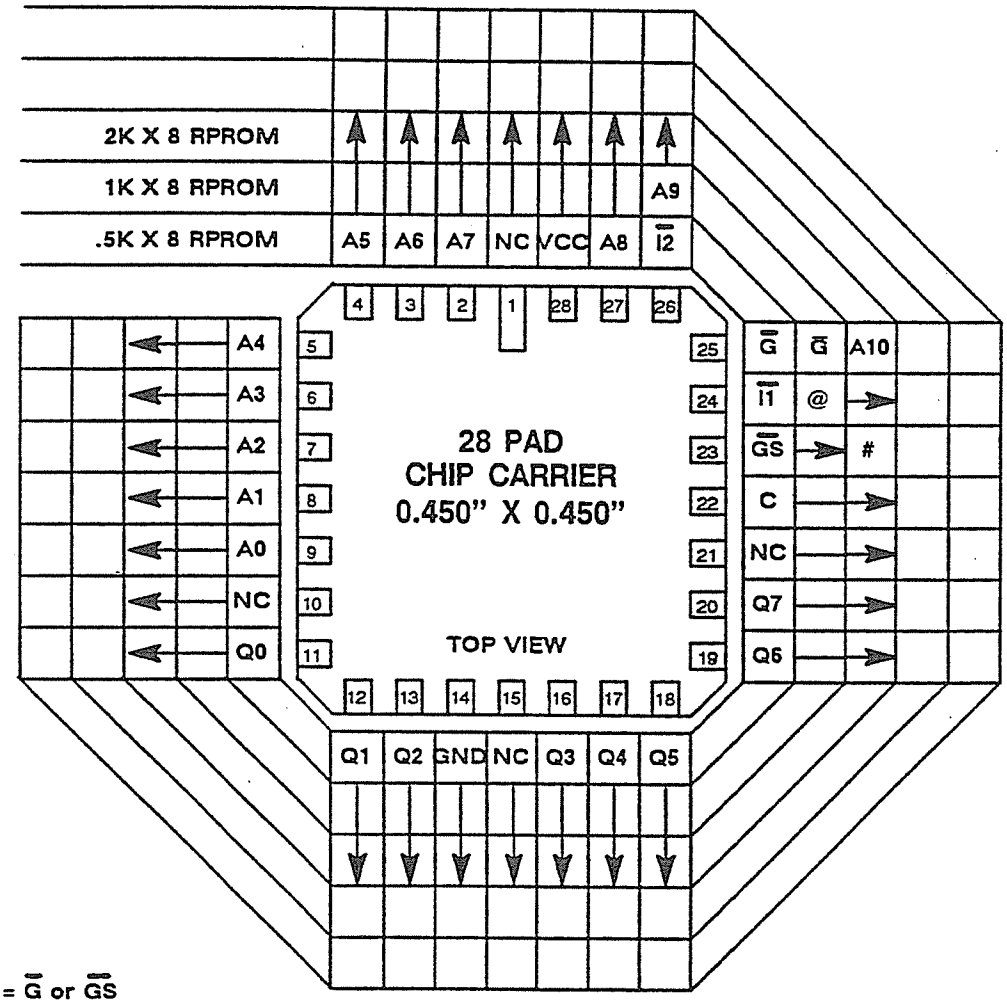


FIGURE 3.3.2-8
.5K TO 8K BY 8 TTL PROM IN RCC



# = $\overline{G}$ or $\overline{GS}$
I1 = ASYNCHRONOUS CLEAR INPUT
I2 = ASYNCHRONOUS PRESET INPUT
@ = $\overline{I}$ or $\overline{IS}$, ASYNCHRONOUS or SYNCHRONOUS INITIALIZE PROGRAMMABLE INPUT

FIGURE 3.3.2-9
.5K TO 2K BY 8 RPROM IN CC

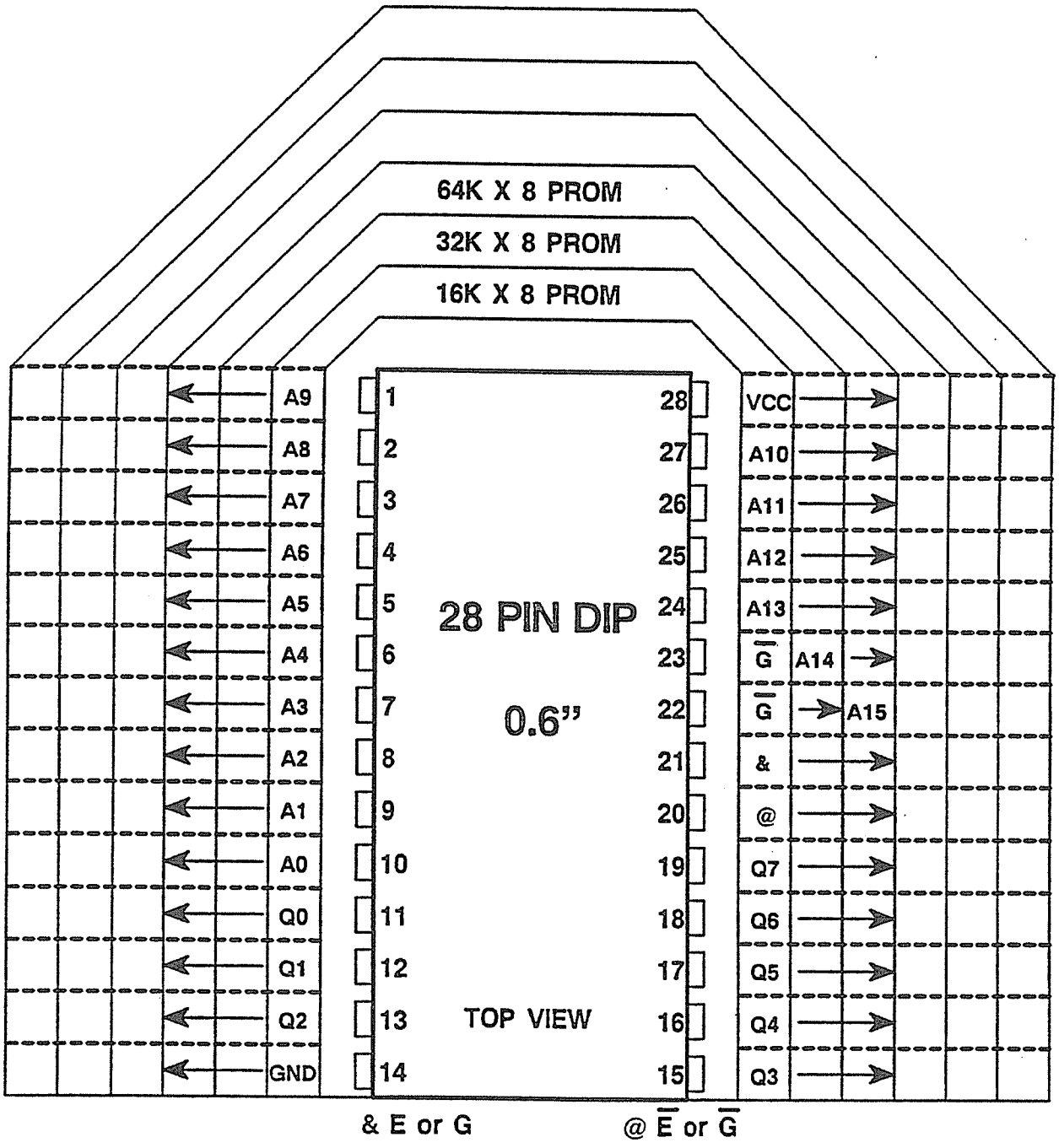
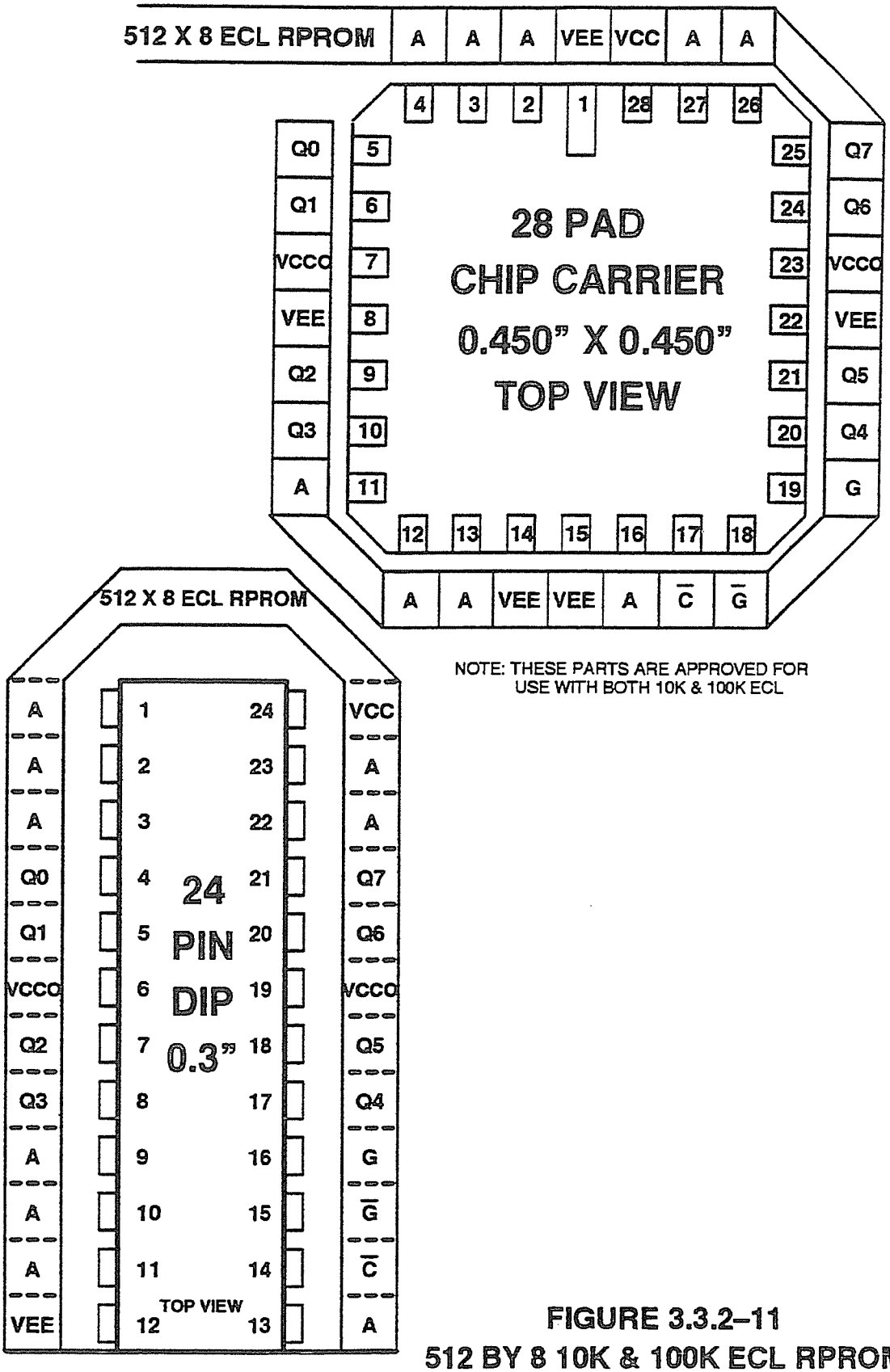


FIGURE 3.3.2-10
16K TO 64K BY 8 TTL PROM IN DIP



NOTE: THESE PARTS ARE APPROVED FOR USE WITH BOTH 10K & 100K ECL

FIGURE 3.3.2–11
512 BY 8 10K & 100K ECL RPROM

3.3.3 PROM, Word Wide

3.3.3.1 32 AND 64 BY 16 PROM IN DIP AND SCC

CAPACITY--32 AND 64 WORDS OF 16 BITS
FAMILY--TTL

There are two versions of these parts: one in DIP and the other in CC

PACKAGE--24 PIN DIP, 0.300" WIDE
PIN ASSIGNMENTS--Fig. 3.3.3-1
PACKAGE--28 PAD (PIN) SCC, 0.450" X 0.450"
PIN ASSIGNMENTS--Fig. 3.3.3-2

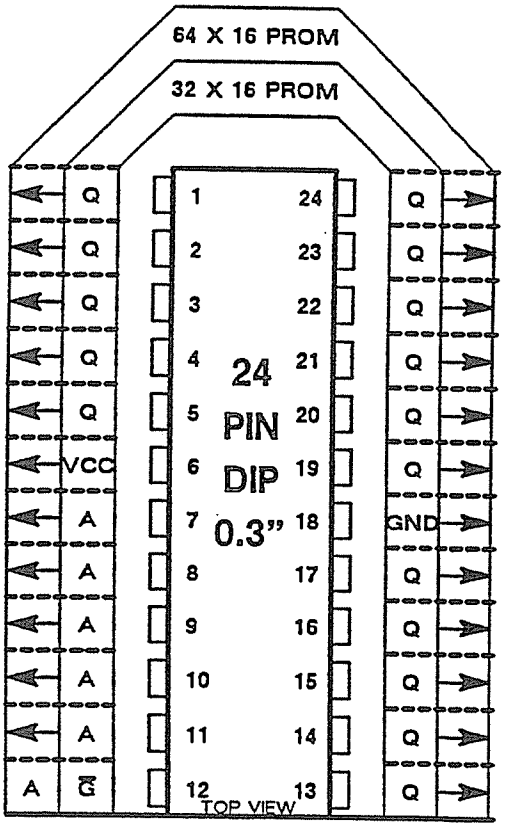


FIGURE 3.3.3-1
32 AND 64 BY 16 TTL PROM IN DIP

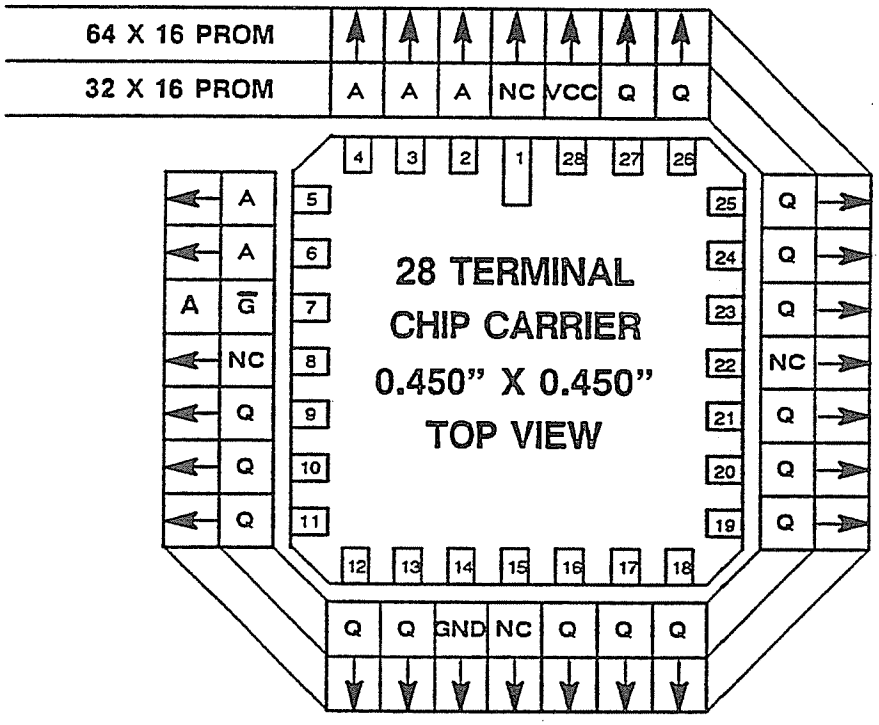


FIGURE 3.3.3-2
32 AND 64 BY 16 TTL PROM IN CC

3.3.4 PROM Package Conversion

3.3.4.1 PROM DIP TO SO CONVERSION, 16, 18, 20, 24 DIP

This standard defines the pin-out conventions for converting a PROM in DIP to an SO package. Conversions are given for four different DIP package sizes.
18 PIN DIP to 20 PIN SO, follow Fig. 3.3.3-3
16 PIN DIP to 16 PIN SO, transfer pins, one to one.
20 PIN DIP to 20 PIN SO, transfer pins, one to one.
24 PIN DIP to 24 PIN SO, transfer pins, one to one.

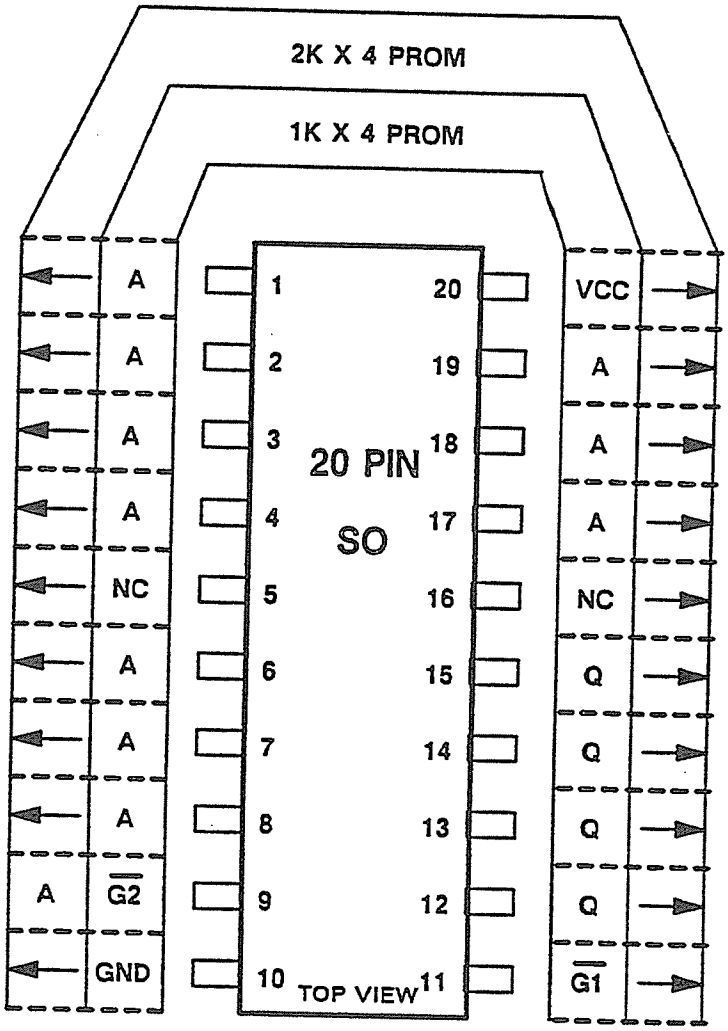


FIGURE 3.3.4-1
1K AND 2K TTL PROM 18 DIP TO 20 SO CONVERSION

3.4 Erasable Programmable Read Only Memory (EPROM)

The following EPROM standards were developed by JC-42.3 Committee and have been implemented using MOS technology.

3.4.1 EPROM, Byte Wide

3.4.1.1 – 4K BY 8 EPROM IN DIP, TYPE A

CAPACITY—4K WORDS OF 8 BITS, TYPE A
PACKAGE—24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.4.1–1

3.4.1.2 – 4K AND 8K BY 8 EPROM IN DIP,

CAPACITY—4K, 8K WORDS OF 8 BITS,
PACKAGE—24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.4.1–1

3.4.1.3 – 8K TO 64K BY 8 EPROM FAMILY IN DIP,

CAPACITY—8K, 16K, 32K, 64K WORDS OF 8 BITS,
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.4.1–2

3.4.1.4 – 2K TO 512K BY 8 EPROM FAMILY IN RCC

CAPACITY—2K, 4K, 8K, 16K, 32K, 64K, 128K, 256K, & 512K WORDS OF 8 BITS
PACKAGE—32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT—Fig. 3.4.1–3

3.4.1.5 – 32K TO 512K BY 8 EPROM FAMILY IN SOJ,

CAPACITY—32K, 64K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—28 OR 32 PIN SOJ, 0.4" WIDE OR NOT DEFINED
PIN ASSIGNMENT—Fig. 3.4.1–4

3.4.1.6 – 128K TO 1M BY 8 EPROM FAMILY IN DIP,

CAPACITY—128K, 256K, 512K, 1M WORDS OF 8 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.4.1–5

3.4.1.7 – 64K TO 512K BY 9 EPROM FAMILY IN DIP,

CAPACITY—64K, 128K, 256K, 512K WORDS OF 9 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.4.1–6

3.4.1.8 – 2 TO 64 X 16K BY 8 PAGE SELECT EPROM FAMILY IN DIP,

CAPACITY—32K, 64K, 128K, 256K, 512K, 1M WORDS OF 8 BITS,
—2, 4, 8, 16, 32, 64 PAGES OF 16K WORDS OF 8 BITS,
LOGIC FEATURES—Selectable pages of 16K words
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.4.1–7

This device contains multiple pages of 16K words which can be selected and the address for which is stored in an internal register.

3.4.1.9 – 128K TO 512K BY 8 EPROM FAMILY IN TSOP–1,

CAPACITY—128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—32 PIN TSOP–1, 8 mm X 20 mm. PP=0.5 mm
PIN ASSIGNMENT—Fig. 3.4.1–8

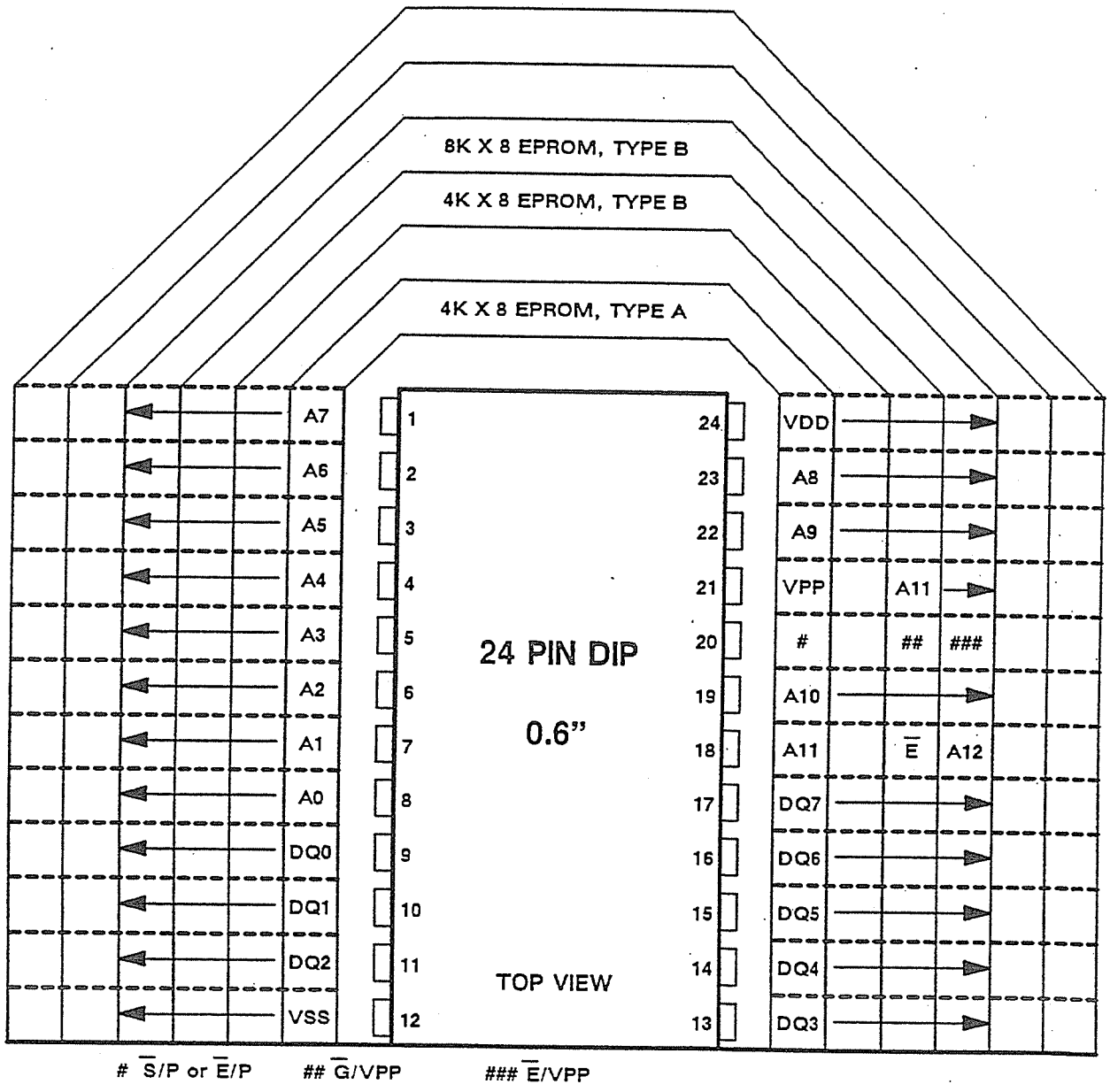


FIGURE 3.4.1-1
4K AND 8K BY 8 EPROM IN DIP, TYPES A & B

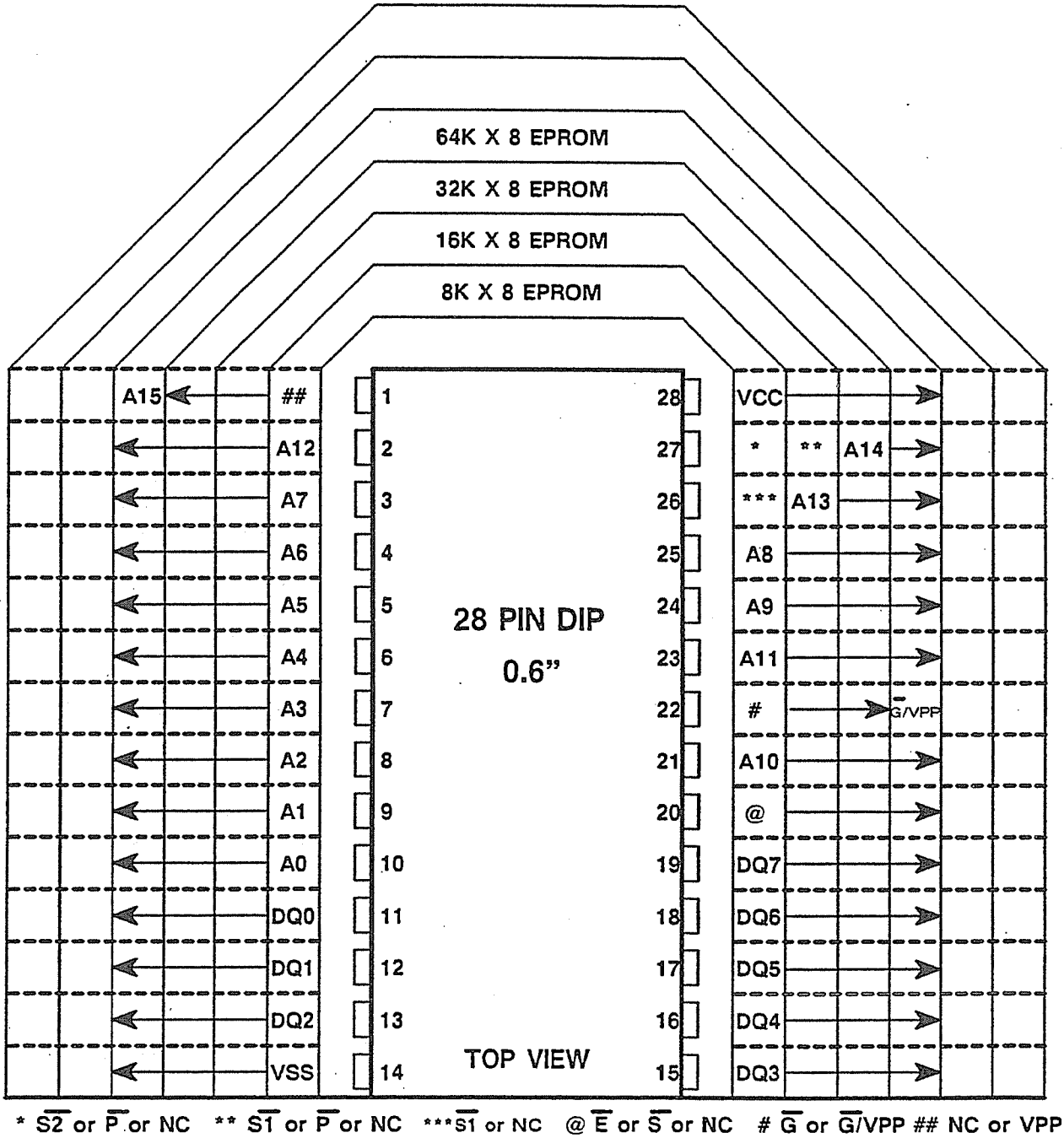


FIGURE 3.4.1-2
8K TO 64K BY 8 EPROM IN DIP

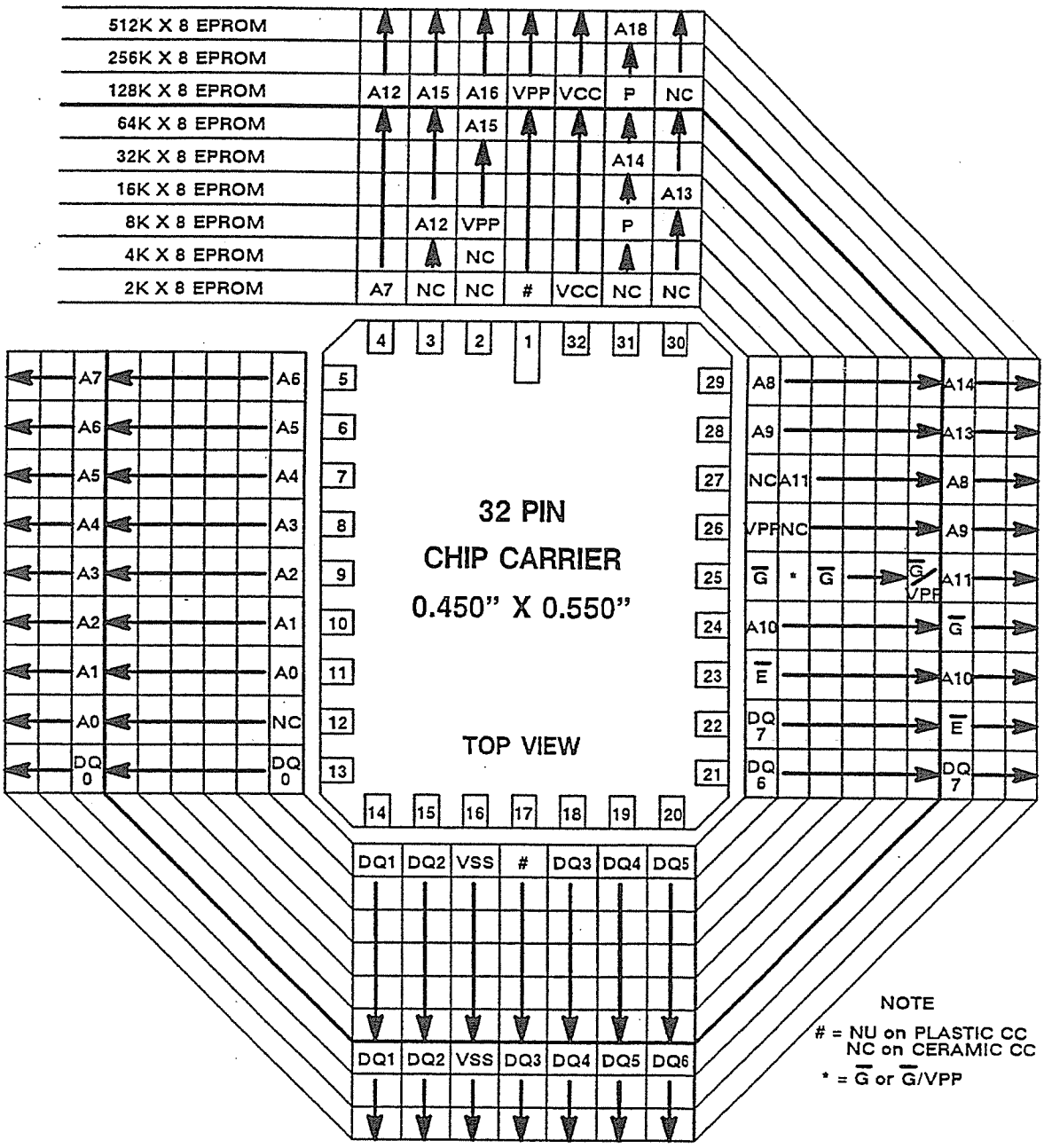


FIGURE 3.4.1-3
2K TO 512K BY 8 EPROM IN CC

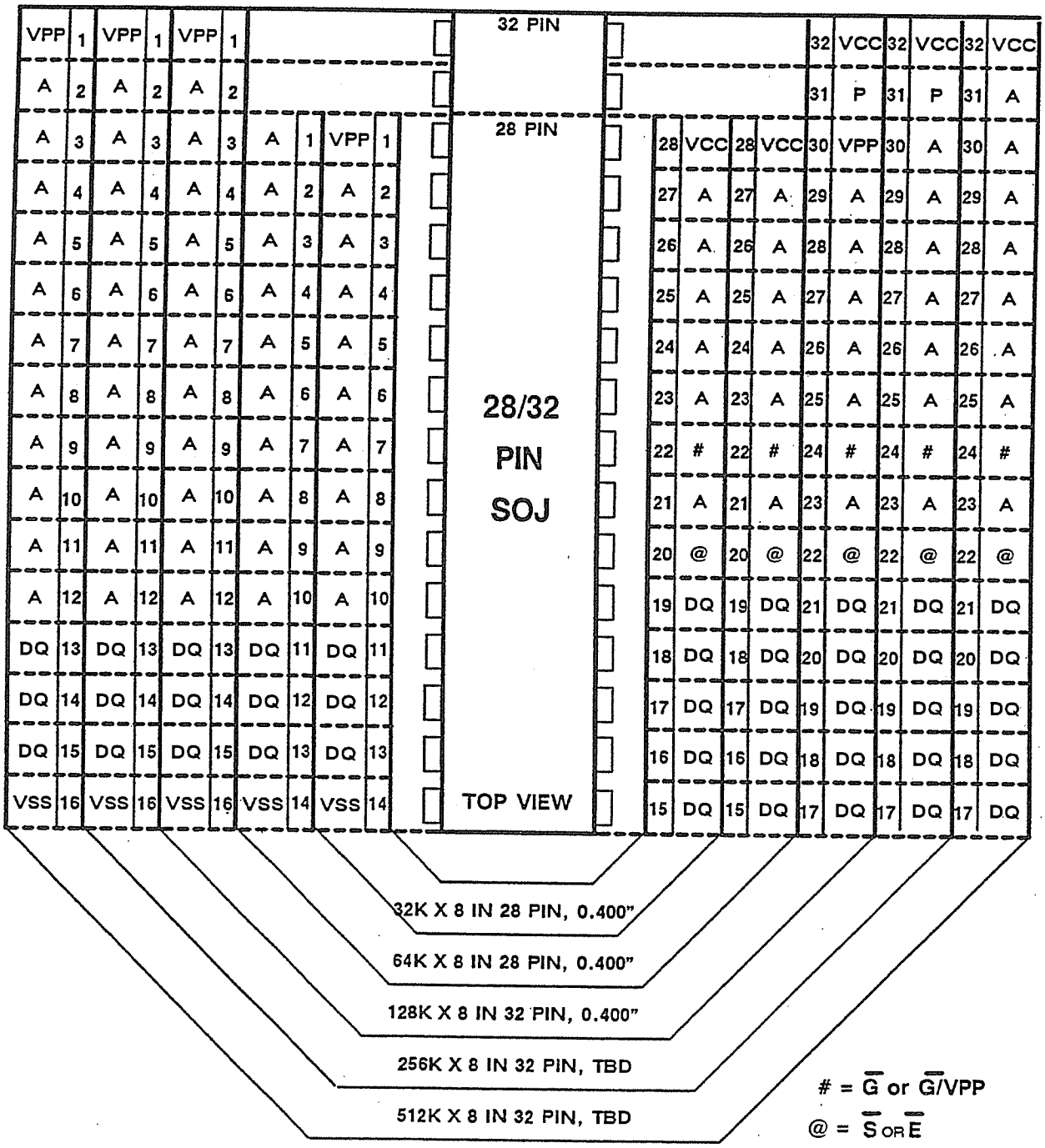


FIGURE 3.4.1-4
32K TO 512K BY 8 EPROM IN SOJ

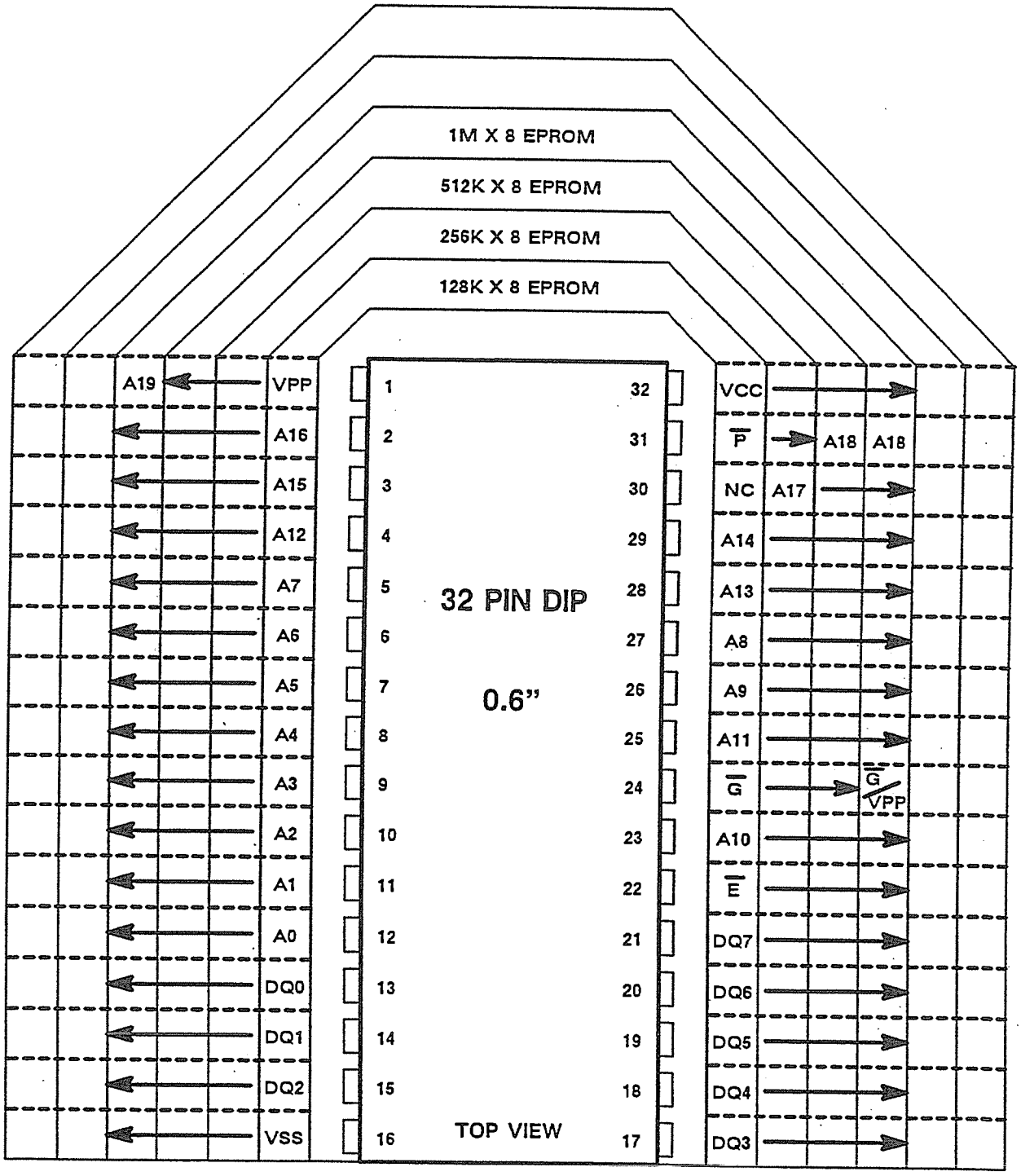


FIGURE 3.4.1-5
128K TO 1M BY 8 EPROM IN DIP

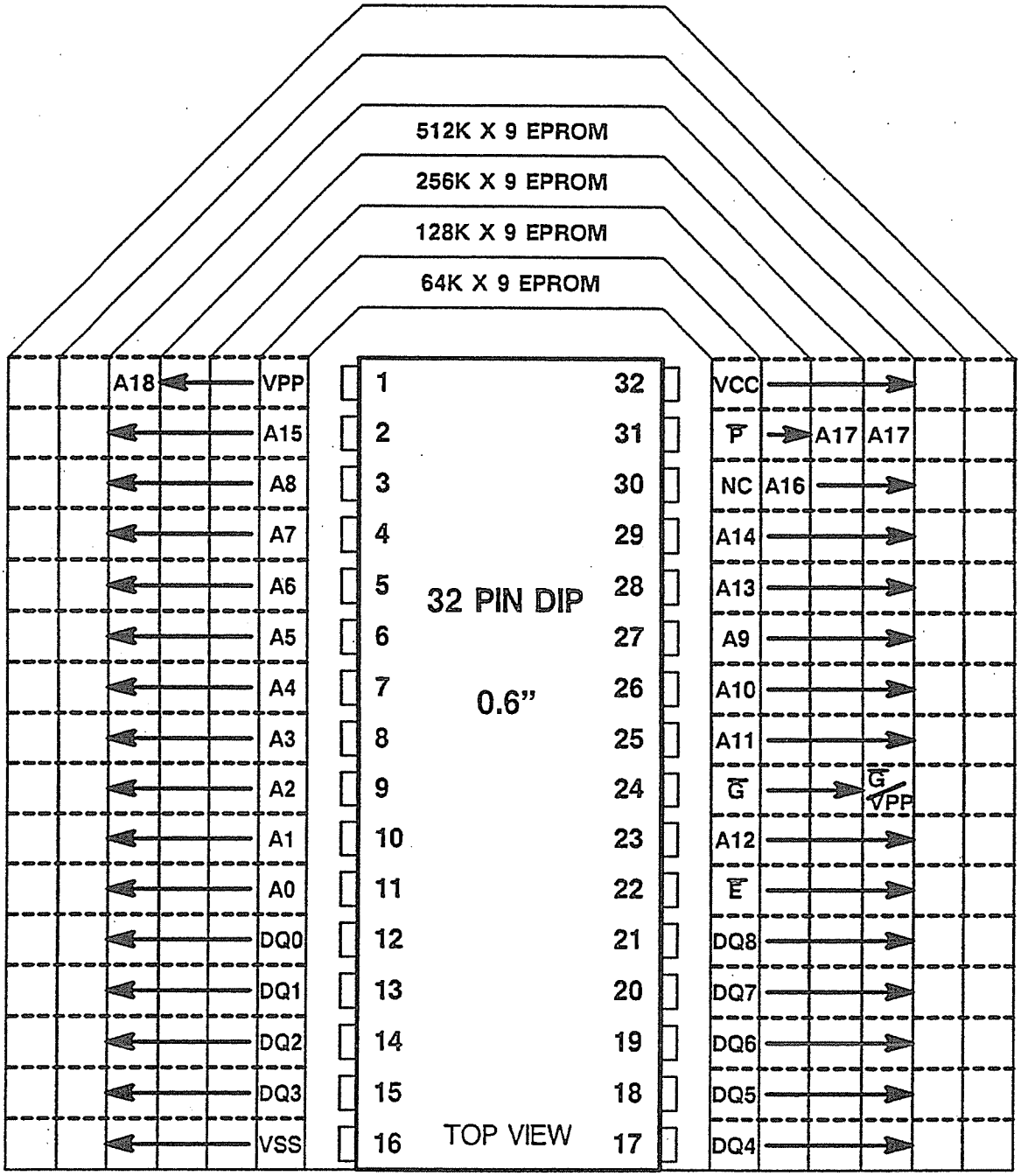
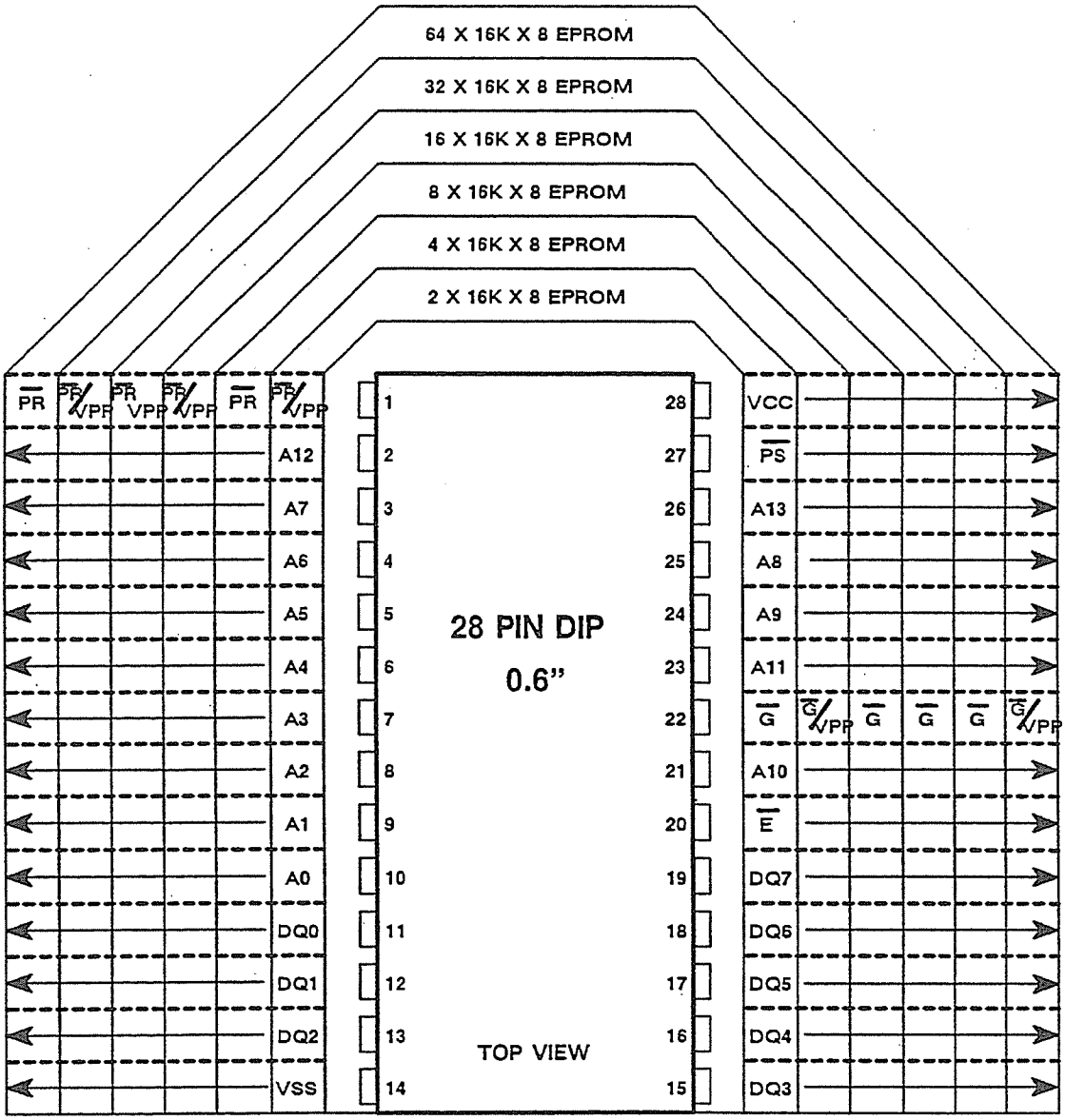


FIGURE 3.4.1-6
64K TO 512K BY 9 EPROM IN DIP



FUNCTION TABLE

MODE \ PIN	$\overline{PS}$	$\overline{PR}$	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
ASYN. RESET (PAGE 0)	H	L	X	X	X	X	X	X
PAGE 0	L	H	L	L	L	L	L	L
PAGE 1	L	H	L	L	L	L	L	H
PAGE 2	L	H	L	L	L	L	H	L
PAGE 3	L	H	L	L	L	L	H	H
PAGE 4	L	H	L	L	L	H	L	L
PAGE 5	L	H	L	L	L	H	L	H
PAGE 6	L	H	L	L	L	H	H	L
PAGE 7	L	H	L	L	L	H	H	H
PAGE n		OUTPUTS = n (BINARY) ACTIVE HIGH						
PAGE 63	L	H	H	H	H	H	H	H

FIGURE 3.4.1-7
2 TO 64 X 16K BY 8 PAGE SELECT EPROM IN DIP

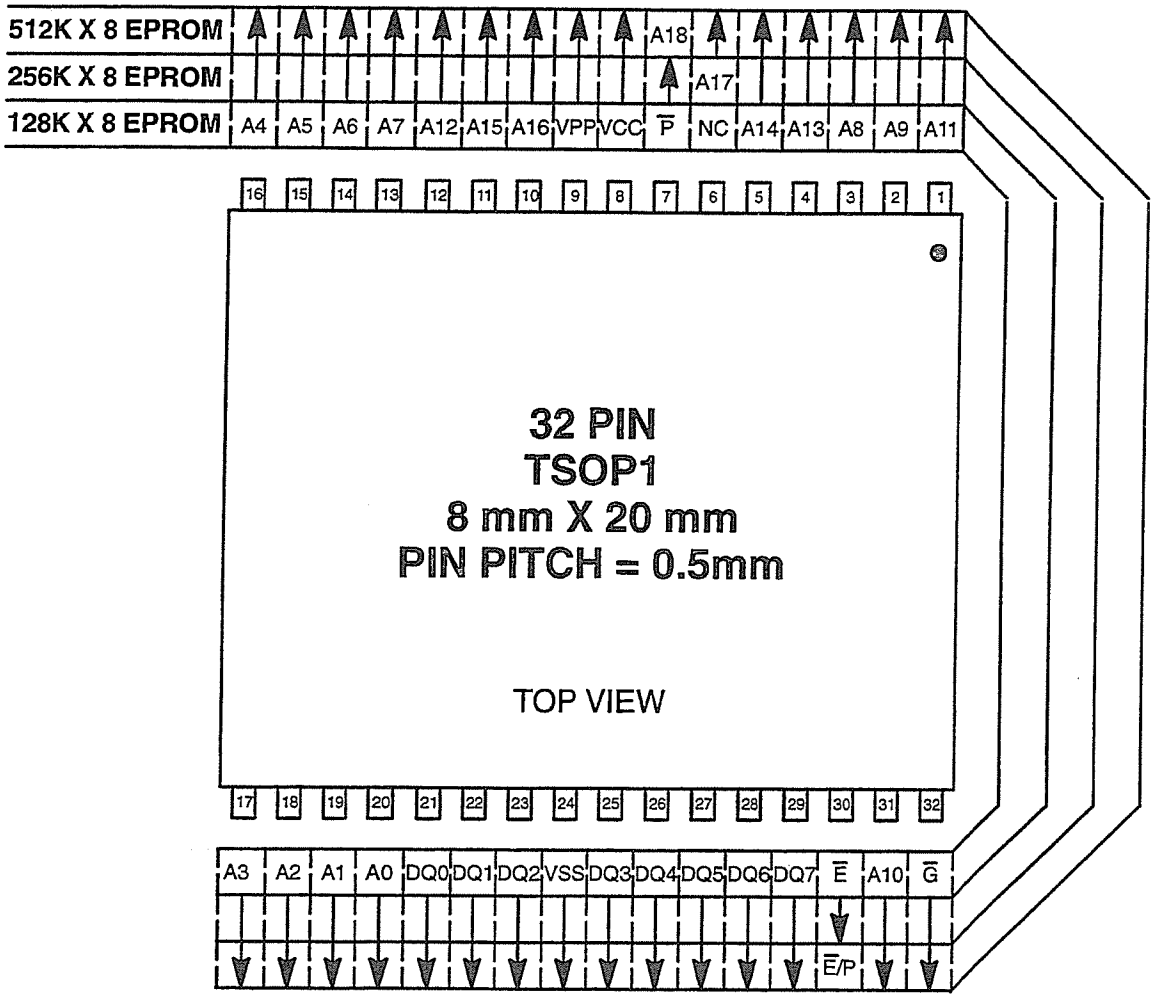


FIGURE 3.4.1–8
128K TO 512K BY 8 EPROM IN TSOP–1

3.4.2 EPROM, Word Wide

3.4.2.1 – 32K TO 256K BY 16 EPROM IN DIP

CAPACITY—32K TO 256K WORDS OF 16 BITS,
PACKAGE—40 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Fig. 3.4.2–1

3.4.2.2 – 32K TO 256K BY 16 EPROM IN SCC

CAPACITY—32K TO 256K WORDS OF 16 BITS,
PACKAGE—44 PAD (PIN) RCC, 0.650" X 0.650"
PIN ASSIGNMENTS—Fig. 3.4.2–2

3.4.2.3 – 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN DIP

CAPACITY—16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES—Address and Data MULTIPLEXED onto common pins.
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Figs. 3.4.2–3

3.4.2.4 – 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN RCC

CAPACITY—16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES—Address and Data MULTIPLEXED onto common pins.
PACKAGE—32 PIN (PAD) RCC, 0.450" X 0.550"
PIN ASSIGNMENTS—Figs. 3.4.2–4

3.4.2.5 – 512K TO 128M BY 16 EPROM IN DIP AND SOP

CAPACITY—512K, 1M, 2M, 4M, 8M, 16M, 32M, 64M, 128M WORDS OF 16 BITS
PACKAGE—42, 44, 48 and 52 PIN DIP or SOP, 0.6" WIDE
PIN ASSIGNMENTS—512K TO 2M, Fig. 3.4.2–8
PIN ASSIGNMENTS—4M TO 128M, Fig. 3.4.2–5

3.4.2.6 – 512K and 1M BY 16 EPROM IN SCC

CAPACITY—512K & 1M WORDS OF 16 BITS
PACKAGE—44TERMINAL SCC, 0.650" X 0.650"
PIN ASSIGNMENTS—Fig. 3.4.2–6

3.4.2.7 – 64K TO 256K BY 16 EPROM IN TSOP–1

CAPACITY—64K, 128K & 256K WORDS OF 16 BITS
PACKAGE—48 PIN TSOP–1 12 mm X 20 mm, PP=0.5 mm
PIN ASSIGNMENTS—Fig. 3.4.2–7

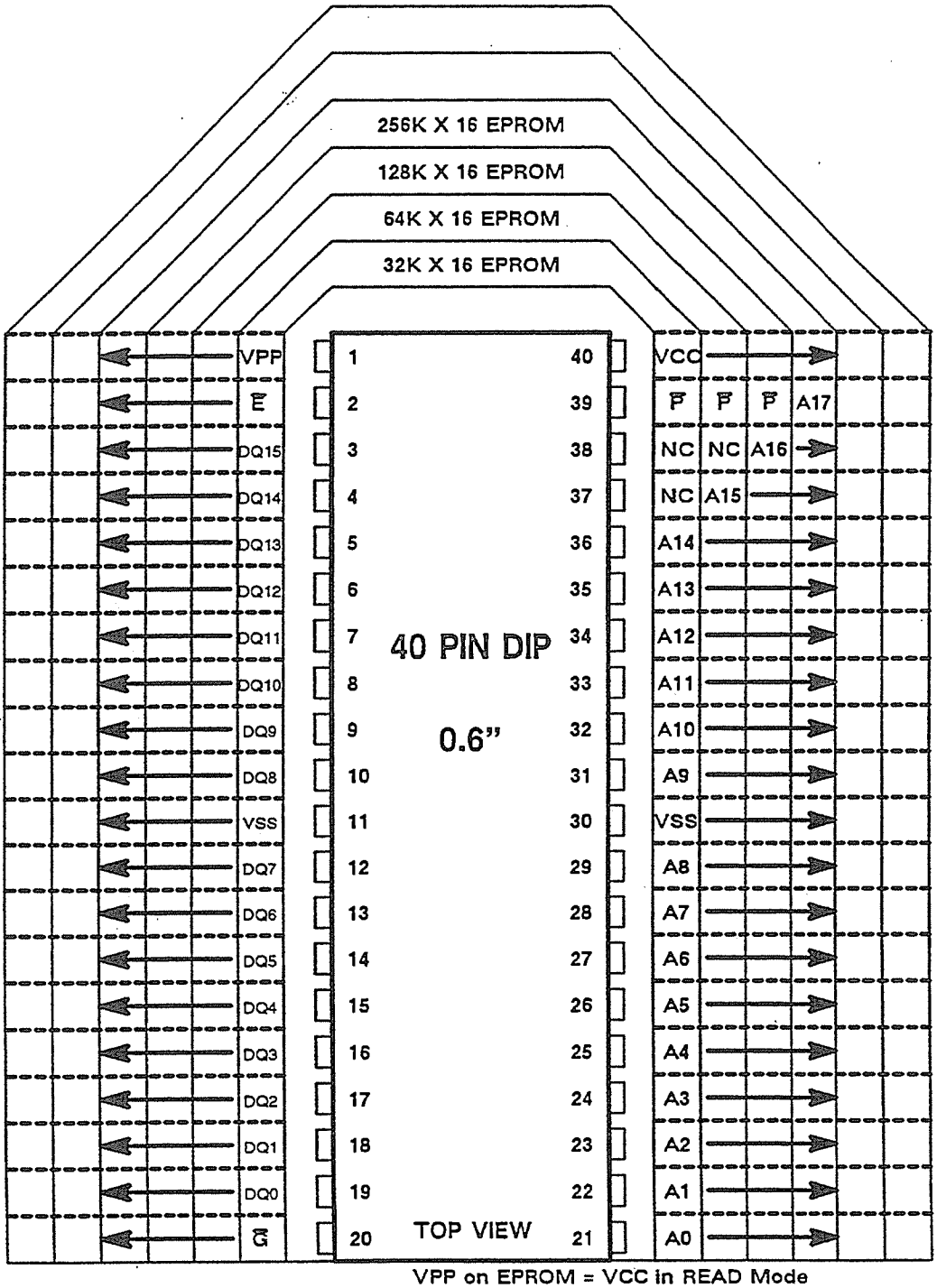


FIGURE 3.4.2-1
32K TO 256K BY 16 EPROM IN DIP

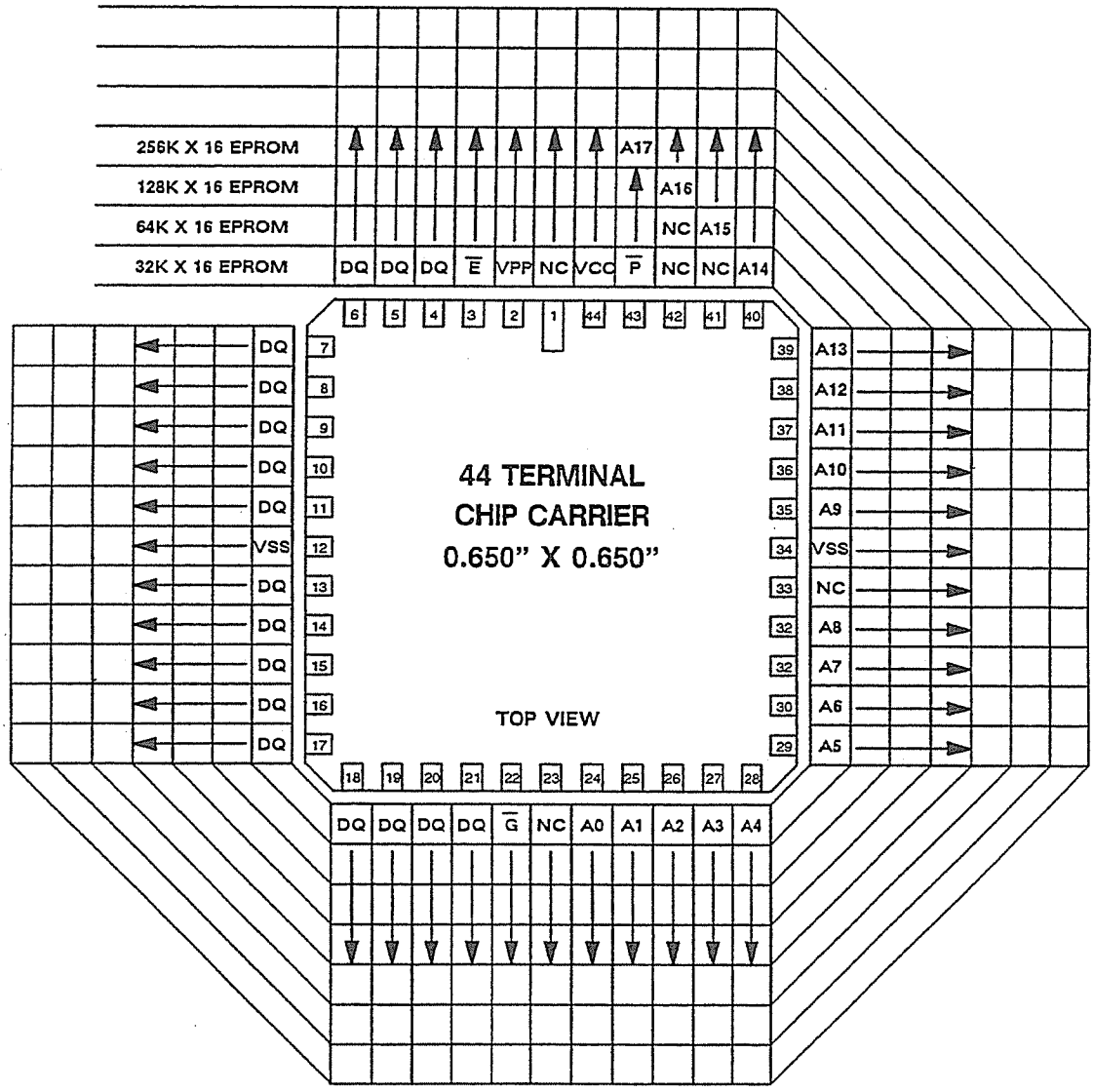
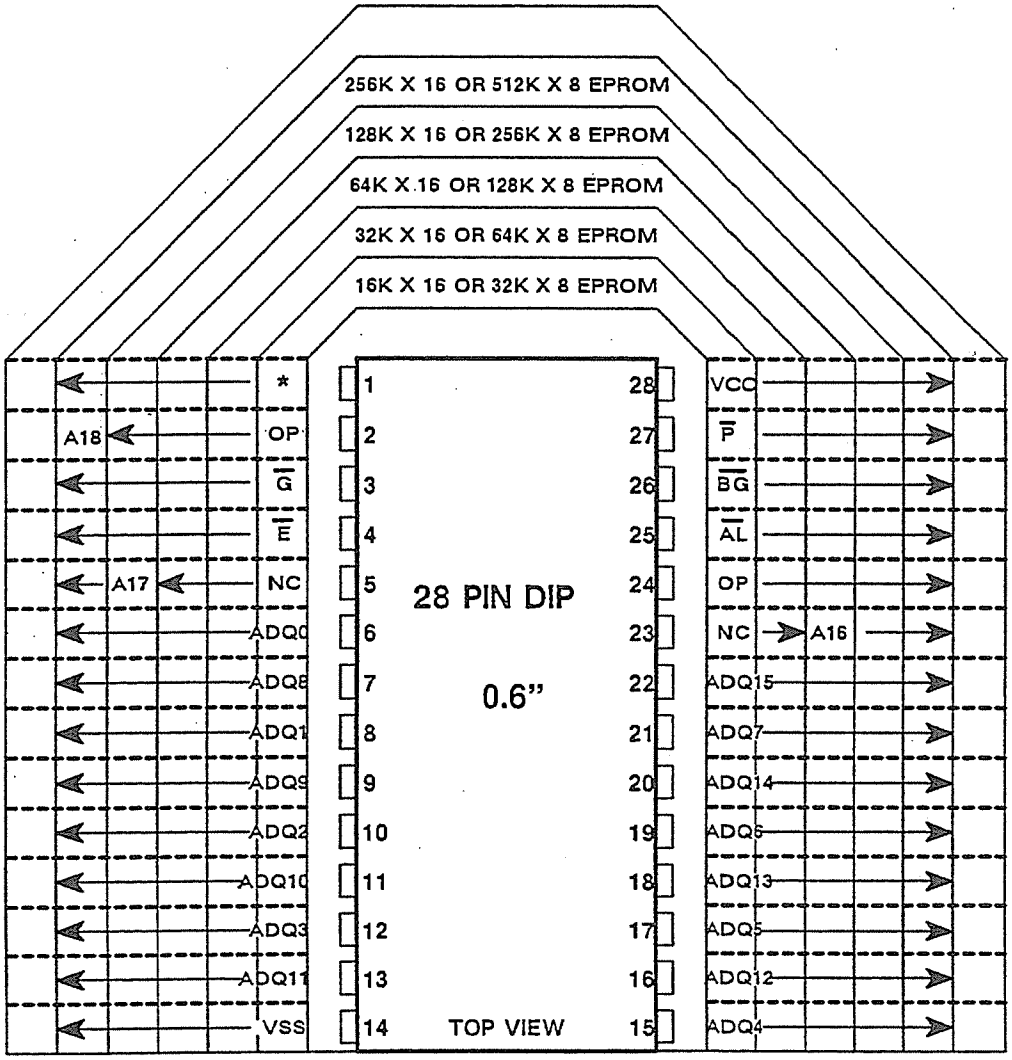


FIGURE 3.4.2-2
32K TO 256K BY 16 EPROM IN SCC

$\overline{BG}$	A0	D0-D7	D8-D15	OPERATION
L	L	LOWER BYTE	UPPER BYTE	WORD
L	H		UPPER BYTE	
H	L	LOWER BYTE		BYTE
H	H	UPPER BYTE		BYTE



* NC or VSS

FIGURE 3.4.2-3
16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN DIP

$\overline{BG}$	A0	D0–D7	D8–D15	OPERATION
L	L	LOWER BYTE	UPPER BYTE	WORD
L	H		UPPER BYTE	
H	L	LOWER BYTE		BYTE
H	H	UPPER BYTE		BYTE

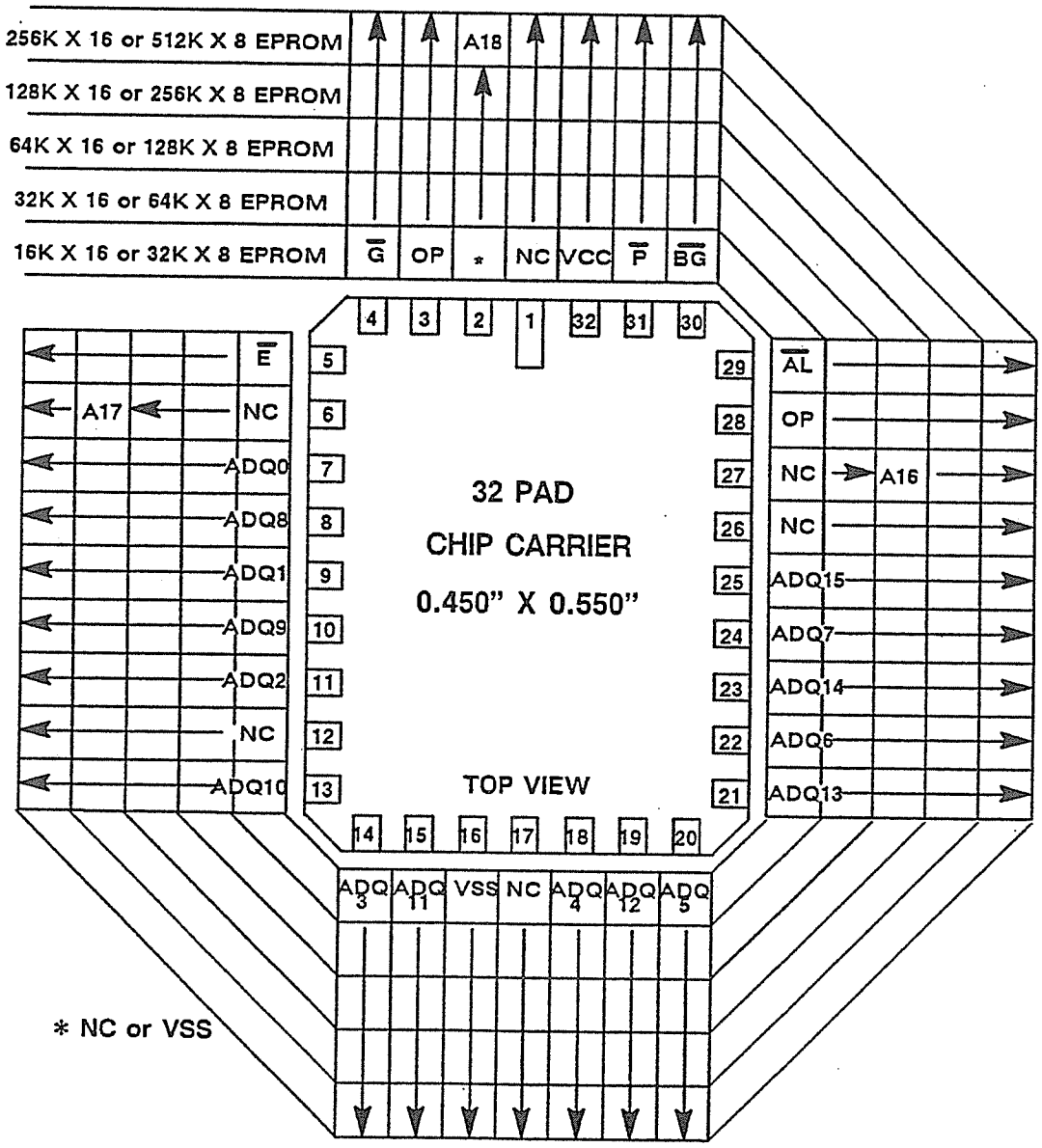
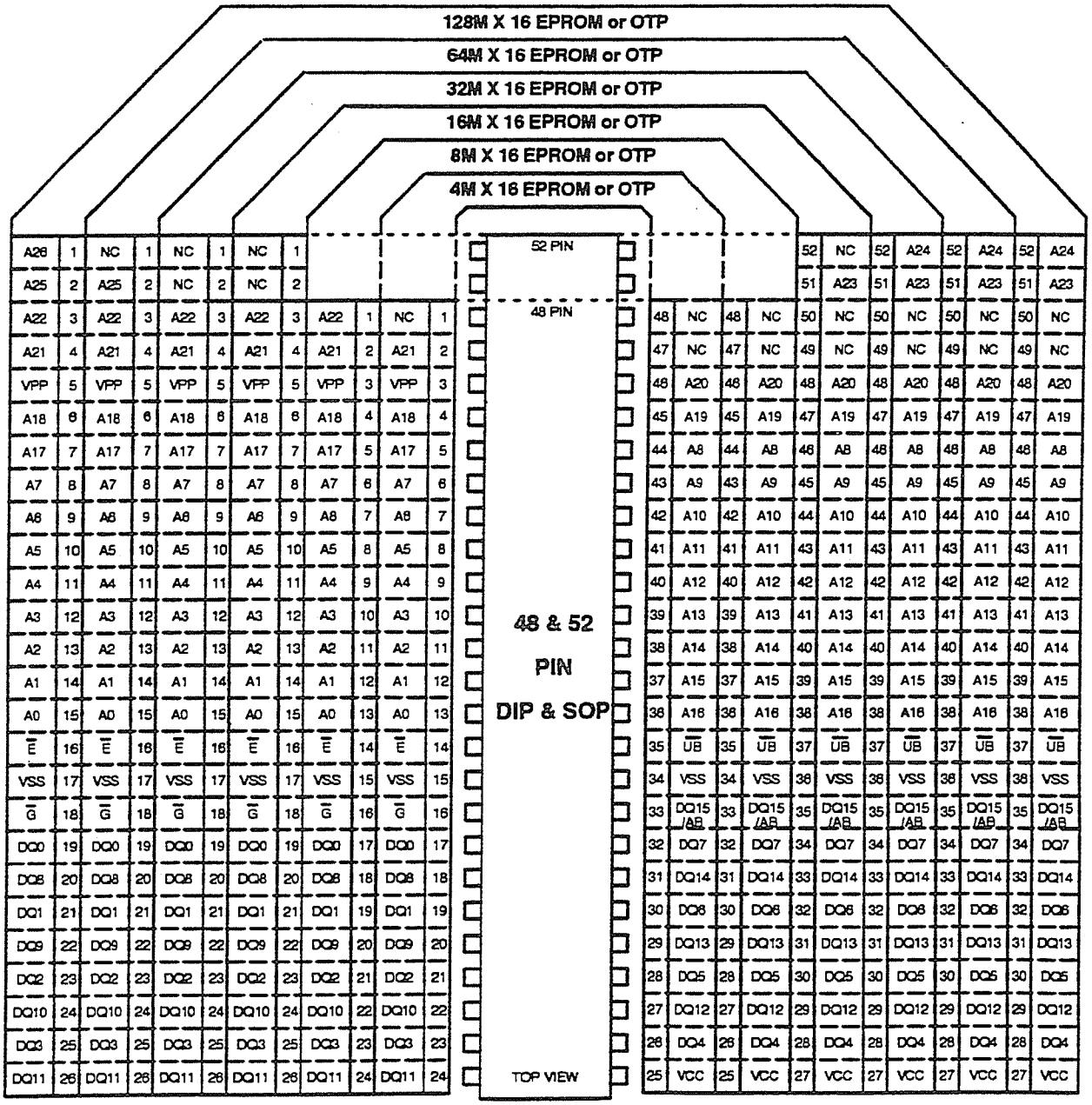
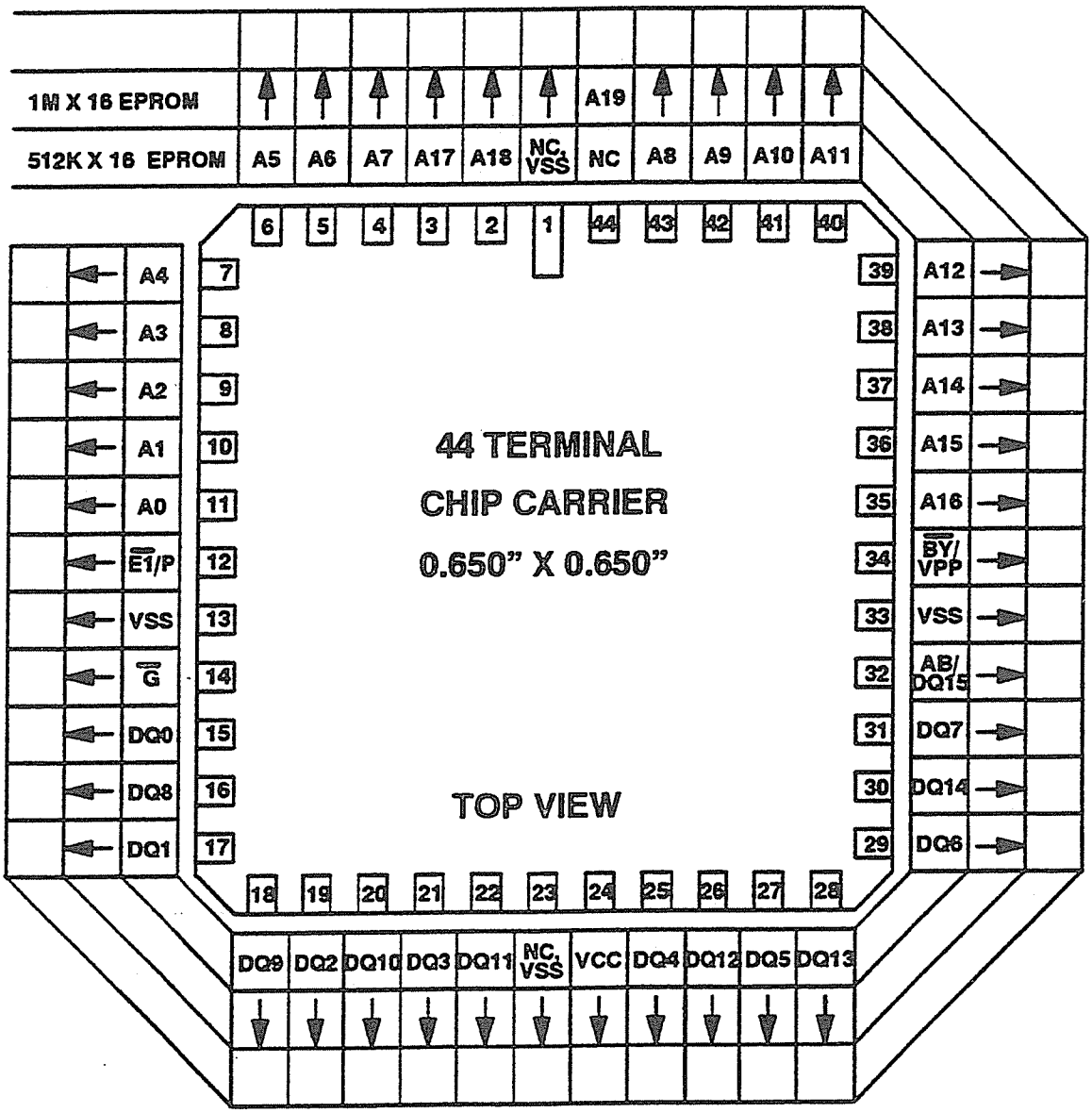


FIGURE 3.4.2-4
16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN RCC



A26	1	NC	1	NC	1	NC	1															52	NC	52	A24	52	A24	52	A24
A25	2	A25	2	NC	2	NC	2															51	A23	51	A23	51	A23	51	A23
A22	3	A22	3	A22	3	A22	3	A22	1	NC	1									48	NC	48	NC	50	NC	50	NC	50	NC	50	NC
A21	4	A21	4	A21	4	A21	4	A21	2	A21	2									47	NC	47	NC	49	NC	49	NC	49	NC	49	NC
VPP	5	VPP	5	VPP	5	VPP	5	VPP	3	VPP	3									46	A20	46	A20	48	A20	48	A20	48	A20	48	A20
A18	6	A18	6	A18	6	A18	6	A18	4	A18	4									45	A19	45	A19	47	A19	47	A19	47	A19	47	A19
A17	7	A17	7	A17	7	A17	7	A17	5	A17	5									44	A8	44	A8	46	A8	46	A8	48	A8	48	A8
A7	8	A7	8	A7	8	A7	8	A7	6	A7	6									43	A9	43	A9	45	A9	45	A9	45	A9	45	A9
A6	9	A6	9	A6	9	A6	9	A6	7	A6	7									42	A10	42	A10	44	A10	44	A10	44	A10	44	A10
A5	10	A5	10	A5	10	A5	10	A5	8	A5	8									41	A11	41	A11	43	A11	43	A11	43	A11	43	A11
A4	11	A4	11	A4	11	A4	11	A4	9	A4	9									40	A12	40	A12	42	A12	42	A12	42	A12	42	A12
A3	12	A3	12	A3	12	A3	12	A3	10	A3	10									39	A13	39	A13	41	A13	41	A13	41	A13	41	A13
A2	13	A2	13	A2	13	A2	13	A2	11	A2	11									38	A14	38	A14	40	A14	40	A14	40	A14	40	A14
A1	14	A1	14	A1	14	A1	14	A1	12	A1	12									37	A15	37	A15	39	A15	39	A15	39	A15	39	A15
A0	15	A0	15	A0	15	A0	15	A0	13	A0	13									36	A16	36	A16	38	A16	38	A16	38	A16	38	A16
$\overline{E}$	16	$\overline{E}$	16	$\overline{E}$	16	$\overline{E}$	16	$\overline{E}$	14	$\overline{E}$	14									35	$\overline{UB}$	35	$\overline{UB}$	37	$\overline{UB}$	37	$\overline{UB}$	37	$\overline{UB}$	37	$\overline{UB}$
VSS	17	VSS	17	VSS	17	VSS	17	VSS	15	VSS	15									34	VSS	34	VSS	36	VSS	36	VSS	36	VSS	36	VSS
$\overline{G}$	18	$\overline{G}$	18	$\overline{G}$	18	$\overline{G}$	18	$\overline{G}$	16	$\overline{G}$	16									33	DQ15 /AP	33	DQ15 /AP	35	DQ15 /AP	35	DQ15 /AP	35	DQ15 /AP	35	DQ15 /AP
DQ0	19	DQ0	19	DQ0	19	DQ0	19	DQ0	17	DQ0	17									32	DQ7	32	DQ7	34	DQ7	34	DQ7	34	DQ7	34	DQ7
DQ8	20	DQ8	20	DQ8	20	DQ8	20	DQ8	18	DQ8	18									31	DQ14	31	DQ14	33	DQ14	33	DQ14	33	DQ14	33	DQ14
DQ1	21	DQ1	21	DQ1	21	DQ1	21	DQ1	19	DQ1	19									30	DQ6	30	DQ6	32	DQ6	32	DQ6	32	DQ6	32	DQ6
DQ9	22	DQ9	22	DQ9	22	DQ9	22	DQ9	20	DQ9	20									29	DQ13	29	DQ13	31	DQ13	31	DQ13	31	DQ13	31	DQ13
DQ2	23	DQ2	23	DQ2	23	DQ2	23	DQ2	21	DQ2	21									28	DQ5	28	DQ5	30	DQ5	30	DQ5	30	DQ5	30	DQ5
DQ10	24	DQ10	24	DQ10	24	DQ10	24	DQ10	22	DQ10	22									27	DQ12	27	DQ12	29	DQ12	29	DQ12	29	DQ12	29	DQ12
DQ3	25	DQ3	25	DQ3	25	DQ3	25	DQ3	23	DQ3	23									26	DQ4	26	DQ4	28	DQ4	28	DQ4	28	DQ4	28	DQ4
DQ11	26	DQ11	26	DQ11	26	DQ11	26	DQ11	24	DQ11	24									25	VCC	25	VCC	27	VCC	27	VCC	27	VCC	27	VCC

FIGURE 3.4.2–5
4M TO 128M BY 16 EPROM & OTP IN DIP AND SOP



The device is x8/x16 programmable via BY (pin 34)
X8 configuration when BY = VIL
X16 configuration when BY = VIH
AB is the least significant address bit for X8 operation

FIGURE 3.4.2–6

512K & 1M BY 16 EPROM FAMILY IN CC

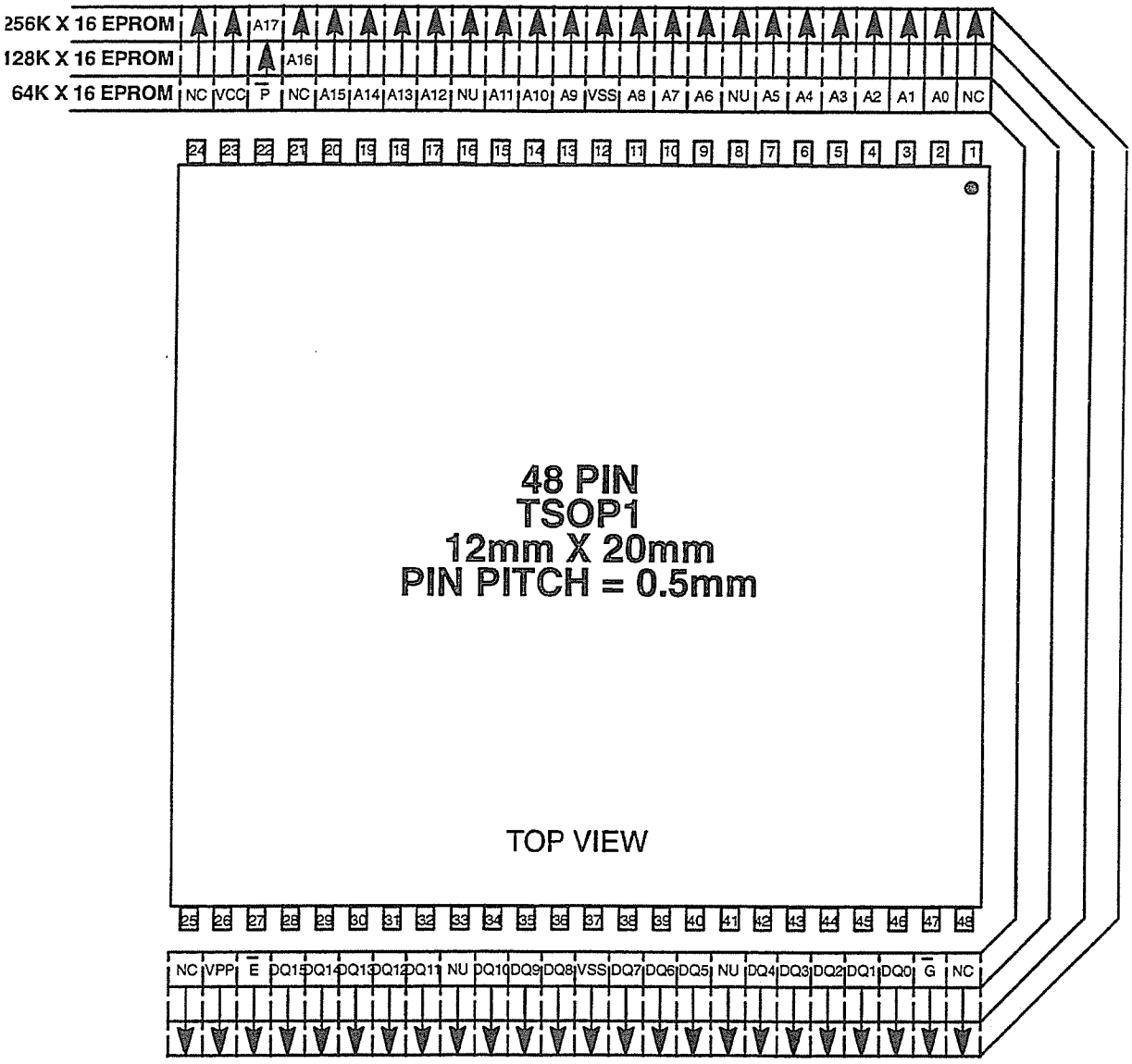
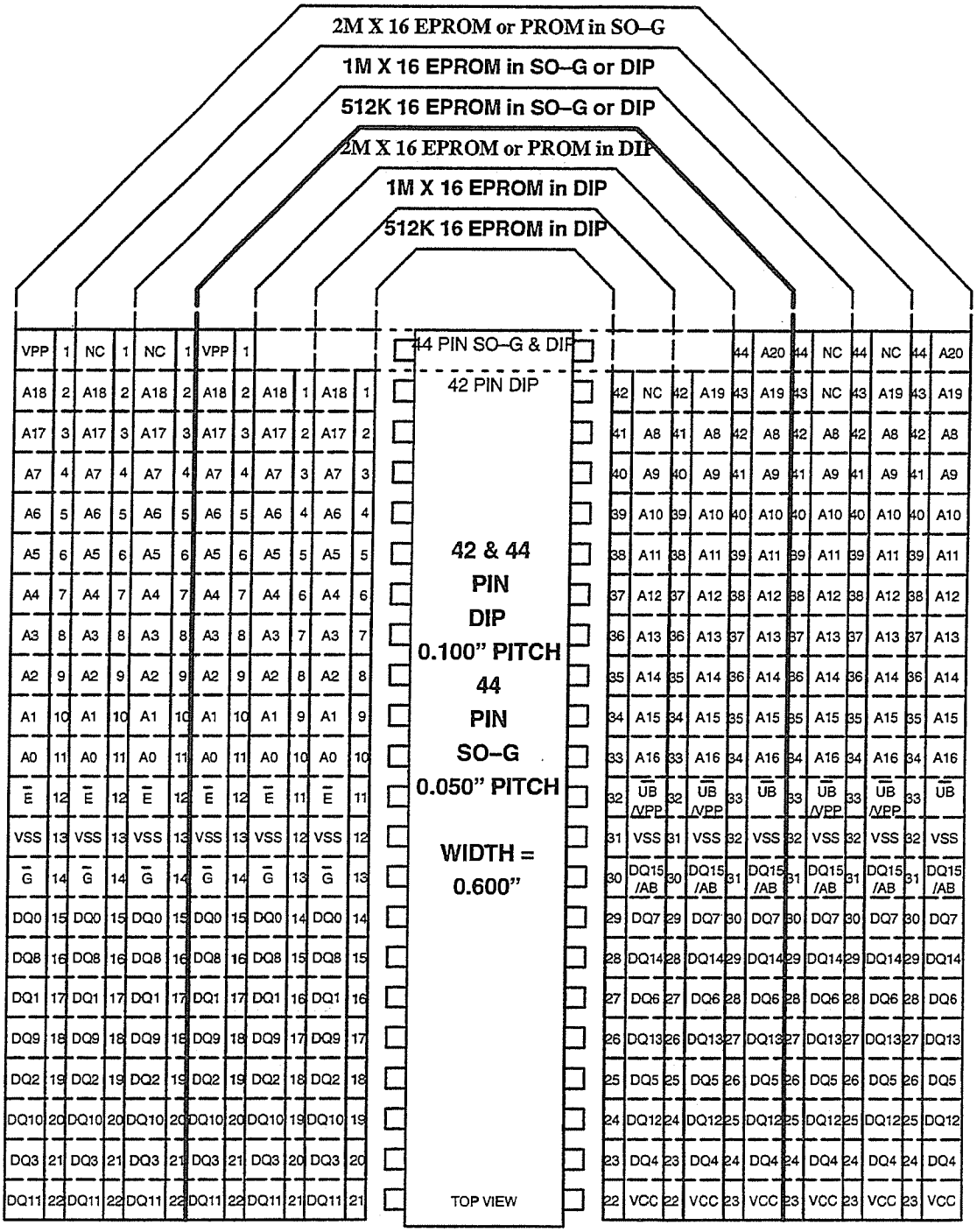


FIGURE 3.4.2–7

64K BY 256K BY 16 EPROM IN TSOP–1



AB: ADDRESS INPUT, UPPER/
LOWER BYTE SELECT
BT: BYTE MODE ENABLE

FIGURE 3.4.2–8
512K TO 2M BY 16 EPROM IN DIP AND SO–G

3.5 Electrically Erasable Programmable Read Only Memory (EEPROM)

The following EEPROM standards were developed by the MOS Committee and have been implemented using MOS technology.

3.5.1 EEPROM, Byte Wide

3.5.1.1 – .5K TO 2K BY 8 EEPROM FAMILY IN DIP

CAPACITY—.5K, 1K, 2K WORDS OF 8 BITS
PACKAGE—24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.5.1–1

3.5.1.2 – 2K & 4K BY 8 EEPROM IN RCC

CAPACITY—2K, 4K WORDS OF 8 BITS
PACKAGE—32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT—Fig. 3.5.1–2
These devices are CC equivalents of 24 pin DIP devices

3.5.1.3 – 1K TO 32K BY 8 EEPROM FAMILY IN DIP

CAPACITY—1K, 2K, 4K, 8K, 16K, 32K WORDS OF 8 BITS
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.5.1–3

3.5.1.4 – .5K TO 32K BY 8 EEPROM FAMILY IN RCC

CAPACITY—.5K, 1K, 2K, 4K, 8K, 16K, 32K WORDS OF 8 BITS
PACKAGE—32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT—Fig. 3.5.1–4

3.5.1.5 – 32K TO 256K BY 8 EEPROM FAMILY IN SOJ,

CAPACITY—32K, 128K, 256K WORDS OF 8 BITS,
PACKAGE—28 OR 32 PIN SOJ, 0.4" WIDE OR NOT DEFINED
PIN ASSIGNMENT—Fig. 3.5.1–5

3.5.1.6 – 32K TO 512K BY 8 EEPROM FAMILY IN DIP,

CAPACITY—32K, 64K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.5.1–6

3.5.1.7 – 32K TO 256K BY 8 EEPROM FAMILY IN RCC,

CAPACITY—32K, 64K, 128K, 256K WORDS OF 8 BITS,
PACKAGE—32 PIN RCC, 0.450" X 0.550"
PIN ASSIGNMENT—Fig. 3.5.1–7

3.5.1.8 – 32K TO 256K BY 9 EEPROM FAMILY IN DIP,

CAPACITY—32K, 64K, 128K, 256K WORDS OF 9 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.5.1–8

3.5.1.9 – 128K TO 1M BY 8 EEPROM FAMILY IN SCC,

CAPACITY—128K, 256K, 512K, & 1M WORDS OF 8 BITS,
PACKAGE—44 PIN SCC, 0.650" x 0.650"
PIN ASSIGNMENT—Fig. 3.5.1–9

3.5.1.10 – 32K TO 256K BY 8 EEPROM FAMILY IN TSOP1

CAPACITY--32K, 64K, 128K, & 256K WORDS OF 8 BITS,
PACKAGE--32 LEAD TSOP-1, 8 mm X 18.4 mm
PIN ASSIGNMENT--Fig. 3.5.1-10

3.5.1.11 – EXTENDED FEATURE SET FOR 256K BIT EEPROM

This standard specifies features beyond the existing pinout standards that need to be standardized for 32KX8 EEPROMs to achieve operational compatibility. A summary of the required and optional features is listed below. The full standard follows the pinout drawings at the end of Sec. 3.5.1..

3.5.1.11.1 – REQUIRED STANDARD FEATURES

The following features are the minimum set necessary to achieve functional compatibility for 32K Byte EEPROMs and must be implemented to be in compliance with this standard:
-Operate with a primary power supply of 5.0 V nominal
-Operate in conformance with the standard truth table
-Have read and write timing cycles which are consistent with the standard timing diagrams
-Contain Data & Address Latches for Write cycles
-Operate with self timed write cycles
-Operate with input levels between 0 and 5 Volts.

3.5.1.11.2 – OPTIONAL FEATURES

The following features are optional and are not required for the part to conform to this standard. If any of these features are implemented, they must operate as defined in order to maintain compatibility and to be in compliance with this standard:
-Page Write Mode with standard write cycle timings
-Minimum page size of 16 Byte in page write mode
-DATA\ Polling
-Software Data Protect Option
-Hardware Mass Erase (All 1's)
-Software Mass Erase (All 1's)

3.5.1.12 – OPTIONAL COMMAND SET FOR DUAL-SUPPLY EEPROM

This Standard provides an optional command set for DUAL-SUPPLY EEPROM devices (commonly known as FLASH EEPROM). This set includes the existing algorithmic commands and adds a series of automatic codes. A component may respond to either or both of the operating modes. The COMMAND SET TRUTH TABLE is shown in Figure 3.5.2-4

3.5.1.13 – 512K BY 8 DUAL-SUPPLY EEPROM IN RCC

CAPACITY--512K WORDS OF 8 BITS,
PACKAGE--32 LEAD RCC, 11.43 mm X 13.97 mm (0.450" X 0.550")
PIN ASSIGNMENT--Fig. 3.5.1-12

3.5.1.14 – 128K TO 512K BY 8 SINGLE-SUPPLY EEPROM FAMILY IN DIP, RCC, & TSOP-1

CAPACITY--32K, 64K, 128K, & 256K WORDS OF 8 BITS,
THESE DEVICES ARE APPROVED IN THREE PACKAGES:
DIP PACKAGE--32 LEAD DIP, 15.24 mm (0.6") WIDE WITH 2.54 mm (0.1") PP
PIN ASSIGNMENT--Fig. 3.5.1-13
RCC PACKAGE--32 LEAD RCC, 11.43 mm X 13.97 mm (0.450" X 0.550")
PIN ASSIGNMENT--Fig. 3.5.1-14
TSOP-1 PACKAGE--32 LEAD TSOP-1, 8 mm X 20 mm WITH 0.5 mm PP
PIN ASSIGNMENT--Fig. 3.5.1-15

3.5.1.15 – 256K, 512K, & 1M BY 8 DUAL–SUPPLY EEPROM IN TSOP–1

CAPACITY—256K, 512K, 1M WORDS OF 8 BITS,
PACKAGE—40 LEAD TSOP–1, 10 mm X 20 mm WITH 0.5 mm PP
PIN ASSIGNMENT—256K, 512K, Fig. 3.5.1–18
PIN ASSIGNMENT—1M, Fig. 3.5.1–16

The 256K & 512K devices have a different pin assignment pattern from the 1M device, therefor are not backward compatible with the 1M device.

3.5.1.16 – 1M TO 8M BY 8 SINGLE–SUPPLY EEPROM FAMILY IN TSOP–1

CAPACITY—1M, 2M, 4M, & 8M WORDS OF 8 BITS,
PACKAGE—48 LEAD TSOP1, 12 mm X 20 mm WITH 0.5 mm PP
PIN ASSIGNMENT—Fig. 3.5.1–17

3.5.1.17 – 8K BY 256B OR 264B SERIAL ACCESS EEPROM IN TSOP–2

CAPACITY—8K WORDS OF 256 OR 264 BYTES, SERIALLY ACCESSED
PACKAGE—44/40 LEAD TSOP2, 10.16 mm WIDE WITH 0.8 mm PP
PIN ASSIGNMENT—Fig. 3.5.1–19 A
CONTROL & LOGIC TABLES—Figs. 3.5.1–19 B & C

3.5.1.18 – 1M & 2M BY 8 SINGLE OR DUAL SUPPLY EEPROM FAMILY IN PSOP

CAPACITY—1M & 2M WORDS OF 8 BITS,
PACKAGE—44 LEAD PSOP 16 mm wide WITH 1.27 mm PP
PIN ASSIGNMENT—Fig. 3.5.1–20

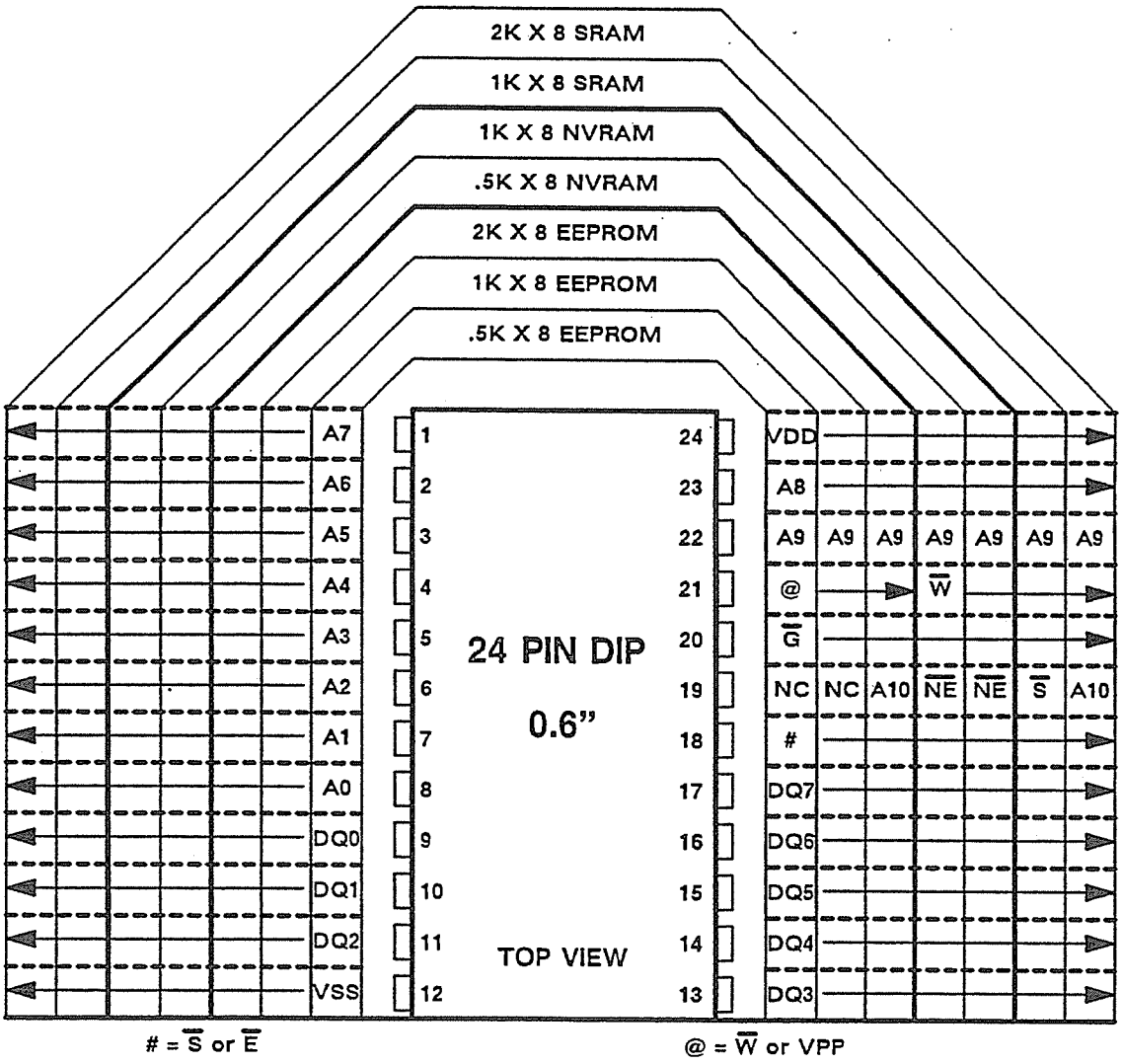


FIGURE 3.5.1-1
.5K TO 2K BY 8 EEPROM IN DIP

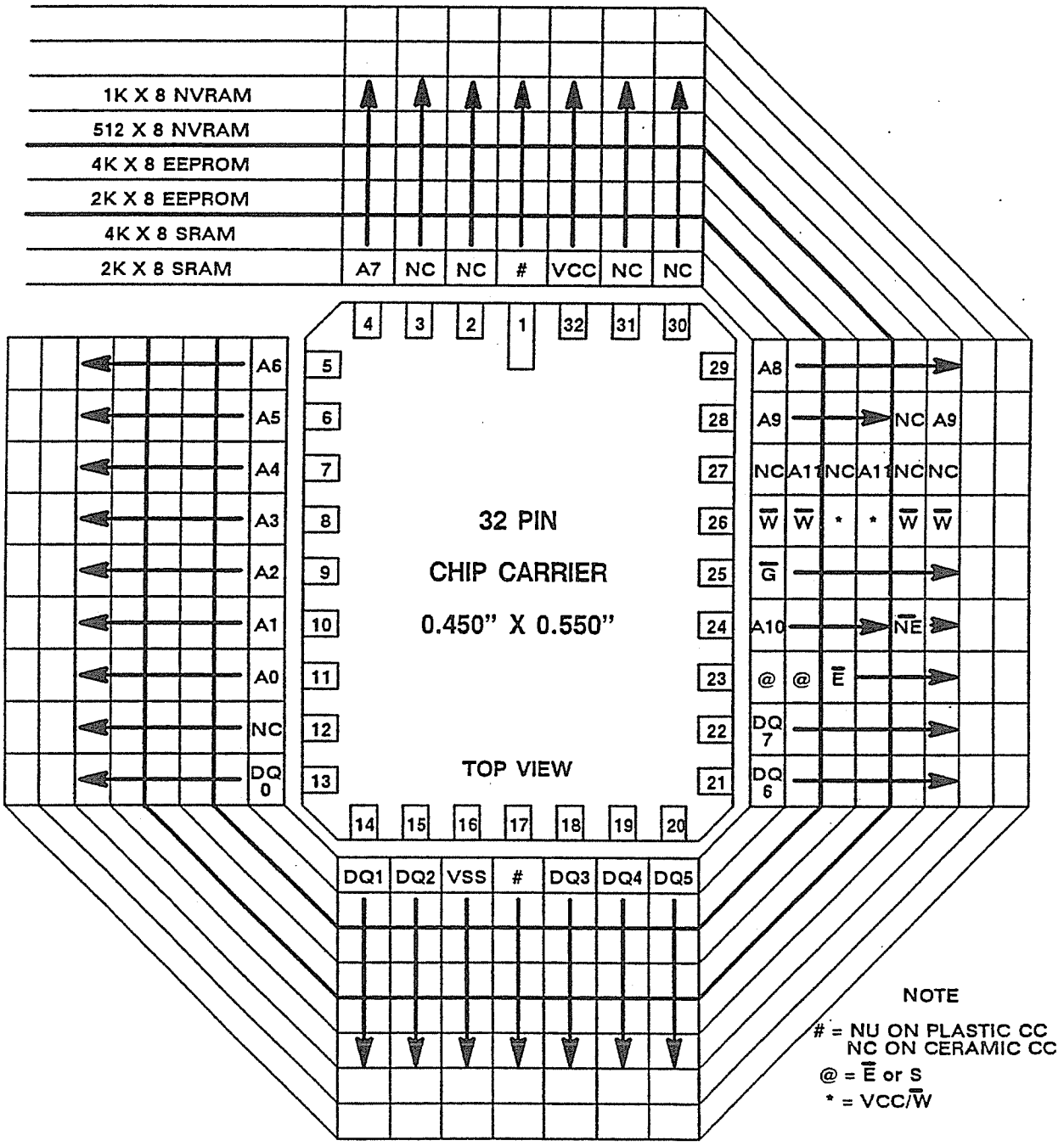


FIGURE 3.5.1-2
2K & 4K BY 8 EEPROM IN RCC

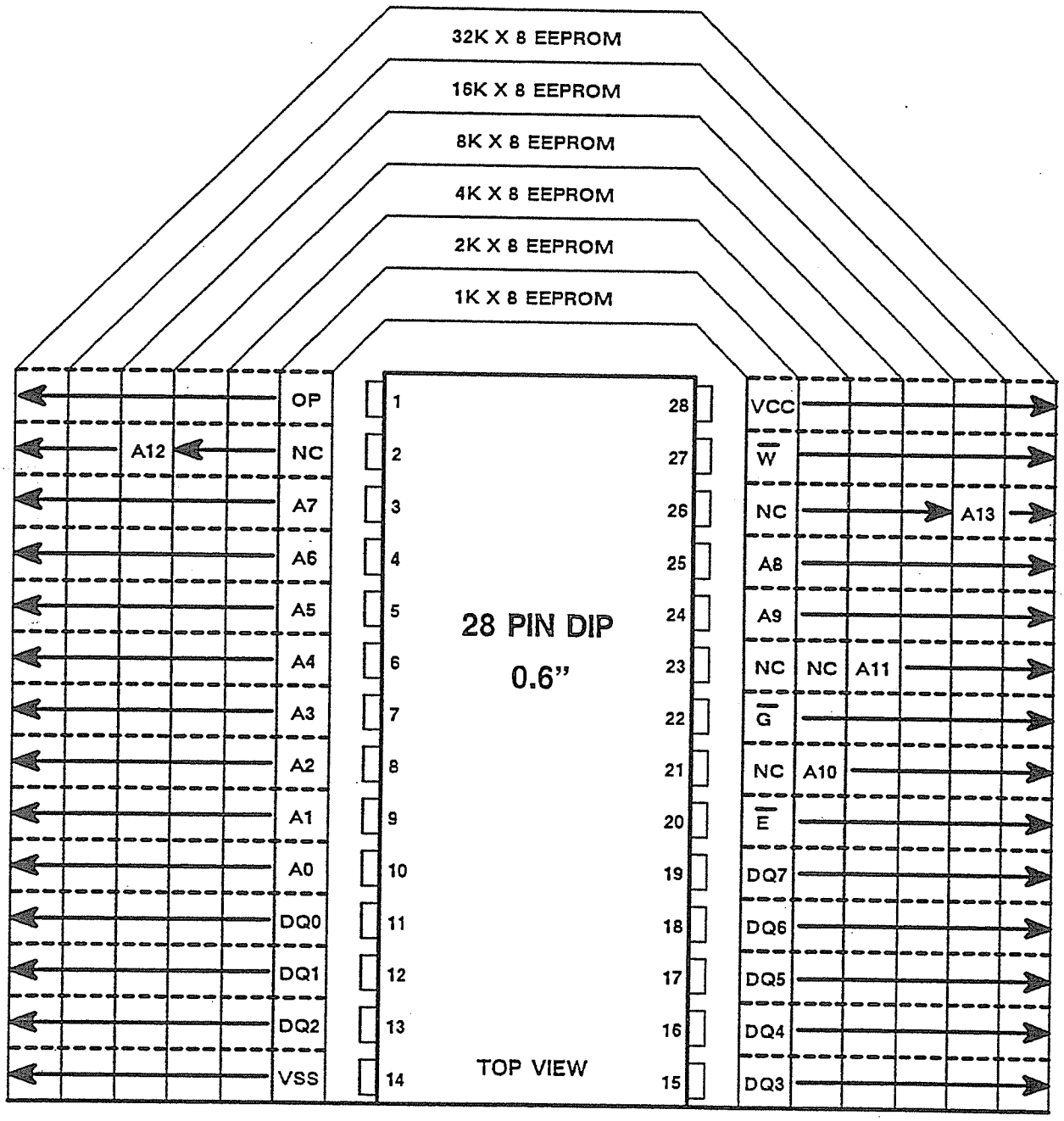


FIGURE 3.5.1-3
1K TO 32K BY 8 EEPROM FAMILY IN DIP

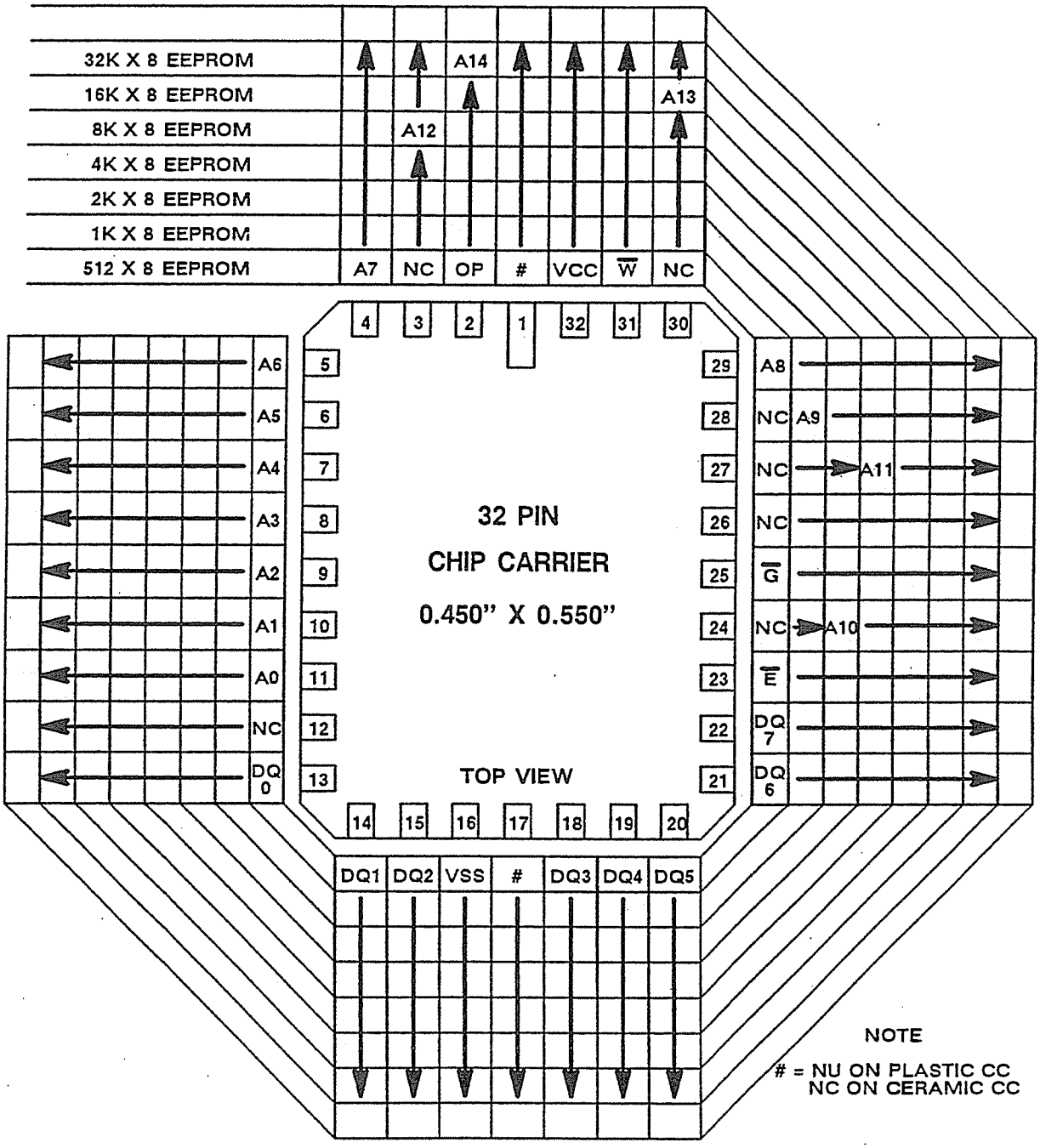


FIGURE 3.5.1-4
.5K TO 32K BY 8 EEPROM FAMILY IN RCC

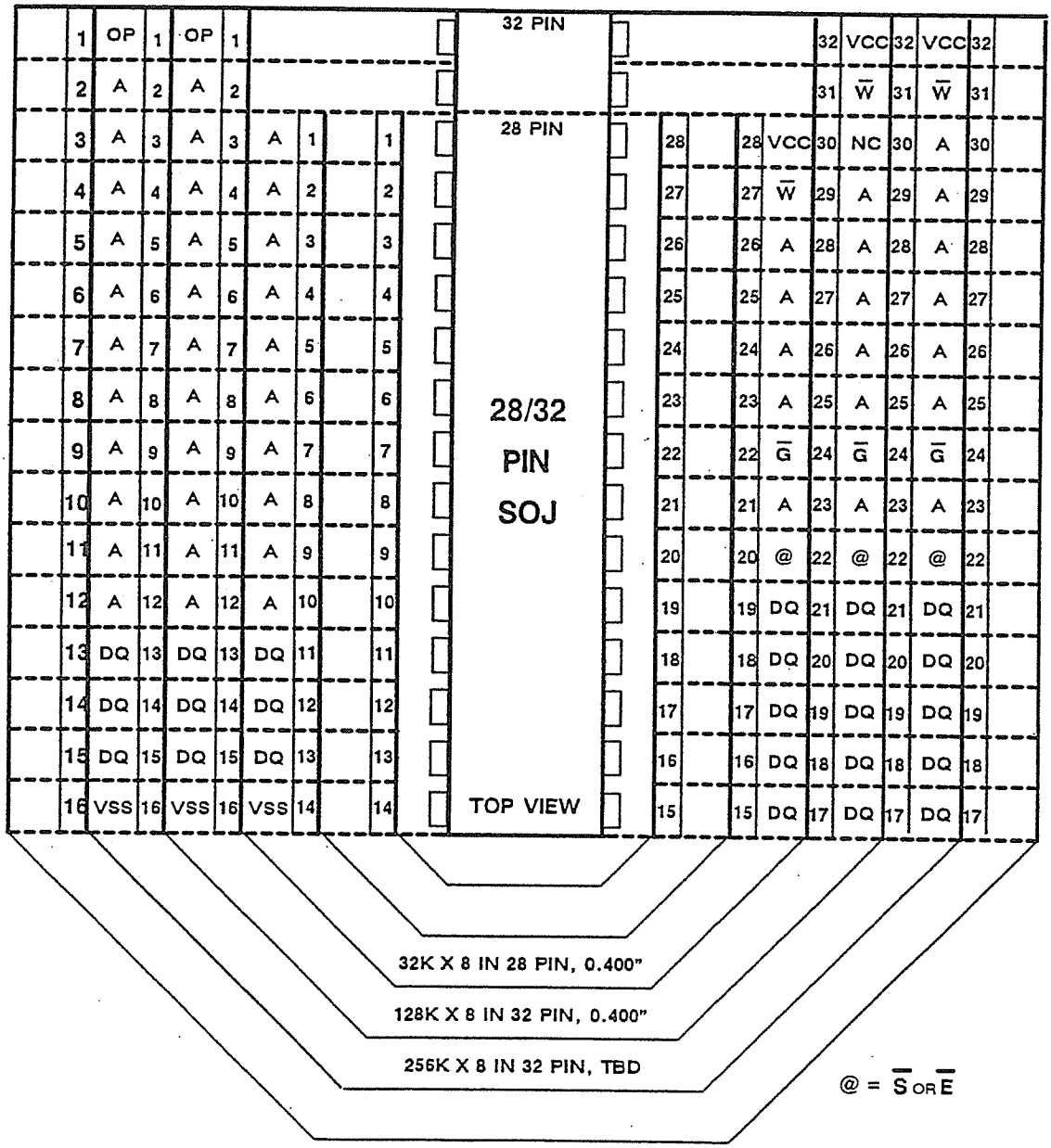


FIGURE 3.5.1-5
32K TO 256K BY 8 EEPROM FAMILY IN SOJ

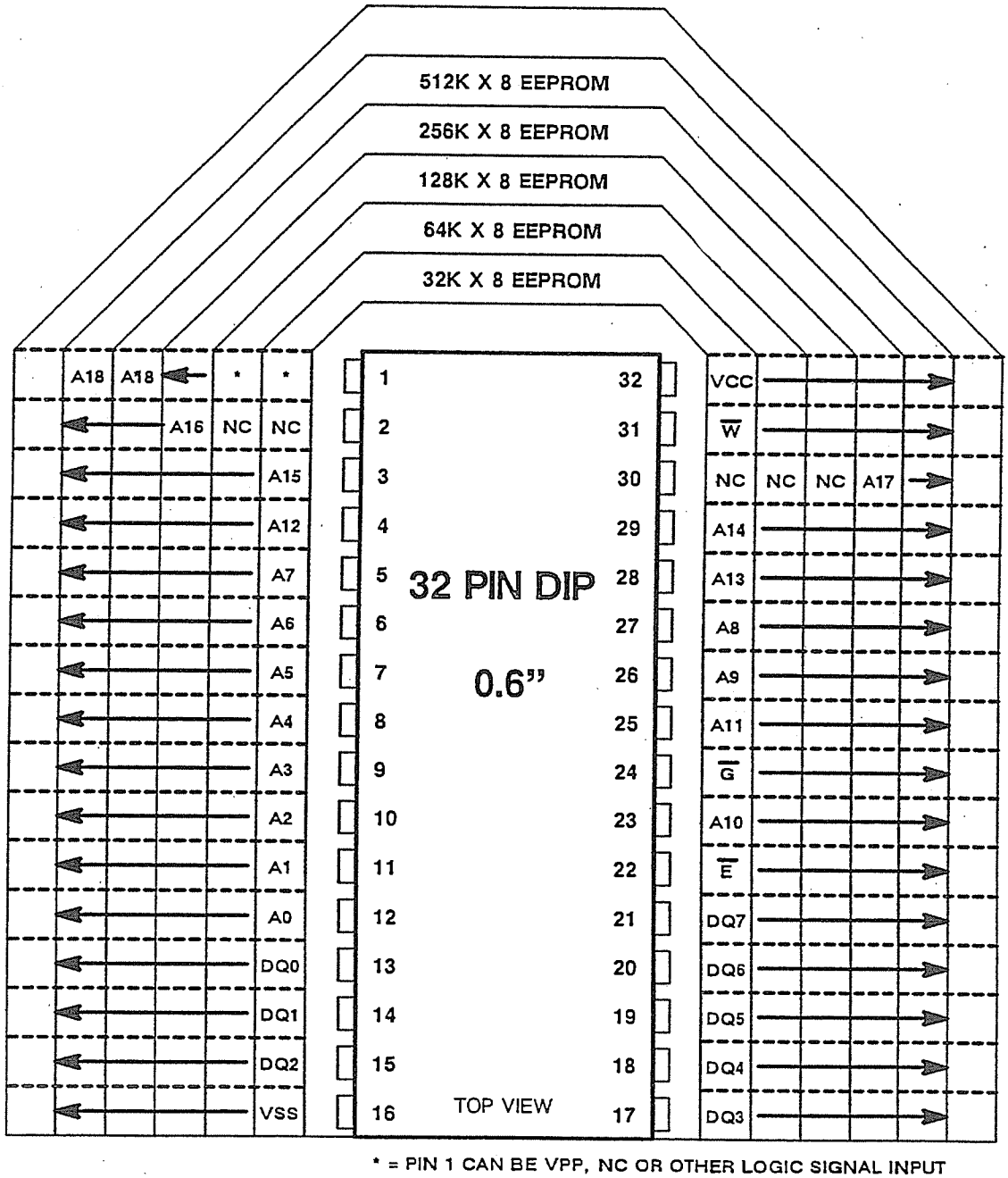


FIGURE 3.5.1-6
32K TO 512K BY 8 EEPROM FAMILY IN DIP

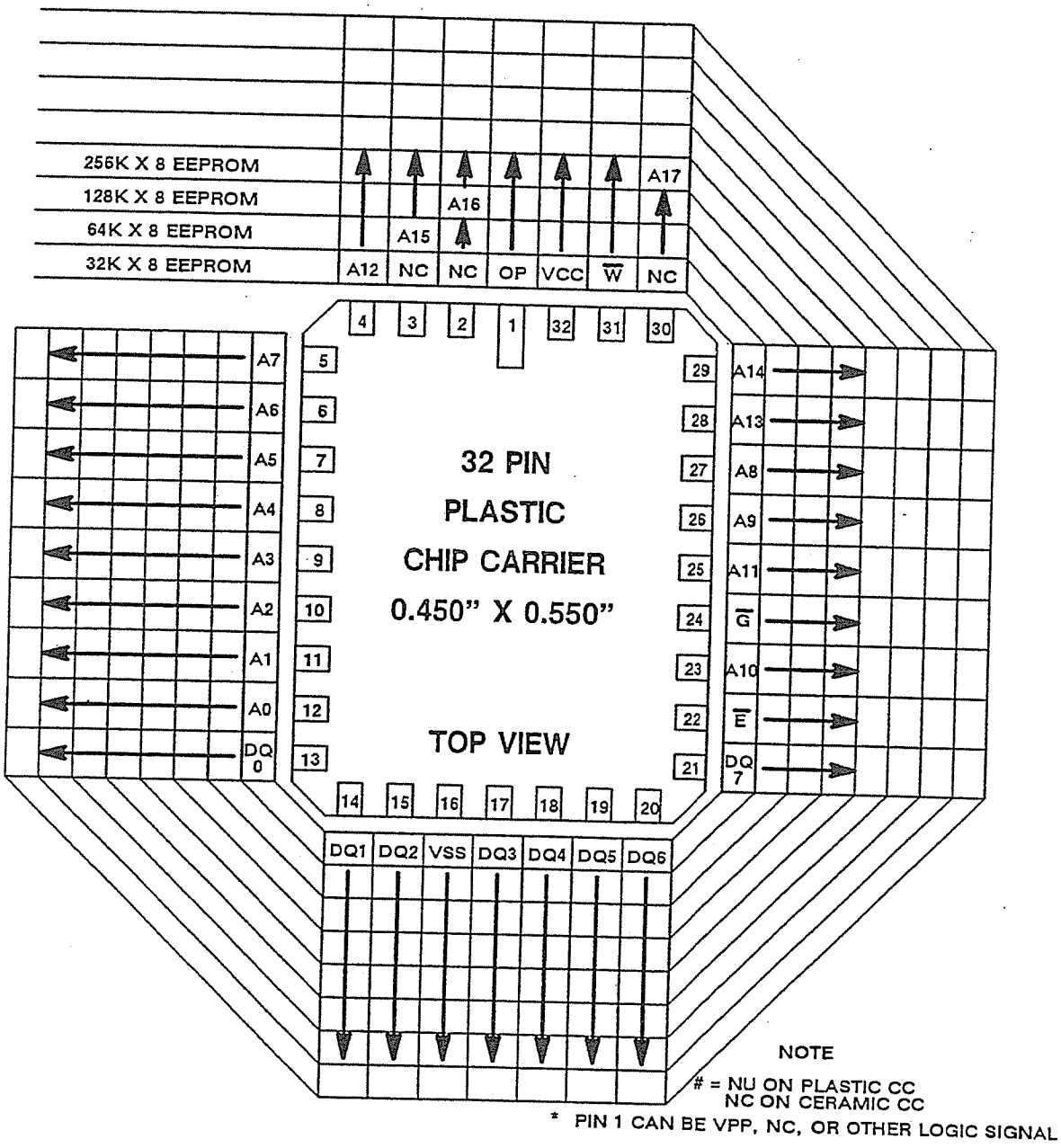


FIGURE 3.5.1-7
32K TO 256K BY 8 EEPROM FAMILY IN RCC

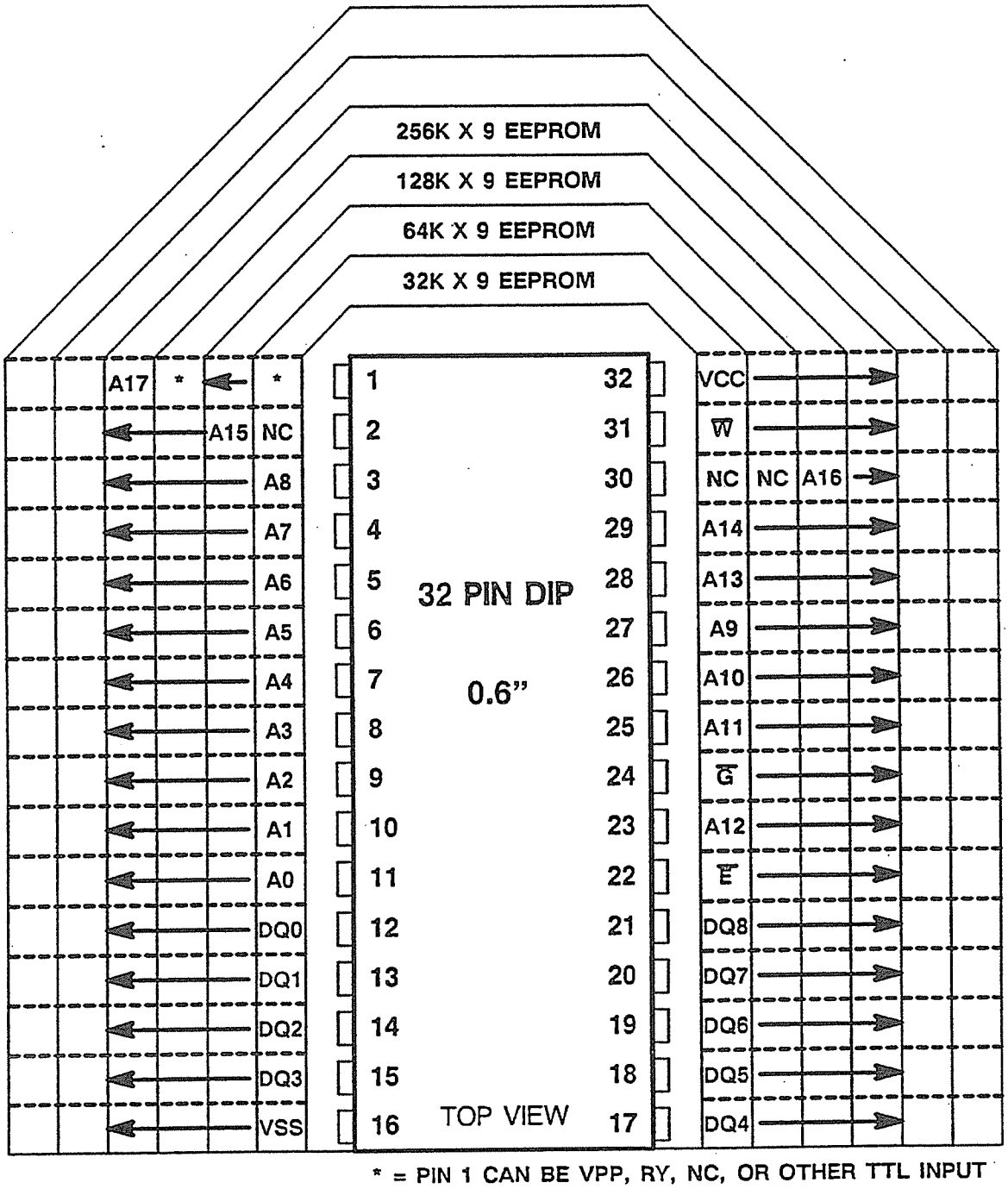


FIGURE 3.5.1-8
32K TO 256K BY 9 EEPROM FAMILY IN DIP

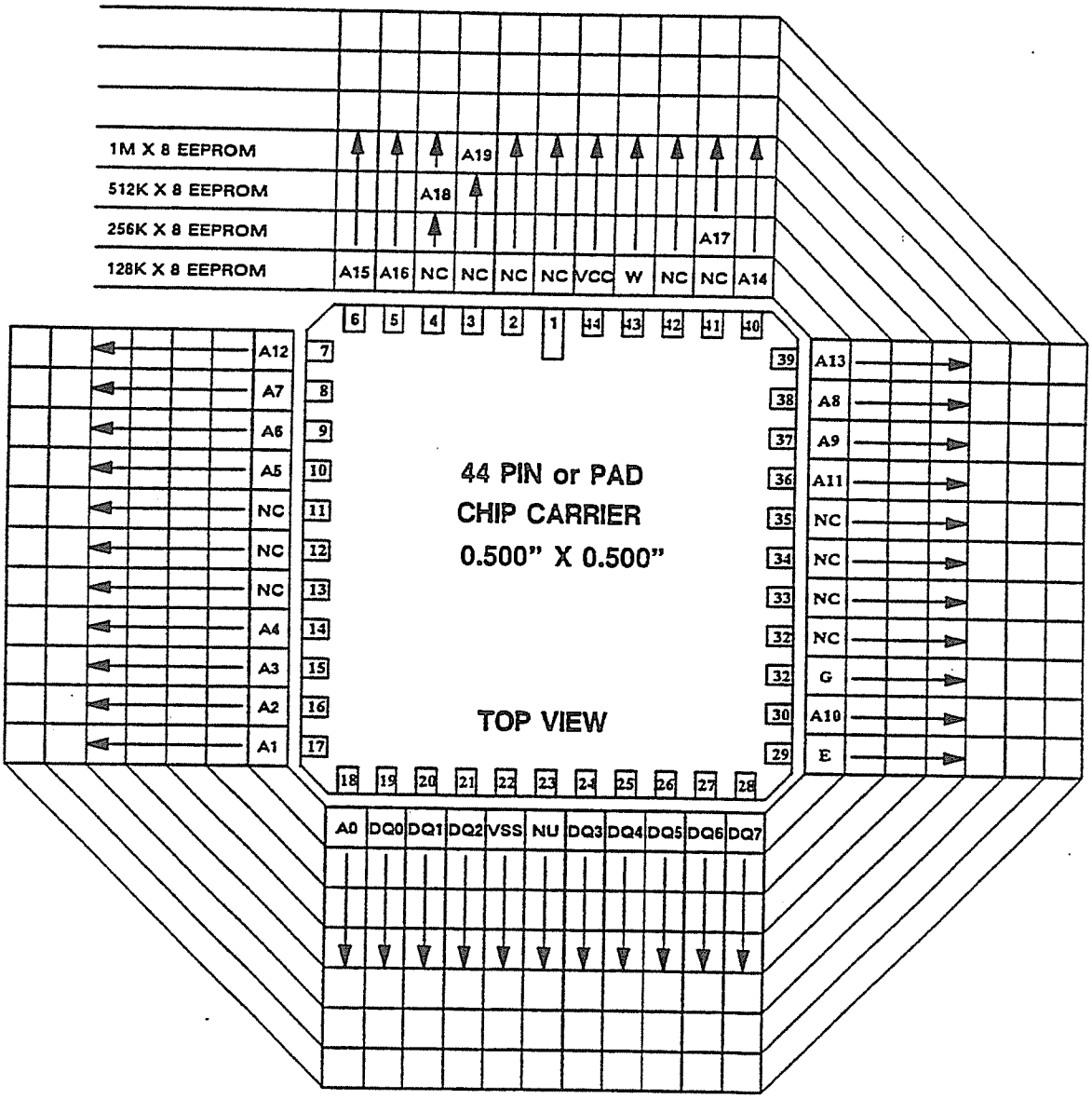
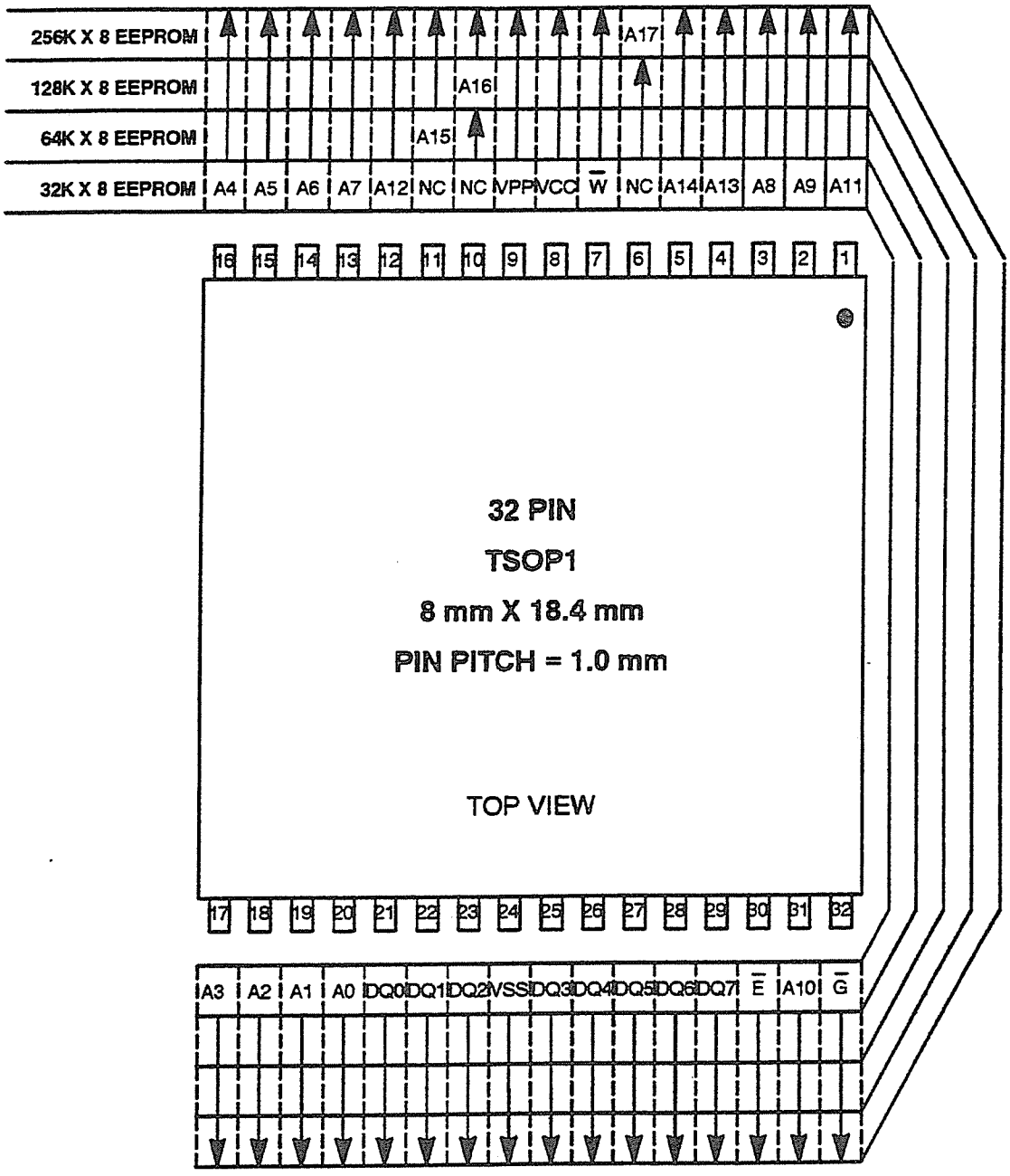


FIGURE 3.5.1-9
128K TO 1M BY 8 EEPROM FAMILY IN SCC



NOTE – This 32k X 8 part is for EEPROM with VPP, and is not compatible with the 5 V only 32k x 8 part derived from the 28 pin dip standard.

The JEDEC Std. No 30 designator for the TSOP1 package is PDSO–G

FIGURE 3.5.1–10
32K TO 256K BY 8 EEPROM IN TSOP1

32K X 8 BIT EEPROM EXTENDED FEATURE STANDARD

This standard specifies features, beyond the existing JEDEC pinout standards, that need to be standardized for 32K x 8, bytewide EEPROMS. Two categories of features are defined in this standard: 1) Mandatory features, 2), Optional features.

The mandatory features, which are the minimum set necessary to achieve functional compatability for 256K EEPROMs, must be implemented to be in compliance with this standard. Any, all, or none of the optional features may be implemented at the manufacturers discretion. However, if an optional feature defined in this standard is implemented, it must operate as specified in this standard to be in compliance with the standard.

Other features not described in the standard may be incorporated and the device still be in compliance as long as they are compatible with the required and optional features in this standard.

256K BIT BYTEWIDE EEPROM REQUIRED STANDARD FEATURES

1. VCC SUPPLY IS 5 VOLTS NOMINAL
2. STANDARD LOGIC TRUTH TABLE (FIG. A1-1)
3. STANDARD READ CYCLE TIMING (FIG. A1-2)
4. STANDARD BYTE WRITE CYCLE FEATURES
   -TIMING (FIG. A1-3)
   -DATA AND ADDRESS LATCHES
   -SELF-TIMED WRITE CYCLES
   -ALL INPUT LEVELS IN RANGE BETWEEN 0 V AND 5 V.

OPTIONAL FEATURES

1. PAGE WRITE MODE (FIG. A1-4)
   -STANDARD PAGE WRITE CYCLE TIMING
   -16 BYTE MINIMUM PAGE SIZE (A0 - A3)
2. DATA POLLING (FIG. A1-5)
   -MUST MEET NORMAL READ CYCLE AND WRITE CYCLE TIMING
3. SOFTWARE DATA PROTECT OPTION (FIGS. A1-6 & A1-7)
4. HARDWARE MASS ERASE (ALL 1'S) (FIG. A1-8)
5. SOFTWARE MASS ERASE (ALL 1'S) (FIG. A1-9)

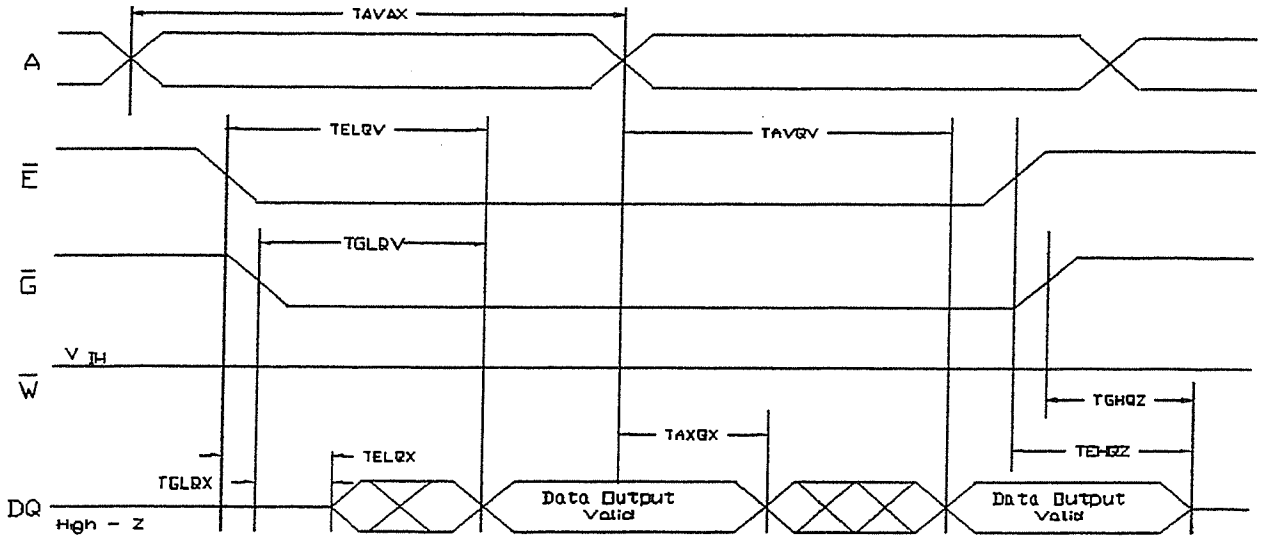
32K BY 8 BIT EEPROM TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
L	L	H	READ	Q	ACTIVE
L	H	L	WRITE	D	ACTIVE
H	X	X	STANDBY AND WRITE INHIBIT	HIGH Z	STANDBY
L	L	L	WRITE INHIBIT	HIGH Z	ACTIVE
L	H	H	WRITE INHIBIT	HIGH Z	ACTIVE

*NOTE: G functions as both an output control and a write inhibit control in this EEPROM Standard.

FIGURE A1-1

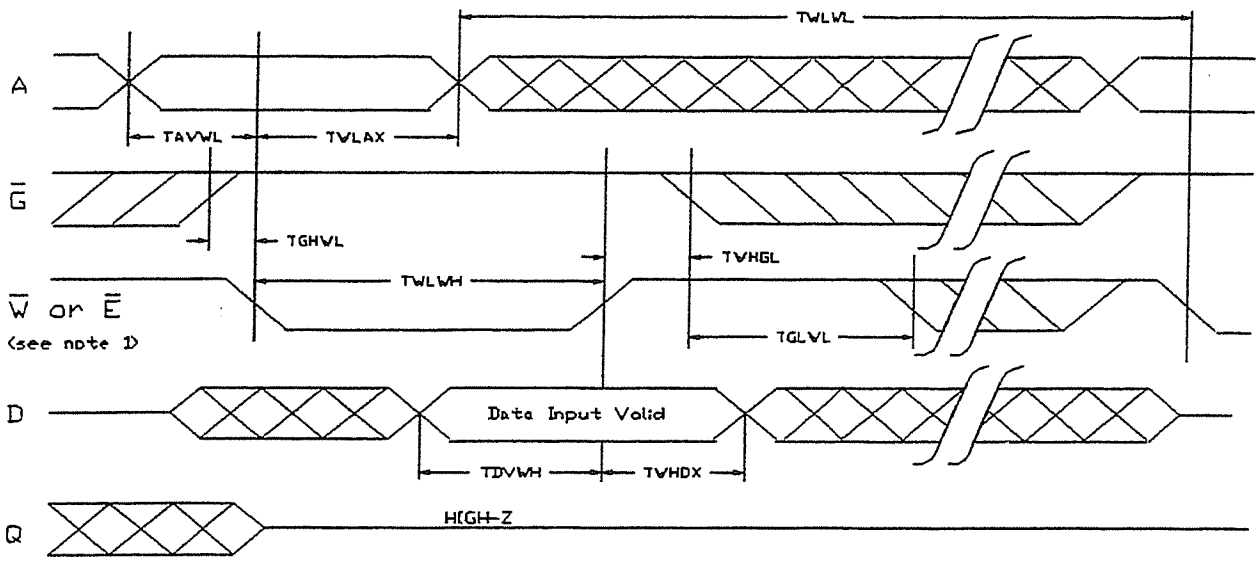
256K BIT EEPROM READ CYCLE TIMING



SYMBOL	DESCRIPTION
tAVAX	ADDRESS VALID TO ADDRESS CHANGE (READ CYCLE TIME)
tELQV	$\overline{E}$ LOW TO OUTPUT VALID (CHIP ENABLE ACCESS TIME)
tAVQV	ADDRESS VALID TO OUTPUT VALID (ADDRESS ACCESS TIME) tGLQV
tELQX	$\overline{E}$ LOW TO ACTIVE OUTPUT
tGLQX	$\overline{G}$ LOW TO ACTIVE OUTPUT
tEHQZ	$\overline{E}$ HIGH TO HIGH-Z OUTPUT
tGHQZ	$\overline{G}$ HIGH TO HIGH-Z OUTPUT
tAXQX	ADDRESS INVALID TO DATA OUT INVALID

FIGURE A1-2

256K BIT EEPROM STANDARD BYTE WRITE CYCLE TIMING

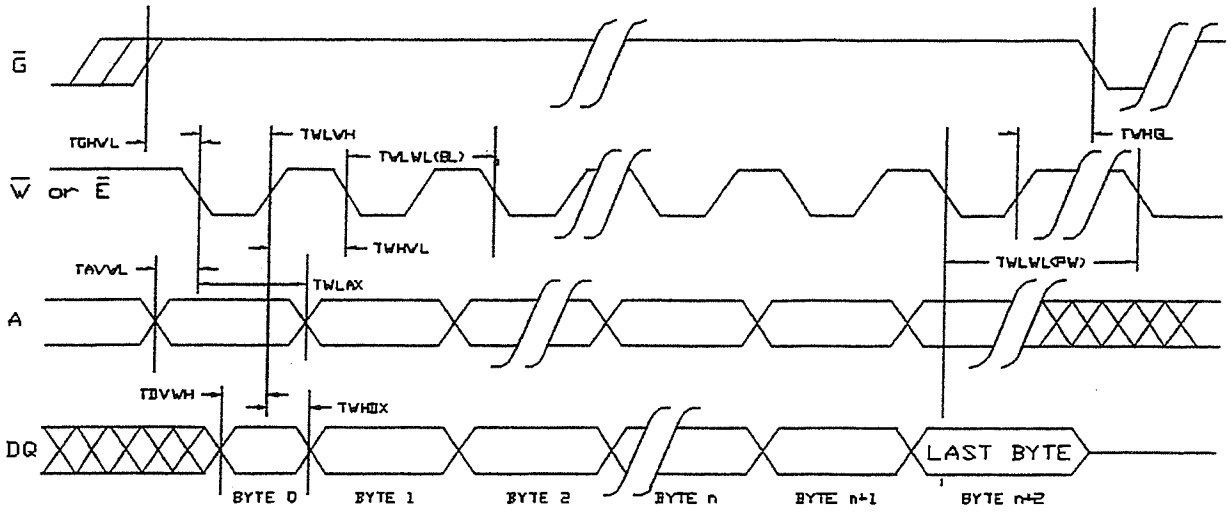


NOTE 1: Write Cycle Timing is referenced to the $\overline{W}$ or $\overline{E}$ inputs, whichever is last going low, and the $\overline{W}$ or $\overline{E}$ inputs, whichever is first, going high.

SYMBOL (NOTE 1)	DESCRIPTION
tWLWL, tELEL	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW CYCLE TIME (WRITE CYCLE TIME)
tAVWL, tAVEL	ADDRESS VALID TO $\overline{W}$ OR $\overline{E}$ LOW TIME (ADDRESS SET-UP TIME)
tWLAX, tELAX	$\overline{W}$ OR $\overline{E}$ LOW TO ADDRESS INVALID (ADDRESS HOLD TIME)
tGHWL, tGHEL	$\overline{G}$ HIGH TO $\overline{W}$ OR $\overline{E}$ LOW TIME
tWHGL, tEHGL	$\overline{G}$ HIGH HOLD TIME FROM $\overline{W}$ OR $\overline{E}$ HIGH
tWLWH, tELEH	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ HIGH (WRITE PULSE DURATION)
tGLWL, tGLEL	$\overline{G}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW ($\overline{G}$ LOW WRITE INHIBIT SETUP TIME)
tDVWH, tDVEH	DATA INPUT VALID TO $\overline{W}$ OR $\overline{E}$ HIGH (DATA SET-UP TIME)
tWHDX, tEHDX	$\overline{W}$ OR $\overline{E}$ HIGH TO DATA INPUT INVALID (DATA HOLD TIME)

FIGURE A1-3

256K BIT EEPROM PAGE MODE WRITE CYCLE TIMING



Note 2: Page Load Timings are referenced to the $\overline{W}$ or $\overline{E}$ inputs, whichever is last when going low, and to the $\overline{W}$ or $\overline{E}$ inputs, whichever is first when going high.

Note 3: Bytes may be loaded and re-loaded at random within a page load cycle. The page address must remain the same throughout the page load cycle.

SYMBOL (NOTE 2), DESCRIPTION	
tWLWL, (PW)	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW PAGE WRITE CYCLE TIME
tAVWL, tAVEL	ADDRESS VALID TO $\overline{W}$ OR $\overline{E}$ LOW TIME (ADDRESS SET-UP TIME
tWLAX, tELAX	$\overline{W}$ OR $\overline{E}$ LOW TO ADDRESS INVALID (ADDRESS HOLD TIME)
tGHWL, tGHEL	$\overline{G}$ HIGH TO $\overline{W}$ OR $\overline{E}$ LOW TIME
tWHGL, tEHGL	$\overline{G}$ HIGH HOLD TIME FROM $\overline{W}$ OR $\overline{E}$ HIGH
tWLWH, tELEH	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ HIGH TIME (WRITE PULSE DURATION)
tWHWL, tEHEL	$\overline{W}$ OR $\overline{E}$ HIGH TO $\overline{W}$ OR $\overline{E}$ LOW TIME (WRITE HIGH RECOVERY)
tDVWH, tDVEH	DATA INPUT VALID TO $\overline{W}$ OR $\overline{E}$ HIGH (DATA SET-UP TIME)
tWHDX, tEHDX	$\overline{W}$ OR $\overline{E}$ HIGH TO DATA INPUT VALID (DATA HOLD TIME)
tWLWL, (BL)	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW BYTE LOAD CYCLE TIME

FIGURE A1-4

256K BIT EEPROM DATA POLLING FEATURE

–The DATA Polling feature is used to determine if a Write Cycle is in Progress in the EEPROM or if the part is available for Reading or another Write Cycle.

–Whenever the part is read during a nonvolatile write cycle, the data available at the outputs is the complement of the last byte written to the part. As a minimum, the data available at only DQ7 is the complement of bit 7 of the last byte written.

–When the nonvolatile write cycle automatically times out, normal valid data is read at outputs which means the last byte written will be true data rather than the complement.

–A software polling routine uses this feature to determine when the nonvolatile write cycle is complete.

–The normal read cycle timing specified for the part must be used for DATA polling read cycles.

–An additional timing parameter tWHQV (COMPLEMENT), must also be specified for the DATA polling cycle.

–tWHQV (COMPLEMENT) = $\overline{W}$ HIGH TO VALID COMPLEMENTED DATA OUTPUT.

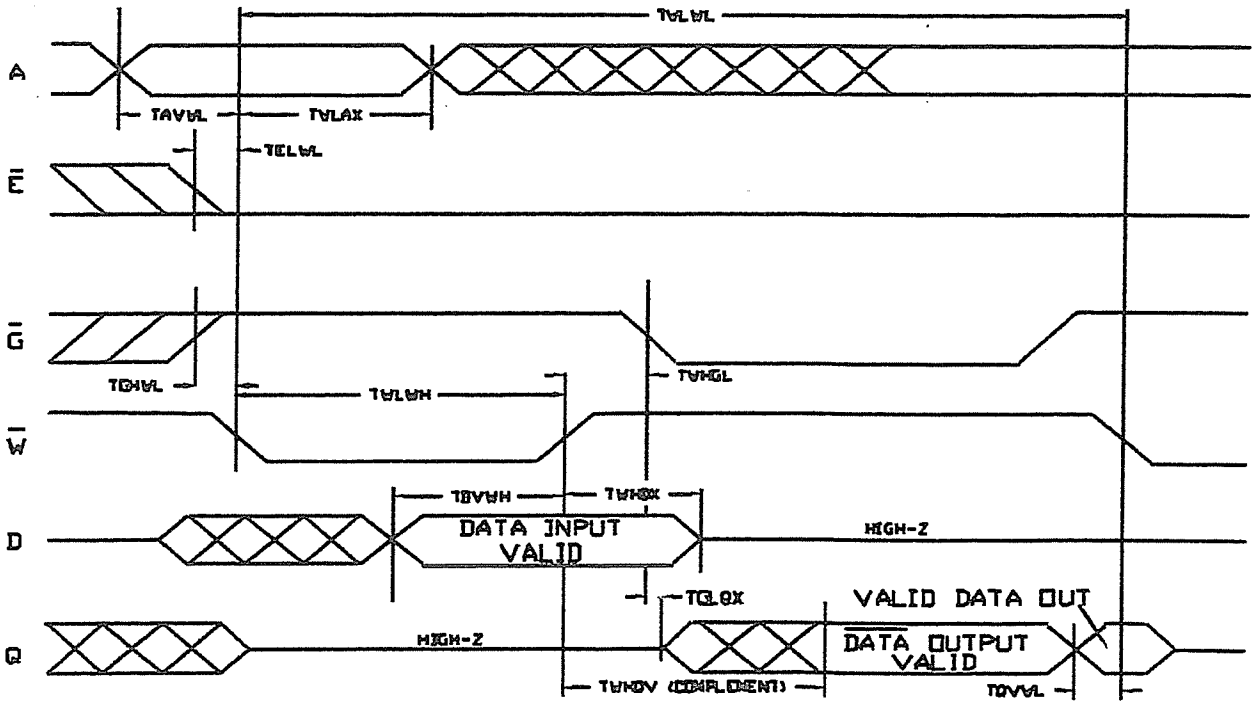


FIGURE A1-5

256K BIT EEPROM OPTIONAL SOFTWARE DATA PROTECTION

–SOFTWARE DATA PROTECTION IS A DIFFERENT METHOD OF PREVENTING INADVERTANT WRITE OPERATIONS IN A NONVOLATILE MEMORY COMPARED TO THE "HARDWARE" METHODS, SUCH AS: $\overline{E}$, $\overline{G}$, AND $\overline{W}$ LOGIC COMBINATIONS, VCC LEVEL DETECTORS, AND POWER UP TIMERS.

–A SPECIFIC DATA AND ADDRESS SOFTWARE SEQUENCE MUST BE ISSUED TO ENABLE A SINGLE PAGE OR BYTE WRITE.

–DATA INPUT FORMAT: D7/D6/D5/D4/D3/D2/D1/D0

–ADDRESS FORMAT: A14/A13/A12/A11/A10/A9/A8/A7/A6/A5/A4/A3/A2/A1/A0

STEP	MODE	A14-A0	DQ7-DQ0
1	"ACCESS WRITE"	5555H	AAH
2	"ACCESS WRITE"	2AAAH	55H
3	"ACCESS WRITE	5555H	A0H
4	"PAGE WRITE"	Address	Data

–ALL WRITES MUST CONFORM TO THE PAGE MODE TIMING REQUIREMENTS FOR THE PART.

–SINCE THE PAGE ADDRESS IS CHANGED (A VIOLATION OF THE NORMAL PAGE MODE WRITE CYCLE), THE FIRST THREE "ACCESS" WRITES (STEPS 1-3) ARE USED ONLY FOR SOFTWARE ACCESS, NO DATA IS ACTUALLY WRITTEN TO THE EEPROM.

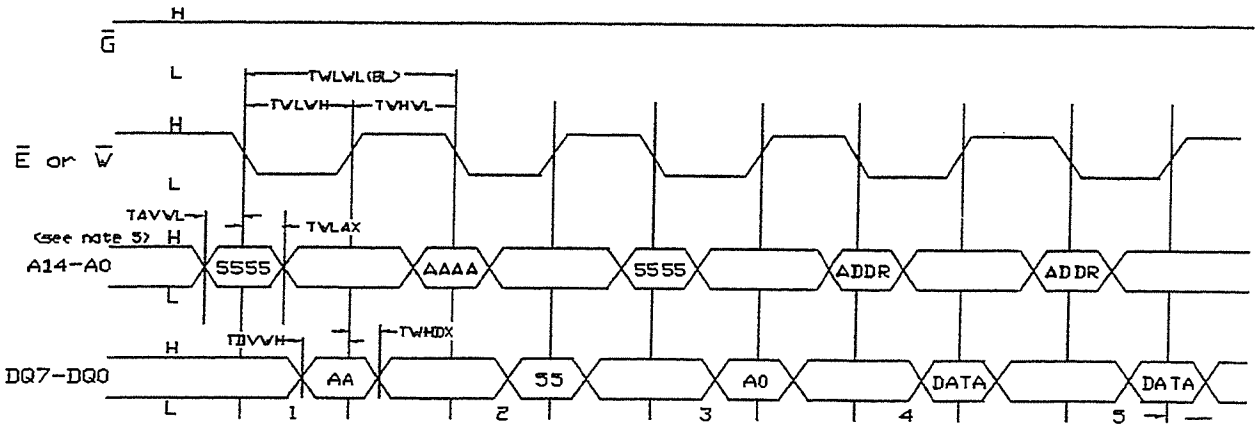
–THE FIRST TIME THIS SEQUENCE IS APPLIED TO THE PART A NONVOLATILE BIT IS SET, WHICH RECONFIGURES THE PART FROM HARDWARE PROTECTED ONLY TO HARDWARE AND SOFTWARE SEQUENCE PROTECTED. ONCE THIS BIT IS SET, THE SOFTWARE SEQUENCE MUST BE USED TO WRITE TO THE PART.

–THE SOFTWARE PROTECTION CAN BE DISABLED AND THE PART RECONFIGURED TO HARDWARE-ONLY PROTECTION, BY APPLYING THE SIX STEP SOFTWARE SEQUENCE BELOW:

STEP	MODE	A14-A0	DQ7-DQ0
1	"ACCESS" WRITE	5555H	AAH
2	"ACCESS" WRITE	2AAAH	55H
3	"ACCESS" WRITE	5555H	80H
4	"ACCESS" WRITE	5555H	AAH
5	"ACCESS" WRITE	2AAAH	55H
6	"ACCESS" WRITE	5555H	20H

FIGURE A1-6

256K BIT EEPROM SOFTWARE DATA PROTECTION TIMING



NOTE 5: Software Data Protection Timings are referenced to the $\overline{W}$ or $\overline{E}$ inputs, whichever is last going LOW, and the $\overline{W}$ or $\overline{E}$ inputs, whichever is first, going HIGH.

SYMBOL (NOTE 5)	DESCRIPTION
tWLWL(BL), tELEL(BL)	$\overline{W}$ OR $\overline{E}$ LOW TO W OR E LOW BYTE LOW CYCLE TIME
tWLWH, tELEH	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ HIGH (WRITE PULSE DURATION)
tWHWL, tEHEL	$\overline{W}$ OR $\overline{E}$ HIGH TO $\overline{W}$ OR $\overline{E}$ LOW TIME (WRITE HIGH RECOVERY)
tAVWL, tAVEL	ADDRESS VALID TO $\overline{W}$ OR $\overline{E}$ LOW TIME (ADDRESS SET-UP TIME)
tWLAX, tELAX	$\overline{W}$ OR $\overline{E}$ LOW TO ADDRESS INVALID TIME (ADDRESS HOLD TIME)
tDVWH, tDVEH	DATA INPUT VALID TO $\overline{W}$ OR $\overline{E}$ HIGH (DATA SET-UP TIME)
tWHDX, tEHDX	$\overline{W}$ OR $\overline{E}$ HIGH TO DATA INPUT INVALID (DATA HOLD TIME)

FIGURE A1-7

256K BIT EEPROM OPTIONAL HARDWARE MASS ERASE (ALL 1'S) FEATURE

– IF A HARDWARE MASS ERASE MODE IS IMPLEMENTED ON THE 256K EEPROM, THE FOLLOWING CONVENTIONS MUST BE FOLLOWED:

– $\overline{E}$ = LOW LOGIC LEVEL

– $\overline{W}$ = LOW LOGIC LEVEL

– $\overline{G}$ = SUPER VOLTAGE (WAVEFORM, LEVEL AND TIMING TO BE DETERMINED BY THE MANUFACTURER).

– DQ0 - DQ7 = ALL HIGH LOGIC LEVEL (FFH)

– A0 - A14 = DON'T CARE (EITHER HIGH OR LOW LOGIC LEVELS)

FIGURE A1-8

256K BIT EEPROM OPTIONAL SOFTWARE MASS ERASE (ALL 1'S) FEATURE

IF A SOFTWARE MASS ERASE FEATURE IS IMPLEMENTED IN THE 256K EEPROM, IT MUST OPERATE BY APPLYING THE FOLLOWING SIX DATA/ADDRESS SEQUENCE TO THE PART.

STEP	MODE	A14-A0	DQ7-DQ0
1	"ACCESS" WRITE	5555H	AAH
2	"ACCESS" WRITE	2AAAH	55H
3	"ACCESS" WRITE	5555H	80H
4	"ACCESS" WRITE	5555H	AAH
5	"ACCESS" WRITE	2AAAH	55H
6	"ACCESS" WRITE	5555H	10H

–ALL ACCESS WRITES MUST FOLLOW THE STANDARD PAGE MODE WRITE CYCLE TIMING SPECIFIED FOR THE PART.

–NO DATA IS ACTUALLY WRITTEN TO THE EEPROM DURING THE "ACCESS" WRITES. ONCE THE 6 STEP SEQUENCE IS COMPLETED, THE PART AUTOMATICALLY COMPLETES A MASS ERASE CYCLE INTERNALLY.

FIGURE A1-9

DUAL POWER SUPPLY EEPROM COMMAND SET

COMMAND CODES

1st CYCLE	2nd CYCLE	OPERATION DESCRIPTION
00		Reserved
10		Automated Write
20	20	Algorithmic Chip Erase
20	D0	Automated Block Erase
30	30	Automated Chip Erase
40		Algorithmic Write
50		Reserved
60	60	Algorithmic Block Erase
70		Reserved
80		Reserved
90		Read ID
A0		Algorithmic Erase Verify
B0		Reserved
C0		Algorithmic Write Verify
D0		Reserved
E0		Reserved
FF		Read/Reset

NOTE: All operands are in HEX.

This Standard provides an optional command set for use with dual supply voltage EEPROM devices. Thes command set comprehends algorithmic commands and adds a set of automatic codes. A device may respond to either or both operating modes

The standard is applicable to devices with all data interface widths.

FIGURE 3.5.1-11

DUAL POWER SUPPLY EEPROM COMMAND SET

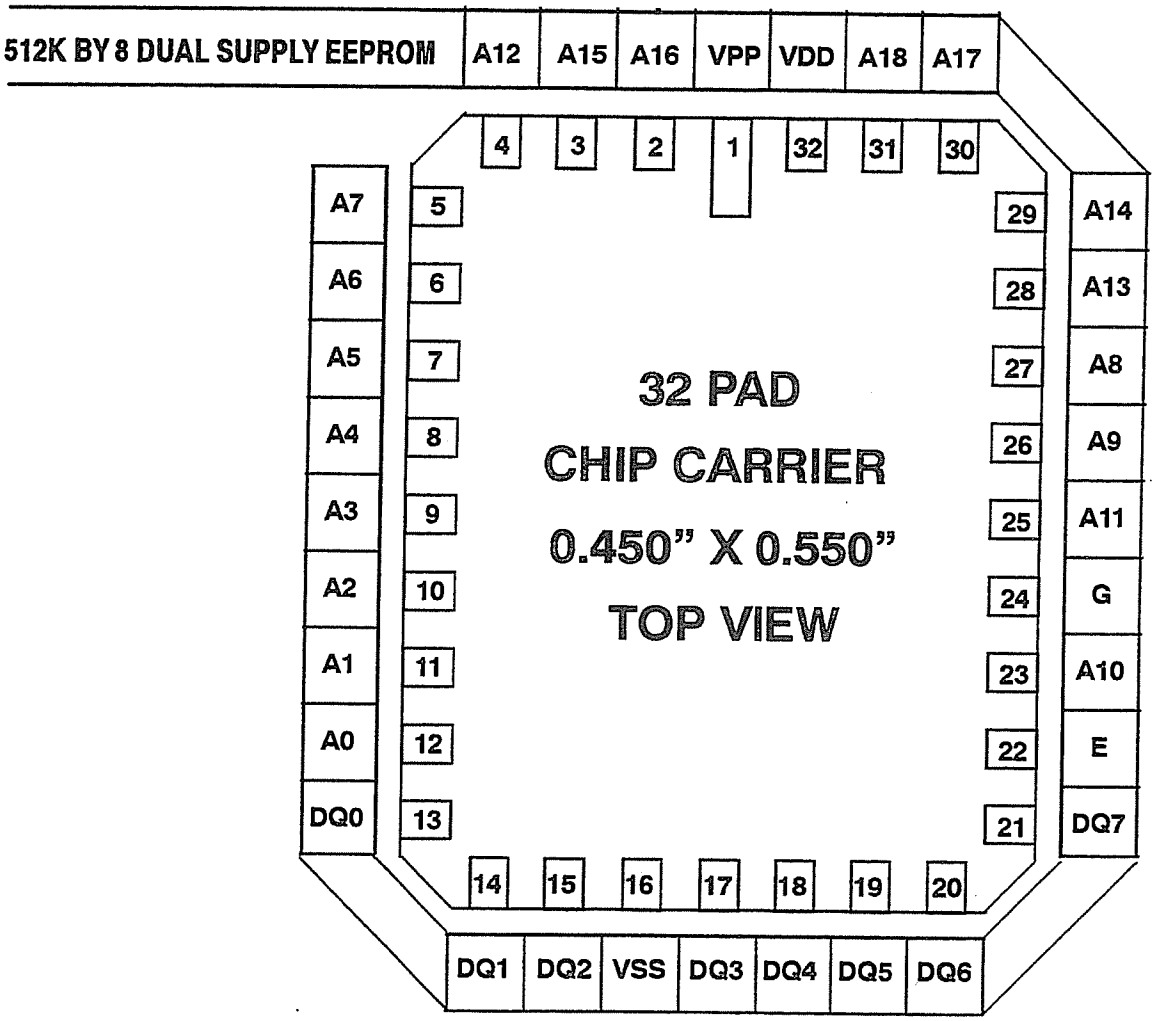


FIGURE 3.5.1-12
512K BY 8 DUAL-SUPPLY EEPROM IN RCC

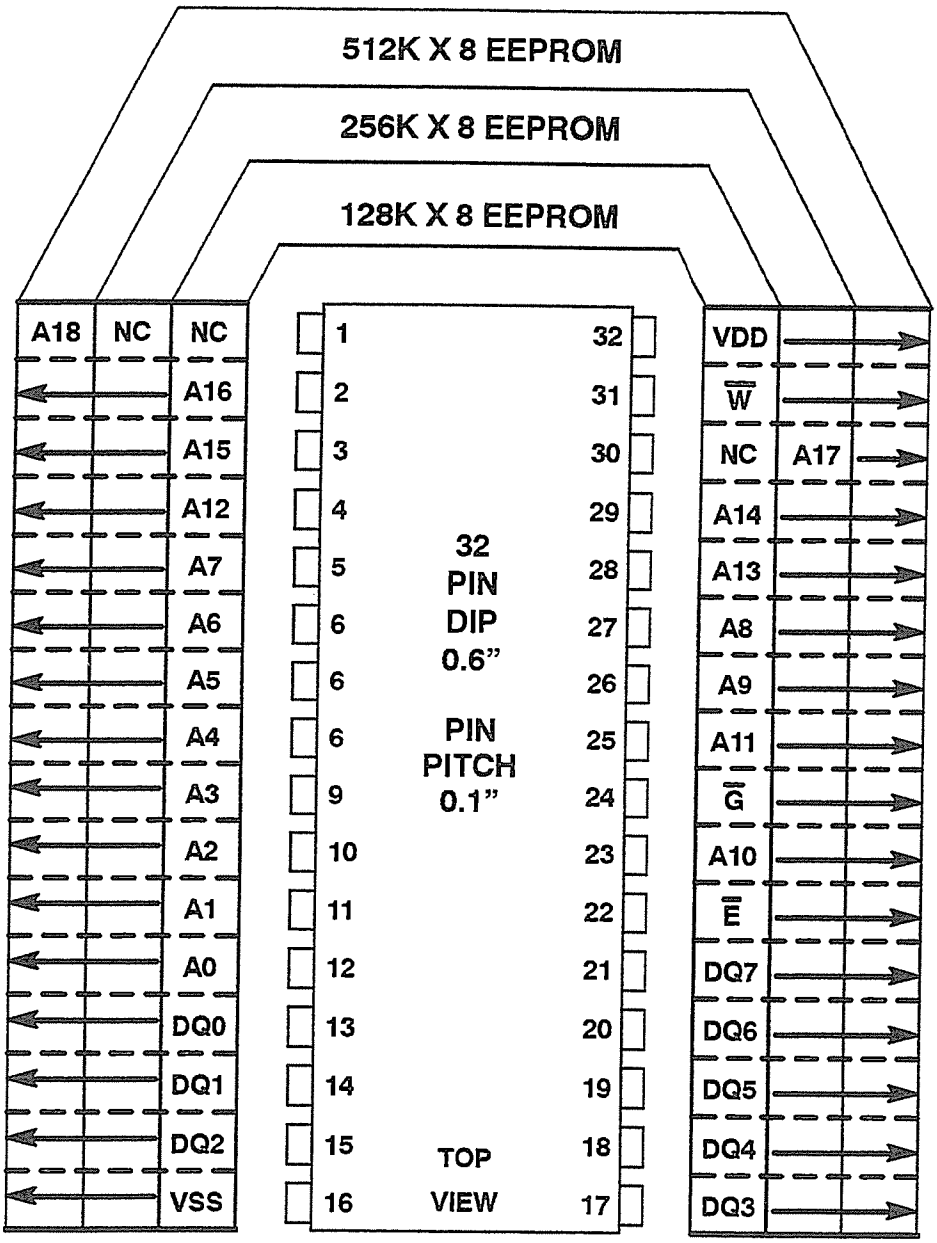


FIGURE 3.5.1-13

128K TO 512K BY 8 SINGLE-SUPPLY EEPROM FAMILY IN DIP

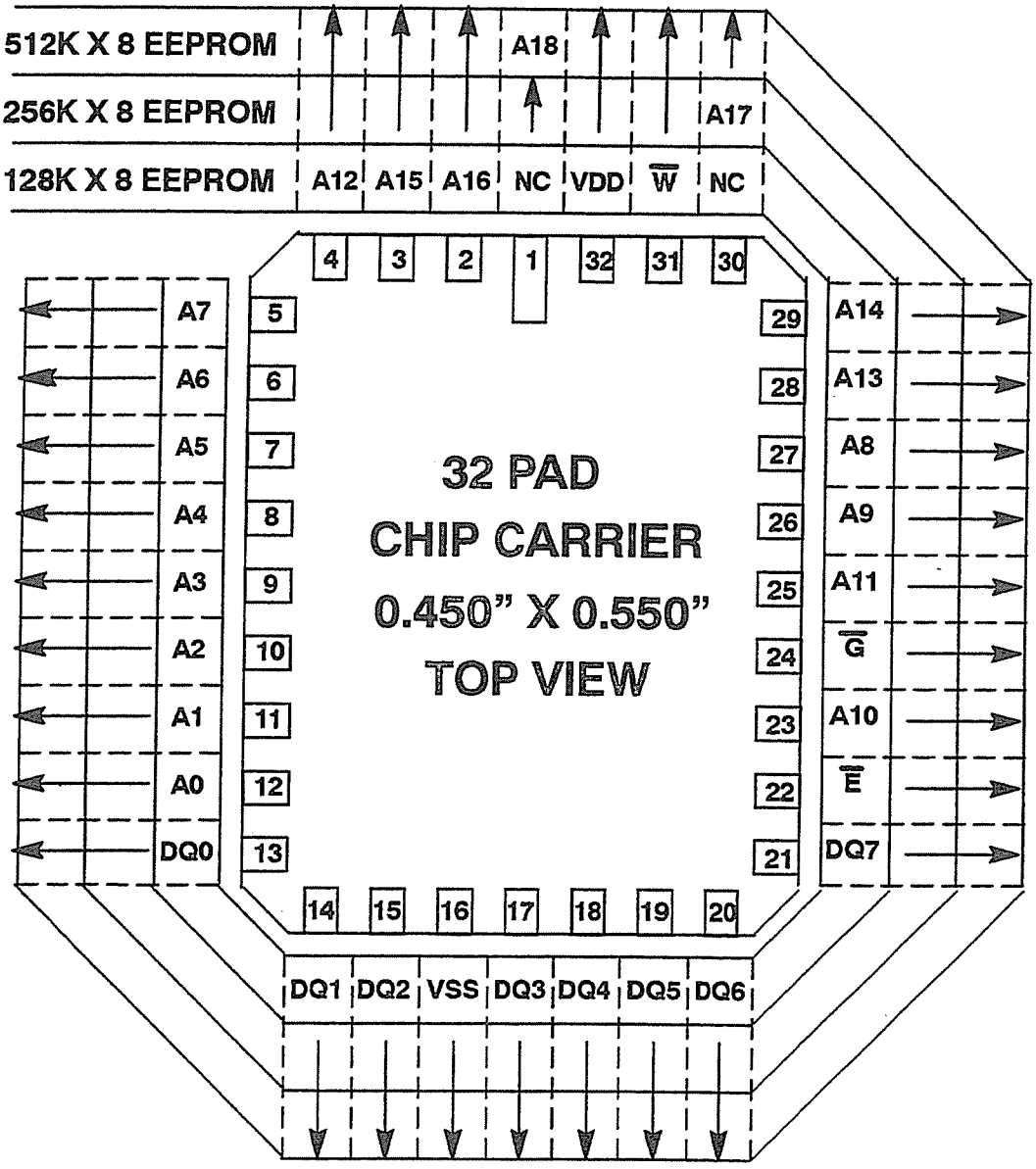


FIGURE 3.5.1-14

128K TO 512K BY 8 SINGLE-SUPPLY EEPROM FAMILY IN RCC

Release 5

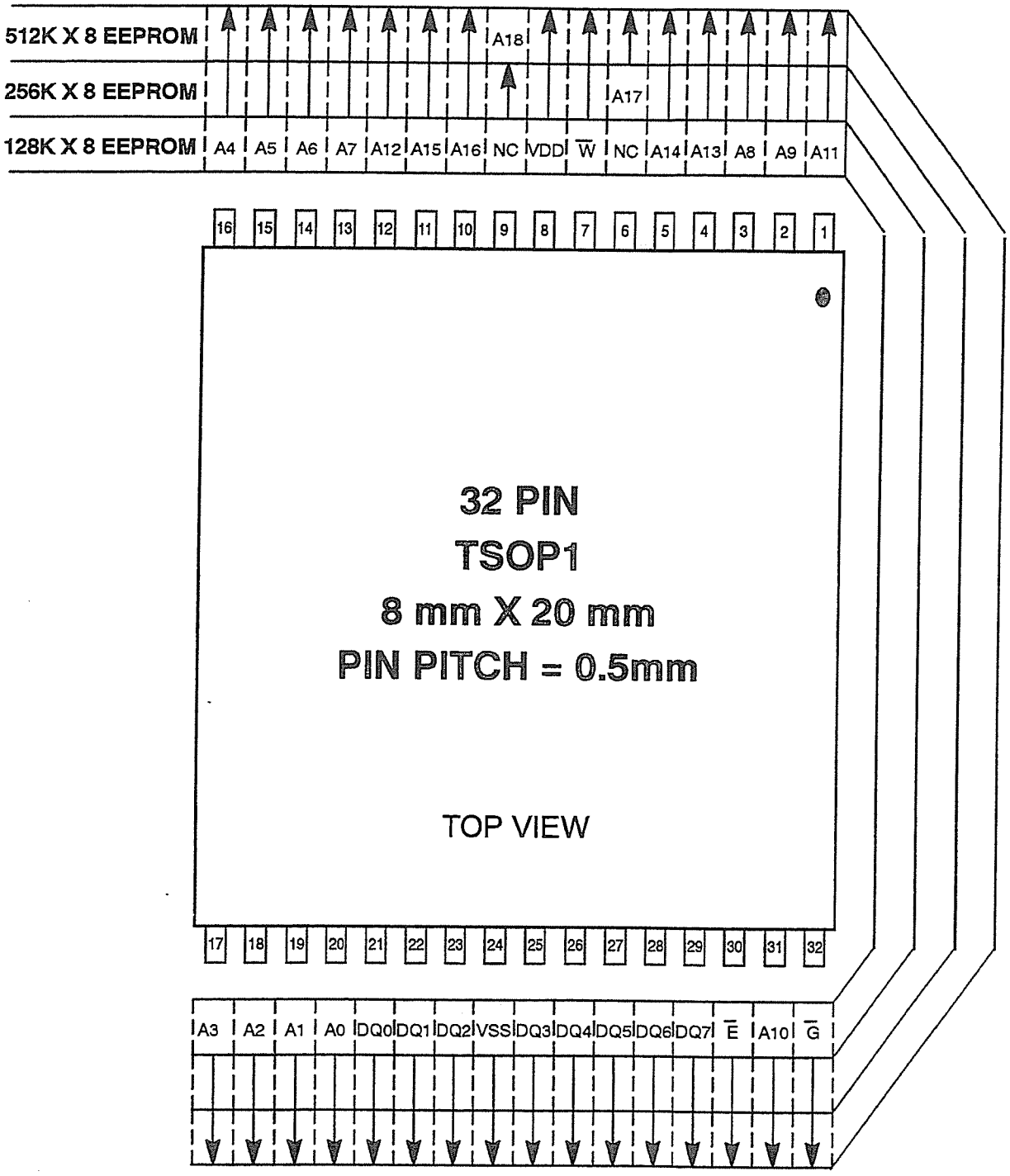
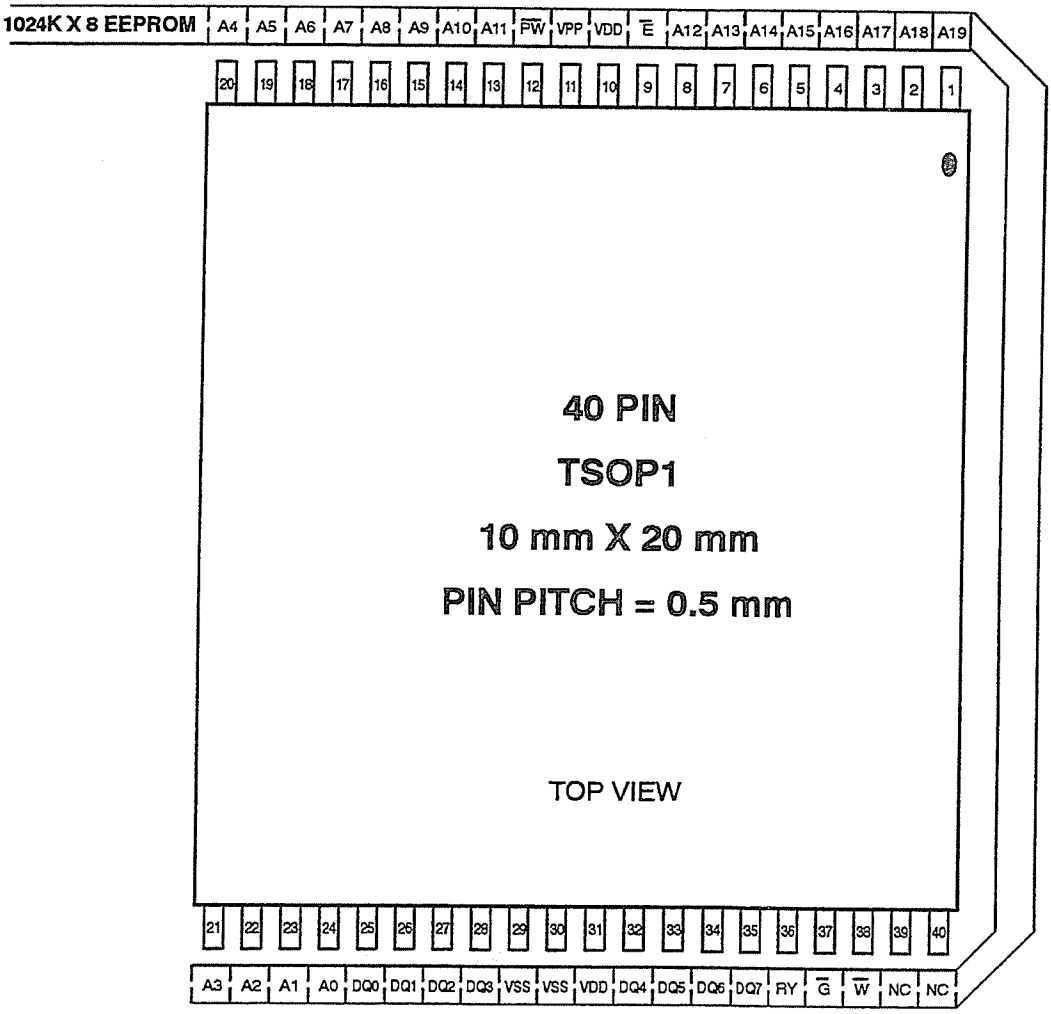


FIGURE 3.5.1-15

128K TO 512K BY 8 SINGLE-SUPPLY EEPROM FAMILY IN TSOP-1



* NOTE: The JEDEC Std. 30 term for the TSOP-1 package is PDSO-G.

FIGURE 3.5.1-16
1M BY 8 DUAL-SUPPLY EEPROM IN TSOP-1

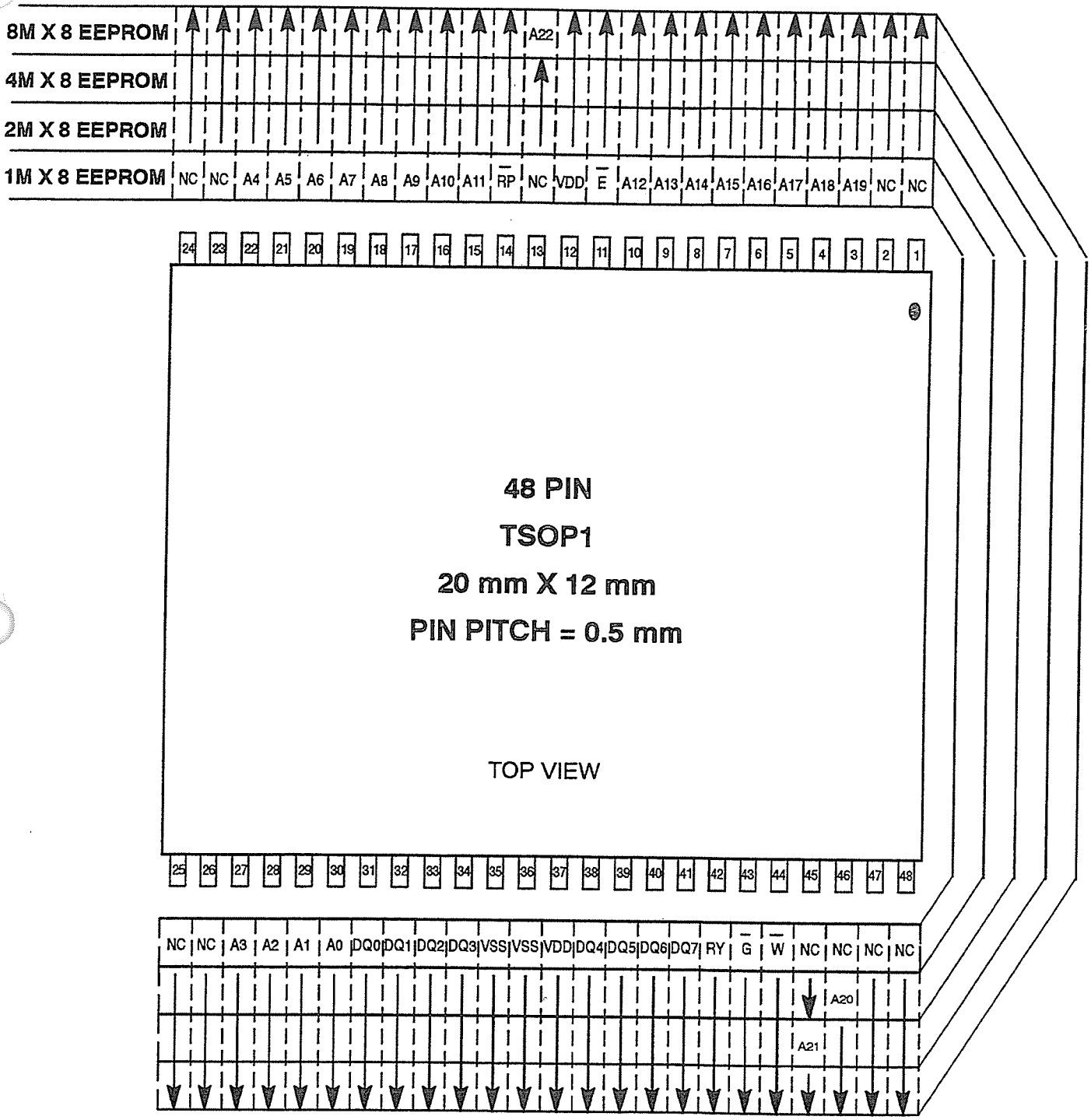


FIGURE 3.5.1-17

1M TO 8M BY 8 SINGLE-SUPPLY EEPROM FAMILY IN TSOP-1

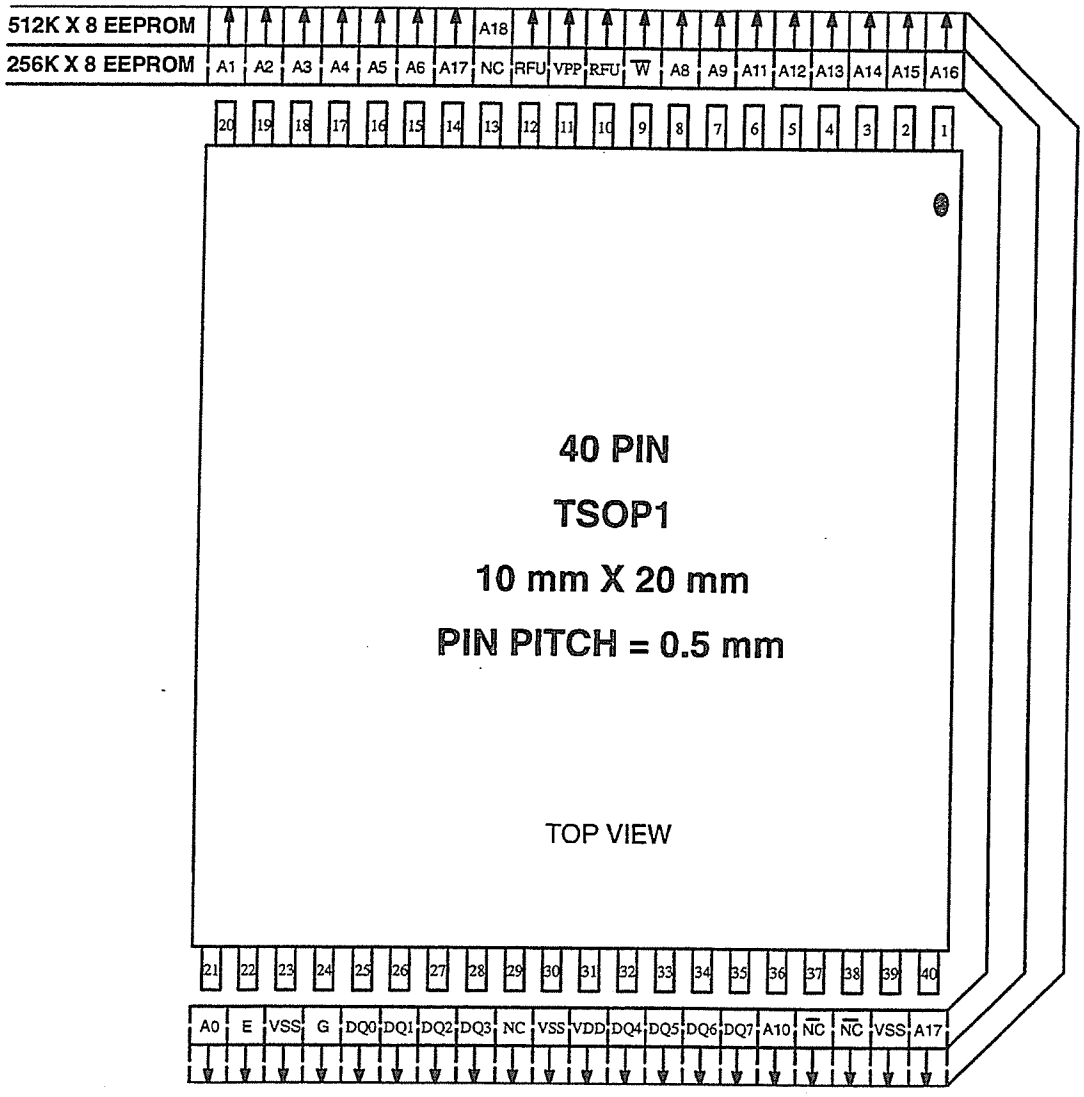
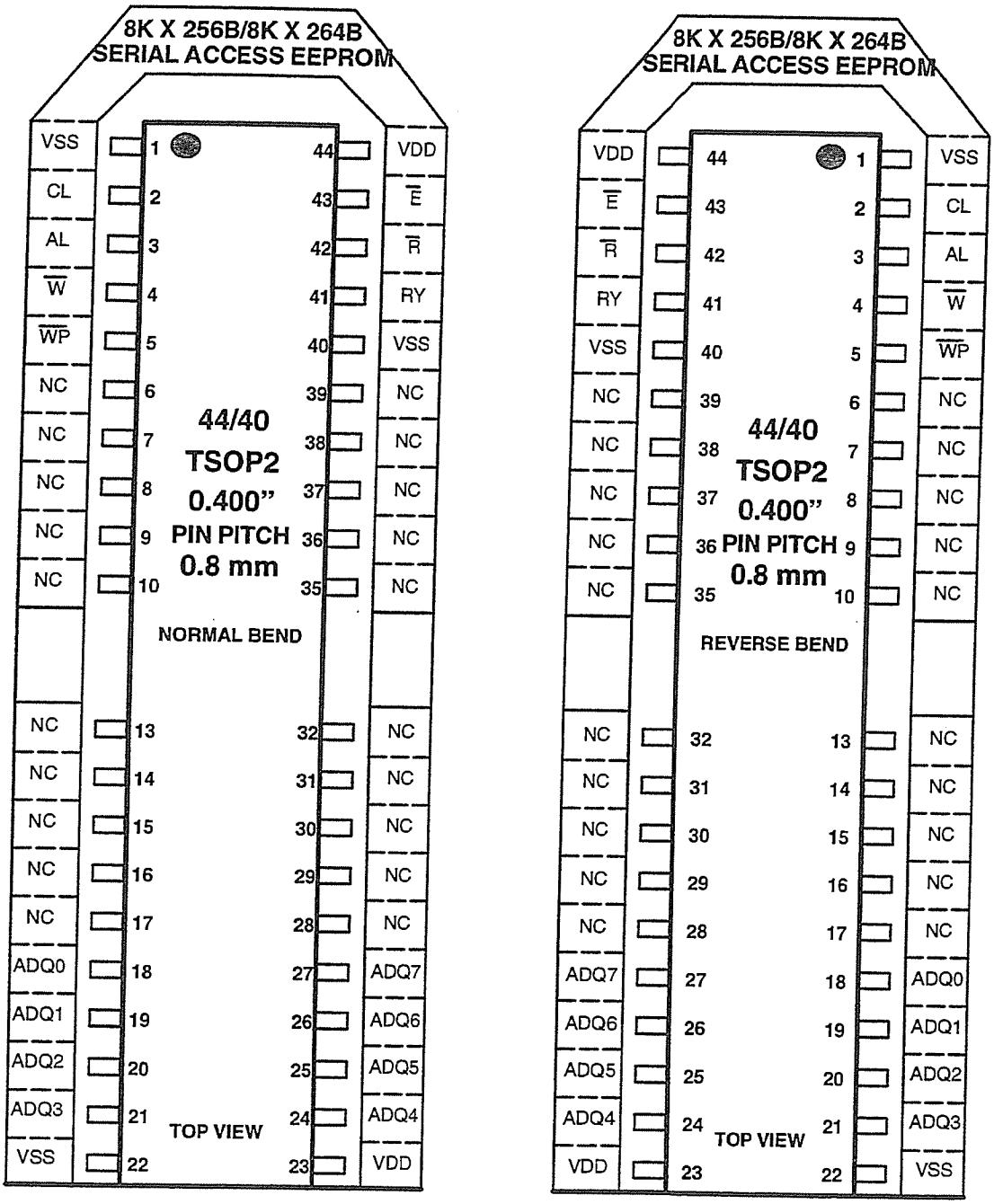


FIGURE 3.5.1–18
256K & 512K BY 8 DUAL SUPPLY EEPROM IN TSOP1

Release 6



The JEDEC Std. No 30 designator
for the TSOP2 package is PDSO–G

FIGURE 3.5.1–19 A
8K BY 256B or 8K BY 264B SERIAL ACCESS EEPROM IN TSOP2

Release 6

The following four tables define the logic and control functions required to make the Sequential Access EEPROM function properly

Sequential Access EEPROM Command Table

Function	First Cycle	Second Cycle	Acceptable Command when not ready
Serial Data Input	80h	None	No
Read Mode (264B)	00h	None	No
Read Mode 2 (8B)	50h	None	No
Reset	FFh	None	Yes
Auto Program	10h	None	No
Auto Block Erase	60h	D0h	No
Auto Multi–Block Erase	60h..60h	D0h	No
Suspend during Auto Multi–Block Erase	B0h	None	Yes
Register Read	E0h	None	No
Resume	D0h	None	No
Status Read	70h	None	Yes
ID Read	90h	None	No

Operation Mode During Read State

	CL	AL	$\overline{E}$	$\overline{W}$	$\overline{R}$	ADQ 0–7	Power
Read Mode	L	L	L	H	L	Data Output	Active
Output Deselect	L	L	L	H	H	High–Z	Active
Standby	L	L	H	H	·	High–Z	Standby

FIGURE 3.5.1–19 B
8K BY 256B or 8K BY 264B SERIAL ACCESS EEPROM COMMAND TABLE

Logic Table

Function	CL	AL	$\overline{E}$	$\overline{W}$	$\overline{R}$	$\overline{WP}$
Command Input	H	L	L	⌐‾⌐	H	·
Data Input	L	L	L	⌐‾⌐	H	·
Address Input	L	H	L	⌐‾⌐	H	·
Address Output	L	H	L	H	⌐‾⌐	·
Serial Read & Output	L	L	L	H	⌐‾⌐	·
During Auto Program	·	·	·	·	·	H
During Auto Erase	·	·	·	·	·	H
During Busy State	·	·	·	·	·	H
Program/Erase Protect	·	·	·	·	·	L

Serial Address Input

	ADQ0	ADQ1	ADQ2	ADQ3	ADQ4	ADQ5	ADQ6	ADQ7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	A12	A13	A14	A15
3rd Cycle	A16	A17	A18	A19	A20	RFU	RFU	RFU

A0 ⇒ A7 : Column Address
A8 ⇒ A11 : NAND Address
A12 ⇒ A20 : Block Address

PIN DEFINITIONS

The following pin terms are used in this device, but some may not appear in Sec. 2 on terminology of this Standard,

CL: Command Latch Enable
$\overline{E}$: Chip Enable
$\overline{R}$: Read Enable
RY: Ready
AL: Address Latch Enable
$\overline{W}$: Write Enable
$\overline{WP}$: Write Protect
ADQn: Address/Data/Command Multiplex

FIGURE 3.5.1–19 C
8K BY 256B or 8K BY 264B SERIAL ACCESS EEPROM LOGIC TABLE

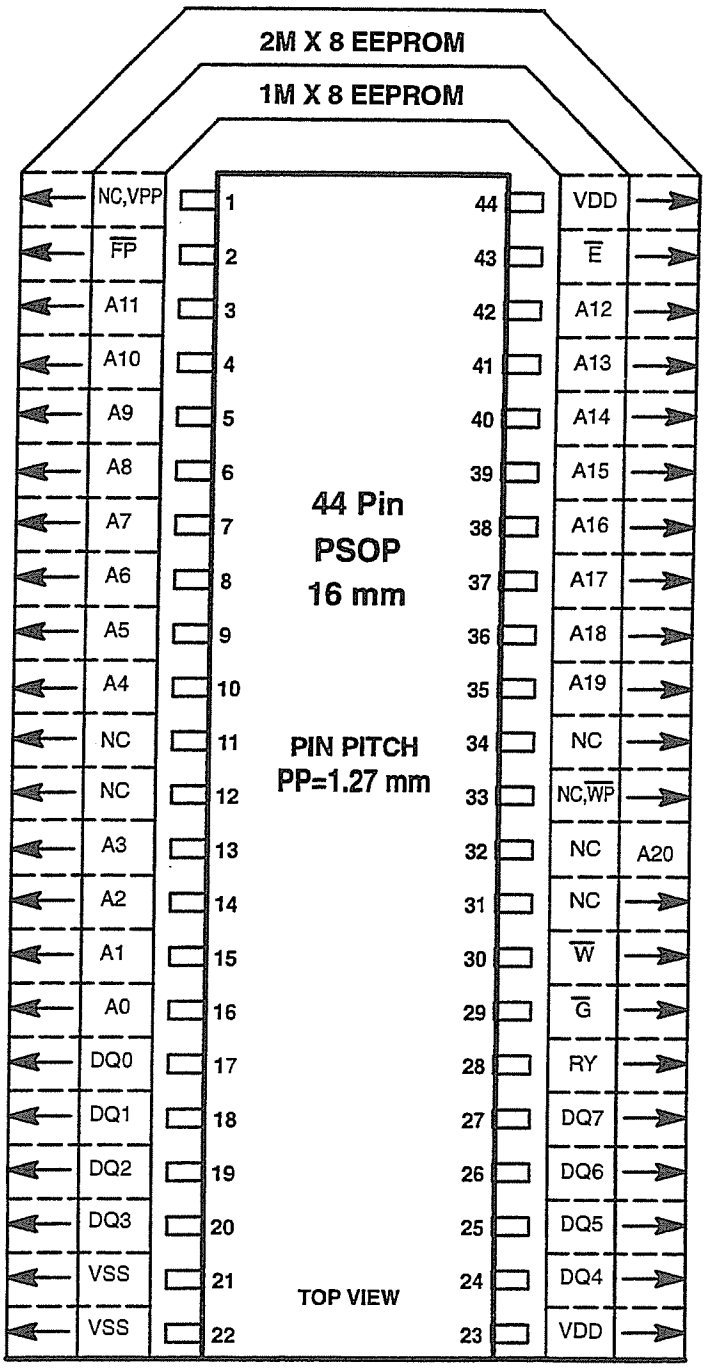


FIGURE FIGURE 3.5.1–20
1M & 2M BY 8 SINGLE OR DUAL SUPPLY EEPROM IN PSOP

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3.5.2 EEPROM, Word Wide

3.5.2.1 – 4K TO 32K BY 16 EEPROM IN DIP

CAPACITY—4K TO 32K WORDS OF 16 BITS,
PACKAGE—40 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Fig. 3.5.2–1

3.5.2.2 – 4K TO 256K BY 16 EEPROM IN SCC

CAPACITY—4K TO 256K WORDS OF 16 BITS,
PACKAGE—44 PAD (PIN) RCC, 0.650" X 0.650"
PIN ASSIGNMENTS—Fig. 3.5.2–2

3.5.2.3 – 256K TO 128M BY 16 EEPROM IN DIP AND SOP

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, 64M, and 128M WORDS OF 16 BITS
PACKAGE—44, 48 or 52 PIN DIP and SOP, 0.600" WIDE
PIN ASSIGNMENTS—256K TO 2M, Fig. 3.5.2–4
PIN ASSIGNMENTS—4M TO 128M, Fig. 3.5.2–3

3.5.2.4 – 1M TO 4M BY 16 DUAL SUPPLY EEPROM IN SSOP

CAPACITY—1M, 2M, 4M WORDS OF 16 BITS,
PACKAGE—56PIN SSOP, 13.5 mm WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENTS—Fig. 3.5.2–5

3.5.2.5 – 1M, 2M, & 4M DENSITY, BY 8 & 16 FEEPROM IN PSOP

CAPACITY—1M, 2M, & 4M, BITS WITH x8 OR x16 DATA INTERFACE.
—128K, 256K, OR 512K WORDS OF 8 BITS
—64K, 128, OR 256K WORDS OF 16 BITS
PACKAGE—44 PIN PSOP, 16 mm WIDE
PIN ASSIGNMENTS—Fig. 3.5.2–6
POWER SUPPLIES—SINGLE OR DUAL SUPPLY DESIGN

3.5.2.6 – 1M TO 32M DENSITY, BY 8 & 16 FEEPROM IN TSOP1

CAPACITY—1M, 2M, 4M, 8M, 16M, & 32M BITS WITH x8 OR x16 DATA INTERFACE.
—128K, 256K, 512K, 1M, 2M, OR 4M WORDS OF 8 BITS
—64K, 128, 256K, 512K, 1M, OR 2M WORDS OF 16 BITS
PACKAGE—44 PIN TSOP1, 20 mm X 16 mm with 0.5 mm PP.
PIN ASSIGNMENTS—Fig. 3.5.2–7
POWER SUPPLIES—SINGLE OR DUAL SUPPLY DESIGN

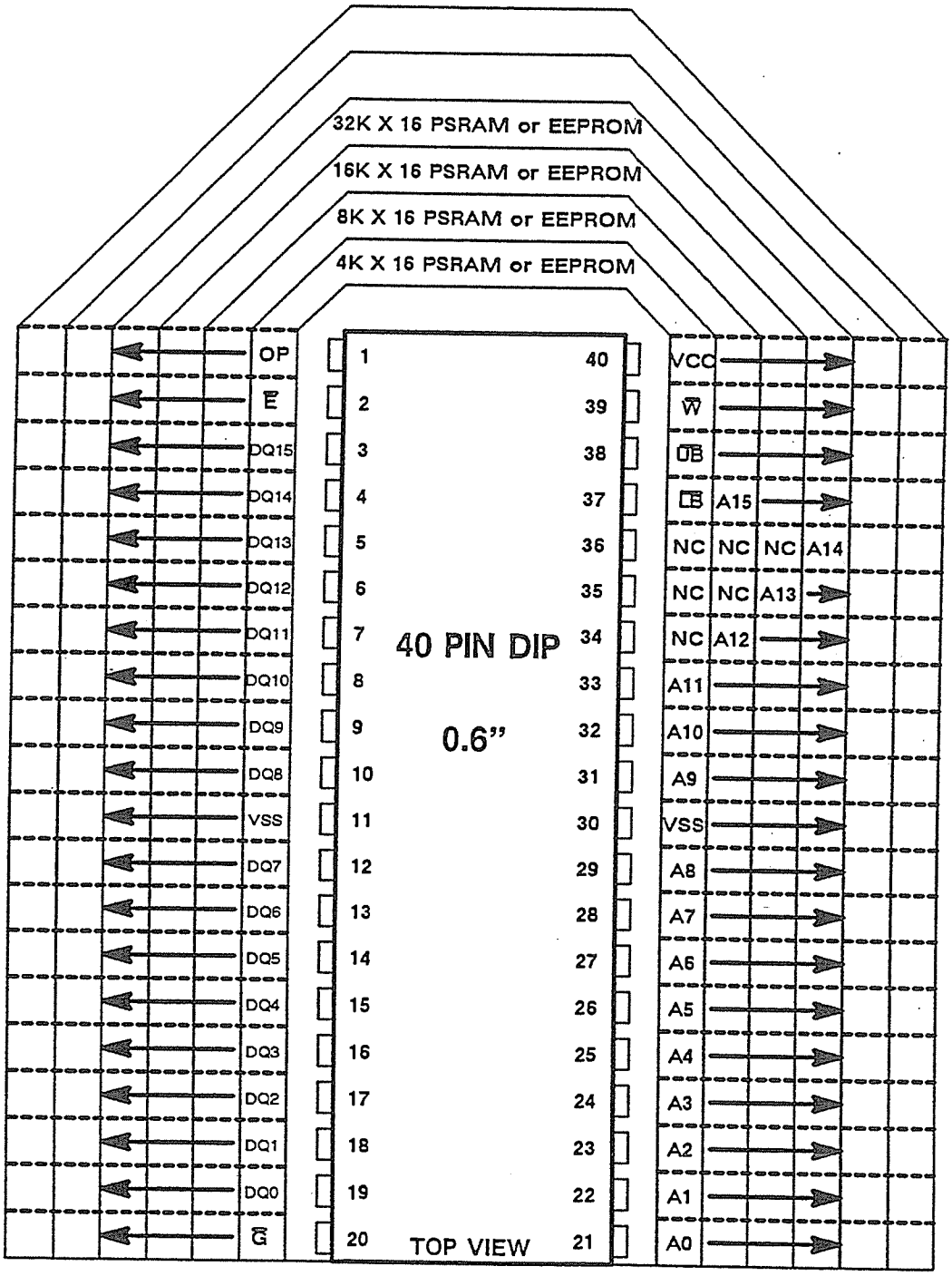


FIGURE 3.5.2-1
4K TO 32K BY 16 EEPROM FAMILY IN DIP

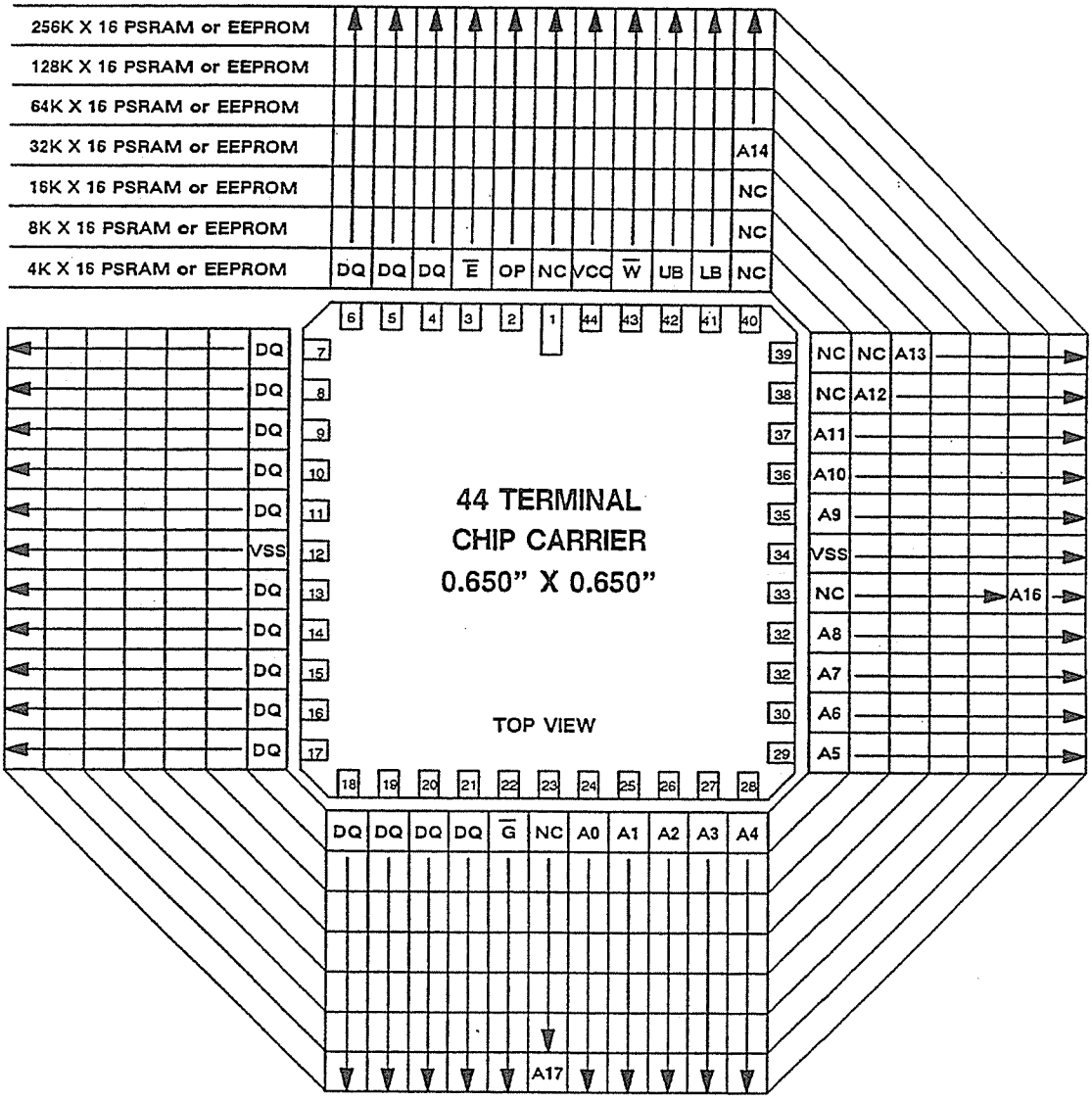
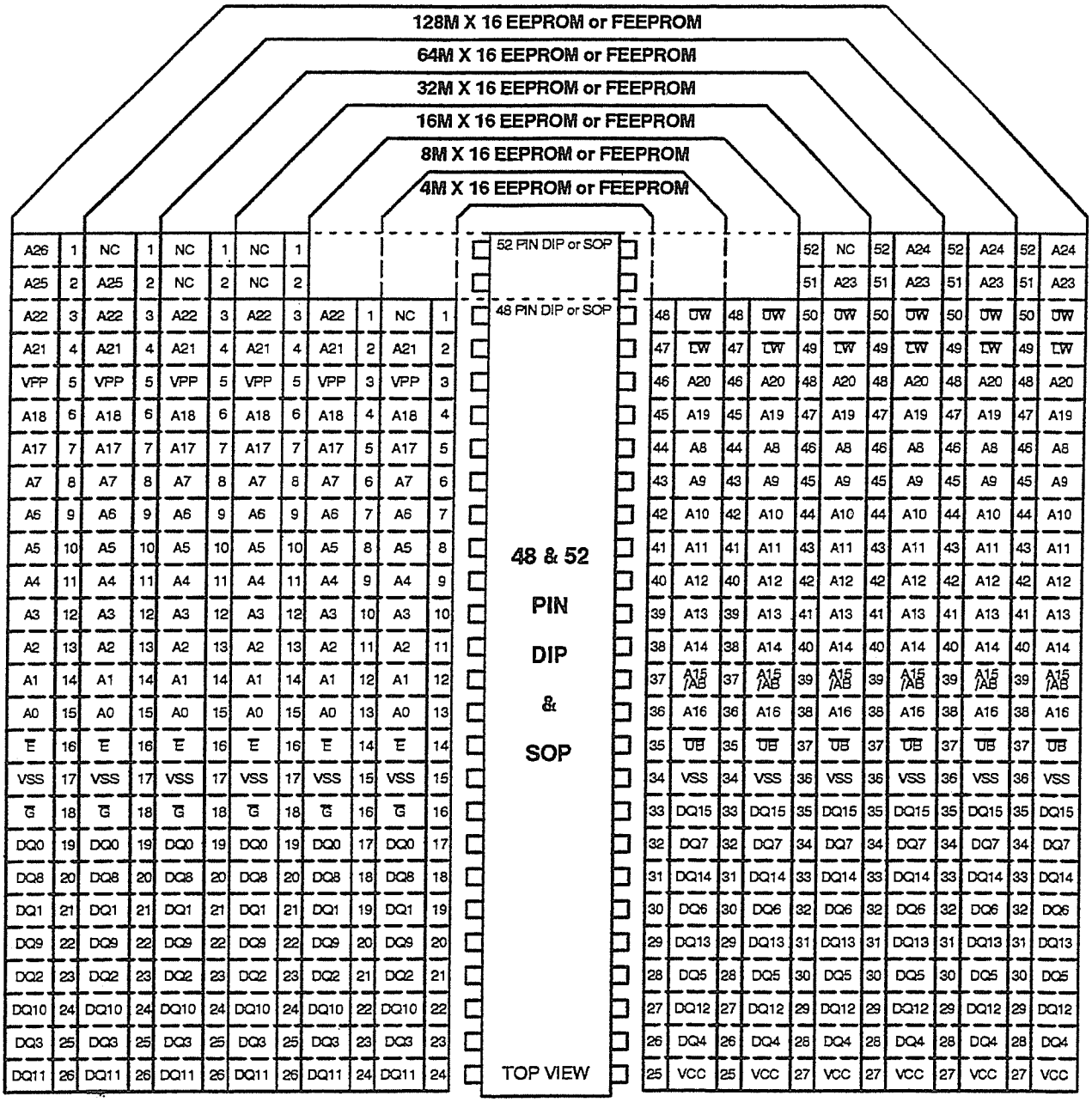
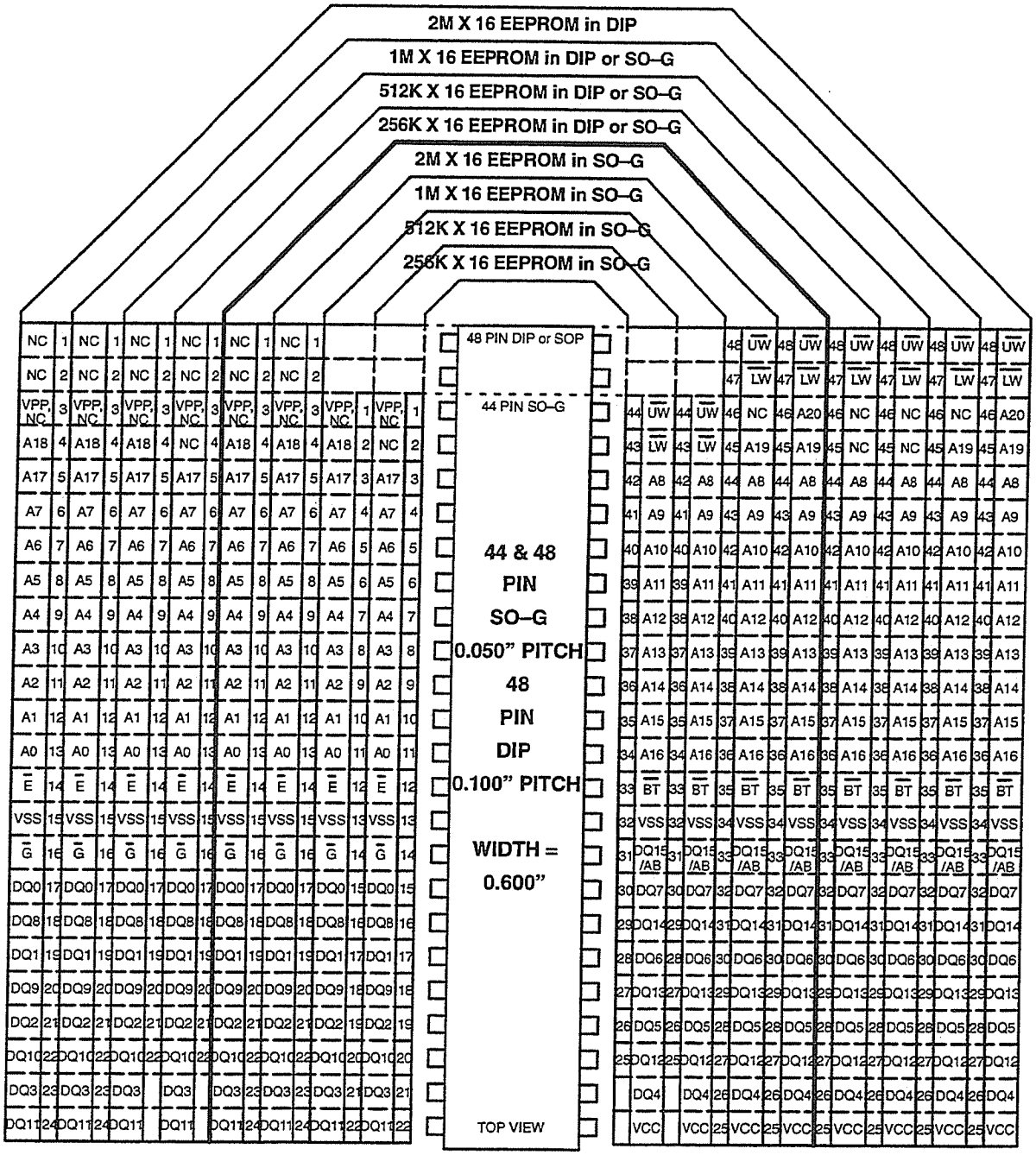


FIGURE 3.5.2-2
4K TO 256K BY 16 EEPROM FAMILY IN SCC



A26	1	NC	1	NC	1	NC	1																						
A25	2	A25	2	NC	2	NC	2																						
A22	3	A22	3	A22	3	A22	3	A22	1	NC	1																		
A21	4	A21	4	A21	4	A21	4	A21	2	A21	2																		
VPP	5	VPP	5	VPP	5	VPP	5	VPP	3	VPP	3																		
A18	6	A18	6	A18	6	A18	6	A18	4	A18	4																		
A17	7	A17	7	A17	7	A17	7	A17	5	A17	5																		
A7	8	A7	8	A7	8	A7	8	A7	6	A7	6																		
A6	9	A6	9	A6	9	A6	9	A6	7	A6	7																		
A5	10	A5	10	A5	10	A5	10	A5	8	A5	8																		
A4	11	A4	11	A4	11	A4	11	A4	9	A4	9																		
A3	12	A3	12	A3	12	A3	12	A3	10	A3	10																		
A2	13	A2	13	A2	13	A2	13	A2	11	A2	11																		
A1	14	A1	14	A1	14	A1	14	A1	12	A1	12																		
A0	15	A0	15	A0	15	A0	15	A0	13	A0	13																		
$\overline{E}$	16	$\overline{E}$	16	$\overline{E}$	16	$\overline{E}$	16	$\overline{E}$	14	$\overline{E}$	14																		
VSS	17	VSS	17	VSS	17	VSS	17	VSS	15	VSS	15																		
$\overline{G}$	18	$\overline{G}$	18	$\overline{G}$	18	$\overline{G}$	18	$\overline{G}$	16	$\overline{G}$	16																		
DQ0	19	DQ0	19	DQ0	19	DQ0	19	DQ0	17	DQ0	17																		
DQ8	20	DQ8	20	DQ8	20	DQ8	20	DQ8	18	DQ8	18																		
DQ1	21	DQ1	21	DQ1	21	DQ1	21	DQ1	19	DQ1	19																		
DQ9	22	DQ9	22	DQ9	22	DQ9	22	DQ9	20	DQ9	20																		
DQ2	23	DQ2	23	DQ2	23	DQ2	23	DQ2	21	DQ2	21																		
DQ10	24	DQ10	24	DQ10	24	DQ10	24	DQ10	22	DQ10	22																		
DQ3	25	DQ3	25	DQ3	25	DQ3	25	DQ3	23	DQ3	23																		
DQ11	26	DQ11	26	DQ11	26	DQ11	26	DQ11	24	DQ11	24																		
												48	$\overline{UW}$	48	$\overline{UW}$	50	$\overline{UW}$	50	$\overline{UW}$	50	$\overline{UW}$	50	$\overline{UW}$	50	$\overline{UW}$	50	$\overline{UW}$	50	$\overline{UW}$
												47	$\overline{LW}$	47	$\overline{LW}$	49	$\overline{LW}$	49	$\overline{LW}$	49	$\overline{LW}$	49	$\overline{LW}$	49	$\overline{LW}$	49	$\overline{LW}$	49	$\overline{LW}$
												46	A20	46	A20	48	A20	48	A20	48	A20	48	A20	48	A20	48	A20	48	A20
												45	A19	45	A19	47	A19	47	A19	47	A19	47	A19	47	A19	47	A19	47	A19
												44	A8	44	A8	46	A8	46	A8	46	A8	46	A8	46	A8	46	A8	46	A8
												43	A9	43	A9	45	A9	45	A9	45	A9	45	A9	45	A9	45	A9	45	A9
												42	A10	42	A10	44	A10	44	A10	44	A10	44	A10	44	A10	44	A10	44	A10
												41	A11	41	A11	43	A11	43	A11	43	A11	43	A11	43	A11	43	A11	43	A11
												40	A12	40	A12	42	A12	42	A12	42	A12	42	A12	42	A12	42	A12	42	A12
												39	A13	39	A13	41	A13	41	A13	41	A13	41	A13	41	A13	41	A13	41	A13
												38	A14	38	A14	40	A14	40	A14	40	A14	40	A14	40	A14	40	A14	40	A14
												37	A15 /AB	37	A15 /AB	39	A15 /AB	39	A15 /AB	39	A15 /AB	39	A15 /AB	39	A15 /AB	39	A15 /AB	39	A15 /AB
												36	A16	36	A16	38	A16	38	A16	38	A16	38	A16	38	A16	38	A16	38	A16
												35	$\overline{UB}$	35	$\overline{UB}$	37	$\overline{UB}$	37	$\overline{UB}$	37	$\overline{UB}$	37	$\overline{UB}$	37	$\overline{UB}$	37	$\overline{UB}$	37	$\overline{UB}$
												34	VSS	34	VSS	36	VSS	36	VSS	36	VSS	36	VSS	36	VSS	36	VSS	36	VSS
												33	DQ15	33	DQ15	35	DQ15	35	DQ15	35	DQ15	35	DQ15	35	DQ15	35	DQ15	35	DQ15
												32	DQ7	32	DQ7	34	DQ7	34	DQ7	34	DQ7	34	DQ7	34	DQ7	34	DQ7	34	DQ7
												31	DQ14	31	DQ14	33	DQ14	33	DQ14	33	DQ14	33	DQ14	33	DQ14	33	DQ14	33	DQ14
												30	DQ6	30	DQ6	32	DQ6	32	DQ6	32	DQ6	32	DQ6	32	DQ6	32	DQ6	32	DQ6
												29	DQ13	29	DQ13	31	DQ13	31	DQ13	31	DQ13	31	DQ13	31	DQ13	31	DQ13	31	DQ13
												28	DQ5	28	DQ5	30	DQ5	30	DQ5	30	DQ5	30	DQ5	30	DQ5	30	DQ5	30	DQ5
												27	DQ12	27	DQ12	29	DQ12	29	DQ12	29	DQ12	29	DQ12	29	DQ12	29	DQ12	29	DQ12
												26	DQ4	26	DQ4	28	DQ4	28	DQ4	28	DQ4	28	DQ4	28	DQ4	28	DQ4	28	DQ4
												25	VCC	25	VCC	27	VCC	27	VCC	27	VCC	27	VCC	27	VCC	27	VCC	27	VCC
																52	NC	52	A24	52	A24	52	A24						
																51	A23	51	A23	51	A23	51	A23						

FIGURE 3.5.2–3
4M TO 128M BY 16 EEPROM AND FEEPROM IN DIP AND SOP



AB: ADDRESS INPUT, UPPER/LOWER BYTE SELECT
BT: BYTE MODE ENABLE

FIGURE 3.5.2–4
256K TO 2M BY 16 EEPROM IN DIP AND SO–G

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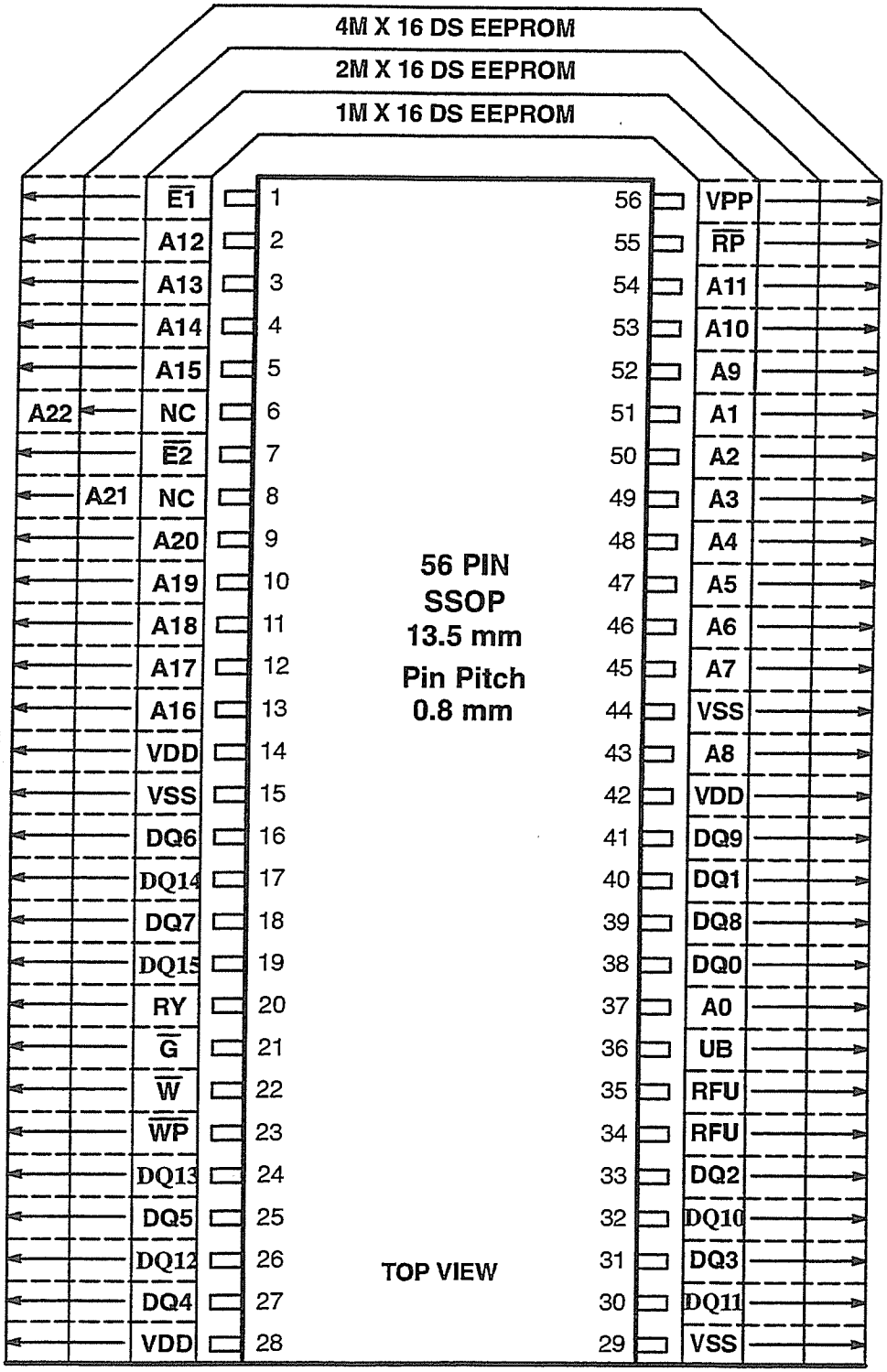


	UB	A0	DQ0 ⇒ DQ7	DQ8 ⇒ DQ15
Word Access	VIH	X	Even Byte	Odd Byte
Odd Byte Access	VIL	VIH	Odd Byte	High Z
Even Byte Access	VIL	VIL	Even Byte	High Z

FIGURE 3.5.2–5
1M TO 4M BY 16 DUAL SUPPLY EEPROM IN SOP

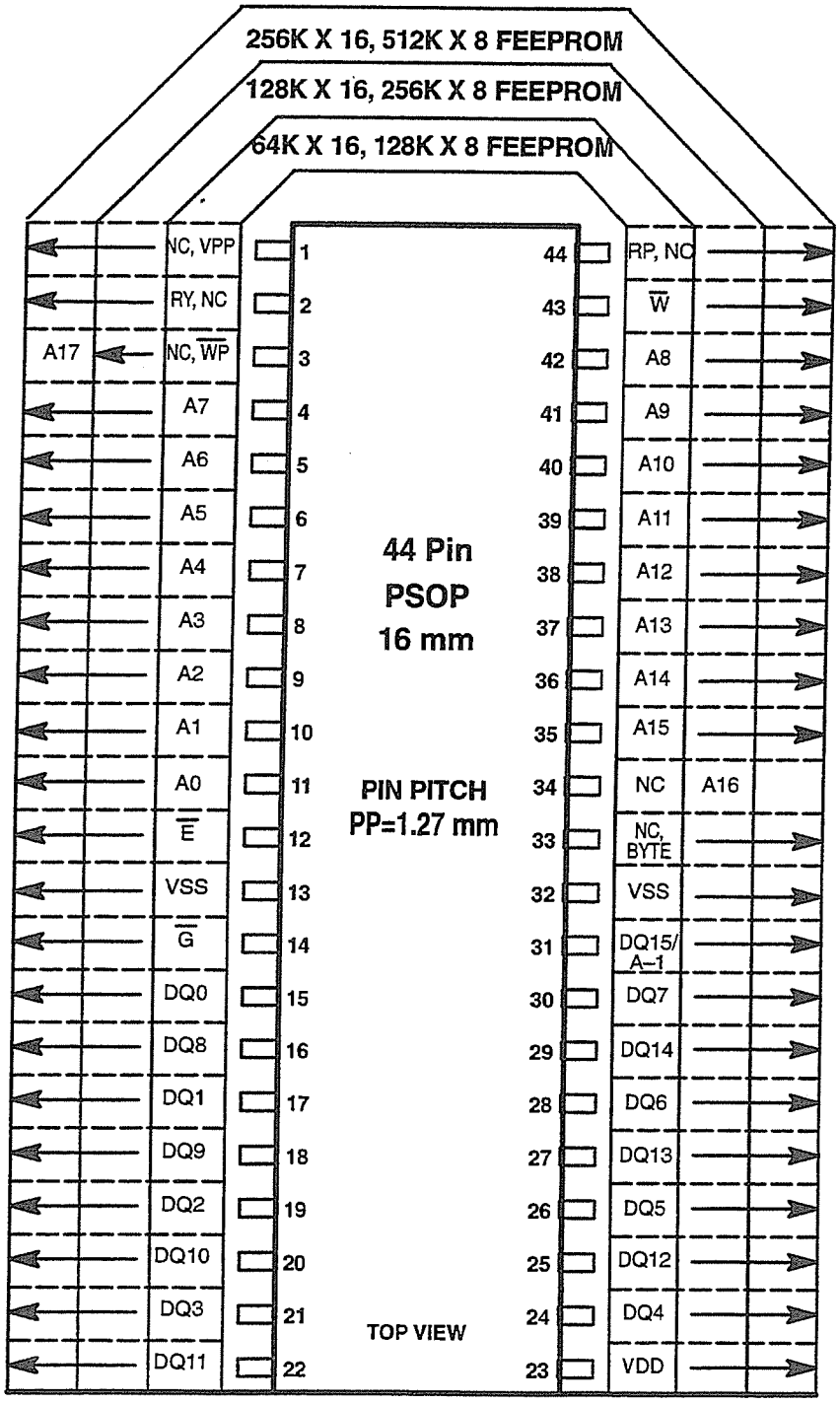
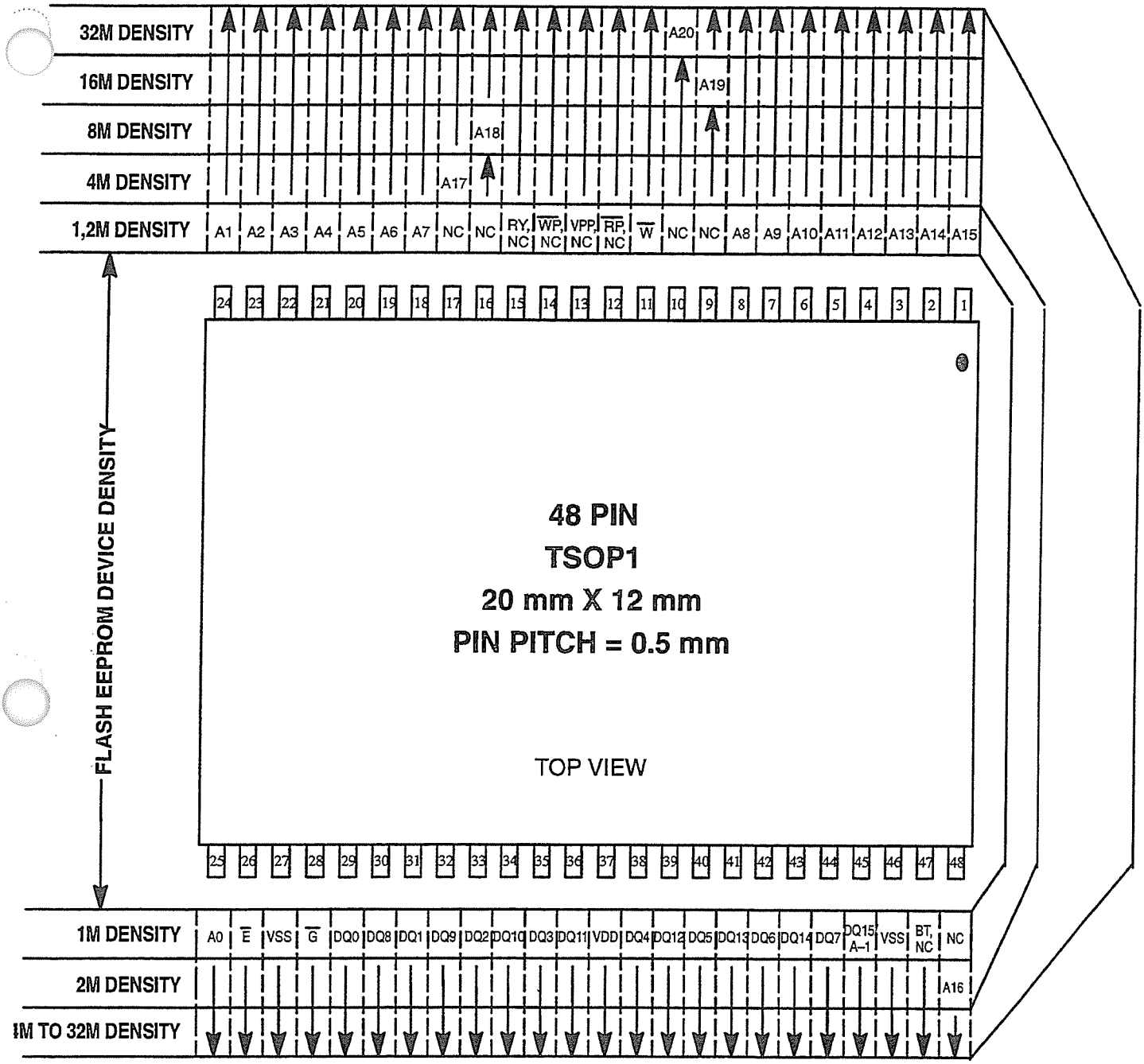


FIGURE 3.5.2–6
1M, 2M, & 4M DENSITY BY 8 & 16 SINGLE OR DUAL SUPPLY FEEPROM IN PSOP, 128K TO 512K BY 8 OR 64K TO 256K BY 16



ORGANIZATION VS. DENSITY TABLE

DENSITY	X16	X8
1Mb	64K X 16,	128K X 8
2Mb	128K X 16	256K X 8
4Mb	256K X 16	512K X 8
8Mb	512K X 16	1M X 8
16Mb	1M X 16	2M X 8
32Mb	2M X 16	4M X 8

FIGURE 3.5.2–7
1M TO 32M DENSITY BY 8 & 16 SINGLE OR DUAL SUPPLY FEEPROM IN TSOP1, 64K TO 2M BY 16 OR 128K TO 4M BY 8

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3.5.3 EEPROM EXTENDED FEATURES

There are a number of extended feature standards for EEPROMS that depend on the capacity and number of power supplies used in the design. The various standards and their location are listed as follows:

– 32K X 8 BIT EEPROM EXTENDED FEATURE STANDARDS. PP 3.5.1–15 to 22

– DUAL POWER SUPPLY EEPROM COMMAND SET. Fig. 3.5.3.2, P 3.5.3–13

– EXTENDED FEATURE SET FOR EEPROM (256Kb and larger) . Sec. 3.5.3.1 following

– SINGLE POWER SUPPLY EEPROM COMMAND CODES. SEC. 3.5.3.3

– EEPROM TOGGLE BIT FEATURE (larger than 256 Kb) . Sec. 3.5.3.4

3.5.3.1 – EXTENDED FEATURE SET FOR EEPROM (256Kb and larger)

This standard specifies features beyond the existing pinout standards that need to be standardized for EEPROMs to achieve operational compatibility. A summary of the required and optional features is listed below. The full standard follows the pinout drawings at the end of Sec. 3.5.3.2

3.5.3.1.1 – REQUIRED STANDARD FEATURES

The following features are the minimum set necessary to achieve functional compatibility for 256Kb and larger EEPROMs and must be implemented to be in compliance with this standard:
–Operate with a primary power supply of 5.0 V and lower nominal
–Operate in conformance with the defines standard command set
–Operate in conformance with the standard truth table
–Have read and write timing cycles which are consistent with the standard timing diagrams
–Contain Data & Address Latches for Write cycles
–Operate with self timed write cycles
–Operate with input levels between 0 and 5 Volts.
–DATA\ Polling

3.5.3.1.2 – OPTIONAL FEATURES

The following features are optional and are not required for the part to conform to this standard. If any of these features are implemented, they must operate as defined in order to maintain compatibility and to be in compliance with this standard:
–Page Write Mode with standard write cycle timings
–Minimum page size of 16 Byte in page write mode
–Software Data Protect Option
–Hardware Mass Erase (All 1's)
–Software Mass Erase (All 1's)

3.5.3.2 – OPTIONAL COMMAND SET FOR DUAL–SUPPLY EEPROM

This Standard provides an optional command set for DUAL–SUPPLY EEPROM devices. This set includes the existing algorithmic commands and adds a series of automatic codes. A component may respond to either or both of the operating modes. The COMMAND SET TRUTH TABLE is shown in Figure 3.5.1–11

3.5.3.3 – SINGLE POWER SUPPLY EEPROM COMMAND CODES

These tables define the three cycle and 6 cycle comand codes for SINGLE SUPPLY EEPROMs with capacities greater than 256 Kb.

3.5.3.4 – EEPROM TOGGLE BIT FEATURE

This standard is applicable to devices with a capacity greater than 256 Kb, with both single and dual power supplies. The Toggle Bit feature is used to determine if a Write Cycle (either Erase, Program, or both) is in progress in the EEPROM or if the part is available for reading or another write cycle.

EEPROM EXTENDED FEATURE STANDARD (256Kb and greater)

The mandatory features, which are the minimum set necessary to achieve functional compability for 256Kb and larger EEPROMs, must be implemented to be in compliance with this standard. Any, all, or none of the optional features may be implemented at the manufacturers discretion. However, if an optional feature defined in this standard is implemented, it must operate as specified in this standard to be in compliance with the standard.

Other features not described in the standard may be incorporated and the device still be in compliance as long as they are compatible with the required and optional features in this standard.

BYTEWIDE EEPROM REQUIRED STANDARD FEATURES (256Kb and larger)

1. VDD SUPPLY IS 5 V OR LESS NOMINAL
2. STANDARD LOGIC TRUTH TABLE (FIG. A1–1)
3. STANDARD COMMAND SET (Fig. A1–2)
4. STANDARD READ CYCLE TIMING (FIG. A1–3)
5. STANDARD BYTE WRITE CYCLE FEATURES
   –TIMING (FIG. A1–4)
   –DATA AND ADDRESS LATCHES
   –SELF–TIMED WRITE CYCLES
   –ALL INPUT LEVELS IN RANGE BETWEEN 0 V AND 5 V.
6. DATA POLLING (FIG. A1–5)
   MUST MEET NORMAL READ CYCLE AND WRITE CYCLE TIMING

OPTIONAL FEATURES

1. PAGE WRITE MODE (FIG. A1–6)
   –STANDARD PAGE WRITE CYCLE TIMING
   –16 BYTE MINIMUM PAGE SIZE (A0 – A3)
2. SOFTWARE DATA PROTECT OPTION (FIGS. A1–7 & A1–8)
3. HARDWARE MASS ERASE (ALL 1'S) (FIG. A1–9)
4. SOFTWARE MASS ERASE (ALL 1'S) (FIG. A1–10)

EEPROM TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
L	L	H	READ	Q	ACTIVE
L	H	L	WRITE	D	ACTIVE
H	X	X	STANDBY AND WRITE INHIBIT	HIGH Z	STANDBY
L	L	L	WRITE INHIBIT	HIGH Z	ACTIVE
L	H	H	WRITE INHIBIT	HIGH Z	ACTIVE

~NOTE: $\overline{G}$ functions as both an output control and a write Inhibit control in this EEPROM Standard.

FIGURE A1–1

SINGLE–SUPPLY EEPROM COMMAND SET

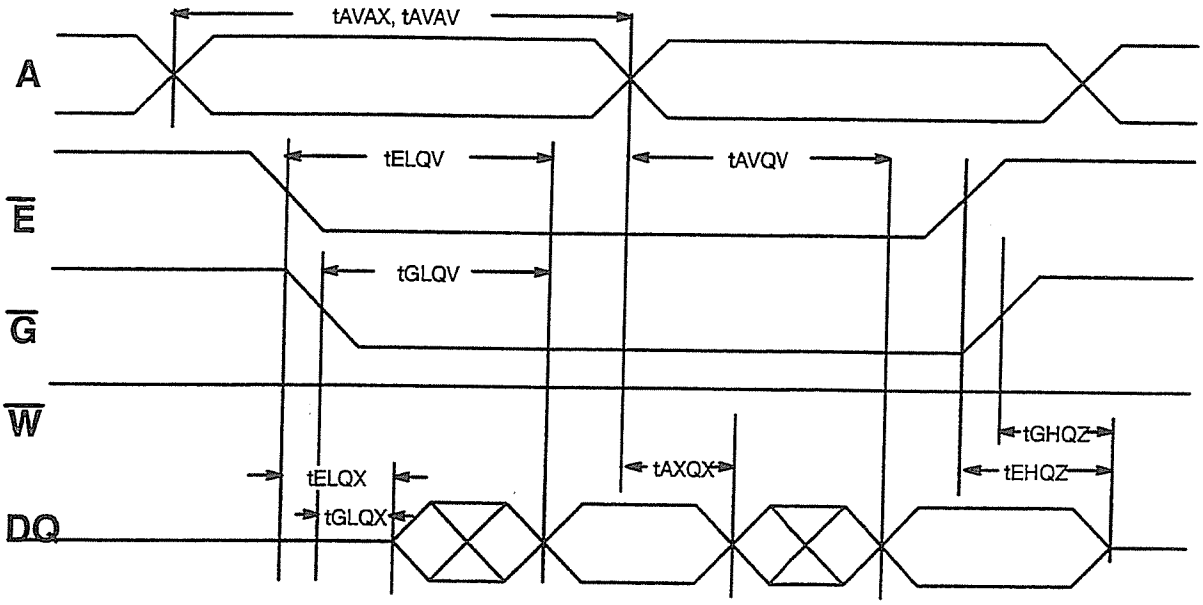
Bus Command Table

Command Sequence Read/Reset	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXH	FOH										
Rearl/Reset	4	5555H	AAH	2AAAH	55H	5555H	FOH	RA	RD				
Autoselect	4	5555H	AAH	2AMH	55H	5555H	90H						
Fyte Program	4	5555H	AAH	2AMH	55H	5555H	AOH	PA	Data				
Chip Erase	6	5555H	AAH	2AMH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	1OH
Sector Erase	6	5555H	AAH	2AMH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (don~t rare), Data (BOH)											
Sector Erase Resume		Erase can be resumed after suspend with Addr (don~t care), Data (30H)											

Note: A0 is always LSB regardless of data width.

FIGURE A1–2

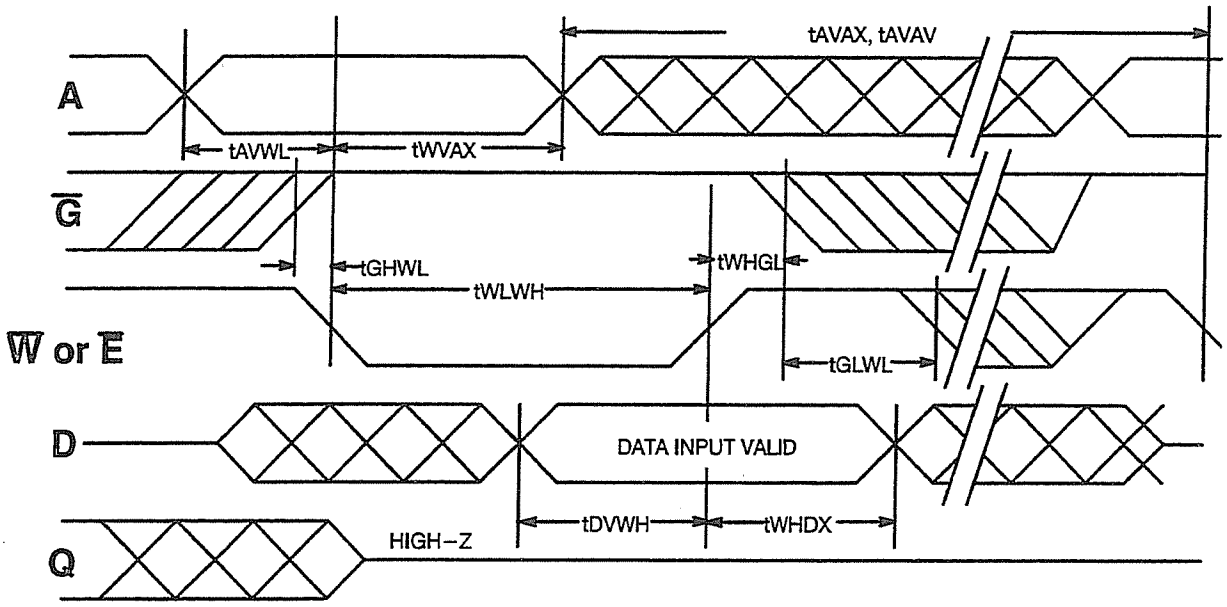
SINGLE SUPPLY EEPROM READ CYCLE TIMING



SYMBOL	DESCRIPTION
tAVAX, tAVAV	ADDRESS VALID TO ADDRESS CHANGE (READ CYCLE TIME)
tELQV	$\overline{E}$ LOW TO OUTPUT VALID (CHIP ENABLE ACCESS TIME)
tAVQV	ADDRESS VALID TO OUTPUT VALID (ADDRESS ACCESS TIME) tGLQV
tELQX	$\overline{E}$ LOW TO ACTIVE OUTPUT
tGLQX	$\overline{G}$ LOW TO ACTIVE OUTPUT
tEHQZ	$\overline{E}$ HIGH TO HIGH–Z OUTPUT
tGHQZ	$\overline{G}$ HIGH TO HIGH–Z OUTPUT
tAXQX	ADDRESS INVALID TO DATA OUT INVALID

FIGURE A1–3

SINGLE SUPPLY EEPROM READ CYCLE TIMING



SYMBOL (NOTE 1)	DESCRIPTION
tWLWL, tELEL	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW CYCLE TIME (WRIITE CYCLE TIME)
tAVWL, tAVEL	ADDRESS VALID TO $\overline{W}$ OR $\overline{E}$ LOW TIME (ADDRESS SETUP TIME)
tWLAX, tELAX	$\overline{W}$ OR $\overline{E}$ LOW TO ADDRESS INVALID (ADDRESS HOLD TIME)
tGHWL, tGHEL	$\overline{G}$ HIGH TO $\overline{W}$ OR $\overline{E}$ LOW TIME
tWHGL, tEHGL	$\overline{G}$ HIGH HOLD TIME FROM $\overline{W}$ OR $\overline{E}$ HIGH
tWLWH, tELEH	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ HIGH (WRITE PULSE DURATION)
tGLWL, tGLEL	$\overline{G}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW ($\overline{G}$ LOW WRITE INHIBIT SETUP TIME)
tDVWH, tDVEH	DATA INPUT VALID TO $\overline{W}$ OR $\overline{E}$ HIGH (DATA SET–UP TIME)
tWHDX, tEHDX	$\overline{W}$ OR $\overline{E}$ HIGH TO DATA INPUT INVALID (DATA HOLD TIME)

FIGURE A1–4

SINGLE SUPPLY EEPROM DATA BAR POLLING AND AUTOMATIC WRITE OPERATION STATUS

IN PROGRESS	AUTO PROGRAMMING	DQ7	TOGGLE	0	0	0	RFU
	PROGRAMMING IN AUTO–ERASE	0	TOGGLE	0	0	1	
	ERASING IN AUTO–ERASE	0	TOGGLE	0	1	1	
EXCEEDED TIME LIMITS	AUTO PROGRAMMING	DQ7	TOGGLE	1	0	0	RFU
	PROGRAMMING IN AUTO–ERASE	0	TOGGLE	1	0	1	
	ERASING IN AUTO–ERASE	0	TOGGLE	1	1	1	

FIGURE A1–5

Definition of Automatic Algorithm

Automated Write
Data Command = 10h/ Byte Address and Data (1st/2nd bus cycle)

Write the automated program set–up command (10h) and program command (Byte address and program data). The device automatically times the program pulse width, provides the program verify to guarantee adequate data retention, and counts the number of pulses required for complete programming.

A data polling status bit (output pin DQ7) and a toggle bit status (output pin DQ6) provide feedback to the system as to the status of the programming operation. Either DQ7 or DQ6 can be used.

Data Polling– DQ7

While the automated algorithms are in operation, an attempt to read the device (address = don't care) will produce the compliment of the intended valid program or erase data on DQ7. Upon completion of the automated algorithm, an attempt to read the device will produce the valid data expected from DQ7.

The data polling feature is valid after the rising edge of the second W pulse of the two write pulse sequence.

Toggle Bit– DQ6

While the automated algorithms are in progress, successive attempts to read data (address = don't care) from the device will result in DQ6 toggling between the logic levels "1" and "O". Once the automated operation is complete, DQ6 will stop toggling and valid data will be read.

The toggle bit is valid after the rising edge of the first W pulse of the two write pulse sequence, unlike data polling which is valid after the rising edge of the second W pulse. This

feature allows the user to determine if the device is partially through the two write pulse sequence.

Exceeded Timing Limits – DQ5

DQ5 will indicate if the program or erase pulse counts have exceeded the specified limits. Under this condition, DQ5 will provide a logic "1 " output.

Hardware Sequence Flash – DQ4

If the device has exceeded the specified erase or program time and DQ5 is at logic level "1", then DQ4 will indicate which step in the algorithm the device exceeded limits. A logic level "O" in DQ4 indicates that the programming limits were exceeded. A logic level "1" indicates erase limits were exceeded.

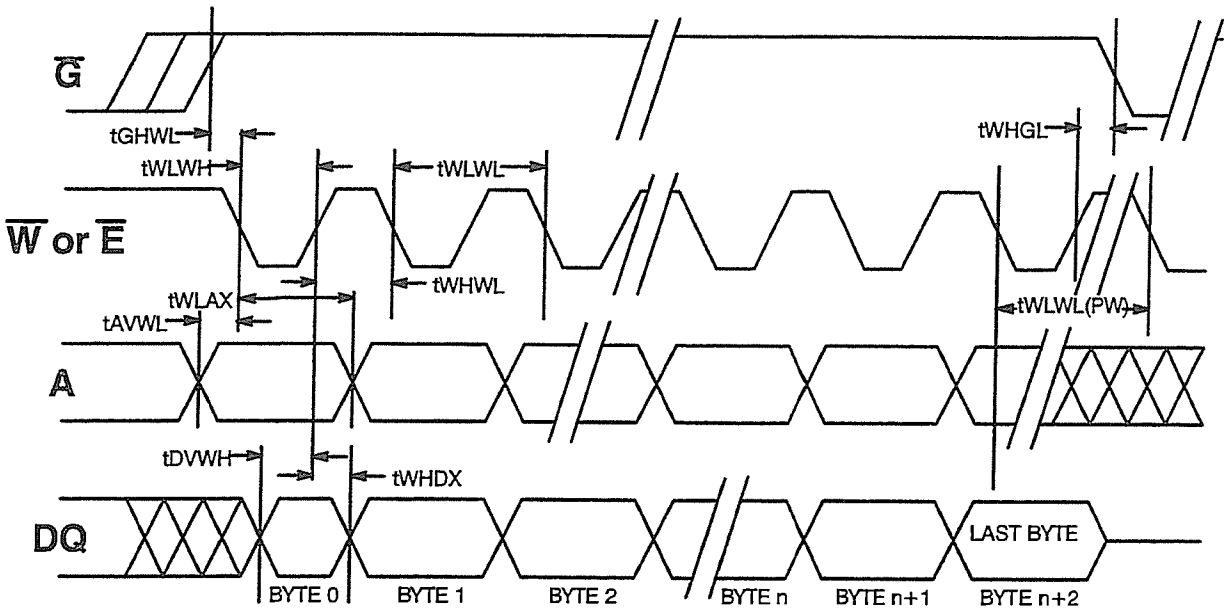
Sector Erase Timer– DQ3

After the compietion of the initial sector erase command sequence, the sector erase time–out of 100μs will begin. If another sector erase command is written within the 100μs time–out window, the timer is reset.

If Data Polling or the Toggle bit (DQ6) indicates that the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is at logic level "1" the intemally controlled erase cycle has begun. Any further attempts to write subsequent commands to the device will be ignored untilthe erase operation is completed which is indicated by Data Polling or the Toggle bit. If DQ3 is at logic level "0", the device will accept additional sector erase commands.

DQ0–DQ2 are reserved for future use.

SINGLE SUPPLY EEPROM PAGE MODE WRITE CYCLE TIMING



SYMBOL (NOTE 1)	DESCRIPTION
tWLWL(PW)	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW CYCLE TIME (PAGE WRIITE CYCLE TIME)
tAVWL, tAVEL	ADDRESS VALID TO $\overline{W}$ OR $\overline{E}$ LOW TIME (ADDRESS SETUP TIME)
tWLAX, tELAX	$\overline{W}$ OR $\overline{E}$ LOW TO ADDRESS INVALID (ADDRESS HOLD TIME)
tGHWL, tGHEL	$\overline{G}$ HIGH TO $\overline{W}$ OR $\overline{E}$ LOW TIME
tWHGL, tEHGL	$\overline{G}$ HIGH HOLD TIME FROM $\overline{W}$ OR $\overline{E}$ HIGH
tWLWH, tELEH	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ HIGH (WRITE PULSE DURATION)
tDVWH, tDVEH	DATA INPUT VALID TO $\overline{W}$ OR $\overline{E}$ HIGH (DATA SET–UP TIME)
tWHDX, tEHDX	$\overline{W}$ OR $\overline{E}$ HIGH TO DATA INPUT INVALID (DATA HOLD TIME)
tWLWL, tELEL	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW (BYTE LOAD CYCLE TIME)

FIGURE A1–6

SINGLE SUPPLY EEPROM OPTIONAL SOFTWARE DATA PROTECTION

–SOFTWARE DATA PROTECTION IS A DIFFERENT METHOD OF PREVENTING INADVERTANT WRITE OPERATIONS IN A NONVOLATILE MEMORY COMPARED TO THE "HARDWAREU METHODS, SUCH AS: E, G, AND W LOGIC COMBINATIONS, VCC LEVEL DETECTORS, AND POWER UP TIMERS.

–A SPECIFIC DATA AND ADDRESS SOFTWARE SEQUENCE MUST BE ISSUED TO ENABLE A SINGLE PAGE OR BYTE WRITE.

–DATA INPUT FORMAT: D7/D6/D5/D4/D3/D2/D1/D0

–ADDRESS FORMAT: A14/A13/A12/A11/A10/A9/A8/A7/A6/A5/A4/A3/A2/A1/A0

STEP	MODE	A14–A0	DQ7–DQ0
1	"ACCESS WRITE"	5555H	AAH
2	"ACCESS WRITE"	2AAAH	55H
3	"ACCESS WRITE"	5555H	A0H
4	"PAGE WRITE"	Address	Data

–ALL WRITES MUST CONFORM TO THE PAGE MODE TIMING REQUIREMENTS FOR THE PART.

–SINCE THE PAGE ADDRESS IS CHANGED (A VIOLATION OF THE NORMAL PAGE MODE WRITE CYCLE), THE FIRST THREE "ACCESS" WRITES (STEPS 1–3) ARE USED ONLY FOR SOFTWARE ACCESS, NO DATA IS ACTUALLY WRITTEN TO THE EEPROM.

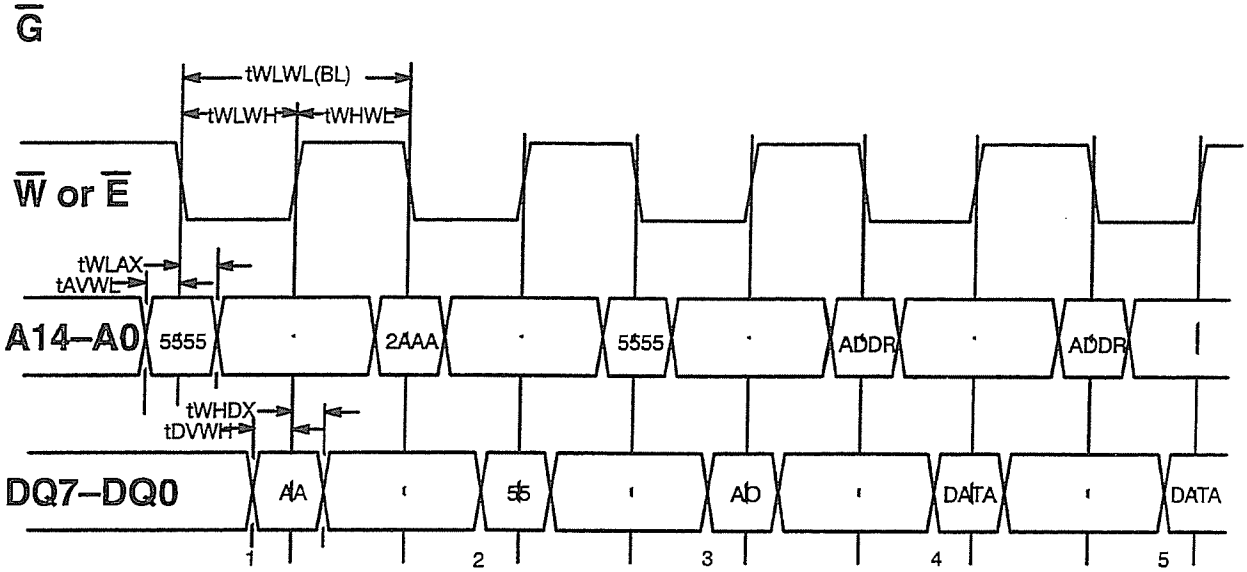
–THE FIRST TIME THIS SEQUENCE IS APPLIED TO THE PART A NON–VOLATILE BIT IS SET, WHICH RECONFIGURES THE PART FROM HARDWARE PROTECTED ONLY TO HARDWARE AND SOFTWARE SEQUENCE PROTECTED. ONCE THIS BIT IS SET, THE SOFTWARE SEQUENCE MUST BE USED TO WRITE TO THE PART.

–THE SOFTWARE PROTECTION CAN BE DISABLED AND THE PART RECONFIGURED TO HARDWARE–ONLY PROTECTION, BY APPLYING THE SIX STEP SOFTWARE SEQUENCE BELOW:

STEP	MODE	A14–A0	DQ7–DQ0
1	"ACCESS" WRITE	5555H	AAH
2	"ACCESS" WRITE	2AAAH	55H
3	"ACCESS" WRITE	5555H	80H
4	"ACCESS" WRITE	5555H	AAH
5	"ACCESS" WRITE	2AAAH	55H
6	"ACCESS" WRITE	5555H	20H

FIGURE A1–7

SINGLE SUPPLY EEPROM SOFTWARE DATA PROTECTION TIMING



NOTE 5: Software Data Protection Timings are referenced to $\overline{W}$ or $\overline{E}$ Inputs, whichever is last going LOW, and the $\overline{W}$ or $\overline{E}$ Inputs, whichever is first going HIGH.

SYMBOL (NOTE 5)	DESCRIPTION
tWLWL(BL), tELEL(BL)	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW BYTE LOW CYCLE TIME
tWLWH, tELEH	$\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ HIGH (WRITE PULSE DURATION)
tWHWL, tEHEL	$\overline{W}$ OR $\overline{E}$ HIGH TO $\overline{W}$ OR $\overline{E}$ LOW TIME (WRITE HIGH RECOVERY)
tAVWL tAVEL	ADDRESS VALID TO $\overline{W}$ OR $\overline{E}$ LOW TIME (ADDRESS SET–UP TIME)
tWLAX, ELAX	$\overline{W}$ OR $\overline{E}$ LOW TO ADDRESS INVALID TIME (ADDRESS HOLD TIME)
tDVWH, tDVEH	DATA INPUT VALID TO $\overline{W}$ OR $\overline{E}$ HIGH (DATA SET–UP TIME)
tWHDX. tEHDX	$\overline{W}$ OR $\overline{E}$ HIGH TO DATA INPUT INVALID (DATA HOLD TIME)

FIGURE A1–8

SINGLE SUPPLY EEPROM OPTIONAL HARDWARE MASS ERASE (ALL 1'S) FEATURE

– IF A HARDWARE MASS ERASE MODE IS IMPLEMENTED ON THE 256K EEPROM, THE FOLLOWING CONVENTIONS MUST BE FOLLOWED:

– $\overline{E}$ = LOW LOGIC LEVEL

– $\overline{W}$ = LOW LOGIC LEVEL

– $\overline{G}$ = SUPER VOLTAGE (WAVEFORM, LEVEL AND TIMING TO BE DETERMINED BY THE MANUFACTURER).

– DQ0 – DQ7 = ALL HIGH LOGIC LEVEL (FFH)

– A0 – A14 = DON'T CARE (EITHER HIGH OR LOW LOGIC LEVELS)

FIGURE A1–9

SINGLE SUPPLY BIT EEPROM OPTIONAL SOFTWARE MASS ERASE (ALL 1'S) FEATURE

IF A SOFTWARE MASS ERASE FEATURE IS IMPLEMENTED IN THE SINGLE SUPPLY EEPROM, IT MUST OPERATE BY APPLYING THE FOLLOWING SIX DATA/ADDRESS SEQUENCE TO THE PART.

STEP	MODE	A14–A0	DQ7–DQ0
1	"ACCESS" WRITE	5555H	AAH
2	"ACCESS" WRITE	2AAAH	55H
3	"ACCESS" WRITE	5555H	80H
4	"ACCESS" WRITE	5555H	AAH
5	"ACCESS" WRITE	2AAAH	55H
6	"ACCESS" WRITE	5555H	10H

–ALL ACCESS WRITES MUST FOLLOW THE STANDARD PAGE MODE WRITE CYCLE TIMING SPECIFIED FOR THE PART,

–NO DATA IS ACTUALLY WRITTEN TO THE EEPROM DURING THE "ACCESS" WRITES. ONCE THE 6 STEP SEQUENCE IS COMPLETED, THE PART AUTOMATICALLY COMPLETES A MASS ERASE CYCLE INTERNALLY.

FIGURE A1–10

3.5.3.2 – DUAL POWER SUPPLY EEPROM COMAND SET

The following command set is applicable to dual power supply EEPROMs of any capacity.

COMAND CODES		
1st CYCLE	2nd CYCLE	OPERATION DESCRIPTION
00		RESERVED
10		Automated Write
20	20	Automated Block Erase
20	D0	Automated Block Erase
30	30	Automated Chip Erase
40		Algorithmic Write
50		Reserved
60	60	Algorithmic Block Erase
70		Reserved
80		Reserved
90		Read ID
A0		Algorithmic Erase Verify
B0		Reserved
C0		Algorithmic Write Verify
D0		Reserved
E0		Reserved
F0		

NOTE: All operands are in HEX.

This Standard provides an optional command set for use with the dual supply voltage EEPROM devices. This command set comprehends algorithmic commands and adds a set of automatic codes. A device may respond to either or both operating modes.

The Standard is applicable to devices with all data interface widths..

3.5.3.3 – SINGLE POWER SUPPLY EEPROM COMMAND CODES

The following tables define the three cycle and 6 cycle comand codes for SINGLE SUPPLY EEPROMs with capacities greater than 256 Kb.

Three cycle Command Codes

Command	1st Cycle		2nd Cycle		3rd Cycle	
	Address	Data	Address	Data	Address	Data
SDP Write Disable	5555	AA	2AAA	55	5555	A0
Product Identification Entry	5555	AA	2AAA	55	5555	90
Reset/Product Identification Exit	5555	AA	2AAA	55	5555	F0
Note: All operands are in HEX.						

Six Cycle Command Codes

	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
Command	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
SDP Write Disable	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	20
Chip Clear (Erase)	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Note: All operands are in HEX												

All timings are per the EEPROM Software Data Protect Timing shown in Fig. A1–7

The address space required is encompassed by A0–A14; other address lines, e.g., A15, A16, can be at any level between VSS minimum and VCC maximum. The data space required is encompassed by DQ0–DQ7; other I/O lines, DQ8, DQ9, can be at any level between VSS minimum and VCC maximum.

3.5.3.4 – EEPROM TOGGLE BIT FEATURE

This standard is applicable to devices with a capacity greater than 256 Kb, with both single and dual power supplies.

–The Toggle Bit feature is used to determine if a Write Cycle (either Erase, Program, or both) is in progress in the EEPROM or if the part is available for reading or another write cycle.

–Whenever the part is read during a nonvolatile write cycle, the data on DQ6 will toggle, i.e., alternate between high and low, on alternate read cycles. Any address can be used when reading to get the Toggle Bit output. Typically, the first toggle out is high (logic "1").

–When the nonvolatile write cycle automatically times out, normal valid data is read at the outputs for any provided address.

–A software routine uses this feature to determine when the nonvolatile write cycle is complete.

–The normal read cycle timing specified for the part must be used for Toggle Bit read cycles.

–An additional parameter, tWHGL (tEHGL), must also be specified for the toggle bit cycle. tWHGL (tEHWL) is the minimum time the system must wait from the last rising edge of $\overline{W}$ ($\overline{WE}$) or $\overline{E}$ until the Toggle Bit read cycle is initiated by the falling edge of $\overline{G}$ ($\overline{OE}$).

–The actual completion of the nonvolatile write cycle is asynchronous with the system; therefore, a Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system will possibly get an erroneous result, i.e., valid data may appear to conflict with DQ6. In order to prevent spurious rejections, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the reject is valid.

3.6 Nonvolatile Random Access Memory (NVRAM)

The following NVRAM standards were developed by JC-42.3 Committee and have been implemented using MOS technology.

3.6.1 NVRAM, Nibble Wide

3.6.1.1 .25K & 1K BY 4 NVRAM IN DIP
CAPACITY--256, 1K WORDS OF 4 BITS
PACKAGE--18, 20 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT--Fig. 3.6-1

3.6.2 NVRAM, Byte Wide

3.6.2.1 .5K, 1K BY 8 NVRAM IN DIP
CAPACITY--.5K & 1K WORDS OF 8 BITS
PACKAGE--24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.6-2

3.6.2.2 .5K & 1K BY 8 NVRAM IN RCC
CAPACITY--.5K, 1K WORDS OF 8 BITS
PACKAGE--32 PAD (PIN) RCC
PIN ASSIGNMENT--Fig. 3.6-3
These devices are CC equivalents of 24 pin DIP devices

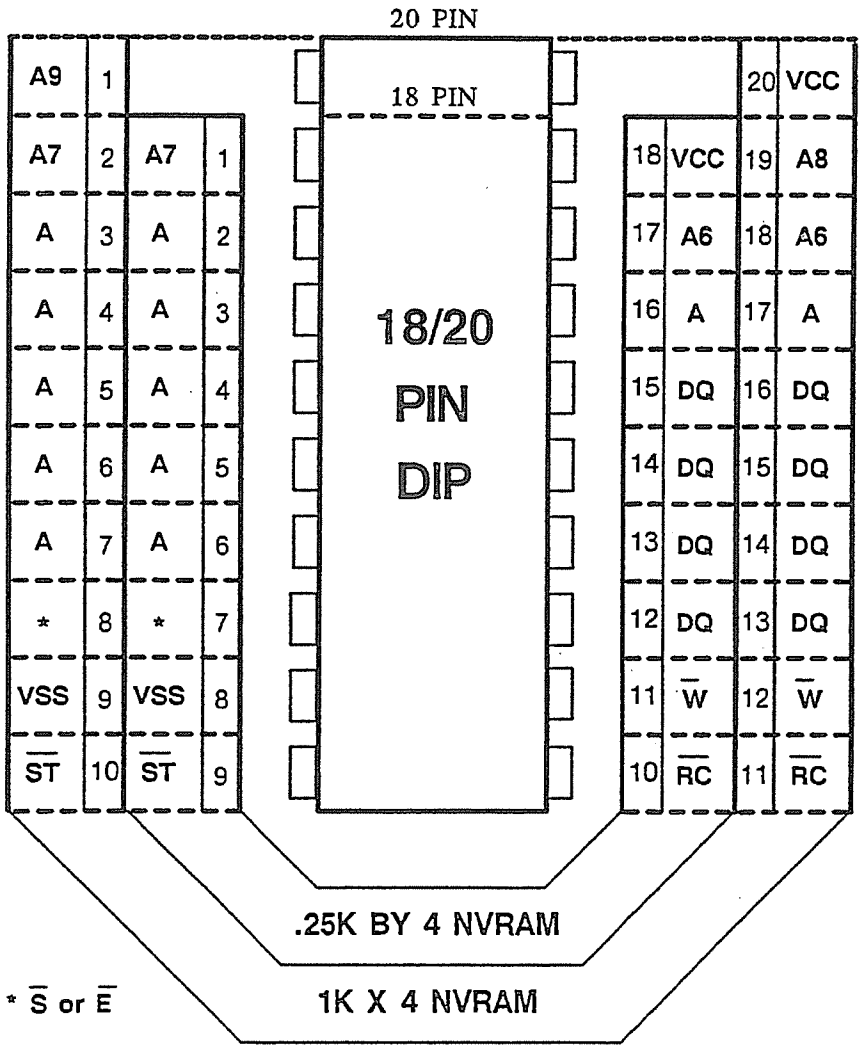
3.6.2.3 .5K TO 16K BY 8 NVRAM FAMILY IN DIP
CAPACITY--.5K, 1K, 2K, 4K, 8K, 16K WORDS OF 8 BITS
PACKAGE--28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.6-4

3.6.2.4 .5K TO 16K BY 8 NVRAM FAMILY IN RCC
CAPACITY--.5K, 1K, 2K, 4K, 8K, 16K WORDS OF 8 BITS
PACKAGE--32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT--Fig. 3.6-5

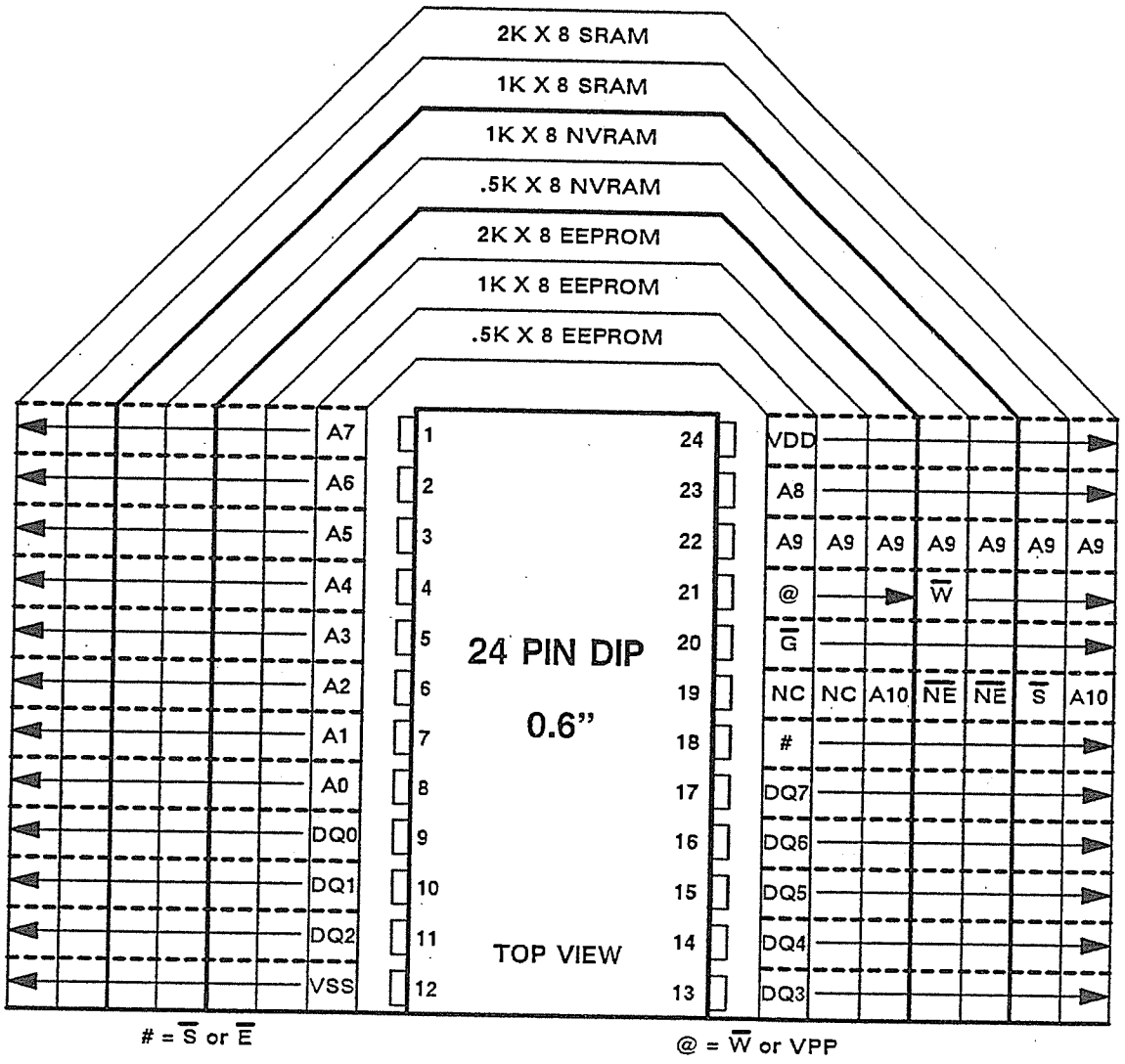
3.6.2.5 32K TO 256K BY 8 NVRAM FAMILY IN SOJ,
CAPACITY--32K, 128K, 256K WORDS OF 8 BITS,
PACKAGE--28 OR 32 PIN SOJ, 0.4" WIDE OR NOT DEFINED
PIN ASSIGNMENT--Fig. 3.6-6

3.6.2.6 32K TO 256K BY 8 NVRAM FAMILY IN DIP,
CAPACITY--32K, 64K, 128K, 256K WORDS OF 8 BITS,
PACKAGE--32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.6-7

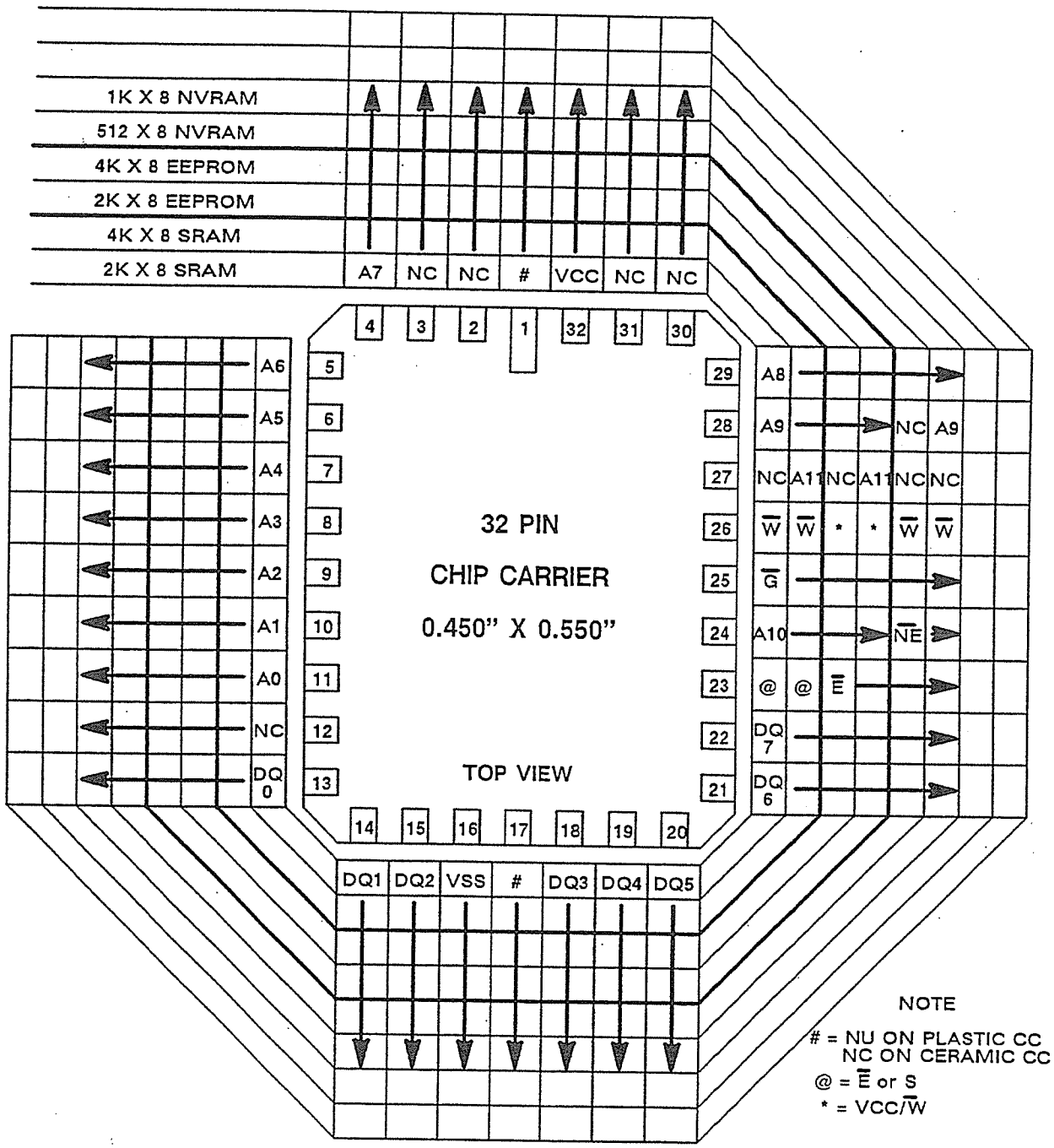
3.6.2.7 16K TO 128K BY 9 NVRAM FAMILY IN DIP,
CAPACITY--16K, 32K, 64K, 128K WORDS OF 9 BITS,
PACKAGE--32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.6-8



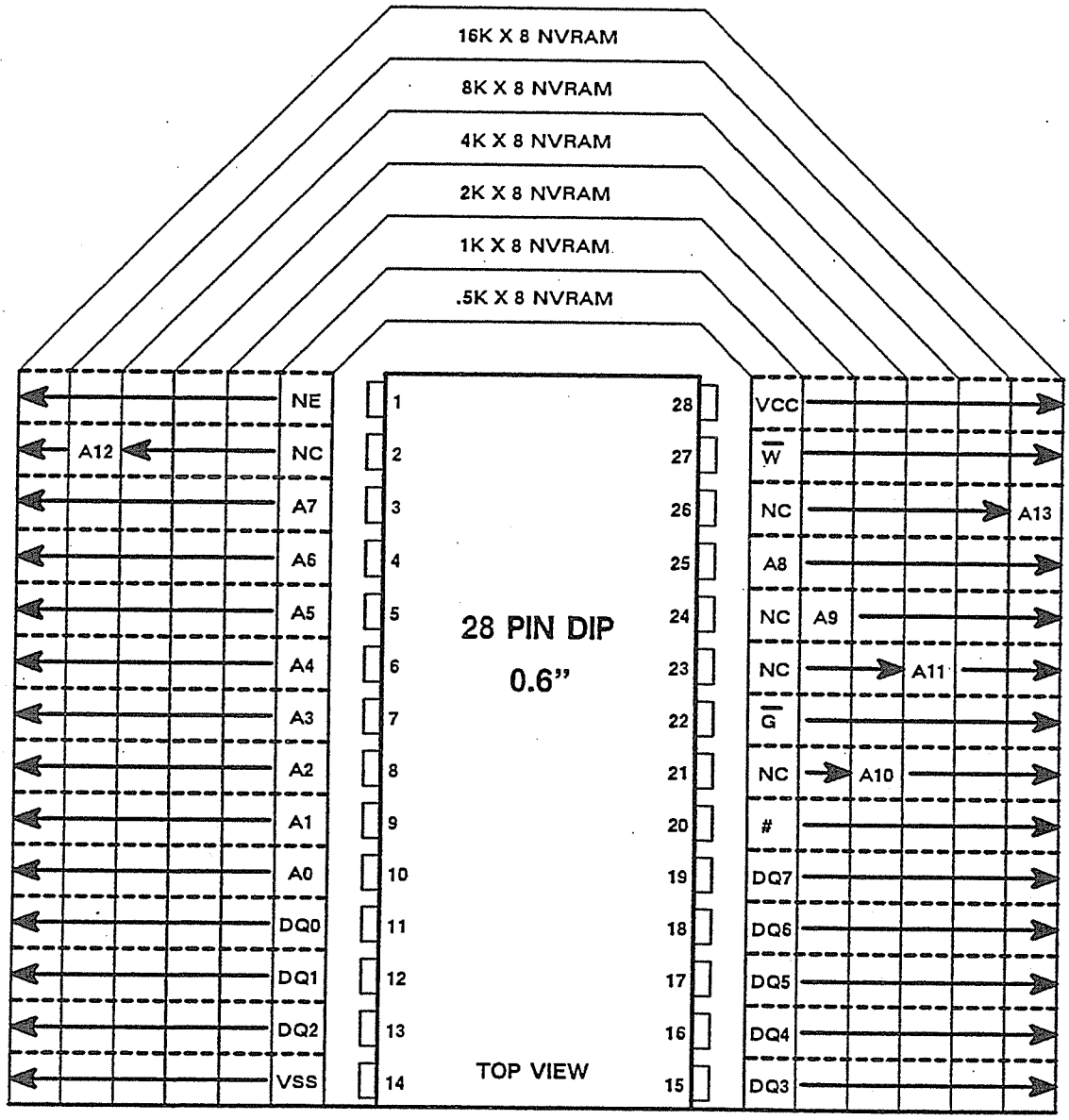
.25K & 1K BY 4 NVRAM IN DIP
FIGURE 3.6-1



.5K & 1K BY 8 NVRAM IN DIP
FIGURE 3.6-2



.5K & 1K BY 8 NVRAM IN RCC
FIGURE 3.6-3

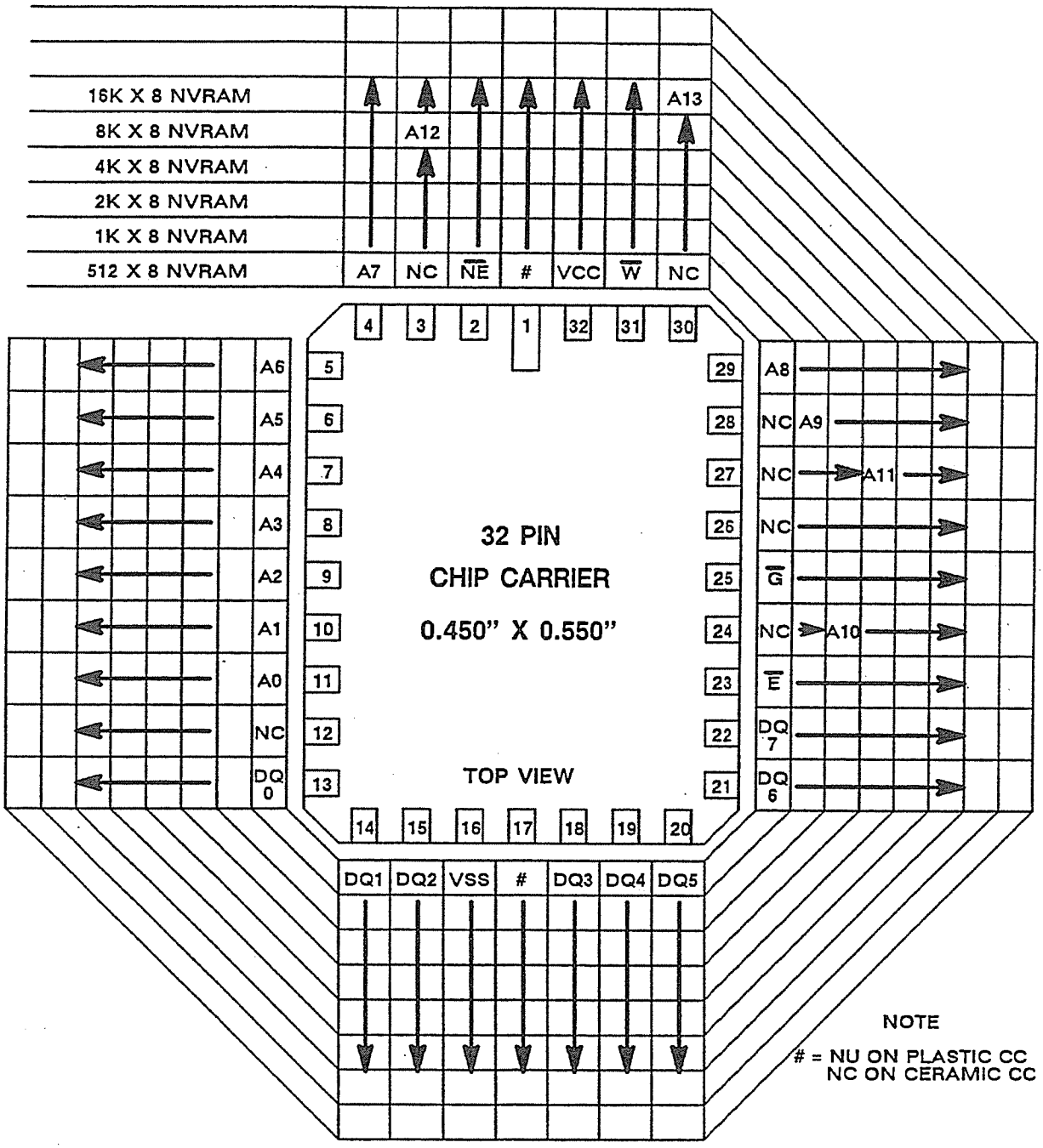


= $\overline{S}$ or $\overline{E}$

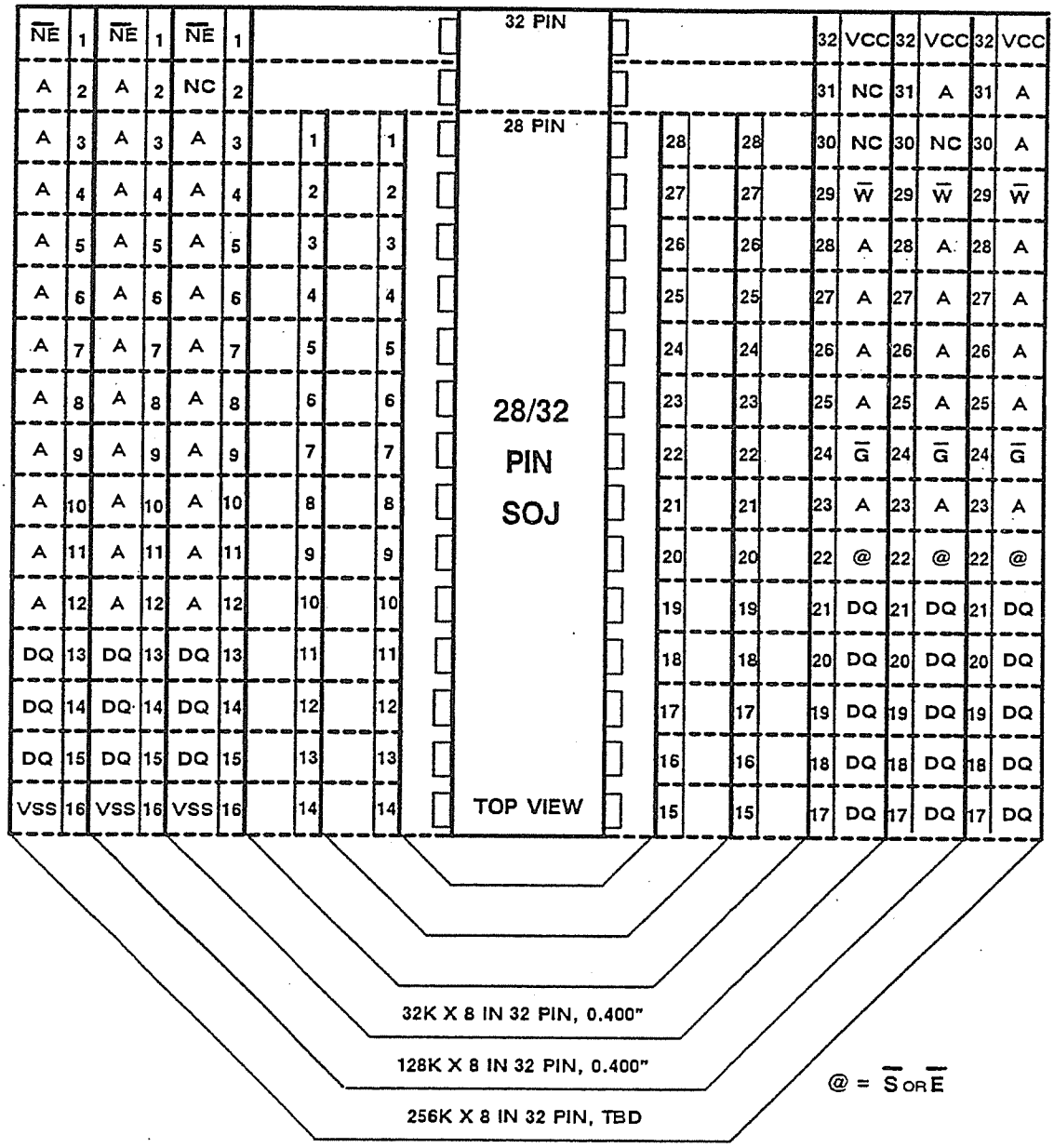
FUNCTION TABLE

PIN / MODE	$\overline{S}$ or $\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{NE}$
READ	L	H	L	H
WRITE	L	L	H	H
STORE	L	L	H	L
RECALL	L	H	L	L

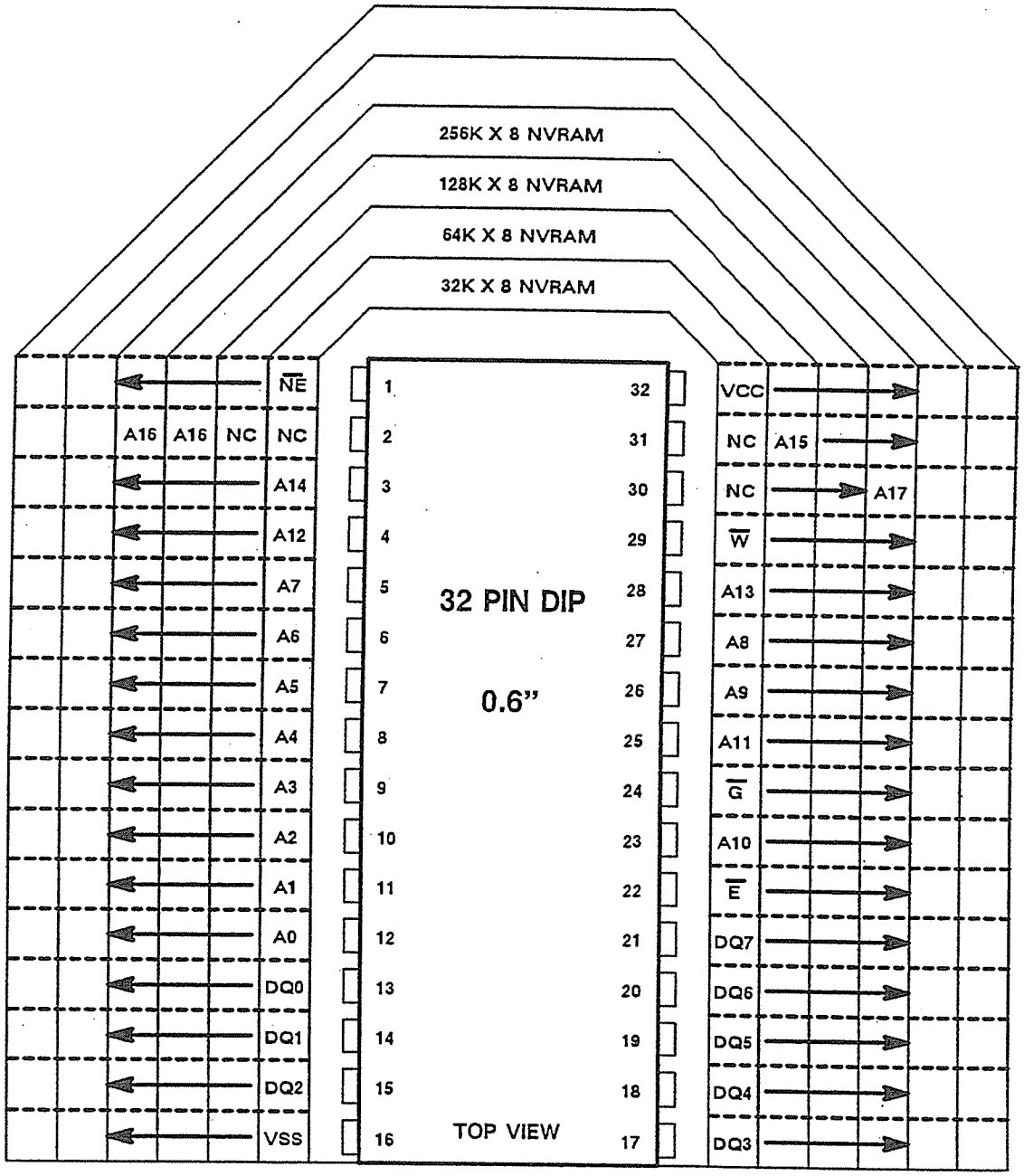
.5K TO 16K BY 8 NVRAM FAMILY IN DIP
FIGURE 3.6-4



.5K TO 16K BY 8 NVRAM FAMILY IN RCC
FIGURE 3.6-5



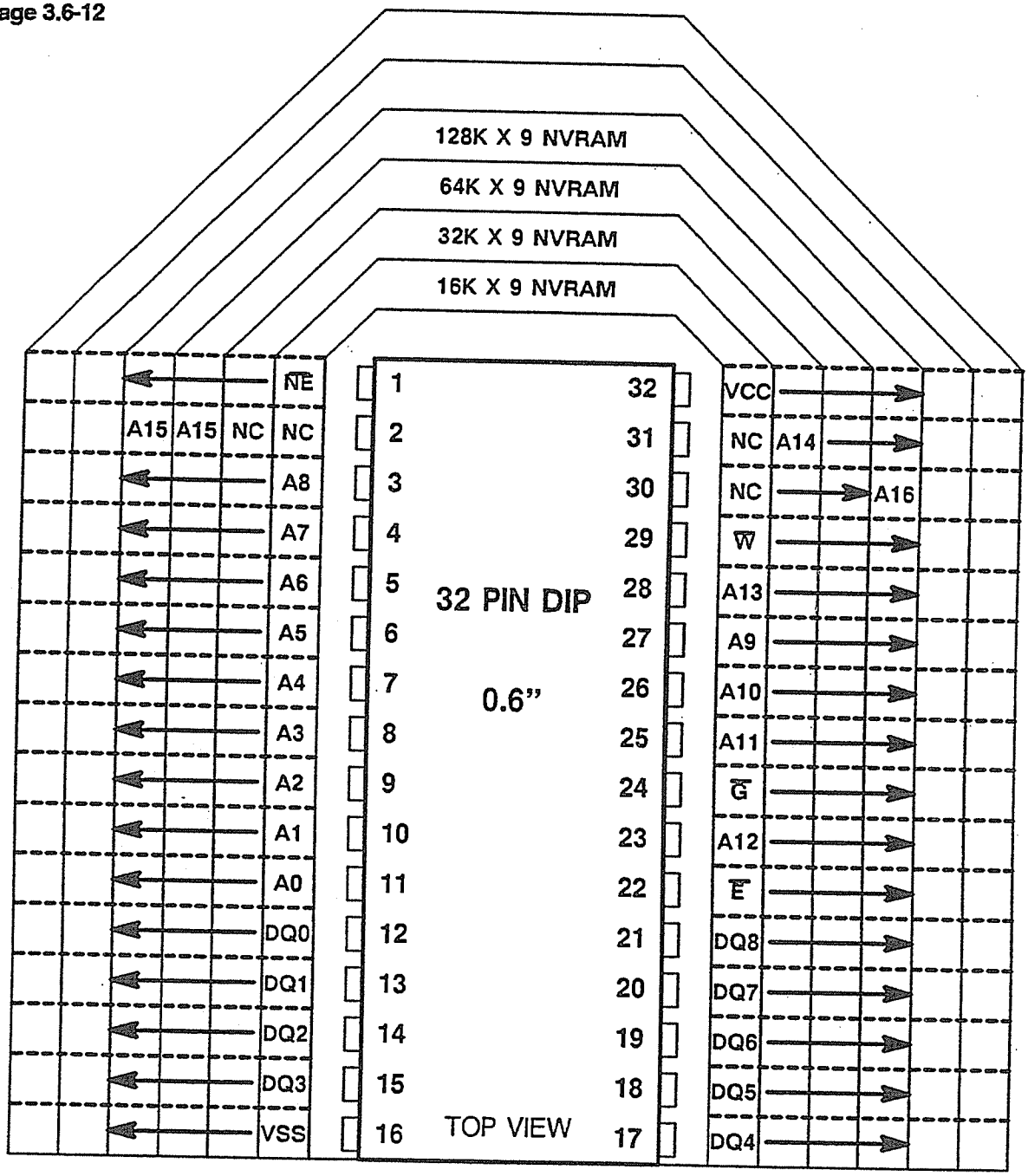
32K TO 256K BY 8 NVRAM FAMILY IN SOJ
FIGURE 3.6-6



FUNCTION TABLE

PIN / MODE	S or E	W	G	NE
READ	L	H	L	H
WRITE	L	L	H	H
STORE	L	L	H	L
RECALL	L	H	L	L

32K TO 256K NY 8 NVRAM FAMILY IN DIP
FIGURE 3.6-7



FUNCTION TABLE

PIN / MODE	$\overline{S}$ or $\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{NE}$
READ	L	H	L	H
WRITE	L	L	H	H
STORE	L	L	H	L
RECALL	L	H	L	L

16K TO 128K BY 9 NVRAM FAMILY IN DIP
FIGURE 3.6-8

3.7 Static Random Access Memory (SRAM)

The following SRAM standards were developed by Committees 42.1 and 42.3. The devices described are compatible with one of several logic circuit families as defined. The device standards require that the memory devices must operate with signal levels and power supply voltages that are consistent with those used in the logic family(s) specified. The nominal power supply voltages for the three families in use are as follows:

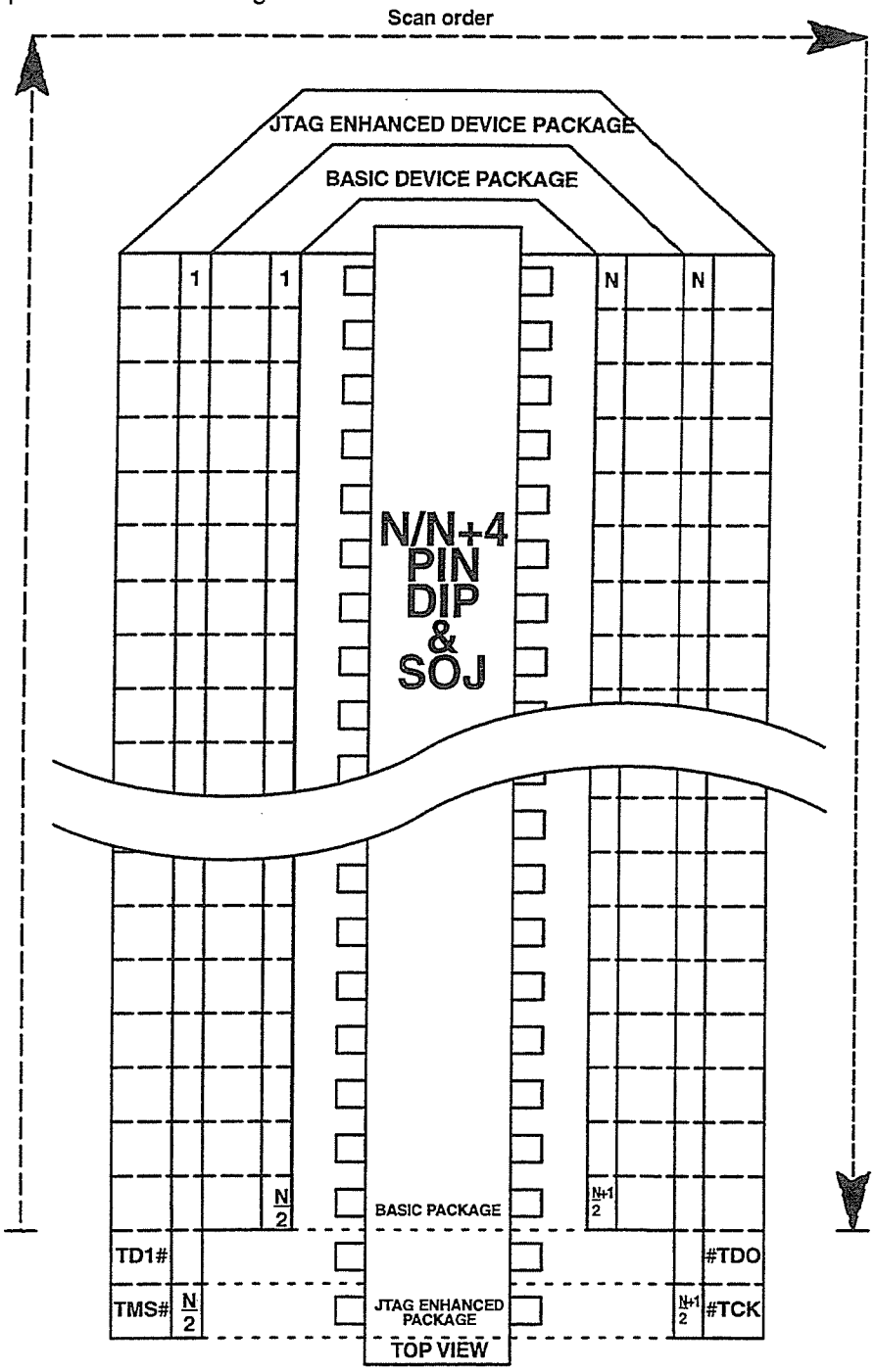
TTL, VCC = 5.0 V
10K ECL, VEE = 5.2 V
100K ECL, VEE = 4.5 V

The standards described on this page are applicable to multiple device configurations as noted in the individual standards.

3.7.1 – JTAG Extension to Revolutionary Pinout SRAM Devices

This standard establishes a convention to provide uniform guidance when it is desired to add the IEEE 1149.1 Boundary Scan feature (JTAG) to a device with a pinout that follows the JEDEC SRAM Revolutionary pinout (RPO, devices with redundant centered power pins). The convention shown if Fig. 3.7–1 shows the convention for this addition. This convention applies to all existing and future RPO SRAM devices in DIP, SOJ, TSOP2, and any other two–sided packages that might be used in the future.

Add IEEE 1149.1 Boundary–Scan (JTAG), as an option, to any existing or future two–sided JEDEC Revolutionary SRAM pinouts by increasing package pin count by 4 as shown. Scan all of the original signal pins clockwise starting from TDI.



 # – These pins are JTAG specific pins defined in IEEE Std. 1149.1

FIGURE 3.7–1

JTAG ADDITION TO REVOLUTIONARY PINOUT SRAM

3.7.1 Bit Wide TTL SRAM

All of the following standards are for devices which operate with TTL interface levels and power voltages.

3.7.1.1 – .25K & 1K BY 1 TTL SRAM IN DIP

CAPACITY—.25K & 1K WORDS OF 1 BIT
PACKAGE—16 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT—Fig. 3.7.1–1
This standard was developed by Committee 42.1.

3.7.1.2 – .25K & 1K BY 1 TTL SRAM IN SCC

CAPACITY—.25K & 1K WORDS OF 1 BIT
PACKAGE—20 PIN (PAD) SCC, 0.350" X 0.350"
PIN ASSIGNMENT—Fig. 3.7.1–2
This standard was developed Committee 42.1.

3.7.1.3 – 4K TO 2M BY 1 TTL SRAM FAMILY IN DIP

CAPACITY—4K, 16K, 64K, 256K, 1M, 2M WORDS OF 1 BIT
PACKAGE—18, 20, 22, 24, or 28 PIN DIP, 0.3", or 0.4" wide or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.1–3

3.7.1.4 – 16K BY 1 TTL SRAM IN RCC

CAPACITY—16K WORDS OF 1 BIT
PACKAGE—20 PAD (PIN) RCC, 0.290" x 0.425"
PIN ASSIGNMENT—Fig. 3.7.1–4

3.7.1.5 – 64K BY 1 TTL SRAM IN RCC

CAPACITY—64K WORDS OF 1 BIT
PACKAGE—22 PAD (PIN) RCC, 0.290" X 0.490"
PIN ASSIGNMENT—Fig. 3.7.1–5

3.7.1.6 – 16K TO 2M BY 1 TTL SRAM IN SOJ

CAPACITY—16K, 64K, 256K, 1M, 2M WORDS OF 1 BIT
PACKAGE—24 or 28 PIN SOJ, 0.3" or 0.4" wide or UNDEFINED
Release 5 adds approval for the 256K X 1 part to be supplied in a 0.3" SOJ or TSOP–2
PIN ASSIGNMENT—Fig. 3.7.1–6

3.7.1.7 – 256K TO 16M BY 1 TTL SRAM AND 4M BY 1 SSRAM IN DIP, SOJ, AND TSOP–2

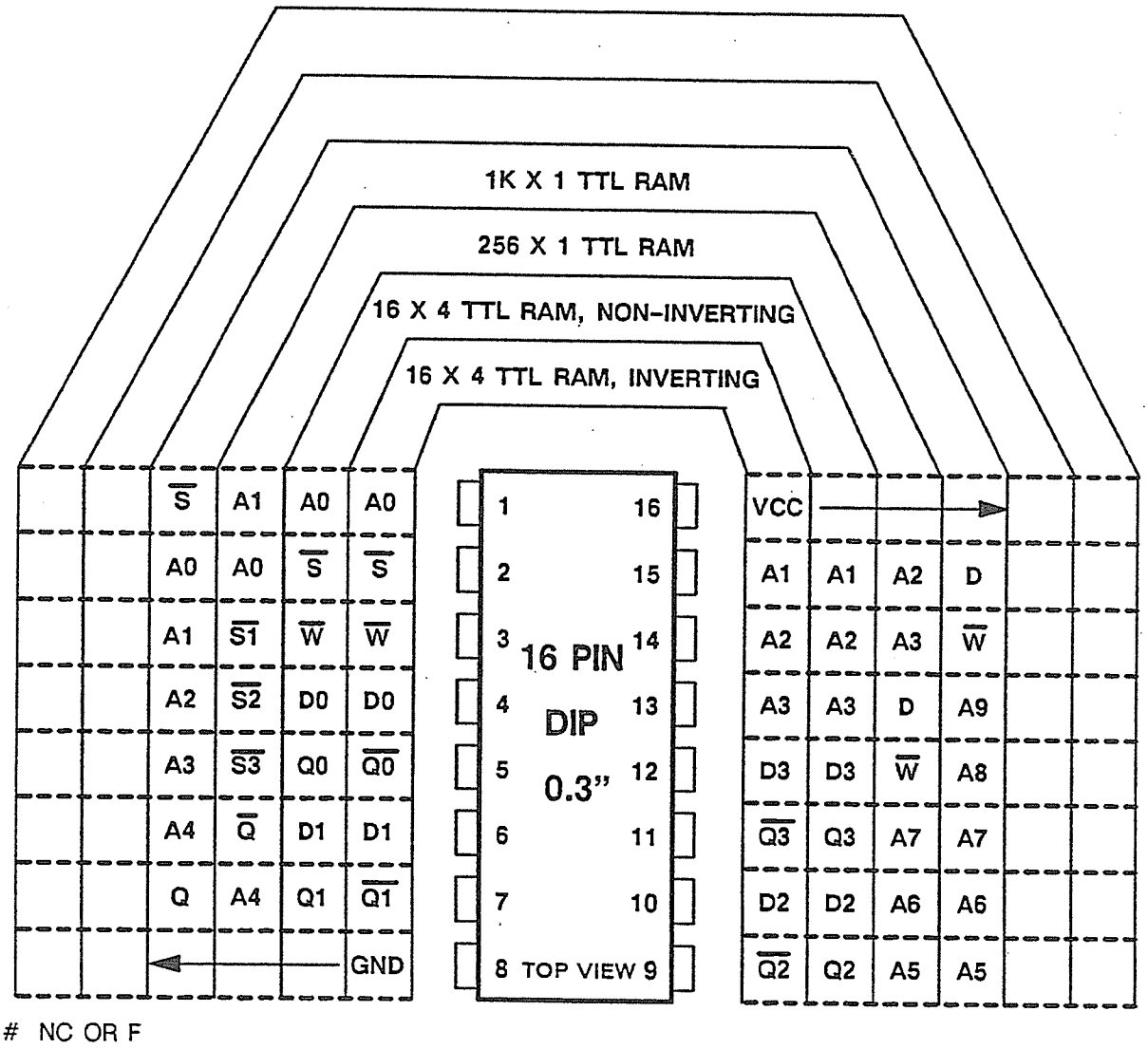
CAPACITY—256K, 1M, 4M, AND 16M WORDS OF 1 BIT
LOGIC FEATURES—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES
—SEPARATE DATA INPUT & OUTPUT PINS
—4M DENSITY PART APPROVED AS SYNCHRONOUS SRAM
PACKAGE—28 or 32 PIN SOJ, & TSOP2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—28 0r 32 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MILTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.1–7

3.7.1.8 – 256K BY 1 TTL SRAM IN RCC

CAPACITY—256K WORDS OF 1 BIT
PACKAGE—28 PAD (PIN) RCC, 0.350" X 0.550"
PIN ASSIGNMENT—Fig. 3.7.1–8

3.7.1.9 – 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP, SOJ, AND TSOP–2

CAPACITY—4M, 16M WORDS OF 1 BITOR 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—THE DATA INTERFACE CONFIGURATION MAY BE SET TO X1 OR X4 UNDER CONTROL OF THE SIGNAL LEVEL TO A CONFIGURATION INPUT
PACKAGE—4M DENSITY, 32 PIN DIP, 0.6" with PP=0.07"; 32 PIN SOJ and TSOP–2, 0.4"
—16M DENSITY; 36 PIN SOJ AND TSOP–2, 0.5"
PIN ASSIGNMENT—Fig. 3.7.1–9



NC OR F

FIGURE 3.7.1-1
.25K & 1K BY 1 TTL SRAM IN DIP

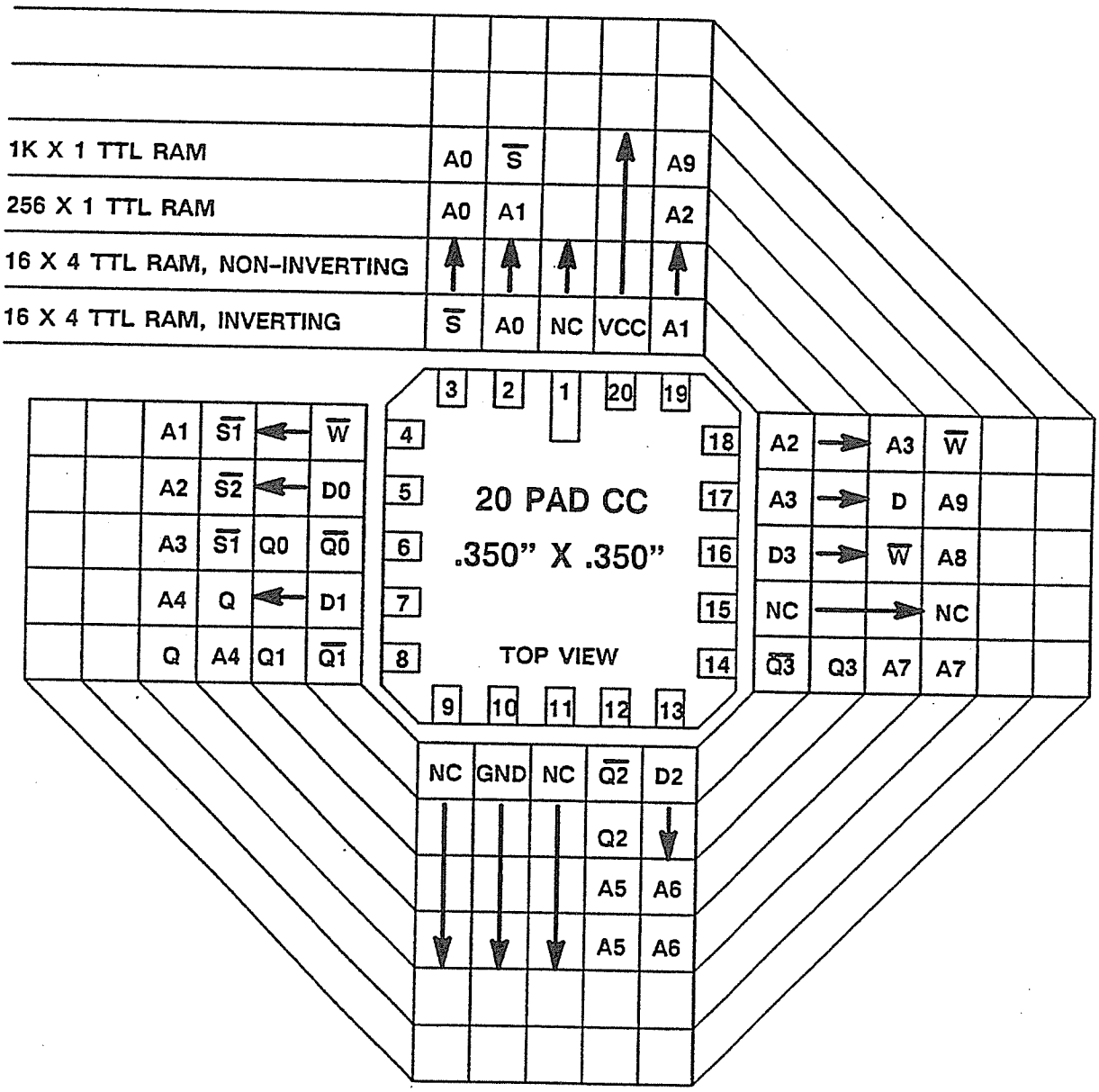


FIGURE 3.7.1-2
.25K & 1K BY 1 TTL SRAM IN SCC

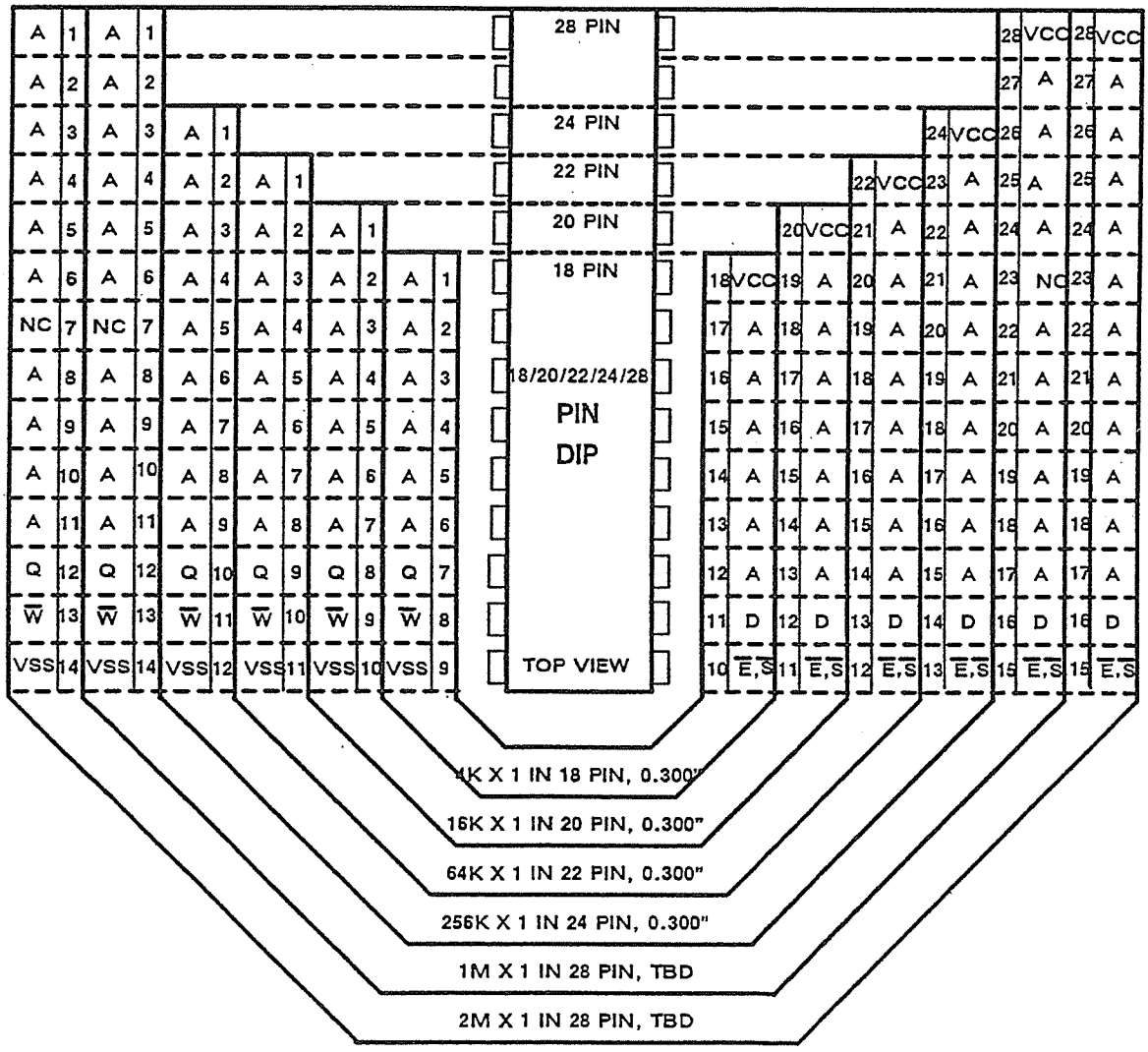


FIGURE 3.7.1-3
4K TO 2M BY 1 TTL SRAM FAMILY IN DIP

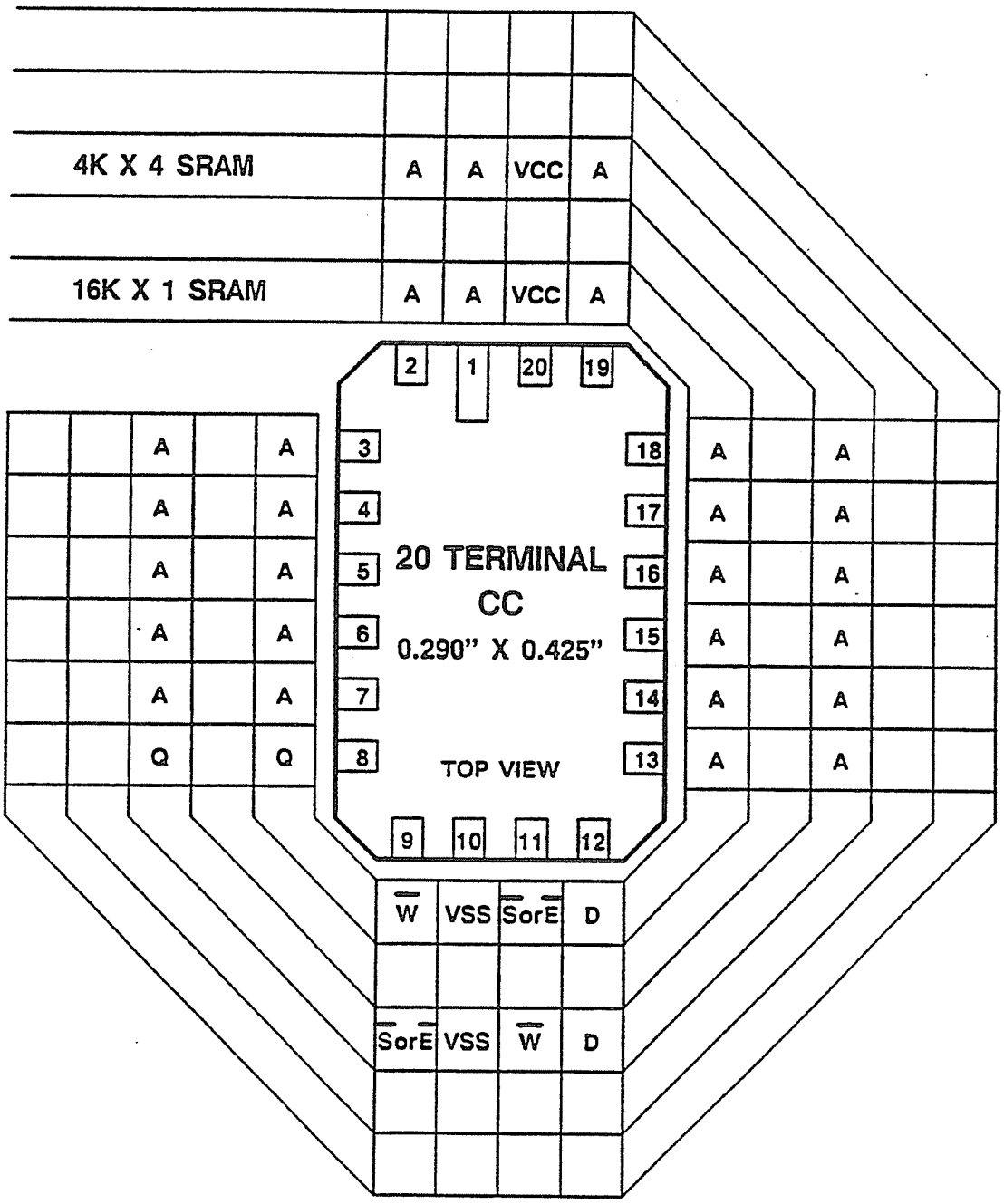


FIGURE 3.7.1-4
16K BY 1 TTL SRAM IN RCC

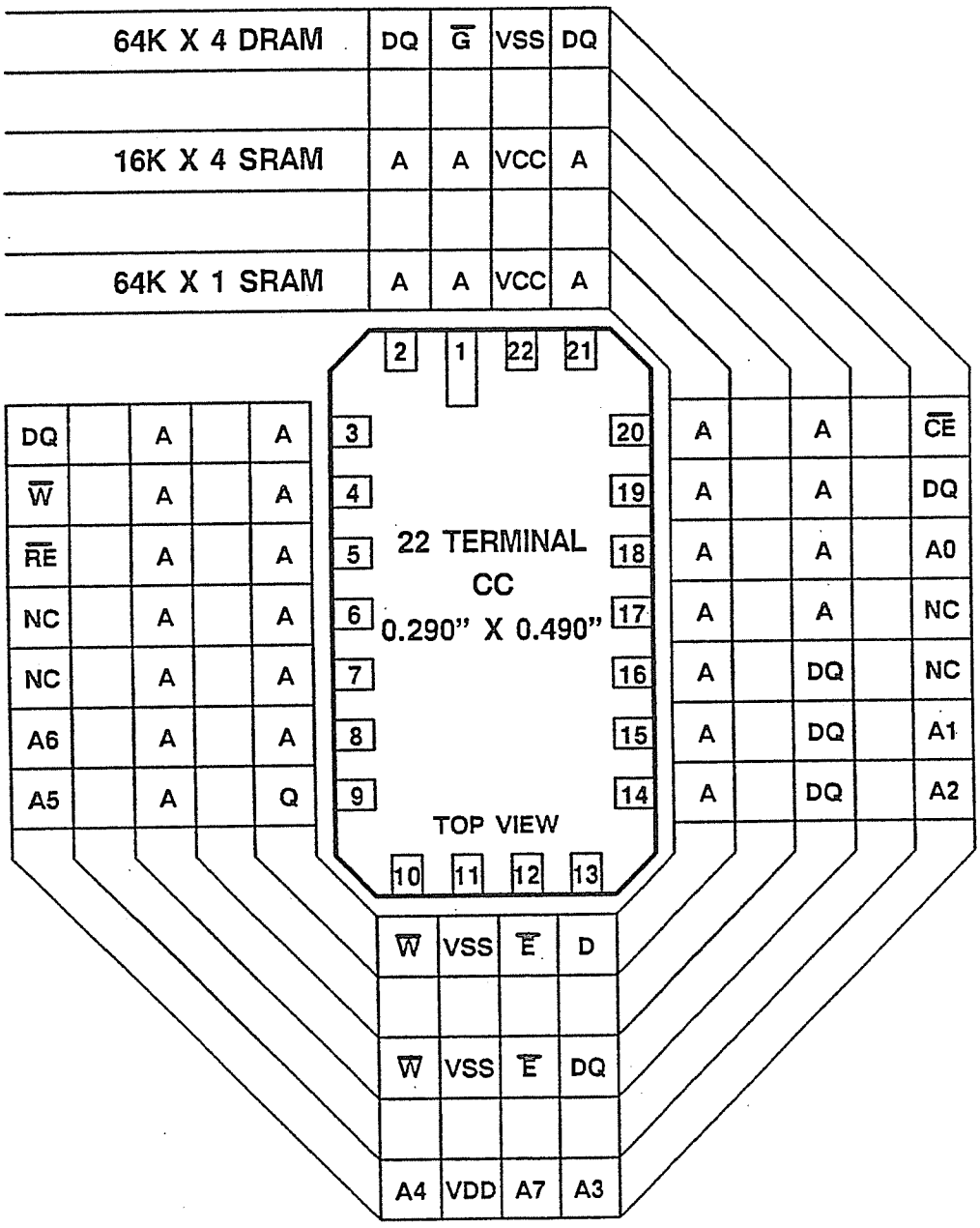
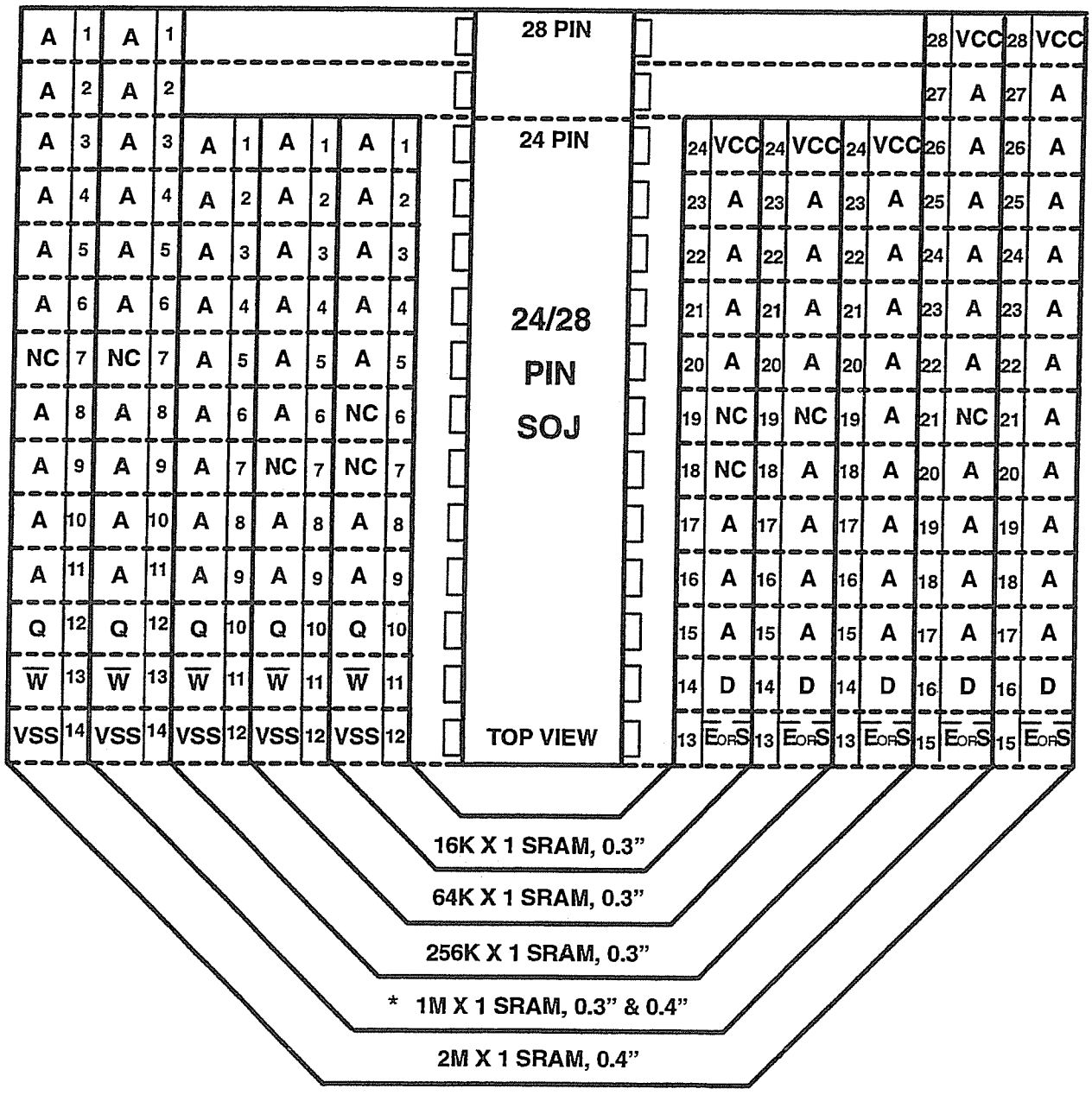


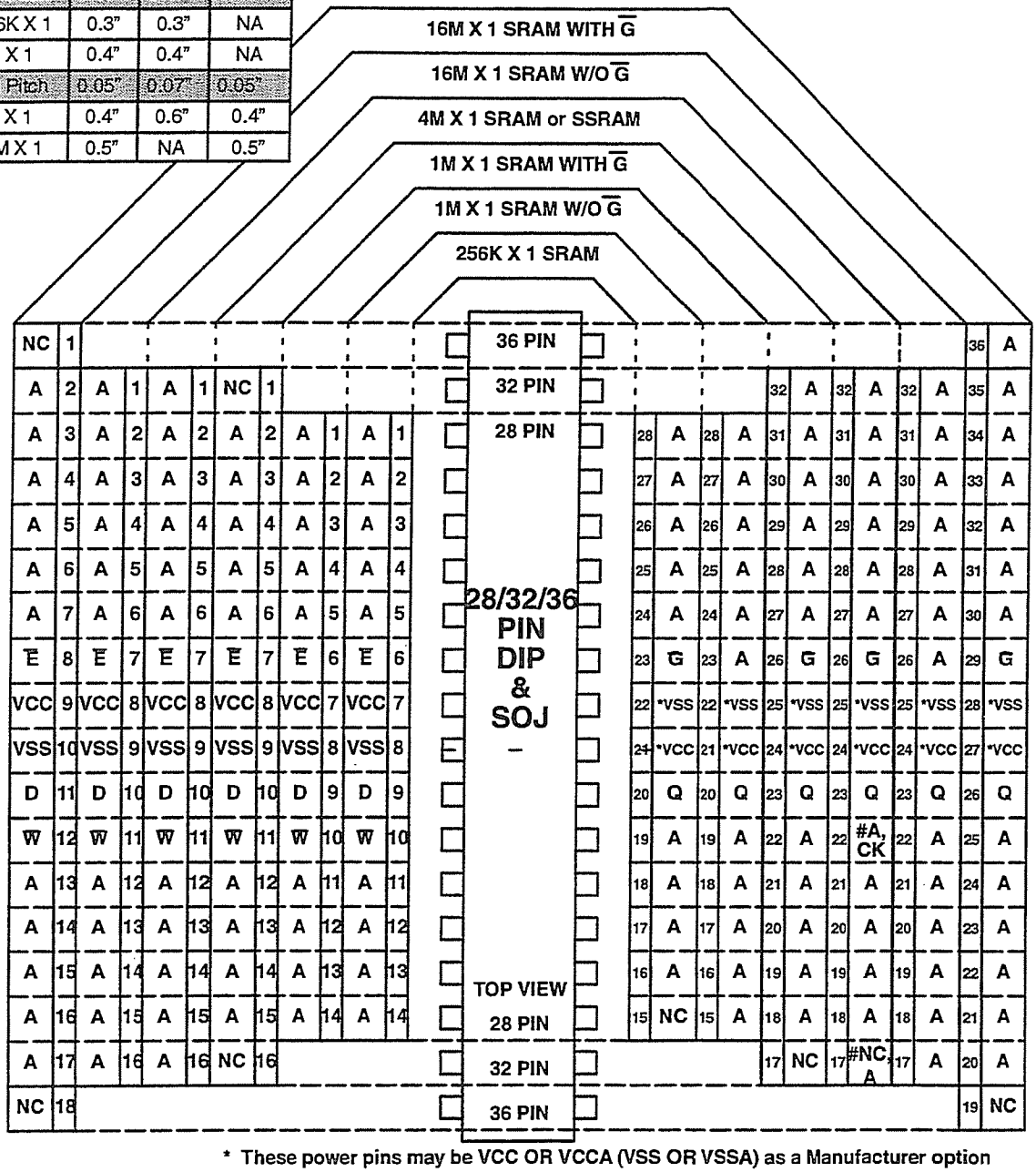
FIGURE 3.7.1-5
64K BY 1 TTL SRAM IN RCC



* The 1M X 1 part is also approved for use in a 0.3" TSOP–2 package

FIGURE 3.7.1–6
16K TO 2M BY 1 TTL SRAM IN SOJ

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
256K X 1	0.3"	0.3"	NA
1M X 1	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
4M X 1	0.4"	0.6"	0.4"
16M X 1	0.5"	NA	0.5"



* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

NOTE: For the 4M X 1 devices, the pin assignments for pins 17 & 22 are different for the SRAM and SSRAM as follows.
For SRAM, P17 = NC, P22 = A
For SSRAM, P17 = A, P22 = CK

FIGURE 3.7.1–7

256K TO 16M BY 1 TTL SRAM AND SSRAM FAMILY IN DIP, TSOP2, AND SOJ

Release 4

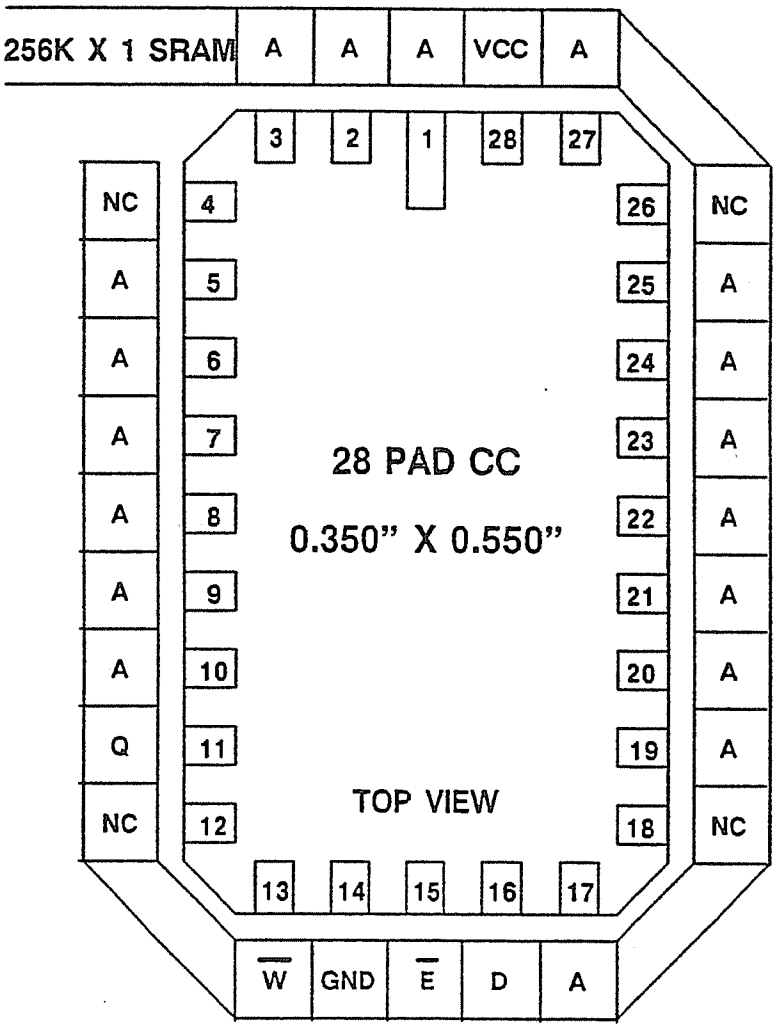


FIGURE 3.7.1-8
256K BY 1 TTL SRAM IN RCC

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.07"	0.05"
4M	0.4"	0.6"	0.4"
16M	0.5"	NA	0.5"

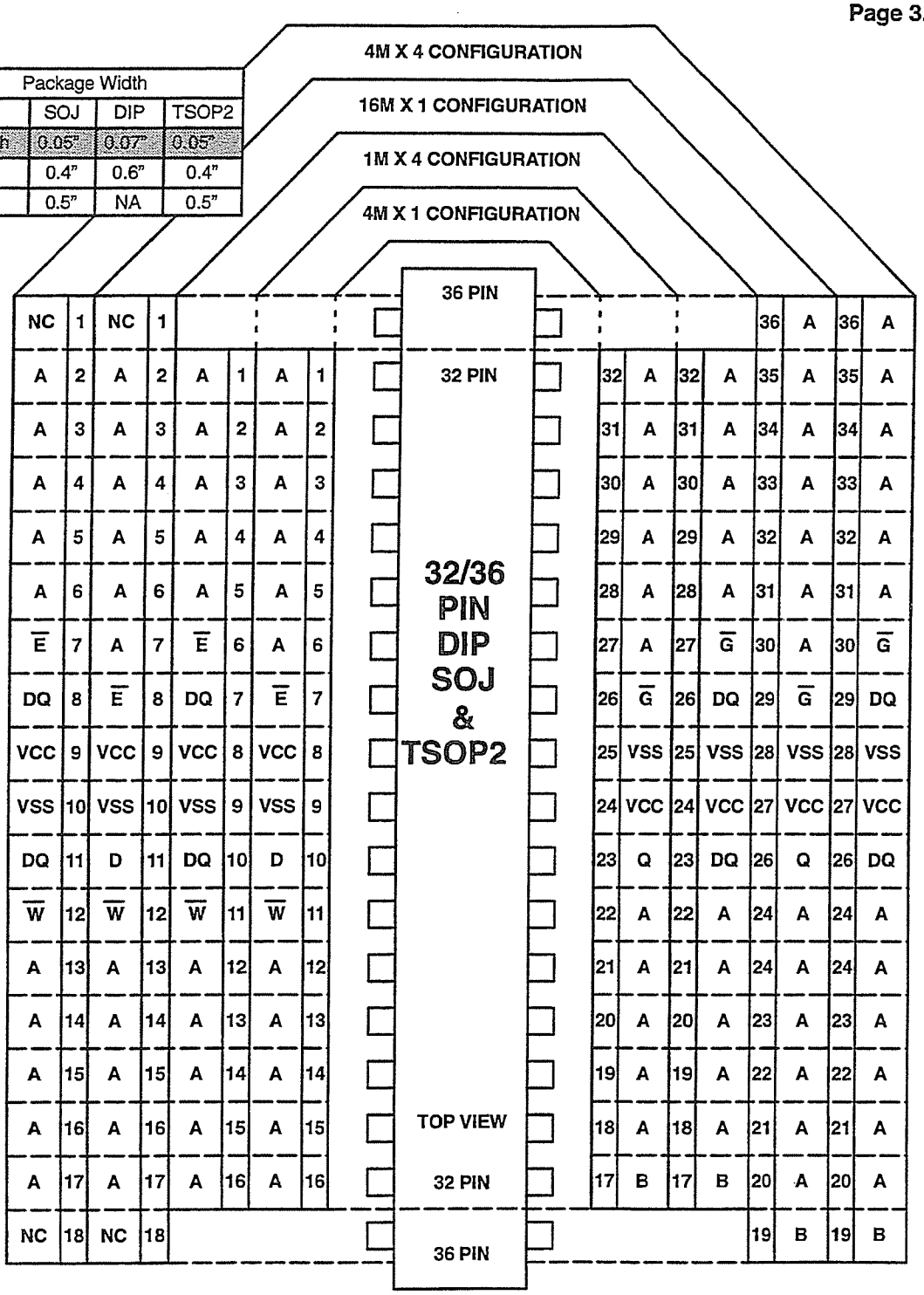


FIGURE 3.7.1–9

4M AND 16M CONFIGURABLE SRAM IN DIP, TSOP2, AND SOJ

3.7.2 Bit Wide ECL SRAM

All of the following standards are for devices which operate with ECL interface levels and power voltages.

3.7.2.1 – 1K TO 256K BY 1 ECL SRAM FAMILY IN DIP

CAPACITY—1K, 4K, 16K, 64K & 256K WORDS OF 1 BIT
ELECTRICAL INTERFACE—10K or 100K ECL
FAMILY—1K, 4K, 16K, & 256K = 10K & 100K ECL
—64K = 10K ECL
PACKAGE—16, 18, 20 OR 22 DIP, 0.4" WIDE
PIN ASSIGNMENT—Fig. 3.7.2–1

3.7.2.2 – 256K TO 16M BY 1 ECL SRAM AND 4M BY 1 SSRAM IN DIP, SOJ, AND TSOP–2

CAPACITY—256K, 1M, 4M, AND 16M WORDS OF 1 BIT
ELECTRICAL INTERFACE—10K or 100K ECL
LOGIC FEATURES—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES
—SEPARATE DATA INPUT & OUTPUT PINS
—4M DENSITY PART APPROVED AS SYNCHRONOUS SRAM
CAPACITY—256K, 1M, 4M, AND 16M WORDS OF 1 BIT
PACKAGE—28 or 32 PIN SOJ, & TSOP2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—28 0r 32 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MILTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.2–2

3.7.2.3 – 64K AND 256K BY 1 ECL SRAM IN FLATPACK

CAPACITY—64K, & 256K WORDS OF 1 BIT
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—22, OR 24 PIN FP, 0.535" WIDE, 0.030 LEAD PITCH
PIN ASSIGNMENT—Fig. 3.7.2–3

3.7.2.4 – 256K TO 16M BY 1 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2

CAPACITY—256K, 1M, 4M, & 16M WORDS OF 1 BIT
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—28, 32, or 36 PIN SOJ, & TSOP2, 0.3", 0.4". or 0.5" wide, PP=0.05"
—28 0r 32 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MILTIPLE CENTERED POWER PINS
—DIFFERENTIAL CLOCKS
PIN ASSIGNMENT—Fig. 3.7.2–4

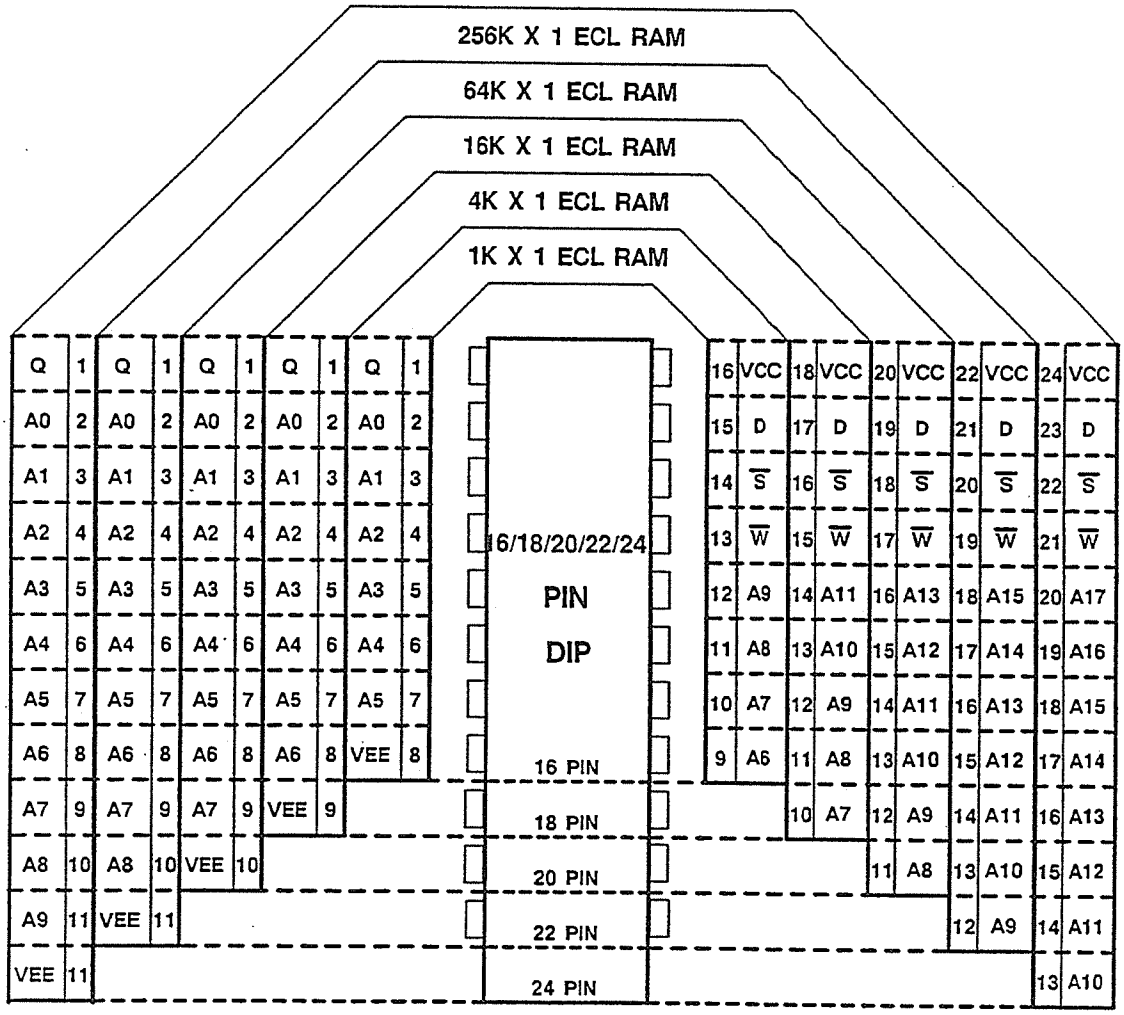
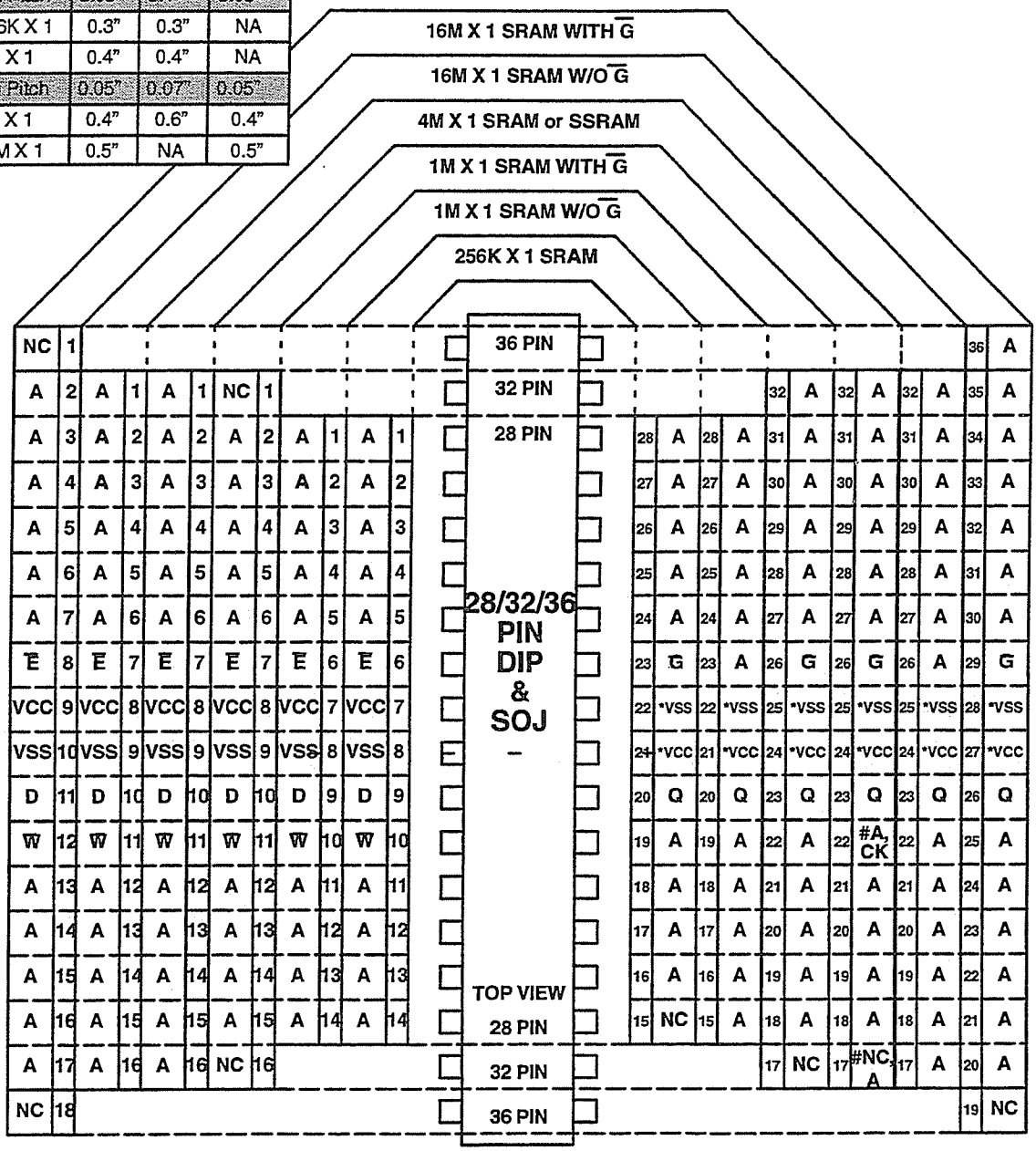


FIGURE 3.7.2-1
1K TO 256K BY 1 ECL SRAM FAMILY IN DIP

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
256K X 1	0.3"	0.3"	NA
1M X 1	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
4M X 1	0.4"	0.6"	0.4"
16M X 1	0.5"	NA	0.5"



* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

NOTE: For the 4M X 1 devices, the pin assignments for pins 17 & 22 are different for the SRAM and SSRAM as follows.
For SRAM, P17 = NC, P22 = A
For SSRAM, P17 = A, P22 = CK

FIGURE 3.7.2–2

256K TO 16M BY 1 ECL SRAM AND SSRAM FAMILY IN DIP, TSOP2, & SOJ

Release 4

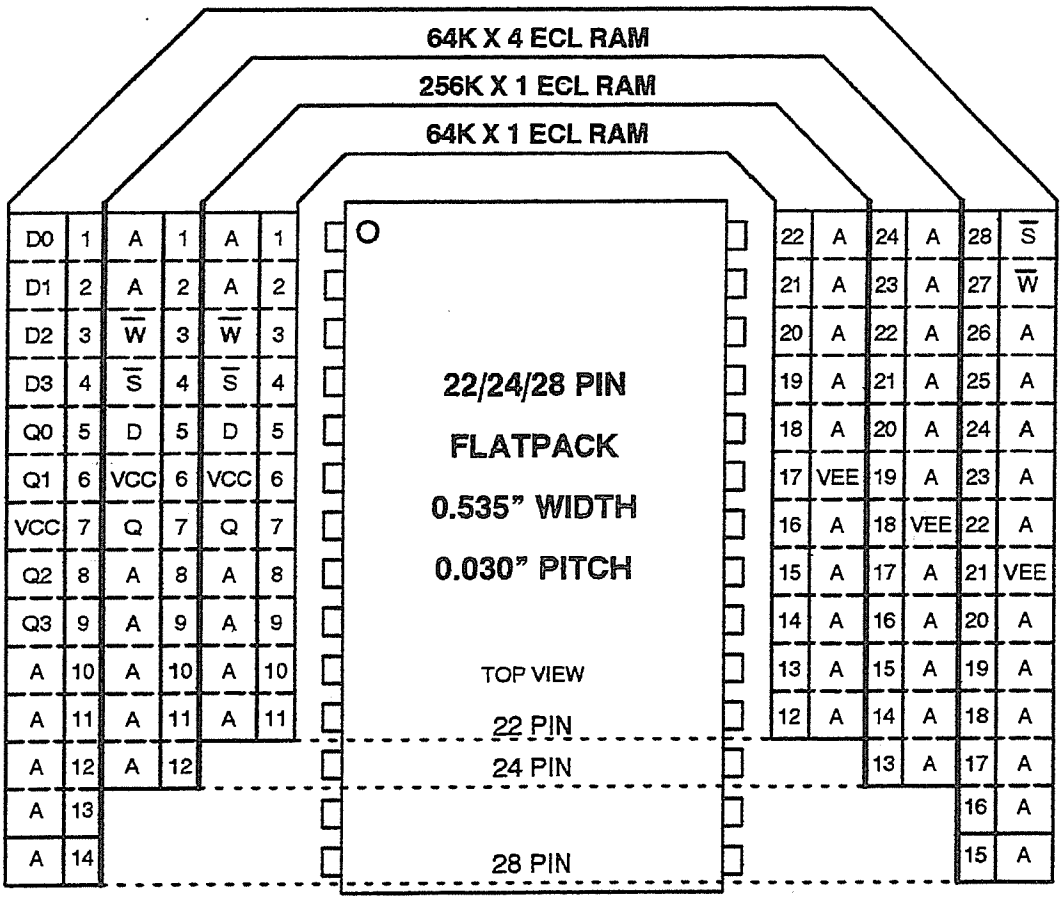
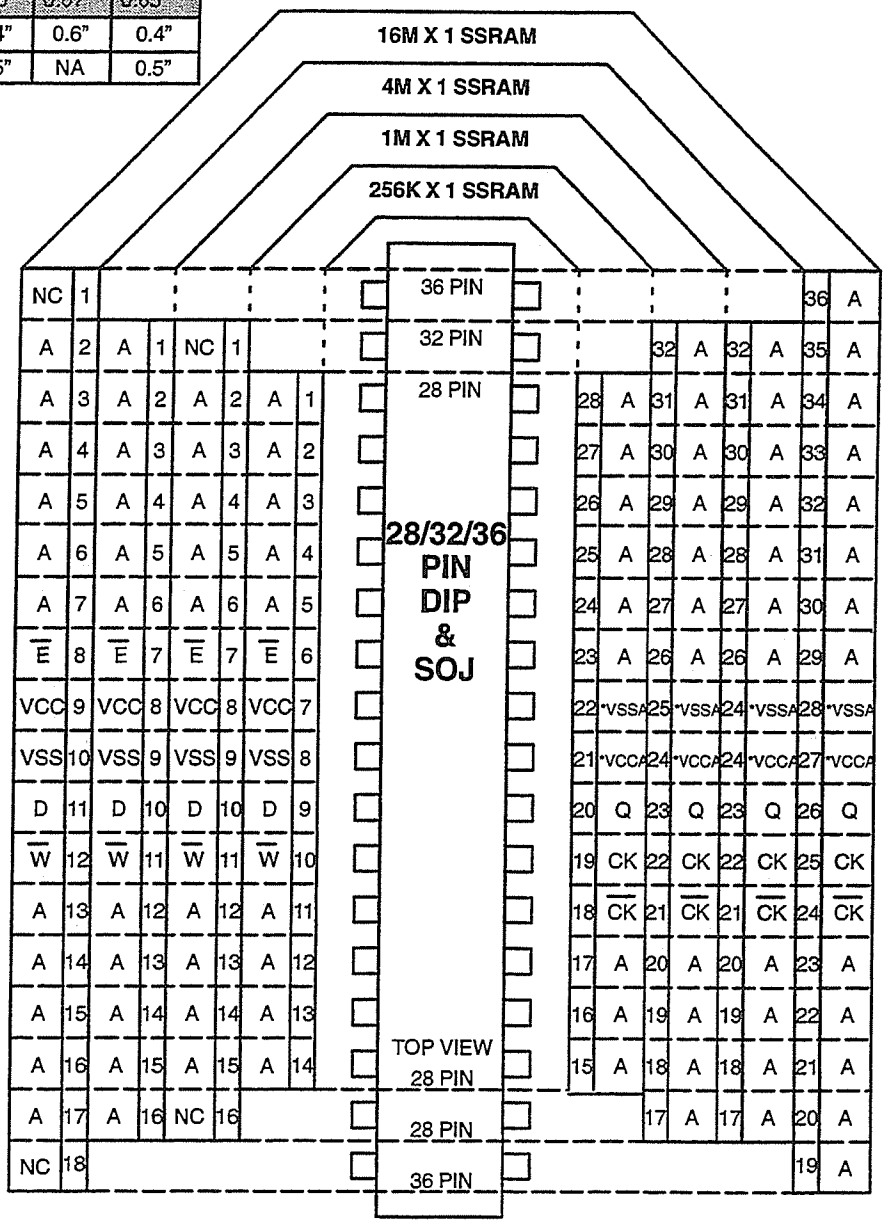


FIGURE 3.7.2–3
64K AND 256K BY 1 ECL RAM IN FP

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
256K X 1	0.3"	0.3"	NA
1M X 1	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
4M X 1	0.4"	0.6"	0.4"
16M X 1	0.5"	NA	0.5"



* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.2–4

256K TO 16M BY 1 ECL SSRAM FAMILY IN DIP, SOJ, & TSOP2

Release 4

3.7.3 Nibble Wide TTL SRAM

All of the following standards are for devices which operate with TTL interface levels and power voltages.

3.7.3.1 16 BY 4, INVERTING AND NON INVERTING TTL SRAM IN DIP & SCC

CAPACITY--16 WORDS OF 4 BITS
LOGIC FEATURES--This part is available in DATA non inverting and inverting versions
There are two package versions of this part: one in DIP and the other in SCC
PACKAGE--16 PIN DIP, 0.300" WIDE
PIN ASSIGNMENT--Fig. 3.7.3-1
PACKAGE--20 PAD (PIN) SCC, 0.350" BY 0.350"
PIN ASSIGNMENT--Fig. 3.7.3-2
This standard was developed by Committee 42.1.

3.7.3.2 .25K BY 4 TTL SRAM IN DIP & RCC

CAPACITY--.25K WORDS OF 4 BITS
FAMILY--TTL
There are two versions of this part: one in DIP and the other in RCC
PACKAGE--22 PIN DIP, 0.400" WIDE
PIN ASSIGNMENT--Fig. 3.7.3-3
PACKAGE--28 PAD (PIN) RCC, 0.350" BY 0.550"
PIN ASSIGNMENT--Fig. 3.7.3-4
This standard was developed by Committee 42.1.

3.7.3.3 256 BY 4 TTL SRAM WITH $\overline{G}$ IN SCC

256 WORDS OF 4 BITS
LOGIC FEATURES--SEPARATE DATA INPUT & OUTPUT PINS
PACKAGE--24 PAD (PIN) SCC, 0.4" X 0.4"
PIN ASSIGNMENT--Fig. 3.7.3-5
This standard was developed by Committee 42.1.

3.7.3.4 4K TO 64K BY 4 TTL SRAM WITHOUT G FAMILY IN DIP

4K, 16K, 64K WORDS OF 4 BITS
PACKAGE--20,22, or 24 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT--Fig. 3.7.3-6

3.7.3.5 4K BY 4 TTL SRAM IN RCC

CAPACITY--4K WORDS OF 4 BITS
PACKAGE--20 PAD (PIN) RCC, 0.290" BY 0.425 "
PIN ASSIGNMENT--Fig. 3.7.3-7

3.7.3.6 4K TO 1M BY 4 TTL SRAM WITH $\overline{G}$ FAMILY IN DIP

4K, 16K, 64K, 256K, & 1M WORDS OF 4 BITS
LOGIC FEATURES--Output Enable, $\overline{G}$
PACKAGE--22, 24 PIN DIP, 0.3" WIDE
--28 PIN DIP, 0.4" WIDE
--32 PIN DIP, UNDEFINED
PIN ASSIGNMENT--Fig. 3.7.3-8

3.7.3.7 16K TO 256K BY 4 TTL SRAM WITH AND WITHOUT $\overline{G}$ FAMILY IN RCC

16K, 64K, 256K WORDS OF 4 BITS
LOGIC FEATURES--Optional Output Enable
PACKAGE--28 PAD (PIN) RCC, 0.350" X 0.550"
PIN ASSIGNMENT--Fig. 3.7.3-9

3.7.3.8 16K BY 4 TTL SRAM IN RCC

CAPACITY--16K WORDS OF 4 BITS
PACKAGE--22 PAD (PIN) RCC, 0.290" X 0.490"
PIN ASSIGNMENT--Fig. 3.7.3-10

3.7.3.9 – 4K TO 1M BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN SOJ

4K, 16K, 64K, 256K, & 1M WORDS OF 4 BITS
LOGIC FEATURES—Optional Output Enable for some densities
—COMMON DATA INPUT & OUTPUT PINS
PACKAGE—24 or 28 PIN SOJ, 0.3" WIDE
—28 PIN SOJ, 0.3" or 0.4" WIDE
—32 PIN SOJ, UNDEFINED
Release 5 adds approval for the 64 X 4 part to be supplied in a 0.3" SOJ or TSOP–2
PIN ASSIGNMENT—Fig. 3.7.3–11

3.7.3.10 – 64K TO 4M BY 4 TTL SRAM IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—COMMON DATA INPUT & OUTPUT PINS
—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES
PACKAGE—28, 32, or 36 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—28 0r 32 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.3–12

3.7.3.11 – 64K TO 4M BY 4 TTL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES
PACKAGE—32 or 36 or 40 PIN SOJ, & TSOP2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 0r 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
CAPACITY—32K, 64K, 128K, 256K WORDS OF 8 BITS
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.3–13

3.7.3.12 – 64K TO 4M BY 4 SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—OUTPUT ENABLE FOR ALL DENSITIES
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.3–14

3.7.3.13 – 4K AND 16K BY 4 CACHE TAG SRAM IN DIP AND SOJ

CAPACITY—4K, 16K WORDS OF 4 BIT
LOGIC FEATURES—OPTIONAL ASHYNCHRONOUS CLEAR INPUT
PACKAGE—4K X 4, 22 PIN DIP AND SOJ, 0.3"
—16K X 4, 24 PIN DIP AND SOJ, 0.3"
PIN ASSIGNMENT—Fig. 3.7.3–15

3.7.3.14 – 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP AND SOJ

SEE PAR. 3.7.1.9 AND FIG. 3.7.1–9 FOR DETAILS OF THIS STANDARD

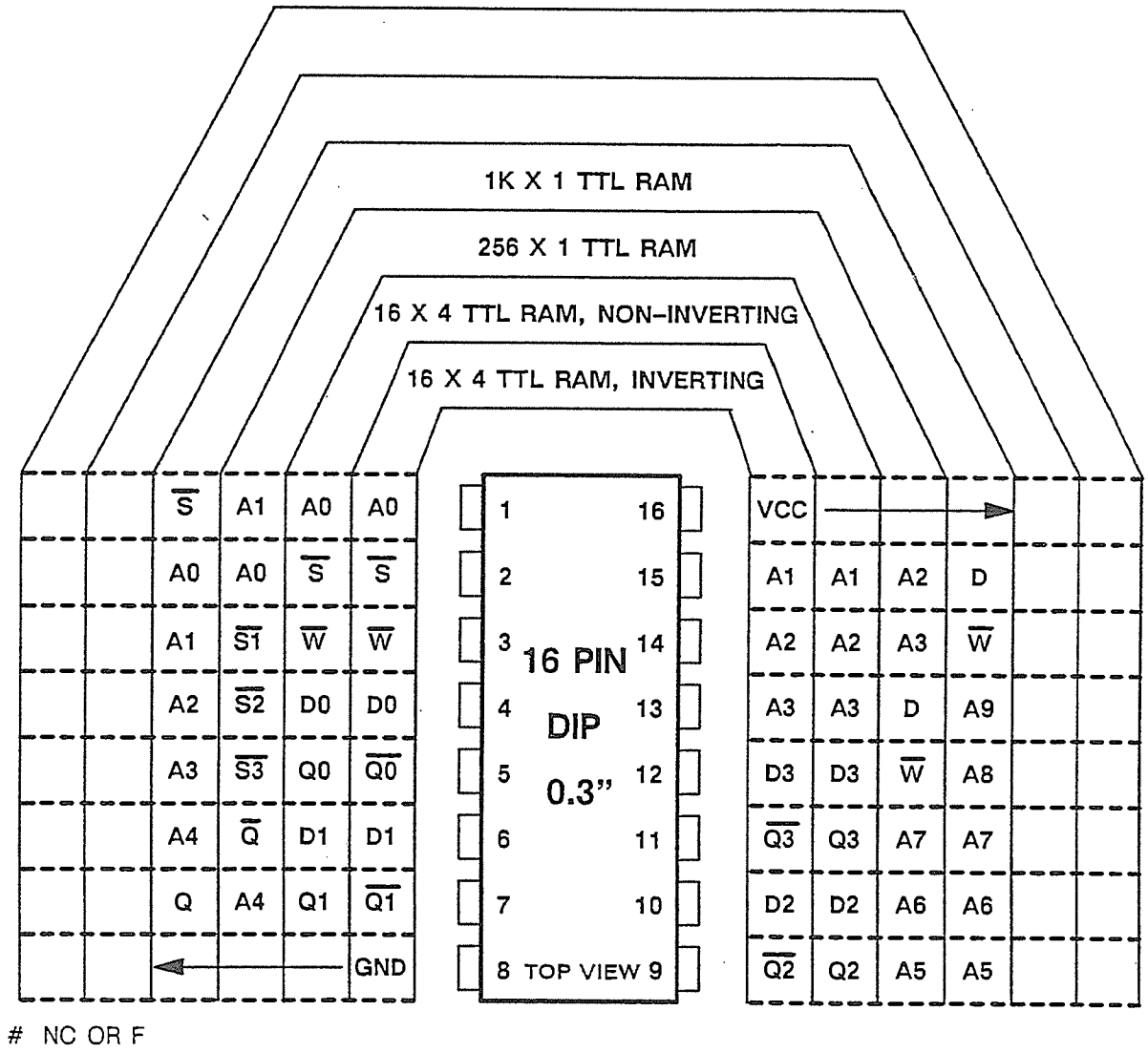


FIGURE 3.7.3-1
16 BY 4 INVERTING AND NON-INVERTING TTL SRAM IN DIP

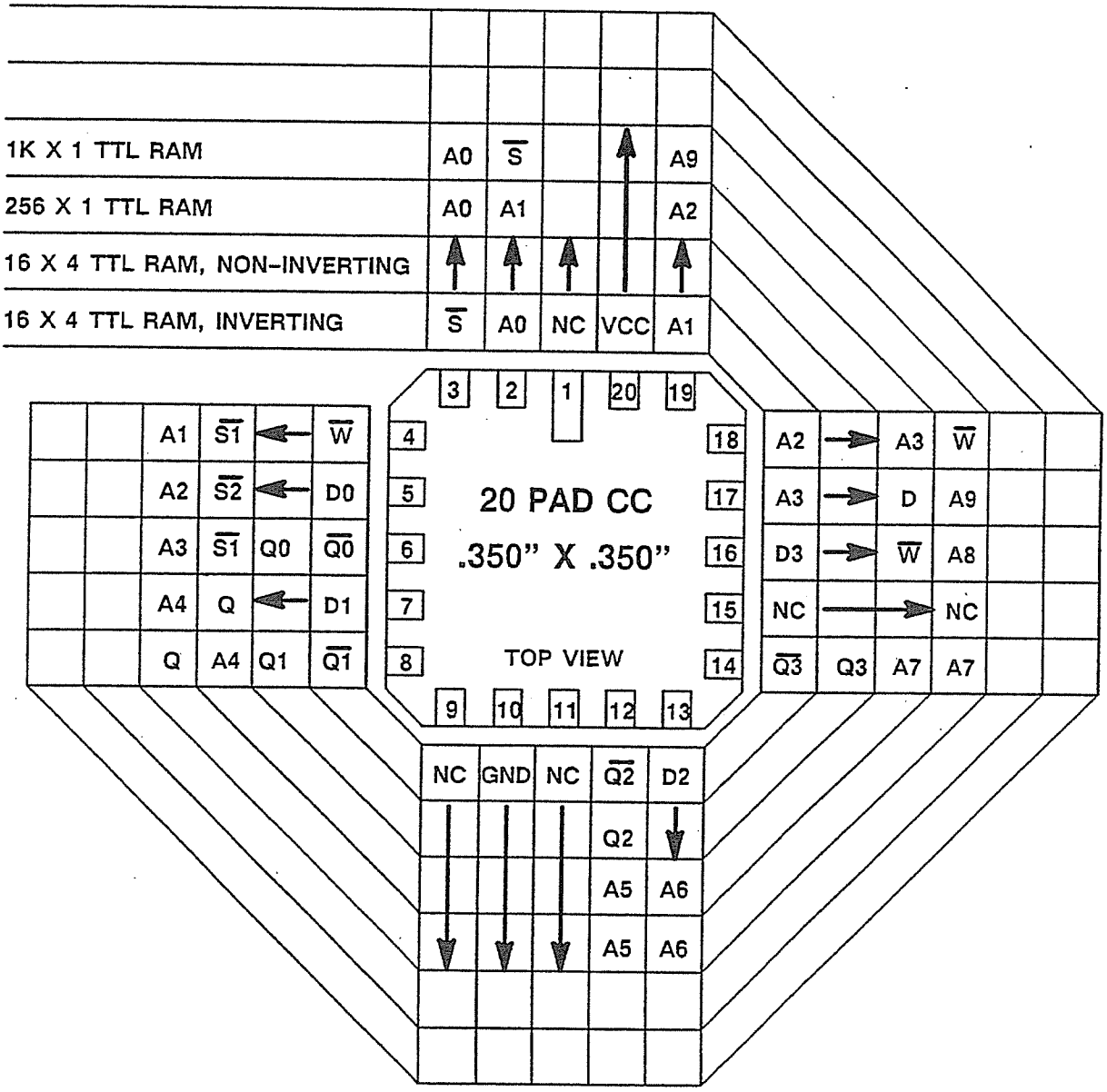


FIGURE 3.7.3-2
16 BY 4 INVERTING AND NON-INVERTING TTL SRAM IN SCC

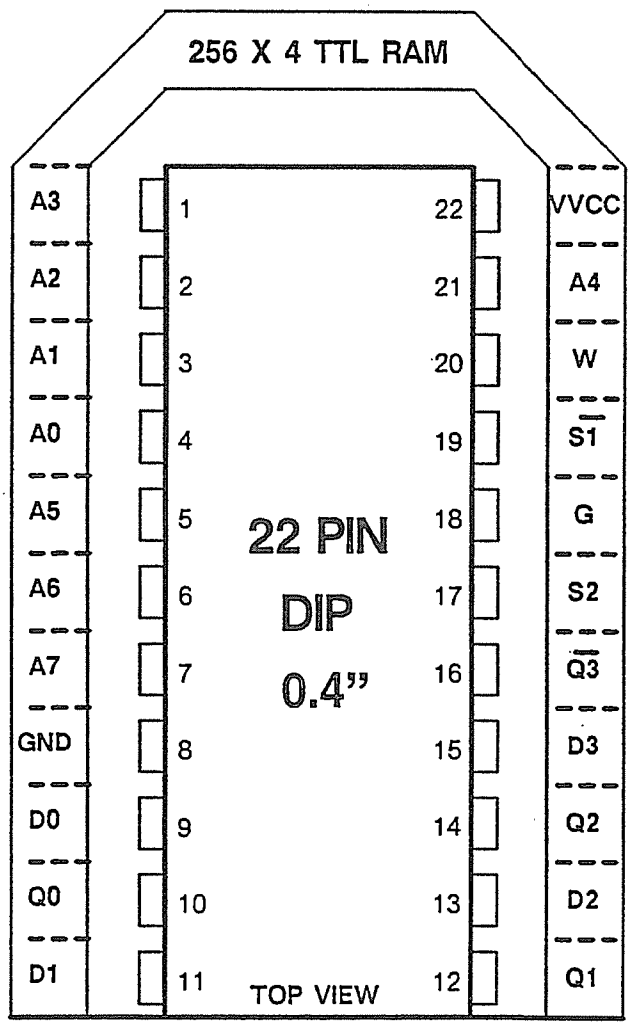


FIGURE 3.7.3-3
256 BY 4 TTL SRAM IN DIP

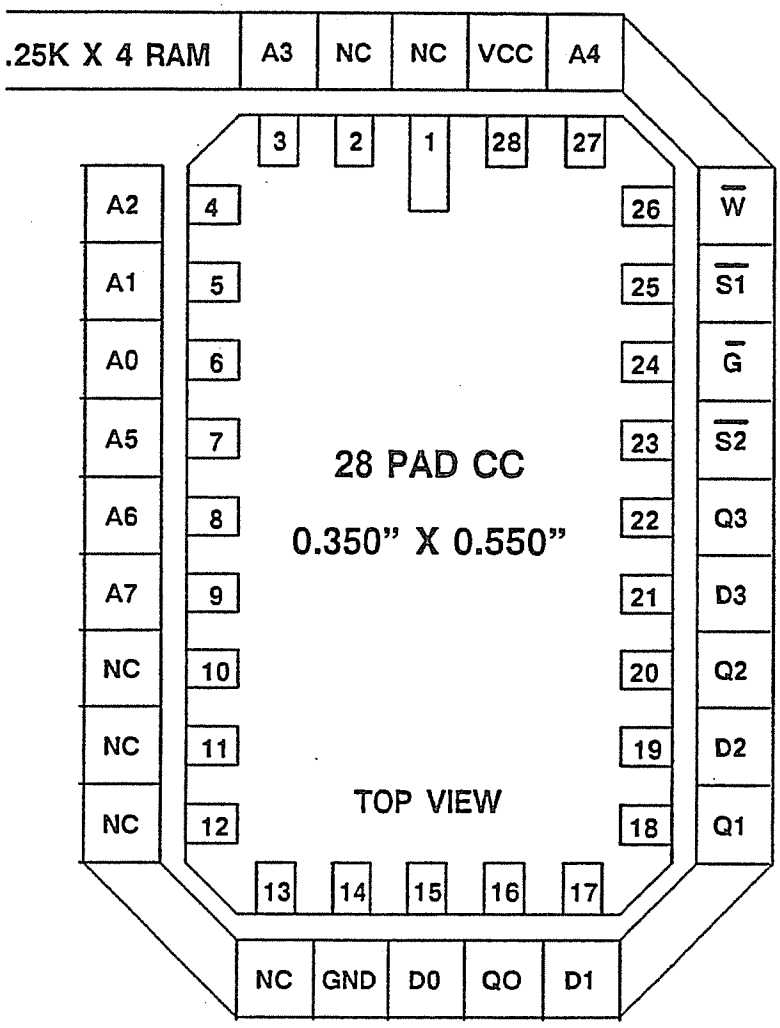


FIGURE 3.7.3-4
256 BY 4 TTL SRAM IN RCC

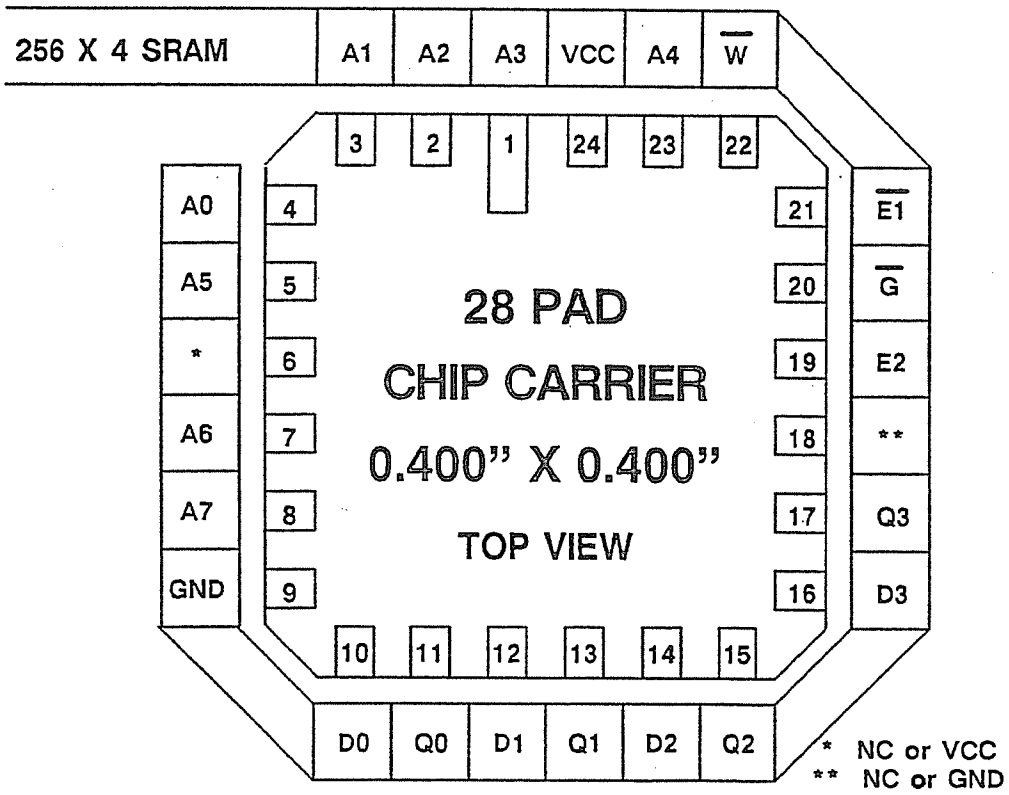


FIGURE 3.7.3-5
256 BY 4 TTL SRAM IN SCC

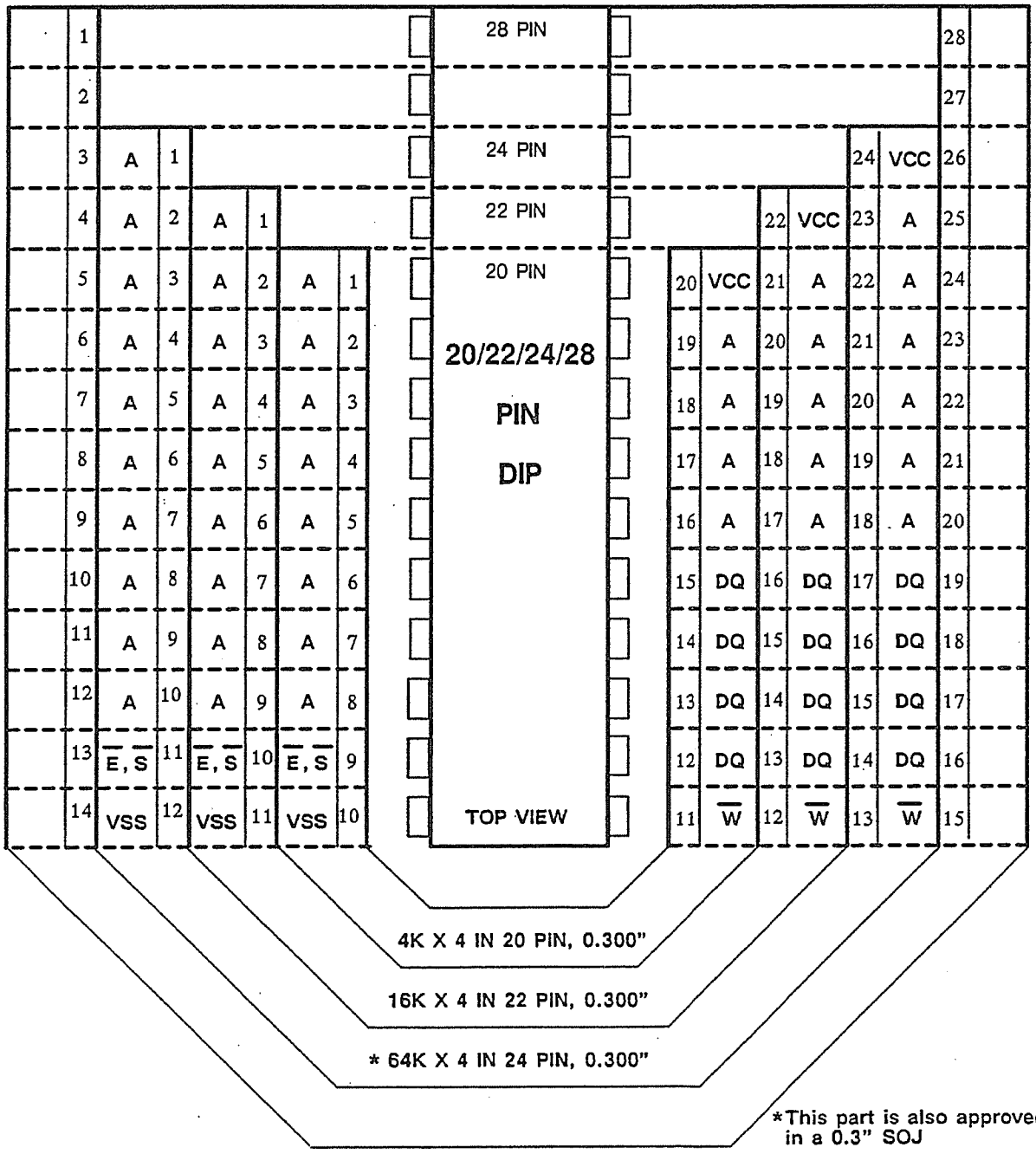


FIGURE 3.7.3-6
4K TO 64K BY 4 TTL SRAM FAMILY WITHOUT $\overline{G}$ IN DIP

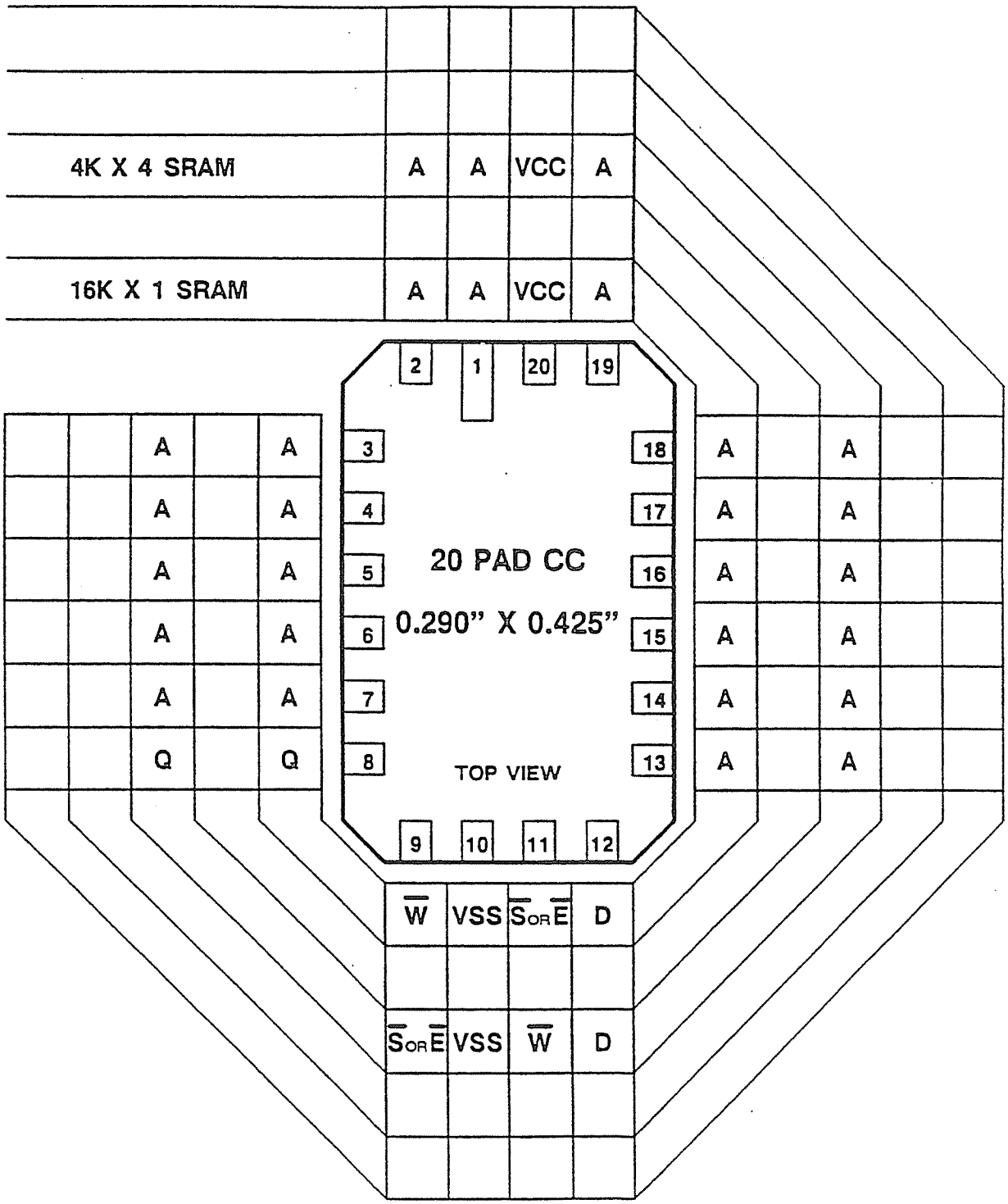


FIGURE 3.7.3-7
4K BY 4 TTL SRAM IN RCC

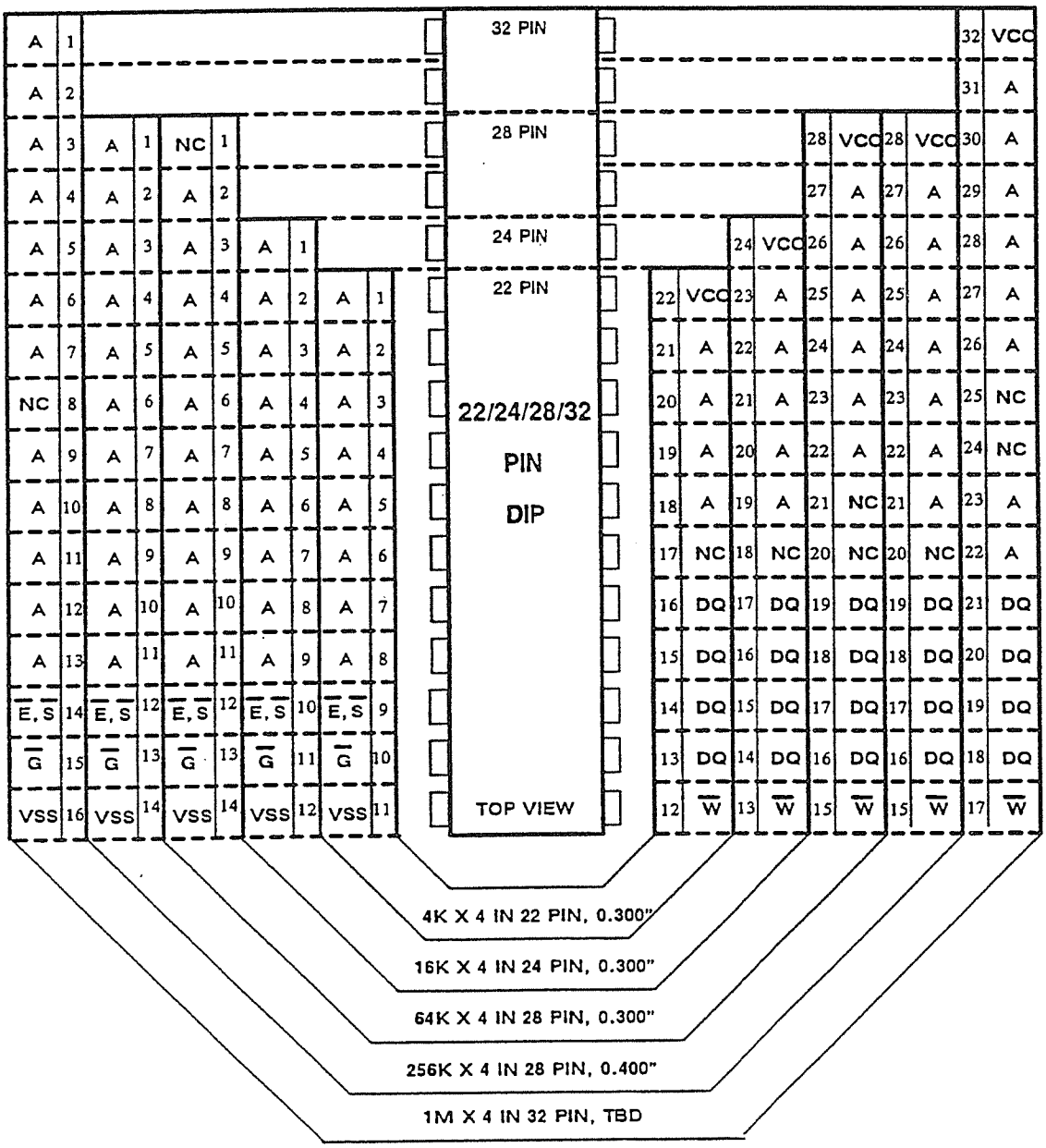


FIGURE 3.7.3-8
4K TO 256K BY 4 TTL SRAM FAMILY WITH $\overline{G}$ IN DIP

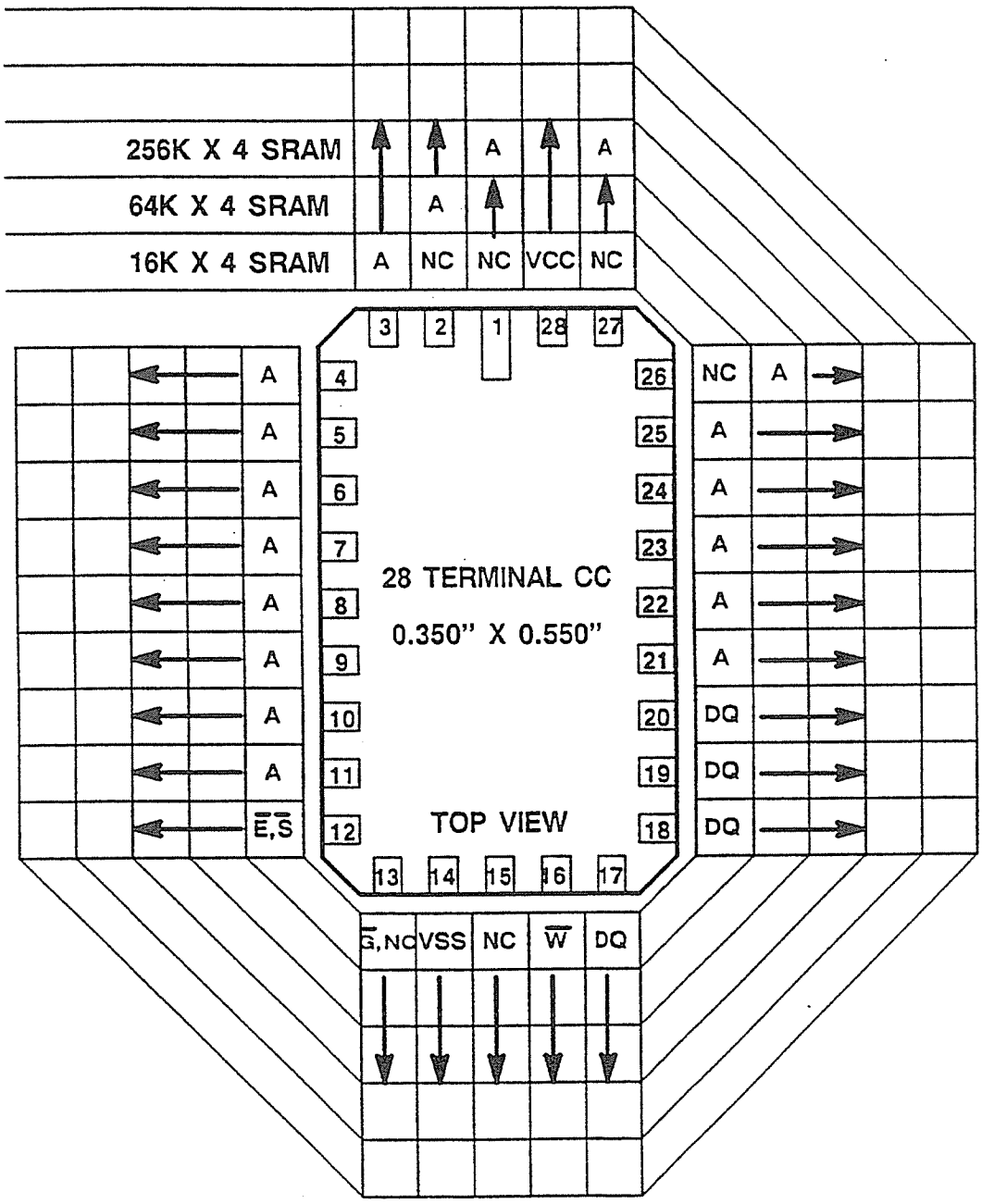


FIGURE 3.7.3-9
16K TO 256K BY 4 TTL SRAM FAMILY IN RCC

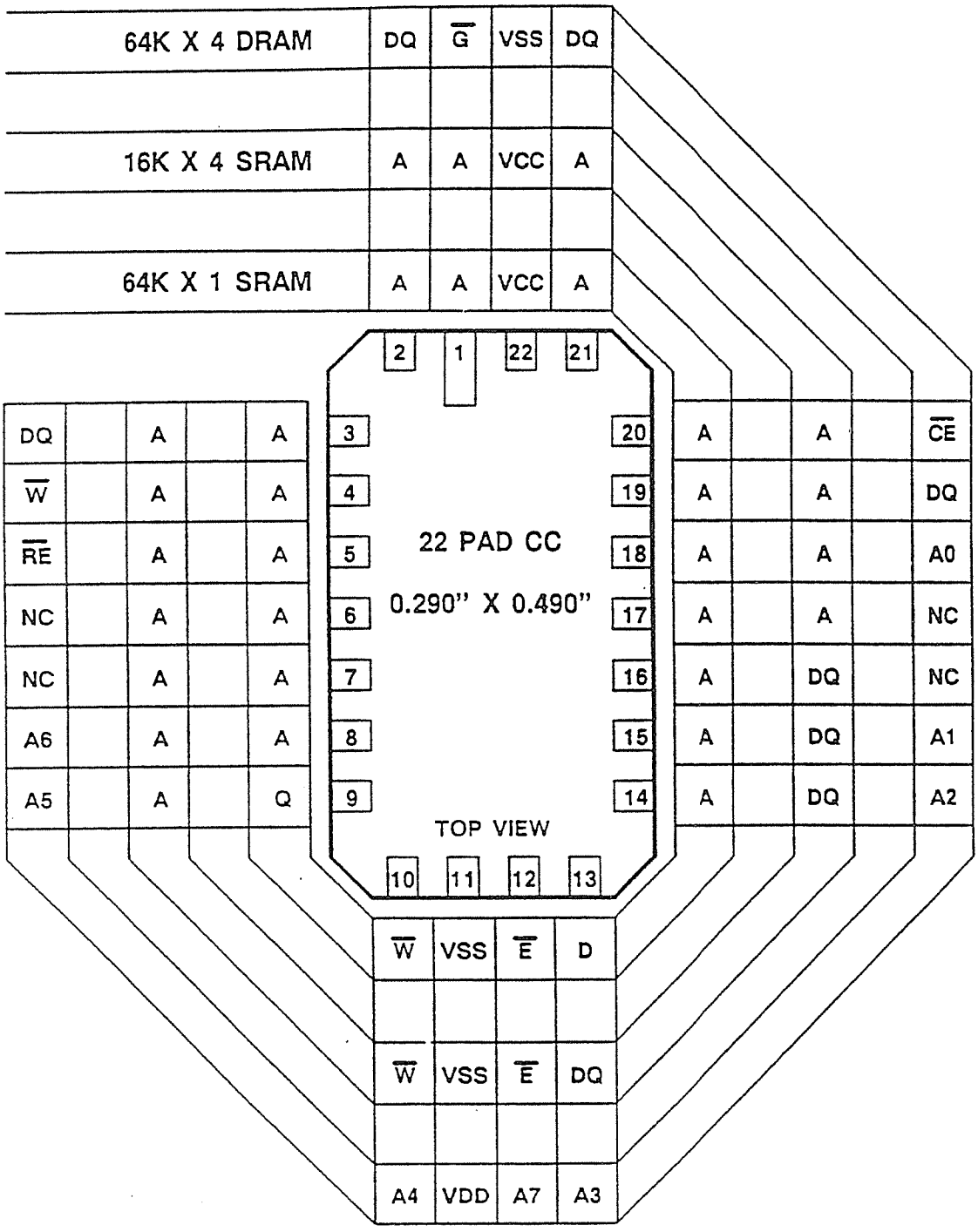
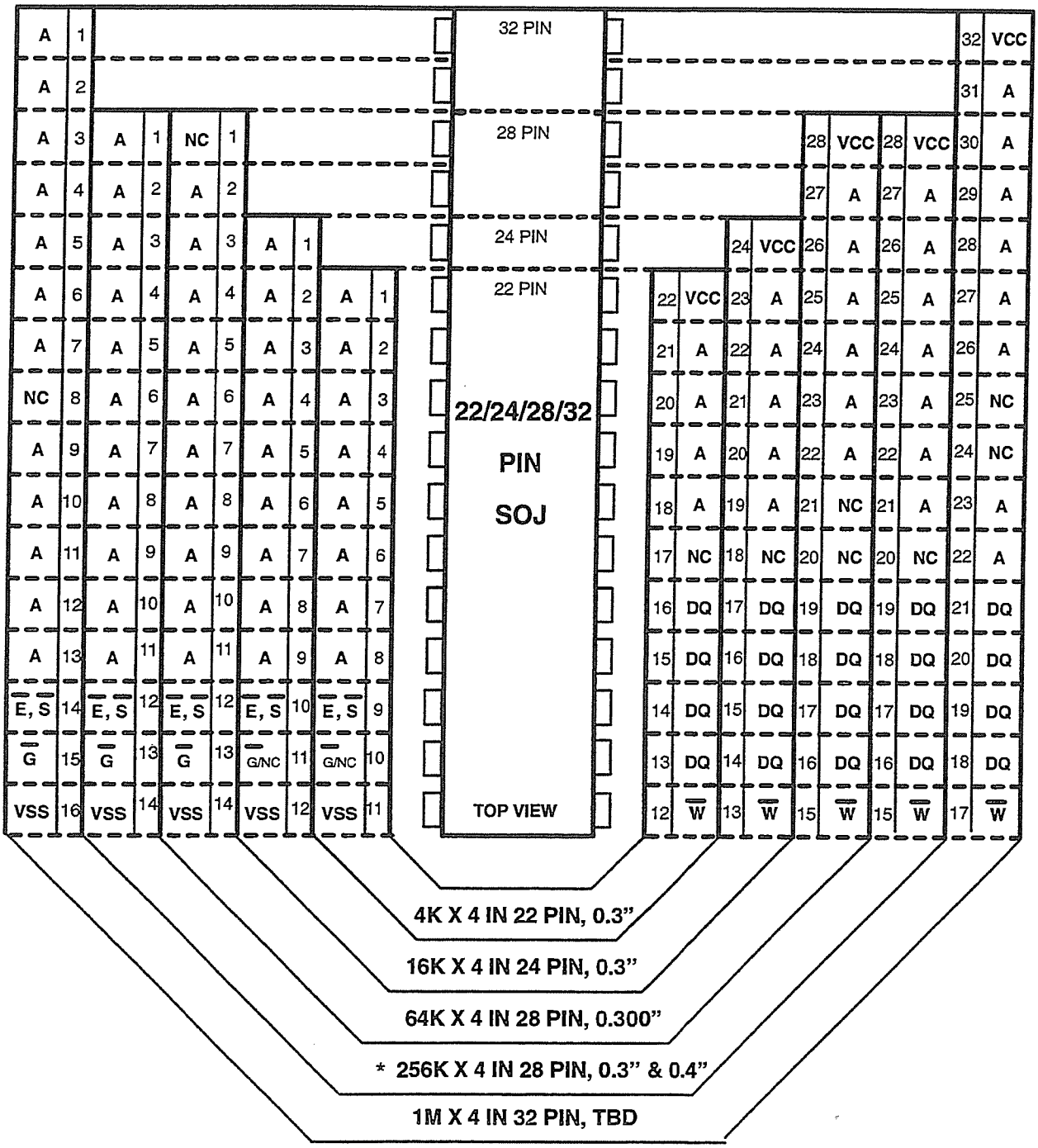


FIGURE 3.7.3-10
16K BY 4 TTL SRAM IN RCC

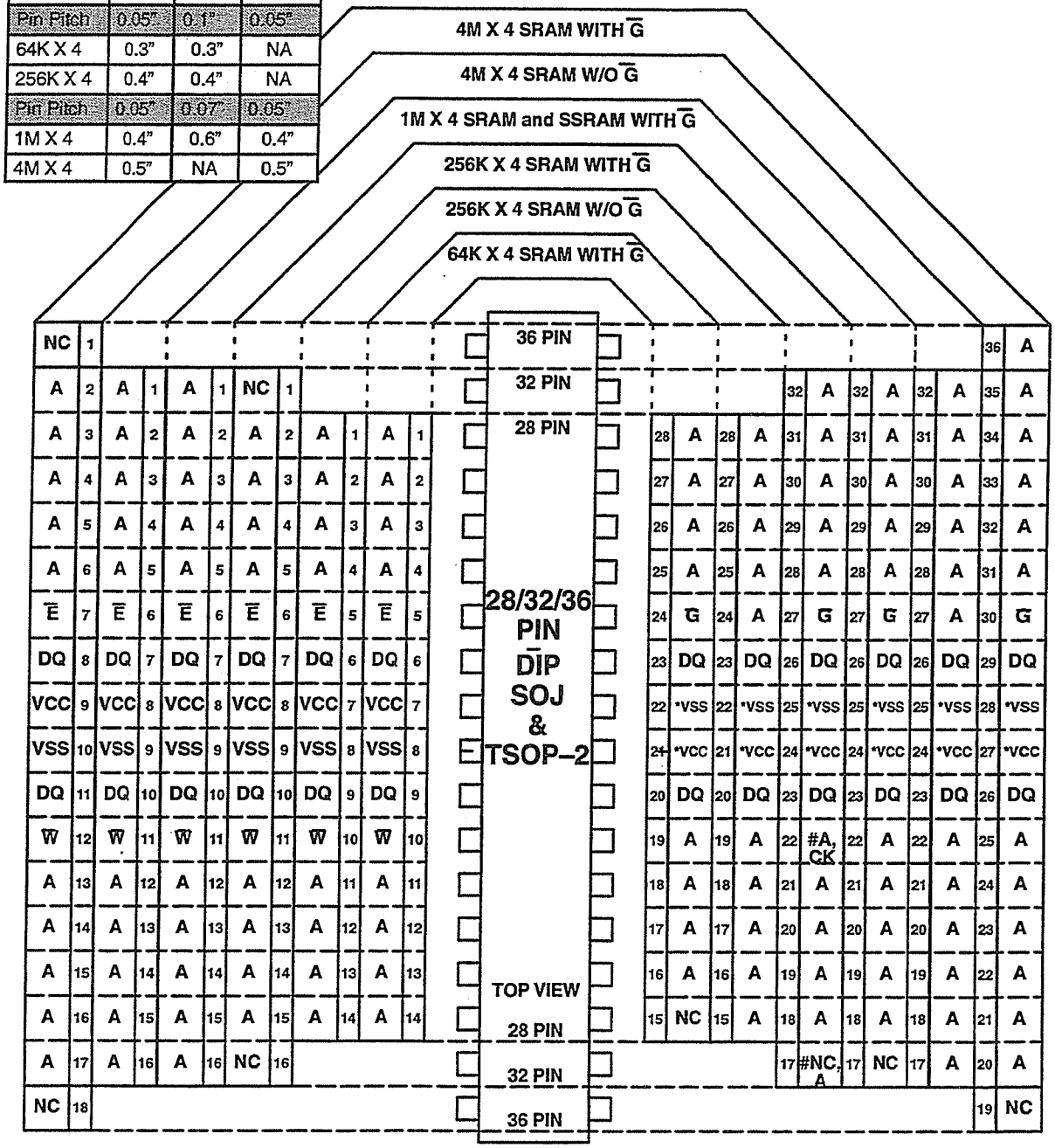


* The 256K X 4 part is also approved for use in a 0.3" TSOP–2 package.

FIGURE 3.7.3–11

4K TO 1M BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN SOJ

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"



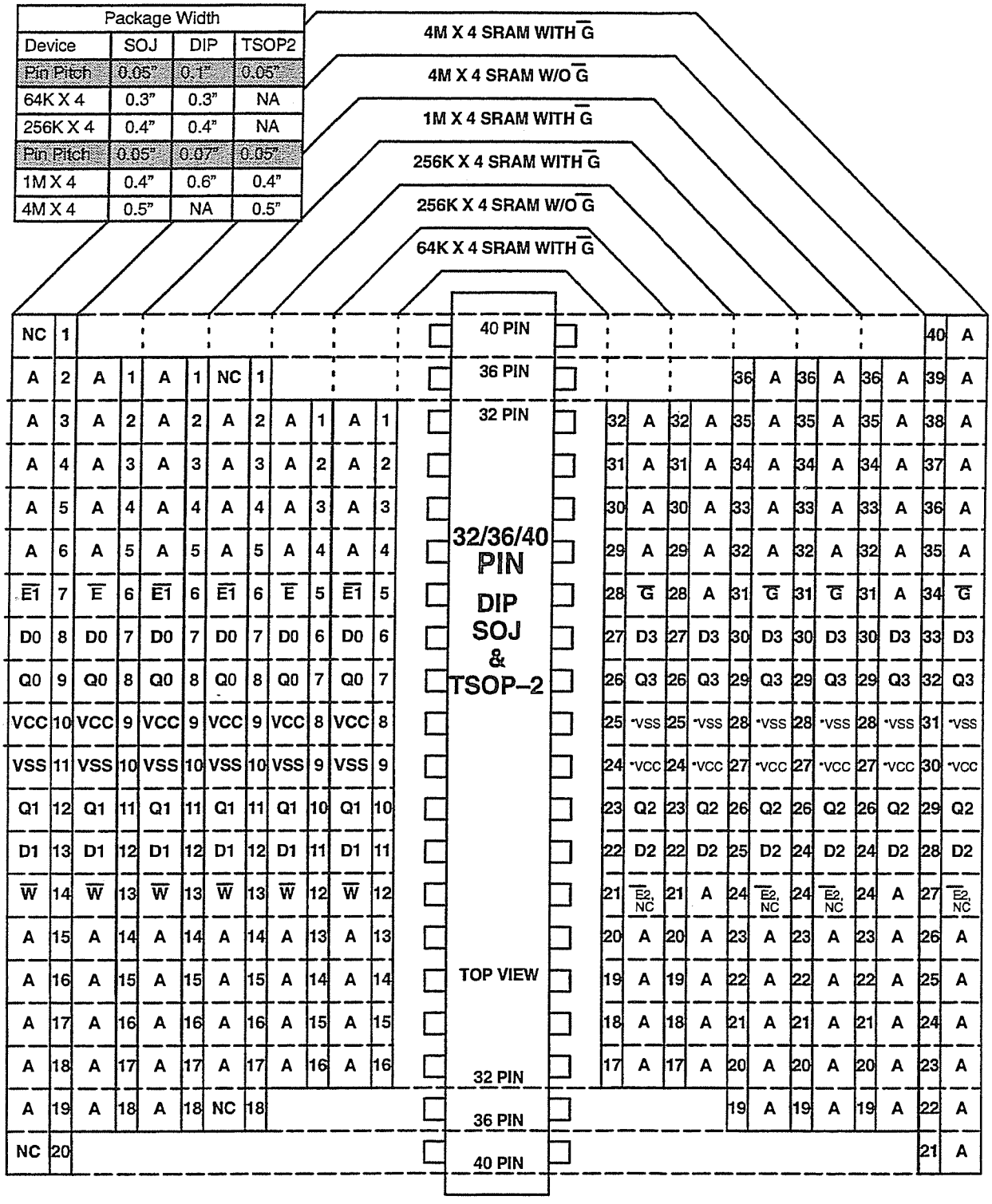
* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option
# NOTE: For the 1M X 4 devices, the pin assignments for pins 17 & 22 are different for the SRAM and SSRAM as follows.
For SRAM, P17 = NC, P22 = A
For SSRAM, P17 = A, P22 = CK

FIGURE 3.7.3–12

64K TO 4M BY 4 TTL SRAM FAMILY IN DIP, TSOP2, AND SOJ

Release 4

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"



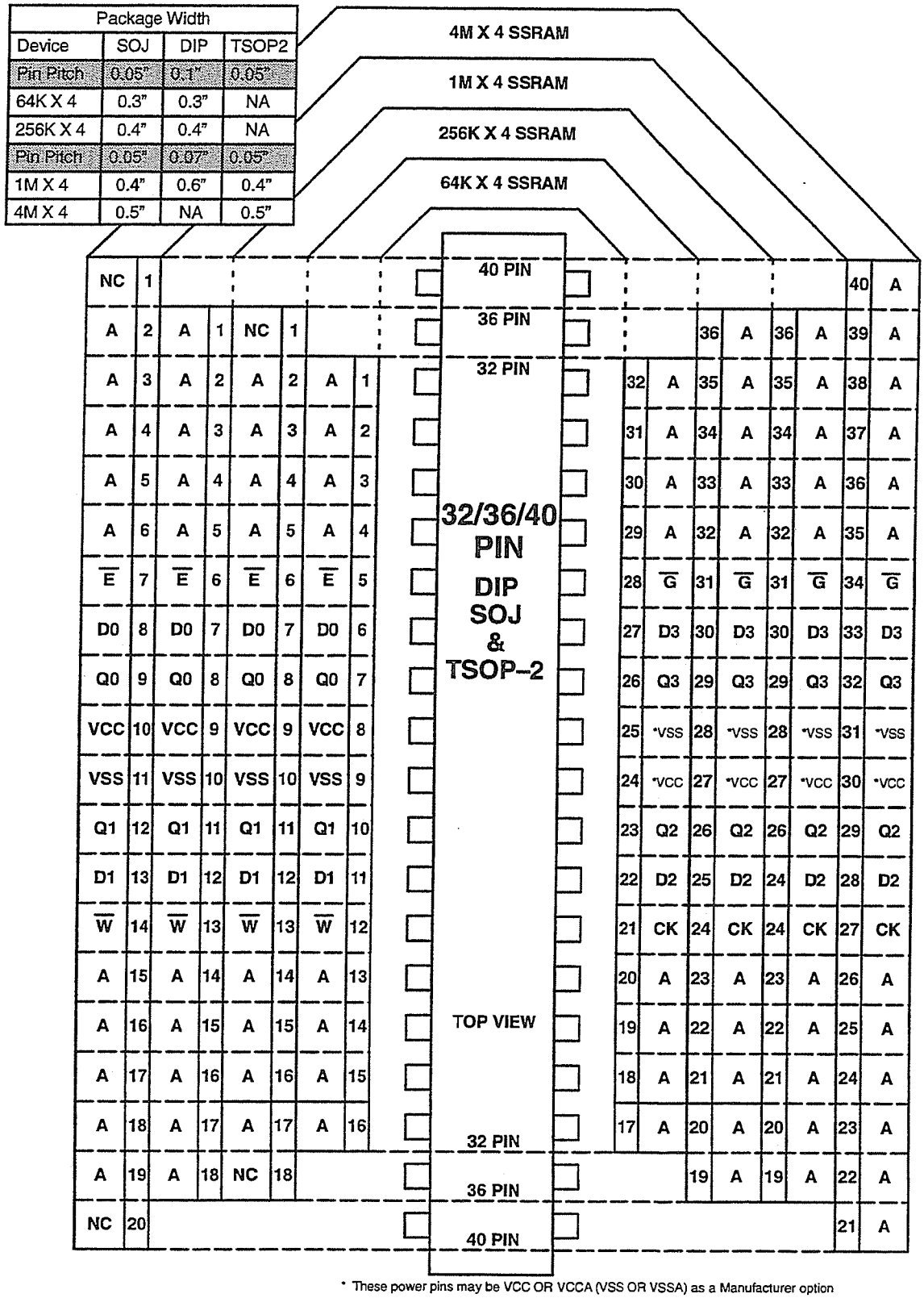
* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.3–13

64K TO 4M BY 4 TTL SRAM FAMILY WITH SEPARATE DATA I/O IN DIP, TSOP2, AND SOJ

Release 4

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"



* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.3–14

64K TO 4M BY 4 SYNCHRONOUS SRAM (SSRAM) FAMILY IN DIP,SOJ,AND TSOP–2

Release 4

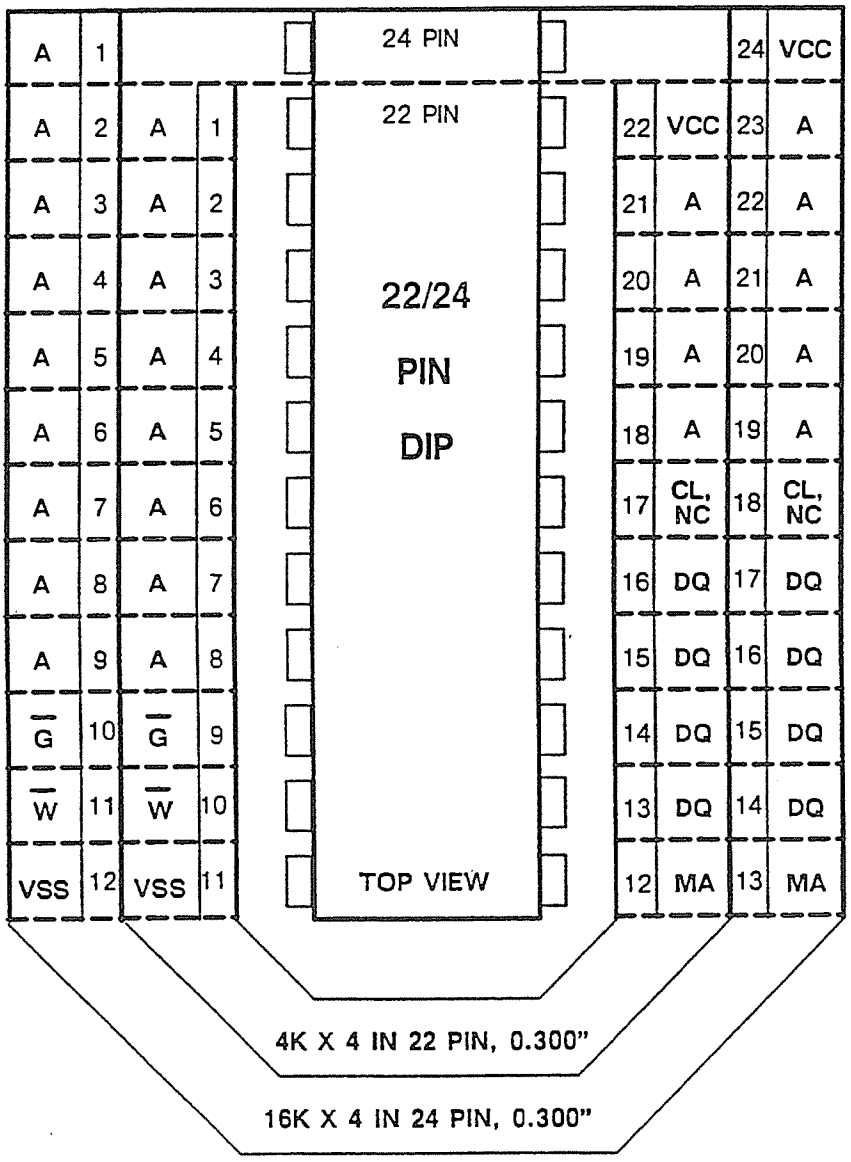


FIGURE 3.7.3-15
4K AND 16K BY 4 CACHE TAG SRAM IN DIP AND SOJ

3.7.4 Nibble Wide ECL SRAM

All of the following standards are for devices which operate with ECL interface levels and power voltages.

3.7.4.1 – .25K AND 1K BY 4, 100K ECL SRAM IN DIP AND SFP

CAPACITY—256, WORDS OF 4 BITS
ELECTRICAL INTERFACE—100K ECL
There are two versions of this part: one in SFP and the other in DIP
PACKAGE—24 PIN DIP, 0.4" WIDE
PIN ASSIGNMENT—Fig. 3.7.4–1
PACKAGE—24 PIN SFP, 0.380" BY 0.380"
PIN ASSIGNMENT—Fig. 3.7.4–2
This standard was developed by Committee 42.1.

3.7.4.2 – 1K TO 16K BY 4, 10K & 100K ECL SRAM IN DIP

CAPACITY—1K, 4K, & 16K, WORDS OF 4 BITS
ELECTRICAL INTERFACE—10K or 100K ECL
—USES 100K ECL CENTERED POWER PINS
PACKAGE—1K in 24 PIN DIP, 0.4" WIDE
—4K & 16K in 28 PIN DIP, 0.4" WIDE
PIN ASSIGNMENT—Fig. 3.7.4–1
This standard was developed by Committee 42.1.

3.7.4.3 – .25K TO 16K BY 4, 10K & 100K ECL SRAM FAMILY IN DIP

CAPACITY—256, 1K, 4K, 16K WORDS OF 4 BITS
ELECTRICAL INTERFACE—10K ECL
—USES 10K ECL CORNERED POWER PINS
—4K part, also 100K ECL
PACKAGE—.25K & 1K, 24 PIN DIP, 0.4" WIDE
—4K & 16K, 28 PIN DIP, 0.4" WIDE
PIN ASSIGNMENT—Fig. 3.7.4–4
This standard was developed by Committee 42.1.

3.7.4.4 – 16K BY 4,10K & 100K ECL SSRAM IN DIP

CAPACITY—16K, WORDS OF 4 BITS
ELECTRICAL INTERFACE—10K or 100K ECL
—USES 100K ECL CENTERED POWER PINS
PACKAGE—32 PIN DIP, 0.4" WIDE
THESE DEVICES CONTAIN BUILT IN WRITE CYCLE TIMING
PIN ASSIGNMENT—Fig. 3.7.4–5
This standard was developed by Committee 42.1.

3.7.4.5 – 64K TO 4M BY 4 ECL SRAM IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURE—COMMON DATA INPUT & OUTPUT PINS
—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES
ELECTRICAL INTERFACE—ECL
PACKAGE—28, 32, or 36 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—28 0r 32 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–6

3.7.4.6 – 64K TO 4M BY 4 ECL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES
ELECTRICAL INTERFACE—ECL
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–7

3.7.4.7 – 64K TO 4M BY 4 ECL SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—OUTPUT ENABLE FOR ALL DENSITIES
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–8

3.7.4.8 – 64K BY 4 ECL SRAM IN FP

CAPACITY—64K WORDS OF 4 BITS
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—28 PIN FP, 0.535" WIDE, 0.030" LEAD PITCH
PIN ASSIGNMENT—Fig. 3.7.4–9

3.7.4.9 – 256K BY 4/512K BY 2 RECONFIGURABLE SRAM IN DIP & SOJ

CAPACITY—256K WORDS OF 4 BITS OR 512K WORDS OF 2 BITS
LOGIC FEATURES—RECONFIGURABLE CAPACITY & DATA INTERFACE
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—32 PIN DIP or SOJ, 0.4" wide
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–10

3.7.4.10 – 64K TO 4M BY 4 SRAM FAMILY IN DIP AND SOJ IN DIP, SOJ, AND TSOP–2

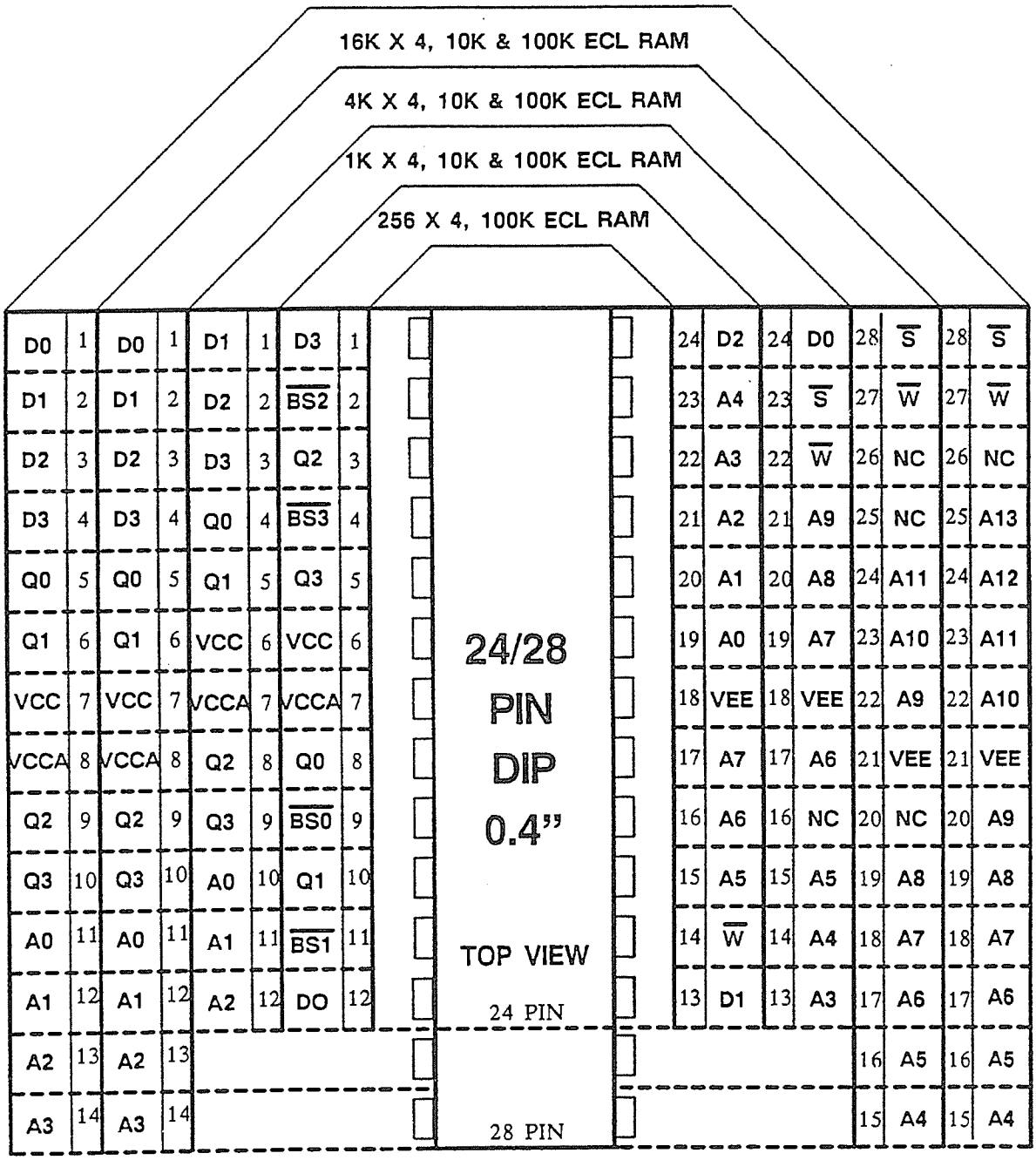
CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—BIT SELECTION
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—36 or 40 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—36 or 40 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–11

3.7.4.11 – 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—DIFFERENTIAL CLOCKS
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–12

3.7.4.12 – 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—BIT SELECTION
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—36, 40, or 44 PIN SOJ, & TSOP2, 0.3", 0.4". or 0.5" wide
—36, 40, or 44 PIN DIP, 0.3", 0.4", or 0.6" wide..
PACKAGE—36, 40, or 44 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—36 or 40 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–13



D0	1	D0	1	D1	1	D3	1			24	D2	24	D0	28	$\overline{S}$	28	$\overline{S}$
D1	2	D1	2	D2	2	$\overline{BS2}$	2			23	A4	23	$\overline{S}$	27	$\overline{W}$	27	$\overline{W}$
D2	3	D2	3	D3	3	Q2	3			22	A3	22	$\overline{W}$	26	NC	26	NC
D3	4	D3	4	Q0	4	$\overline{BS3}$	4			21	A2	21	A9	25	NC	25	A13
Q0	5	Q0	5	Q1	5	Q3	5			20	A1	20	A8	24	A11	24	A12
Q1	6	Q1	6	VCC	6	VCC	6			19	A0	19	A7	23	A10	23	A11
VCC	7	VCC	7	VCCA	7	VCCA	7			18	VEE	18	VEE	22	A9	22	A10
VCCA	8	VCCA	8	Q2	8	Q0	8			17	A7	17	A6	21	VEE	21	VEE
Q2	9	Q2	9	Q3	9	$\overline{BS0}$	9			16	A6	16	NC	20	NC	20	A9
Q3	10	Q3	10	A0	10	Q1	10			15	A5	15	A5	19	A8	19	A8
A0	11	A0	11	A1	11	$\overline{BS1}$	11			14	$\overline{W}$	14	A4	18	A7	18	A7
A1	12	A1	12	A2	12	DO	12			13	D1	13	A3	17	A6	17	A6
A2	13	A2	13											16	A5	16	A5
A3	14	A3	14											15	A4	15	A4

FIGURE 3.7.4-1
256 BY 4, 100K ECL SRAM IN DIP
1K TO 16K BY 4, 10K & 100K ECL SRAM IN DIP

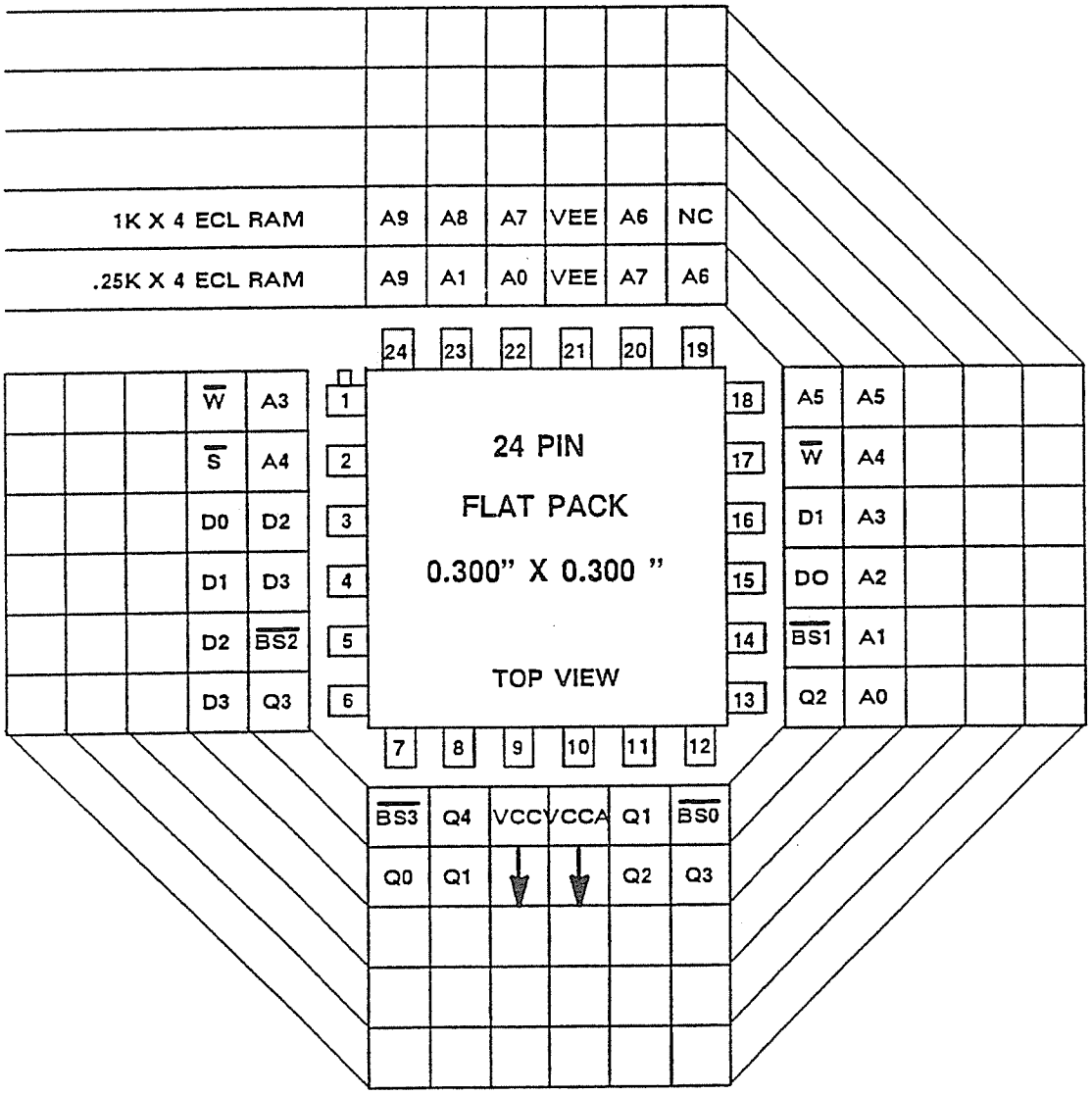
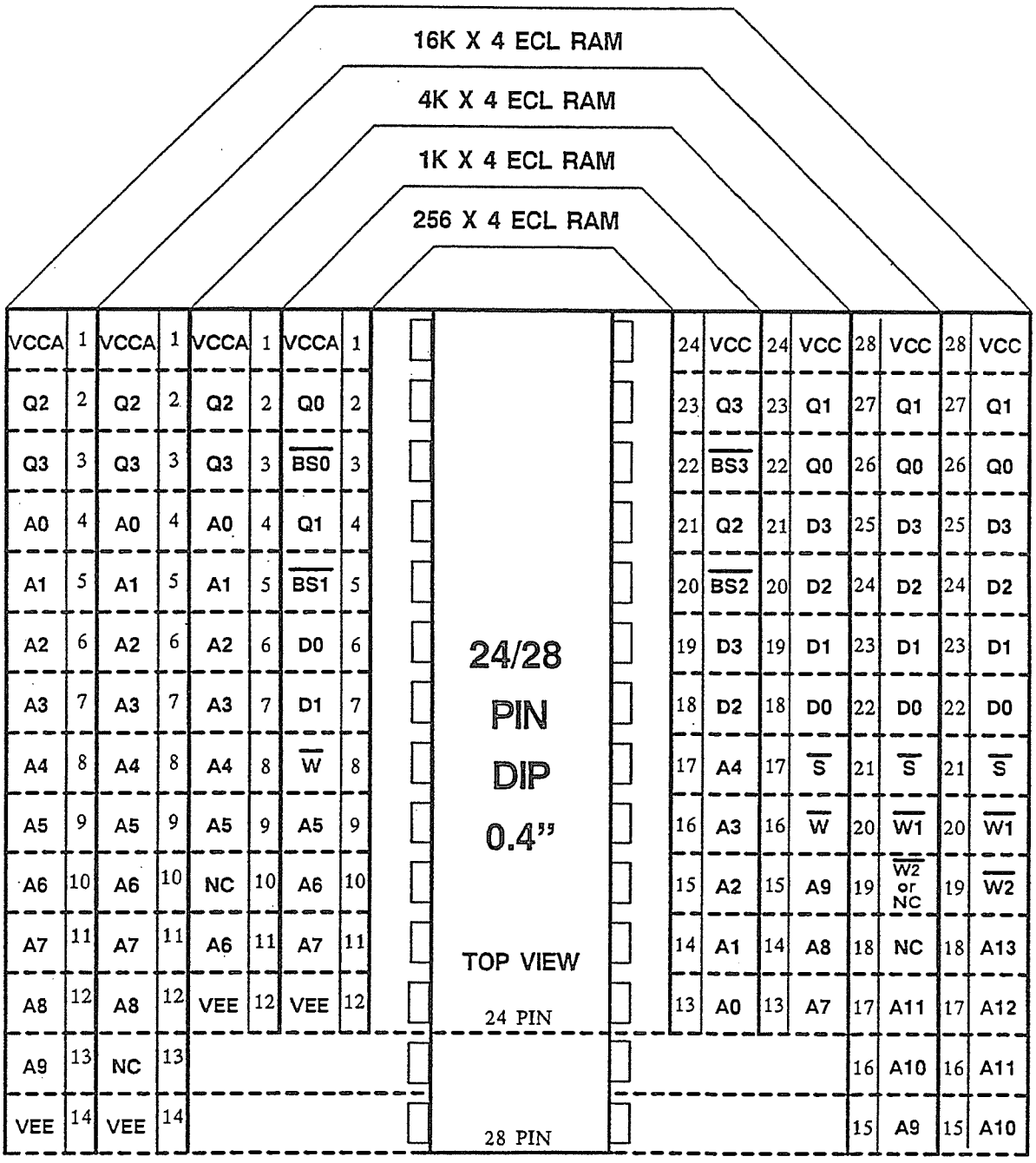


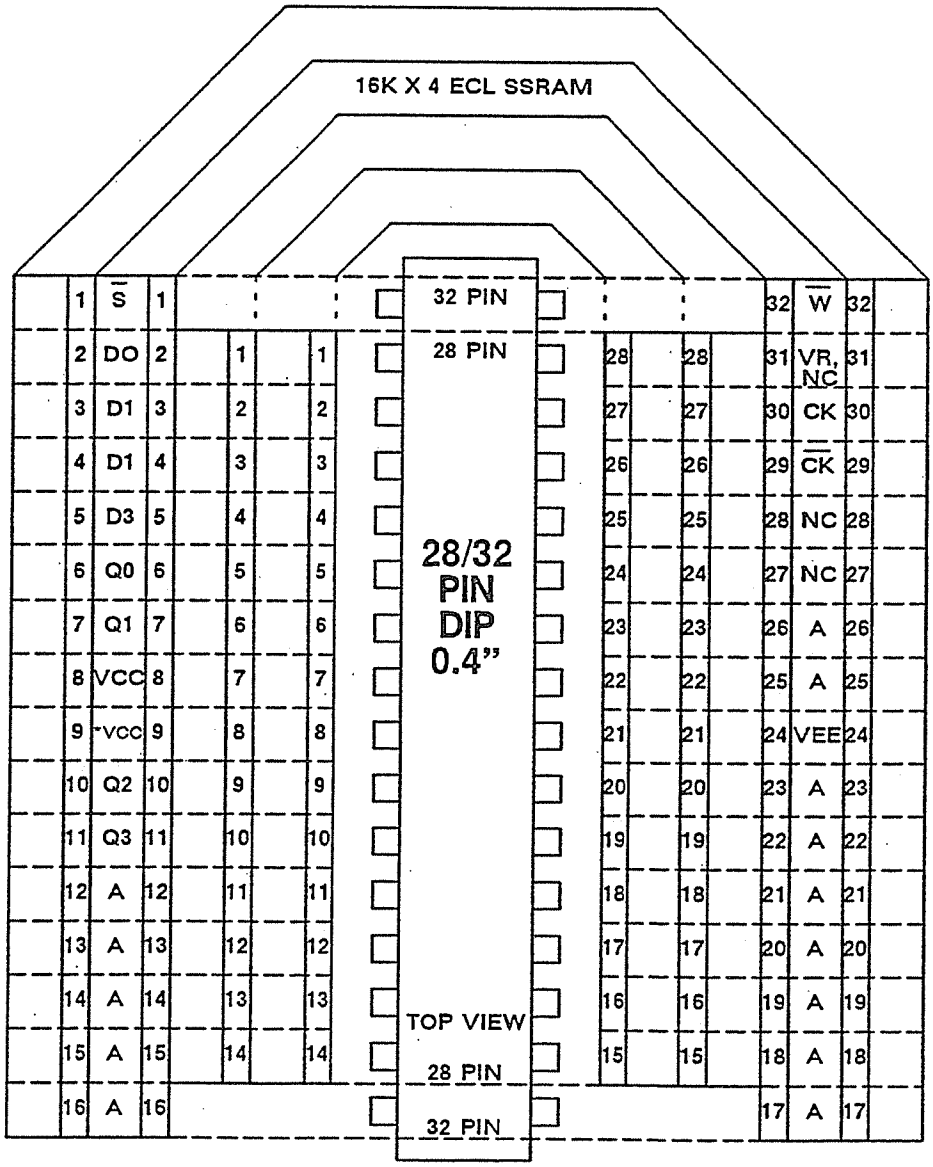
FIGURE 3.7.4-2
256 & 1K BY 4, 100K ECL SRAM IN SFP

Release 1



VCCA	1	VCCA	1	VCCA	1	VCCA	1			24	VCC	24	VCC	28	VCC	28	VCC		
Q2	2	Q2	2	Q2	2	Q0	2			23	Q3	23	Q1	27	Q1	27	Q1		
Q3	3	Q3	3	Q3	3	$\overline{BS0}$	3			22	$\overline{BS3}$	22	Q0	26	Q0	26	Q0		
A0	4	A0	4	A0	4	Q1	4			21	Q2	21	D3	25	D3	25	D3		
A1	5	A1	5	A1	5	$\overline{BS1}$	5			20	$\overline{BS2}$	20	D2	24	D2	24	D2		
A2	6	A2	6	A2	6	D0	6			19	D3	19	D1	23	D1	23	D1		
A3	7	A3	7	A3	7	D1	7			18	D2	18	D0	22	D0	22	D0		
A4	8	A4	8	A4	8	$\overline{W}$	8			17	A4	17	$\overline{S}$	21	$\overline{S}$	21	$\overline{S}$		
A5	9	A5	9	A5	9	A5	9			16	A3	16	$\overline{W}$	20	$\overline{W1}$	20	$\overline{W1}$		
A6	10	A6	10	NC	10	A6	10			15	A2	15	A9	19	$\overline{W2}$ or NC	19	$\overline{W2}$		
A7	11	A7	11	A6	11	A7	11			14	A1	14	A8	18	NC	18	A13		
A8	12	A8	12	VEE	12	VEE	12			13	A0	13	A7	17	A11	17	A12		
A9	13	NC	13											16	A10	16	A11		
VEE	14	VEE	14											15	A9	15	A10		

FIGURE 3.7.4-4
.25K TO 16K BY 4, 10K & 100K ECL SRAM FAMILY IN DIP



* This power pin may be VCC or VCCA as a manufacturers option

VR = ECL Threshold Reference Voltage

FIGURE 3.7.4-5
16K BY 4, 10K & 100K ECL SSRAM IN DIP

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"

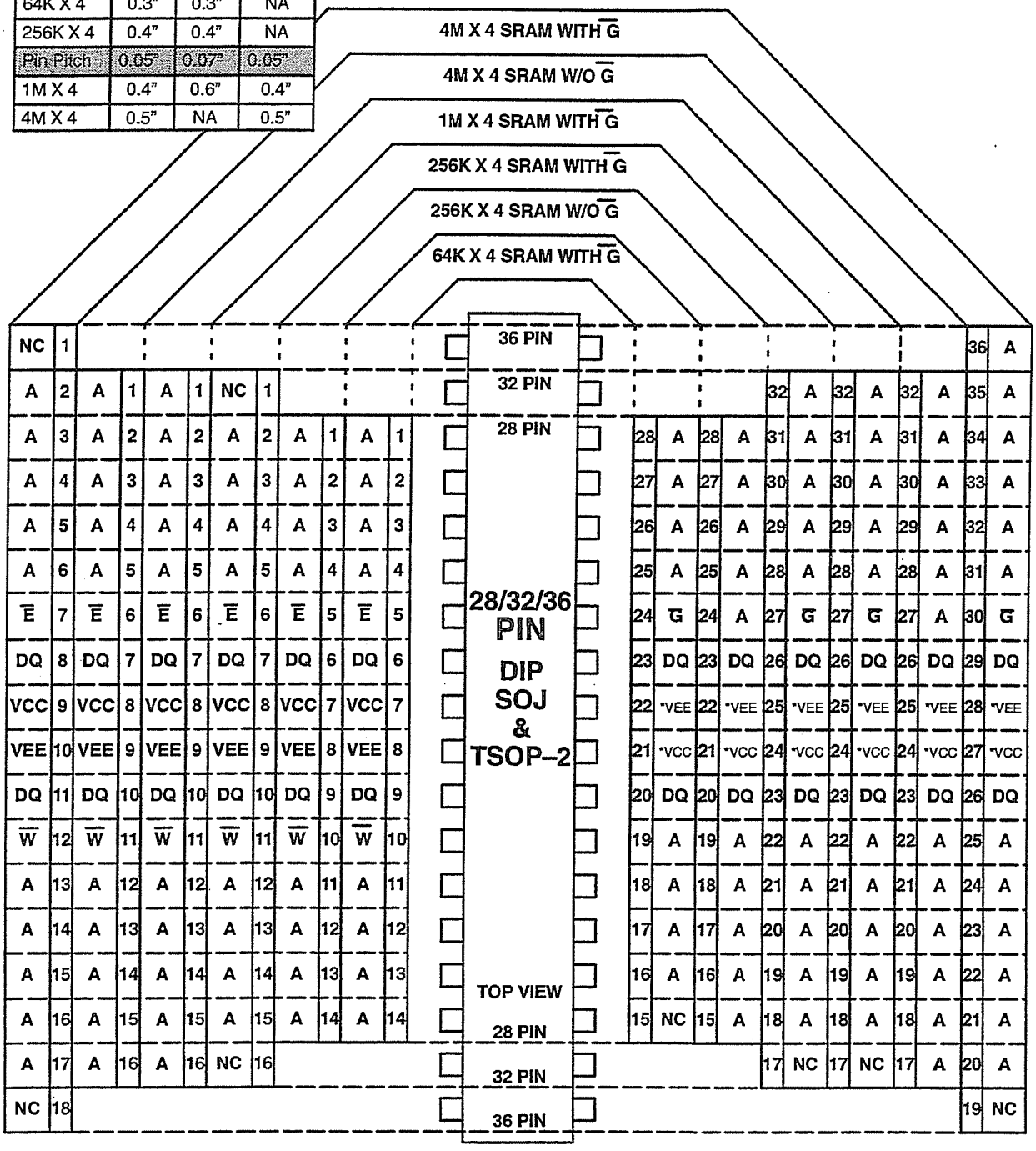
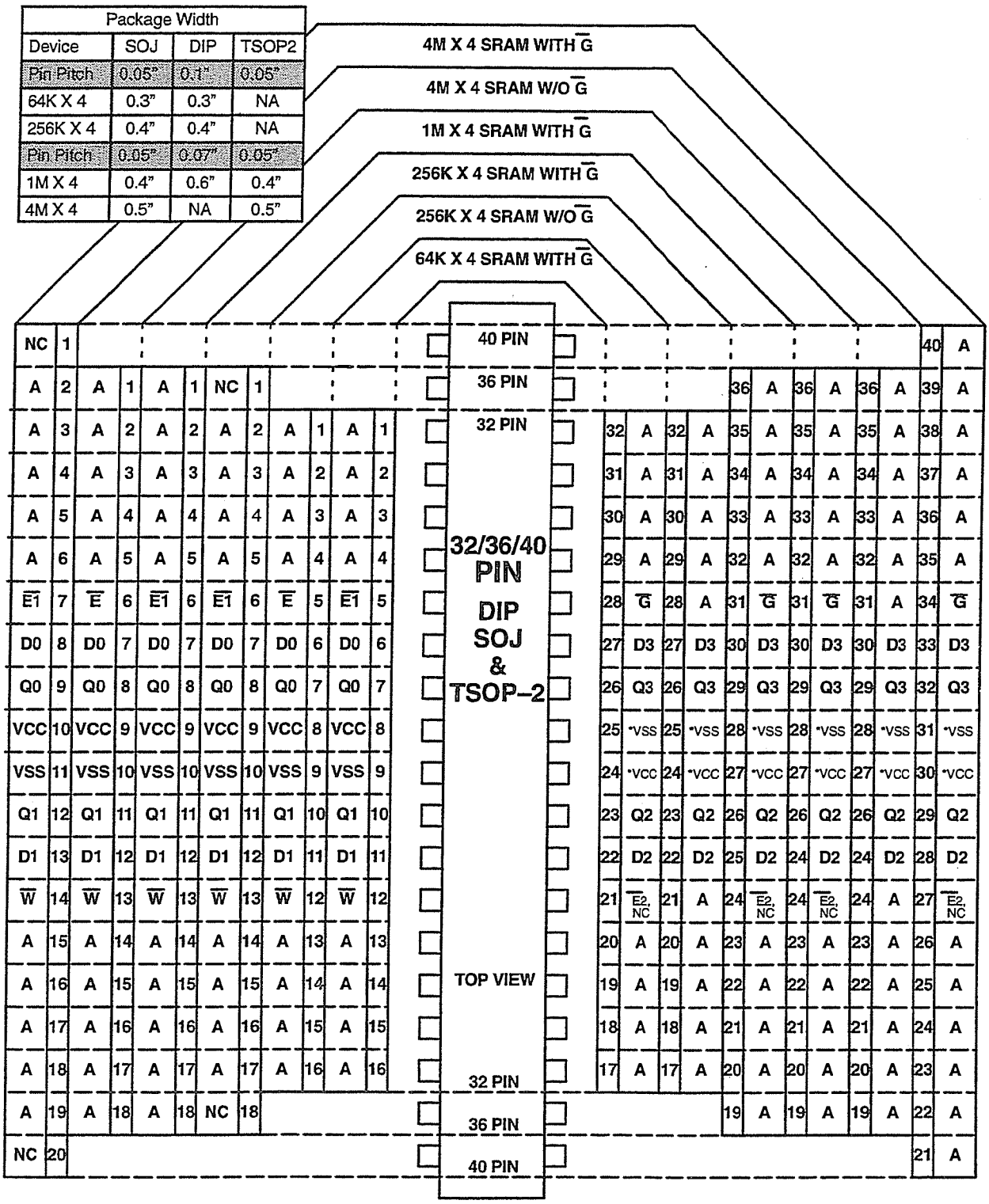


FIGURE 3.7.4–6

64K TO 4M BY 4 ECL SRAM FAMILY IN DIP, SOJ, AND TSOP–2

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"



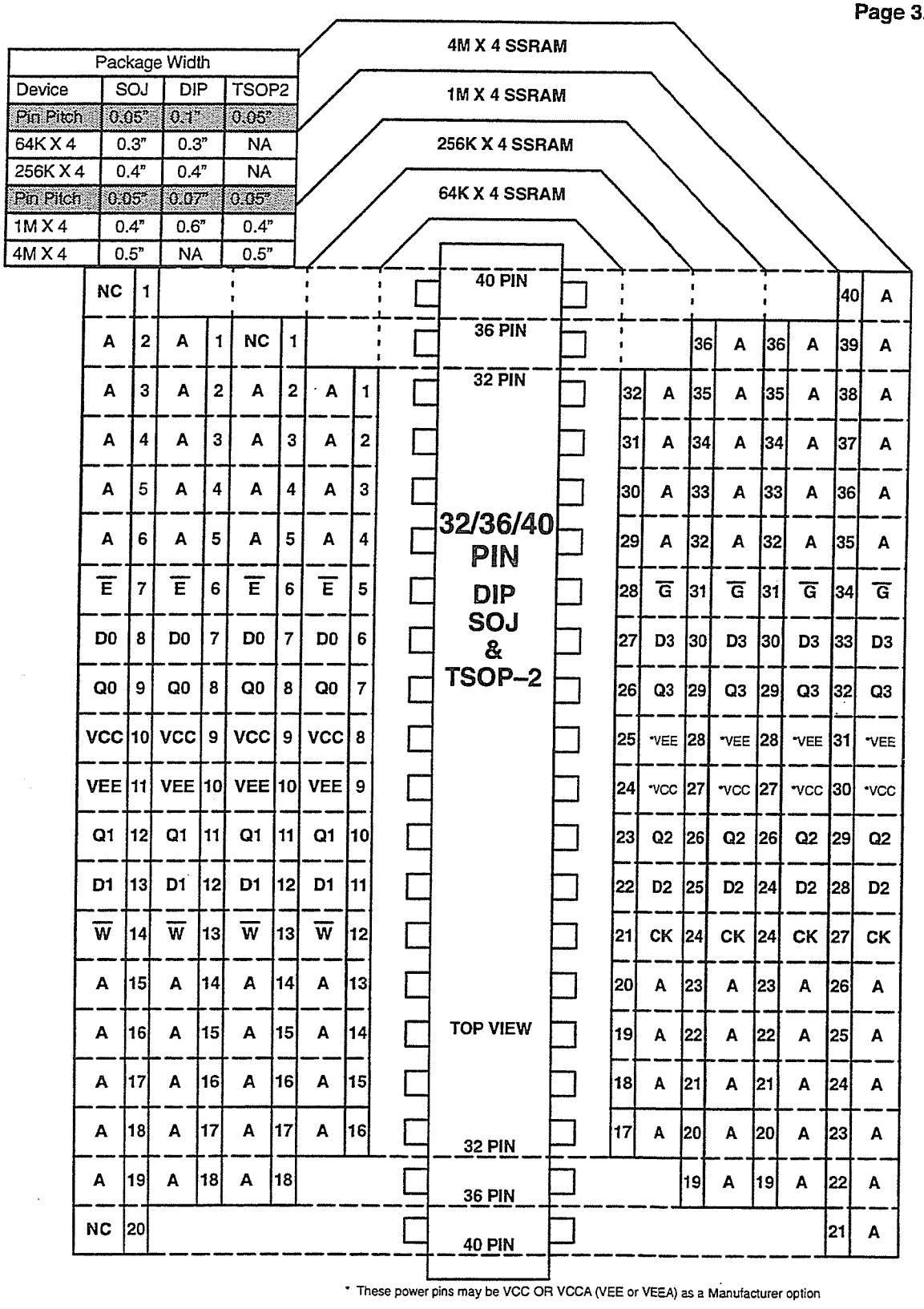
* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.4–7

64K TO 4M BY 4 ECL SRAM WITH SEPARATE I/O FAMILY IN DIP, SOJ, AND TSOP–2

Release 4

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"



* These power pins may be VCC OR VCCA (VEE or VEEA) as a Manufacturer option

FIGURE 3.7.4–8

64K TO 4M BY 4 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2

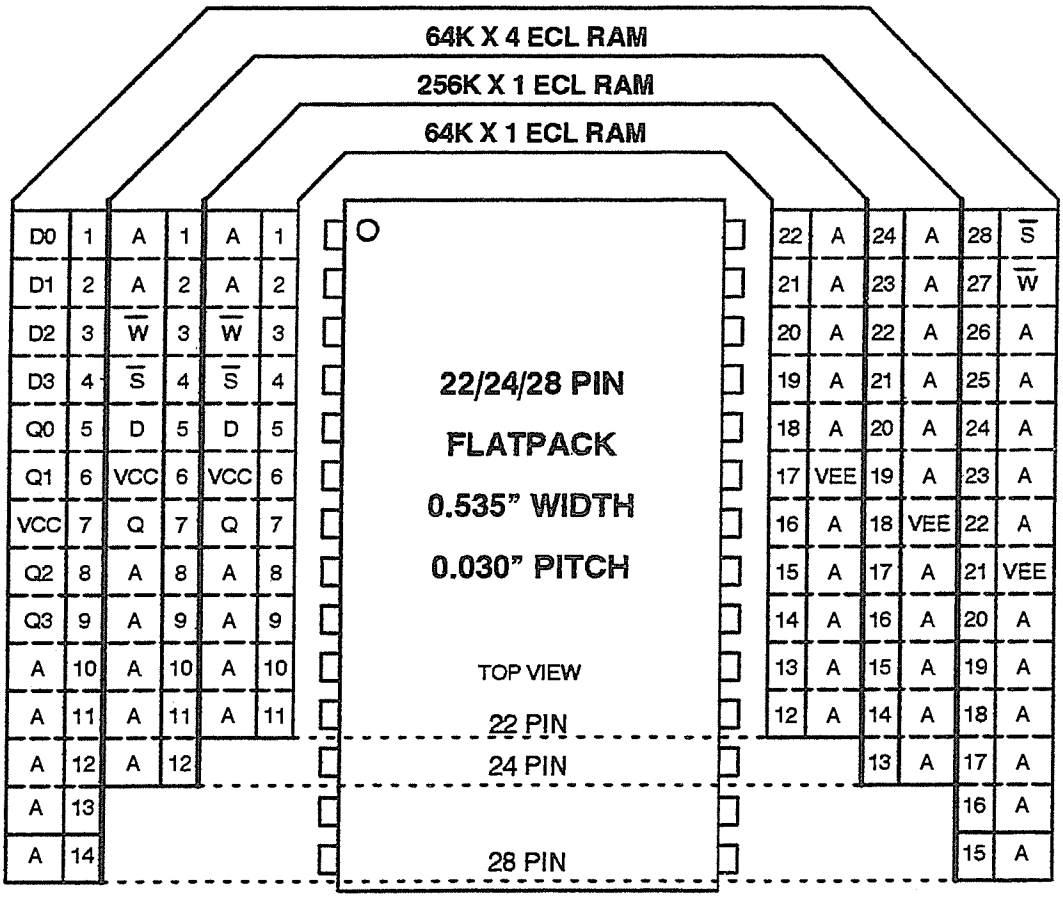
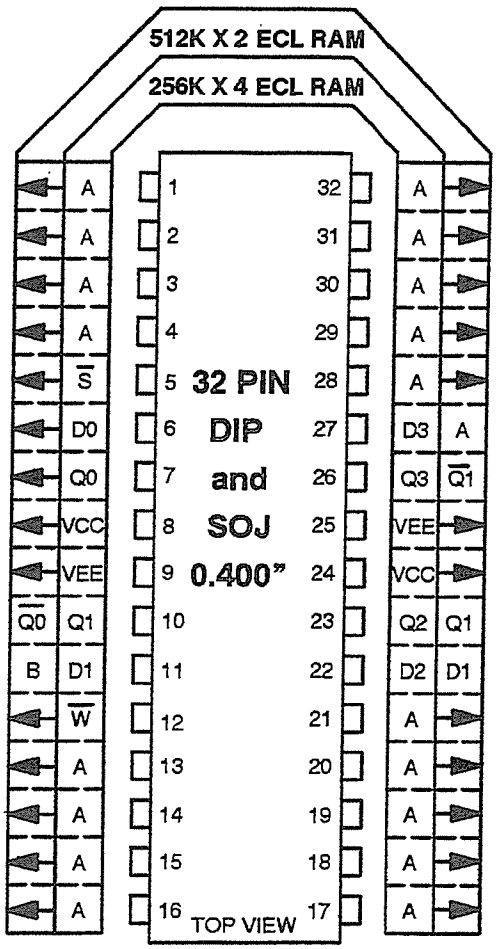


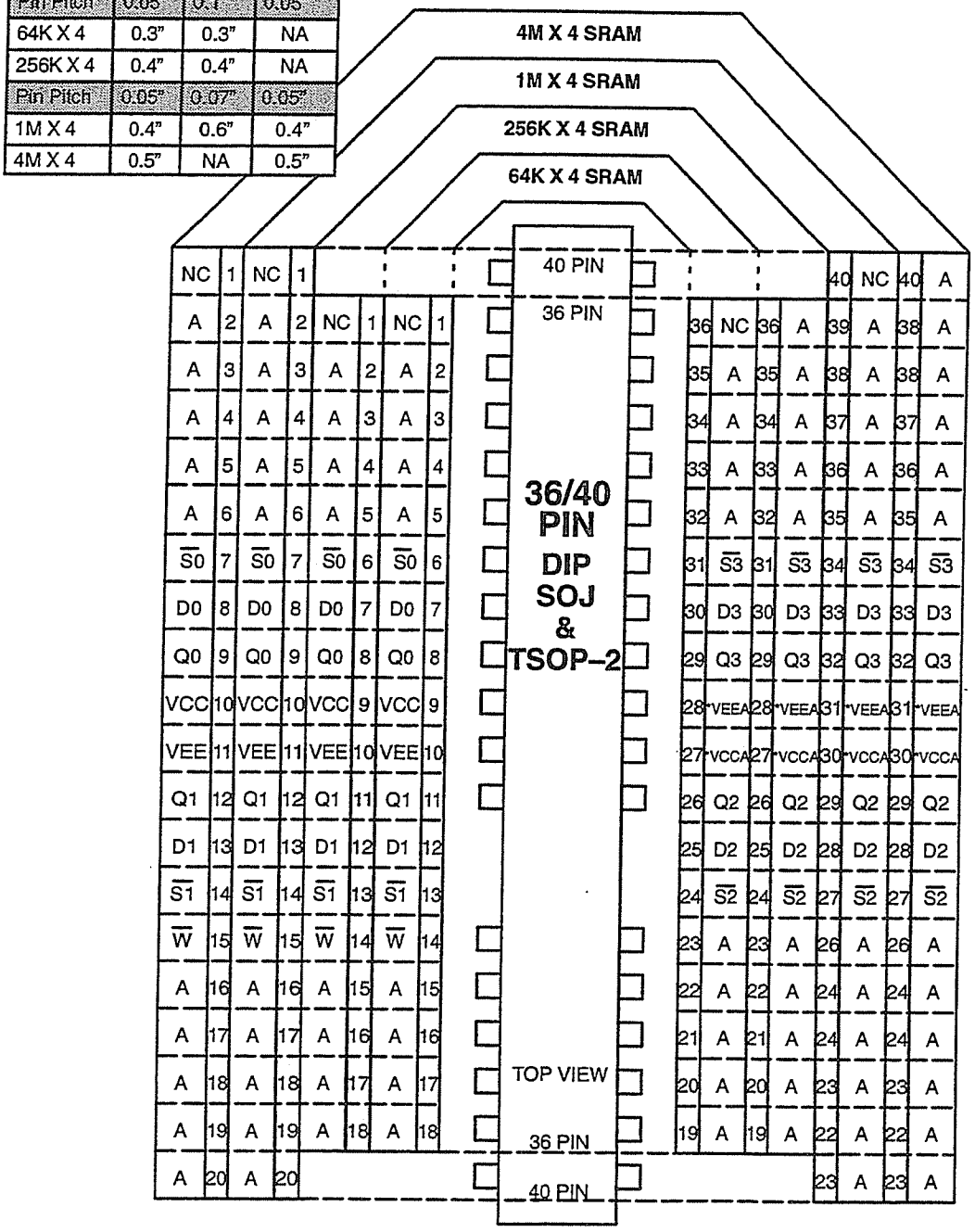
FIGURE 3.7.4–9
64K AND 256K BY 1 ECL RAM
64K BY 4 ECL RAM
IN FLATPACK



Multi–function Pin Truth Table Function vs. Mode Select Pin (11) Level		
Pin 11 Level/Function	> VEE / D1	VEE / B
RAM Organization	256K X 4	512K X 2
Pin #		
6	D0	D0
7	Q0	Q0
10	Q1	$\overline{Q0}$
11	D1	B (VEE)
22	D2	D1
23	Q2	Q1
26	Q3	$\overline{Q1}$
27	D3	A18

FIGURE 3.7.4–10
256K X 4 or 512K X 2 CONFIGURABLE SRAM
IN SOJ & DIP

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"



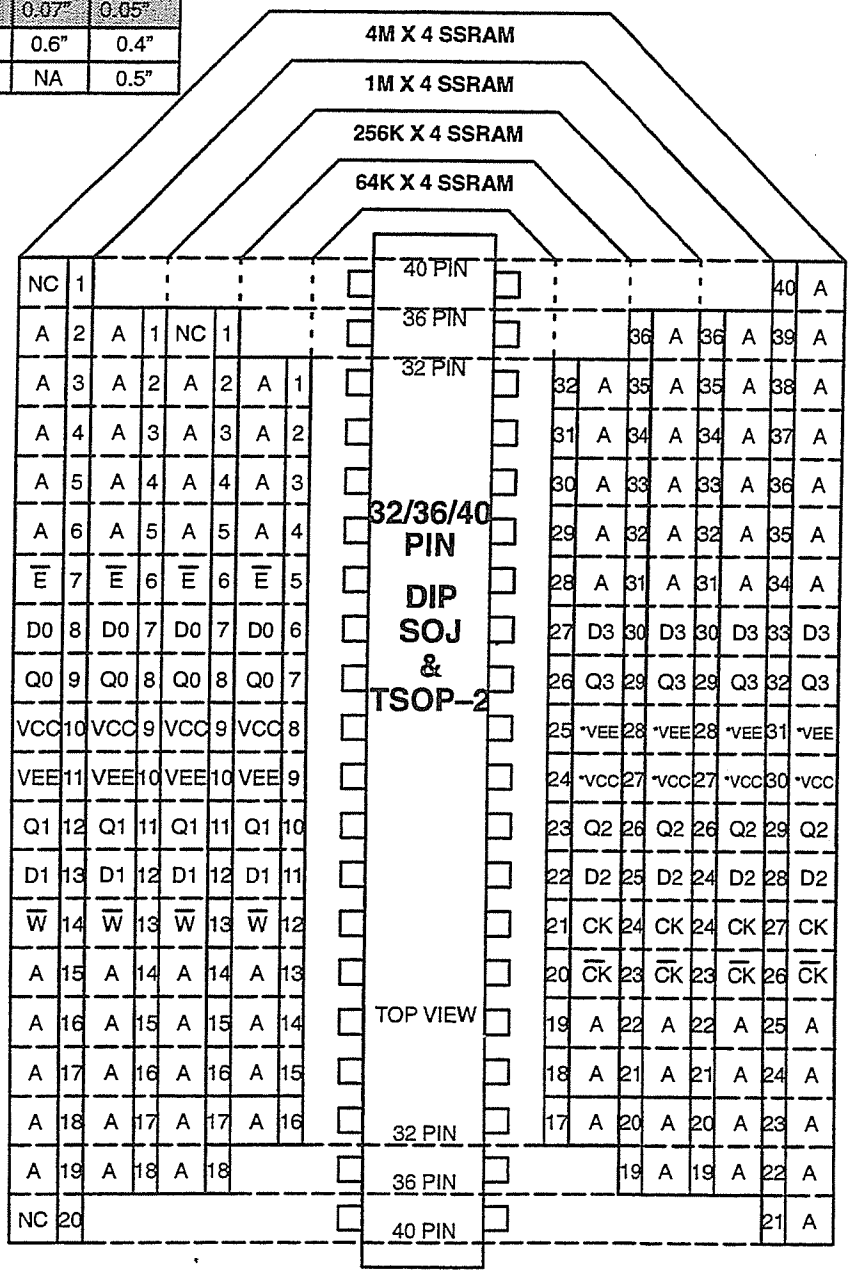
* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.4–11

64K TO 4M BY 4 BIT SELECTABLE ECL SRAM FAMILY IN DIP, SOJ, AND TSOP–2

Release 4

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"

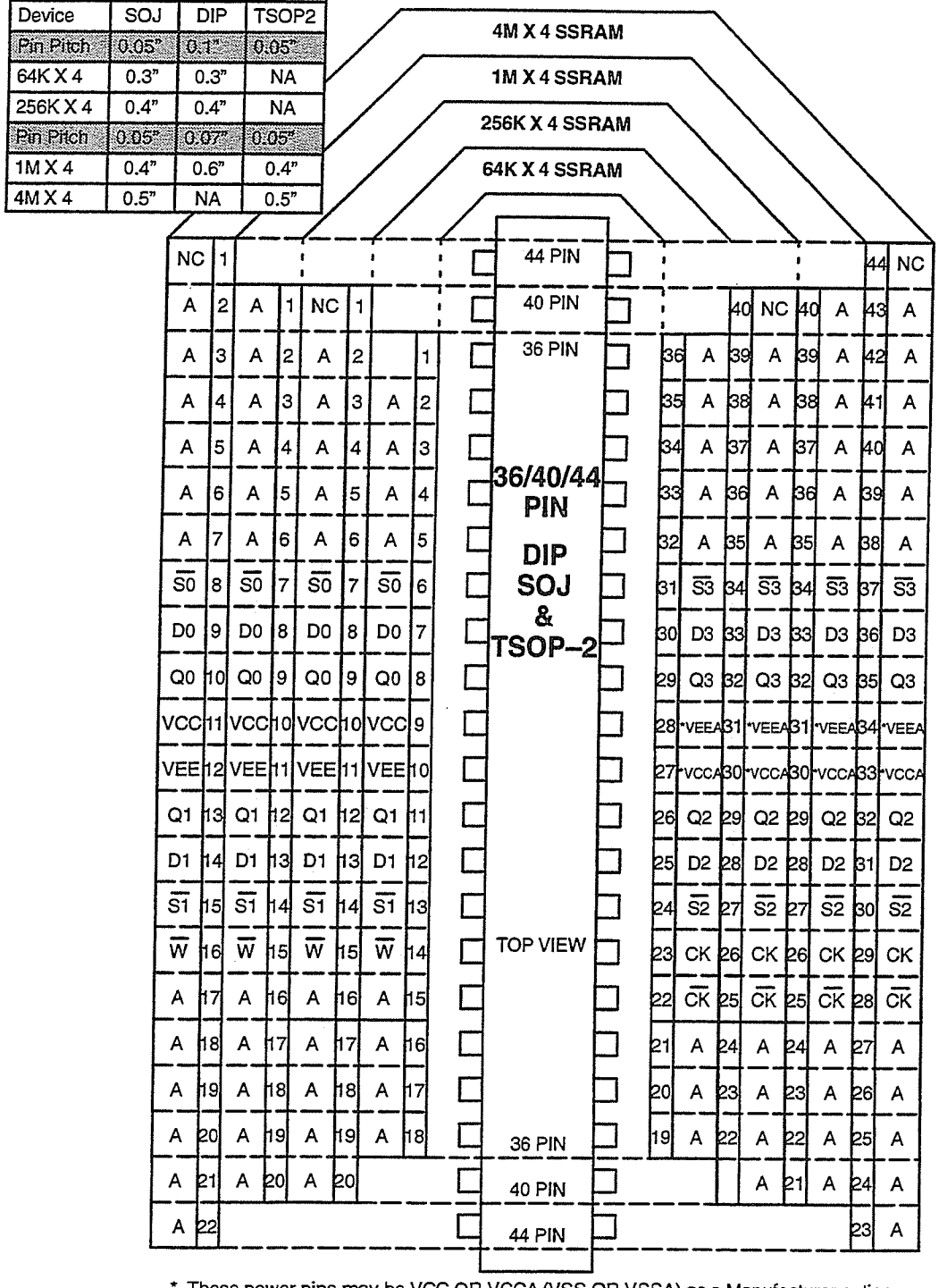


* These power pins may be VCC OR VCCA (VEE or VEEA) as a Manufacturer option

FIGURE 3.7.4–12

64K TO 4M BY 4 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"



* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.4–13

64K TO 4M BY 4 BIT SELECTABLE ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2

Release 4

3.7.5 Byte Wide TTL SRAM

All of the following standards are for devices which operate with TTL interface levels and power voltages.

3.7.5.1 – 64 BY 9 TTL SRAM IN SCC

CAPACITY—64 WORDS OF 9 BITS
PACKAGE—28 PAD (PIN) SCC, 0.450" X 0.450"
PIN ASSIGNMENTS—Fig. 3.7.5–1
This standard was developed by Committee 42.1.

3.7.5.2 – 1K & 2K BY 8 TTL SRAM IN DIP

CAPACITY—1K, 2K WORDS OF 8 BITS
PACKAGE—24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.7.5–2

3.7.5.3 – 2K & 4K BY 8 TTL SRAM IN RCC

CAPACITY—2K, 4K WORDS OF 8 BITS
PACKAGE—32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT—Fig. 3.7.5–3
These parts are CC equivalents of 24 Pin DIP devices.

3.7.5.4 – 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ,

CAPACITY—2K, 4K, 8K, 16K, & 32K WORDS OF 8 BITS,
PACKAGE—28 PIN DIP, 0.6" WIDE
—28 PIN DIP, 0.3" WIDE OPTIONAL FOR 8K & 32K DEVICES
PIN ASSIGNMENT—Fig. 3.7.5–4

3.7.5.5 – .5K TO 32K BY 8 TTL SRAM FAMILY IN RCC

CAPACITY—.5K, 1K, 2K, 4K, 8K, 16K, 32K WORDS OF 8 BITS
PACKAGE—32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT—Fig. 3.7.5–5

3.7.5.6 – 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ or TSOP–2,

CAPACITY—32K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—28 OR 32 PIN SOJ, 0.3", 0.4" WIDE OR NOT DEFINED
—32 PIN TSOP–2 (see Fig. 3.7.5–6 for package approvals)
PIN ASSIGNMENT—Fig. 3.7.5–6

3.7.5.7 – 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP,

CAPACITY—64K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.7.5–7

3.7.5.8 – 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP,

CAPACITY—32K, 64K, 128K, 256K WORDS OF 9 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
—OPTIONAL 32 PIN DIP & SOJ, 0.3" WIDE FOR 32K DEVICE
PIN ASSIGNMENT—Fig. 3.7.5–8

3.7.5.9 – 32K TO 2M BY 8 AND 512K TO 2M BY 9 TTL SRAM IN DIP, SOJ, AND TSOP–2

CAPACITY—32K, 128K, 512K, 2M WORDS OF 8 BIT AND 512K, 2M WORDS OF 9 BITS
LOGIC FEATURES—COMMON DATA INPUT & OUTPUT PINS
—OUTPUT ENABLE FOR ALL DENSITIES
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.5–9

3.7.5.10 – 32K and 128K BY 8 TTL SSRAM IN DIP AND SOJ

CAPACITY—32K, & 128K WORDS OF 8 BIT
LOGIC FEATURES—SEPARATE DATA INPUT & OUTPUT PINS
—OUTPUT ENABLE
PACKAGE—40 PIN DIP, 0.6" wide
—40 PIN SOJ, UNDEFINED
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.5–10

3.7.5.11 – 2K TO 32K BY 9 DPSRAM FAMILY IN 68 SCC

CAPACITY—2K, 8K, 32K WORDS OF 9 BITS,
LOGIC FEATURES—Two identical access ports
PACKAGE—68 PAD (PIN) SCC, 0.950" X 0.950"
PIN ASSIGNMENT—Fig. 3.7.5–11
This part contains two identical ports for access to the storage array. These ports include full sets of address, data, and control signals.

3.7.5.12 – 32K BY 9 CACHE SRAM IN 44 SCC

CAPACITY—32K WORDS OF 9 BITS,
LOGIC FEATURES—Internal CACHE data compare logic
PACKAGE—44 TERMINAL SCC, 0.500" X 0.500"
PIN ASSIGNMENT—Fig. 3.7.5–12
This part contains specialized logic functions which allow it to be used to implement the CACHE memory function conveniently.

3.7.5.13 – 128K BY 8 SRAM IN TSOP1

CAPACITY—128K WORDS OF 8 BITS
PACKAGE—32 PIN TSOP1, 20 mm X 8 mm, 0.5 mm PIN PITCH
PIN ASSIGNMENTS—Fig. 3.7.5–13

3.7.5.14 – 128K BY 8 & 9 SSRAM IN SOJ

CAPACITY—128K WORDS OF 8 BITS
PACKAGE—32 PIN SOJ, 0.400"
PIN ASSIGNMENTS—Fig. 3.7.5–14

3.7.5.15 – 1K AND 2K BY 8 DPSRAM FAMILY IN 48 DIP

CAPACITY—1K, 2K WORDS OF 8 BITS,
LOGIC FEATURES—Two identical access ports
PACKAGE—48 PIN DIP, 0.600"
PIN ASSIGNMENT—Fig. 3.7.5–15
This part contains two identical ports for access to the storage array. These ports include full sets of address, data, and control signals.

3.7.5.16 – 128K TO 512K BY 8 SRAM FAMILY IN 32 CDSO–N

CAPACITY—128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—32 PIN LEADLESS CERAMIC SO, 0.400"
PIN ASSIGNMENT—Fig. 3.7.5–16
This family of parts is based on the evolutionary SRAM pinout family described in Sec. 3.7.5.7

3.7.5.17 – 128K TO 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN 33 DIP, TSOP2, AND SOJ

CAPACITY—128K & 512K WORDS OF 8 OR 9 BITS,
LOGIC FEATURES—Both Synchronous and Asynchronous versions of the 128K part
PACKAGE—36 PIN DIP, TSOP2, or SOJ, 0.400" or 0.600",
— See Fig. 3.7.5–17 for specific package approvals and dimensions.
PIN ASSIGNMENT—Fig. 3.7.5–17

3.7.5.18 – 128K TO 2M BY 8/9 BURST SRAM IN BGA

CAPACITY—128K, 256K, 512K, 1M, 2M WORDS OF 8 OR 9 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.5–18
These parts contain BURST addressing capability.

3.7.5.19 – 128K TO 2M BY 8/9 SSRAM IN BGA

CAPACITY—128K, 256K, 512K, 1M, 2M WORDS OF 8 OR 9 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.5–19
Included with this standard is a table of the BOUNDRY SCAN ORDER to be used in testing the parts.
BOUNDRY SCAN ORDER TABLE—Fig. 3.7.5–20

3.7.5.20 – 32K BY 8 SRAM IN TSOP1

CAPACITY—32K WORDS OF 8 BITS
PACKAGE—32 PIN TSOP1, 8 mm X 11.8 mm, 0.55 mm PP
PIN ASSIGNMENTS—Fig. 3.7.5–21

3.7.5.18 – 128K TO 2M BY 8/9 BURST SRAM IN BGA

CAPACITY—128K, 256K, 512K, 1M, 2M WORDS OF 8 OR 9 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.5–18
These parts contain BURST addressing capability.

3.7.5.19 – 128K TO 2M BY 8/9 SSRAM IN BGA

CAPACITY—128K, 256K, 512K, 1M, 2M WORDS OF 8 OR 9 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.5–19
Included with this standard is a table of the BOUNDRY SCAN ORDER to be used in testing the parts.
BOUNDRY SCAN ORDER TABLE—Fig. 3.7.5–20

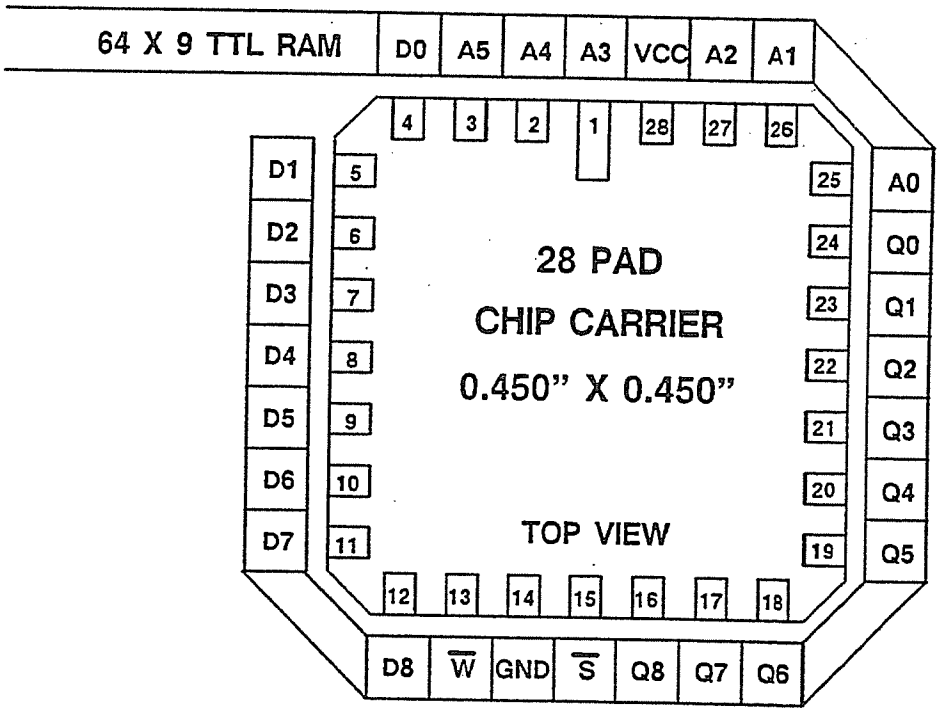


FIGURE 3.7.5-1
64 BY 9 SRAM IN SCC

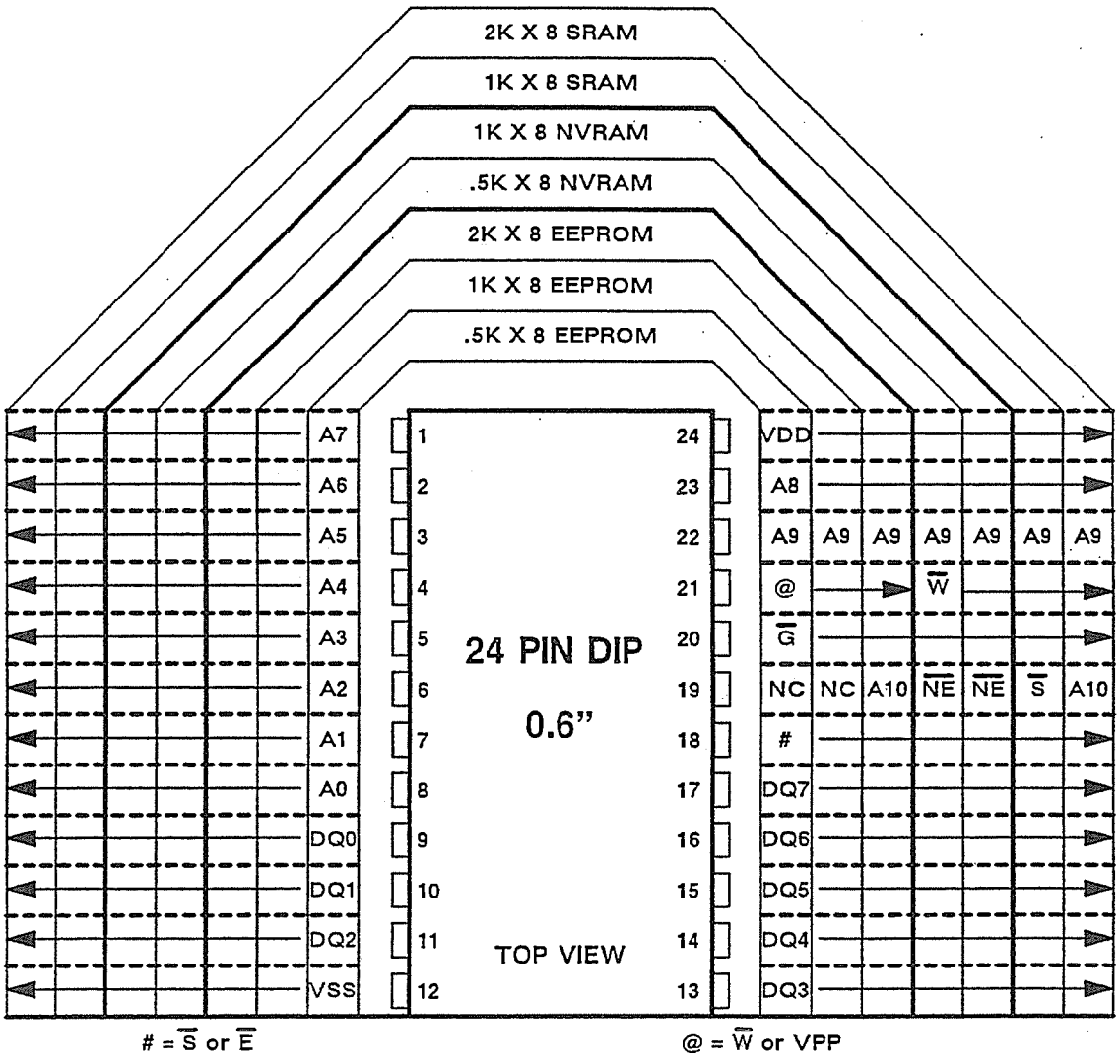


FIGURE 3.7.5-2
1K & 2K BY 8 TTL SRAM IN DIP

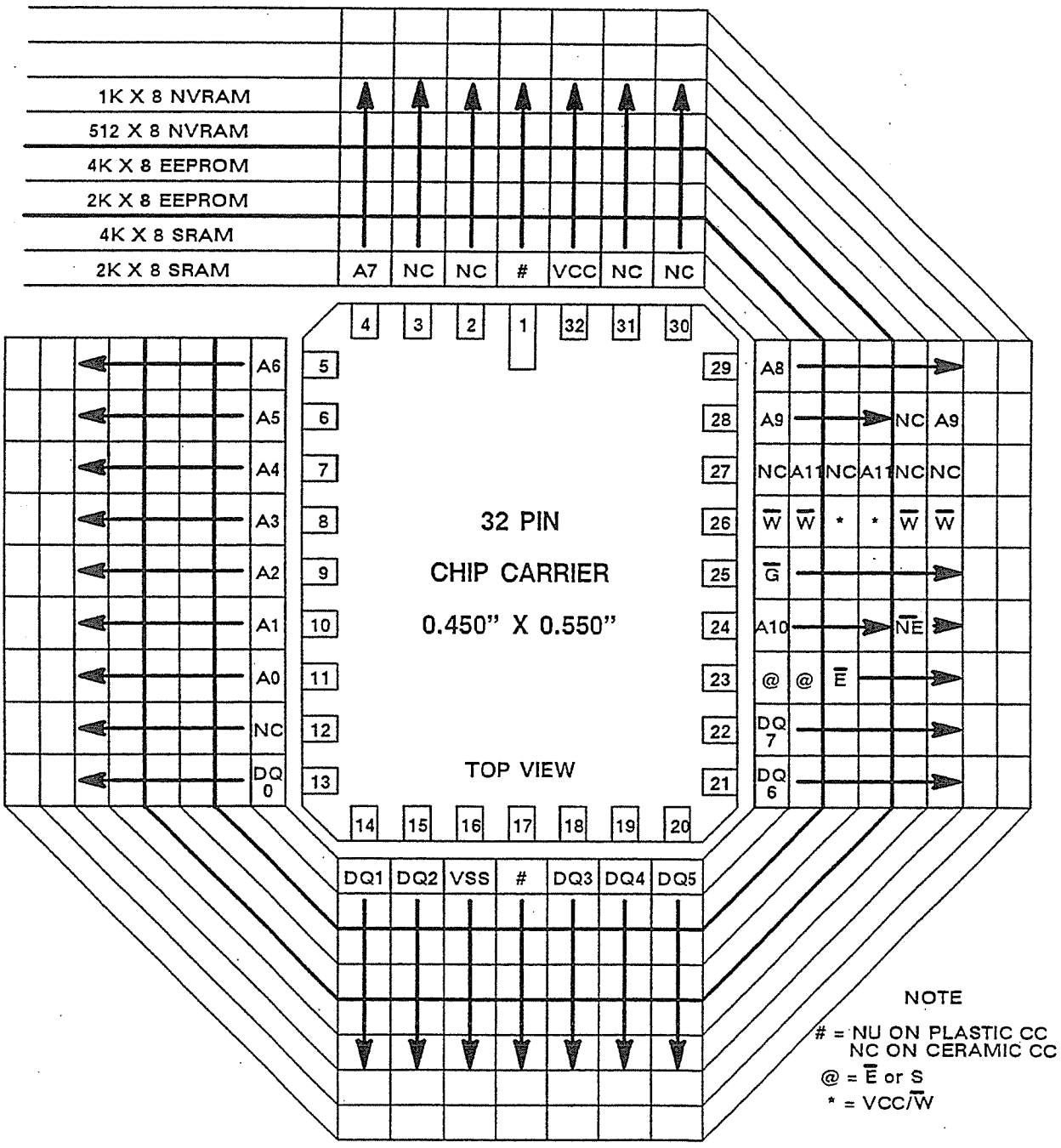


FIGURE 3.7.5-3
2K & 4K BY 8 TTL SRAM IN RCC

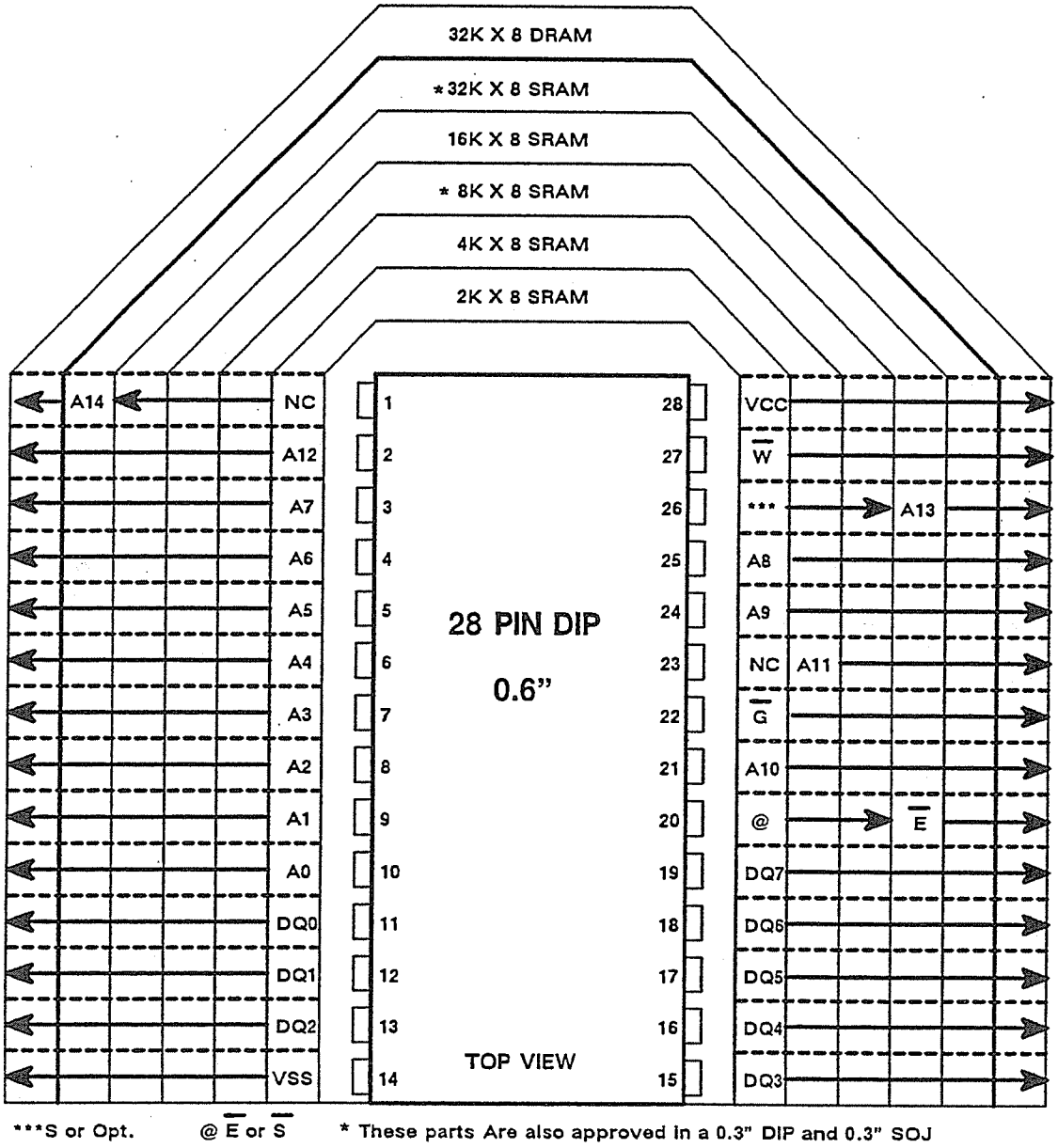


FIGURE 3.7.5-4
2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ

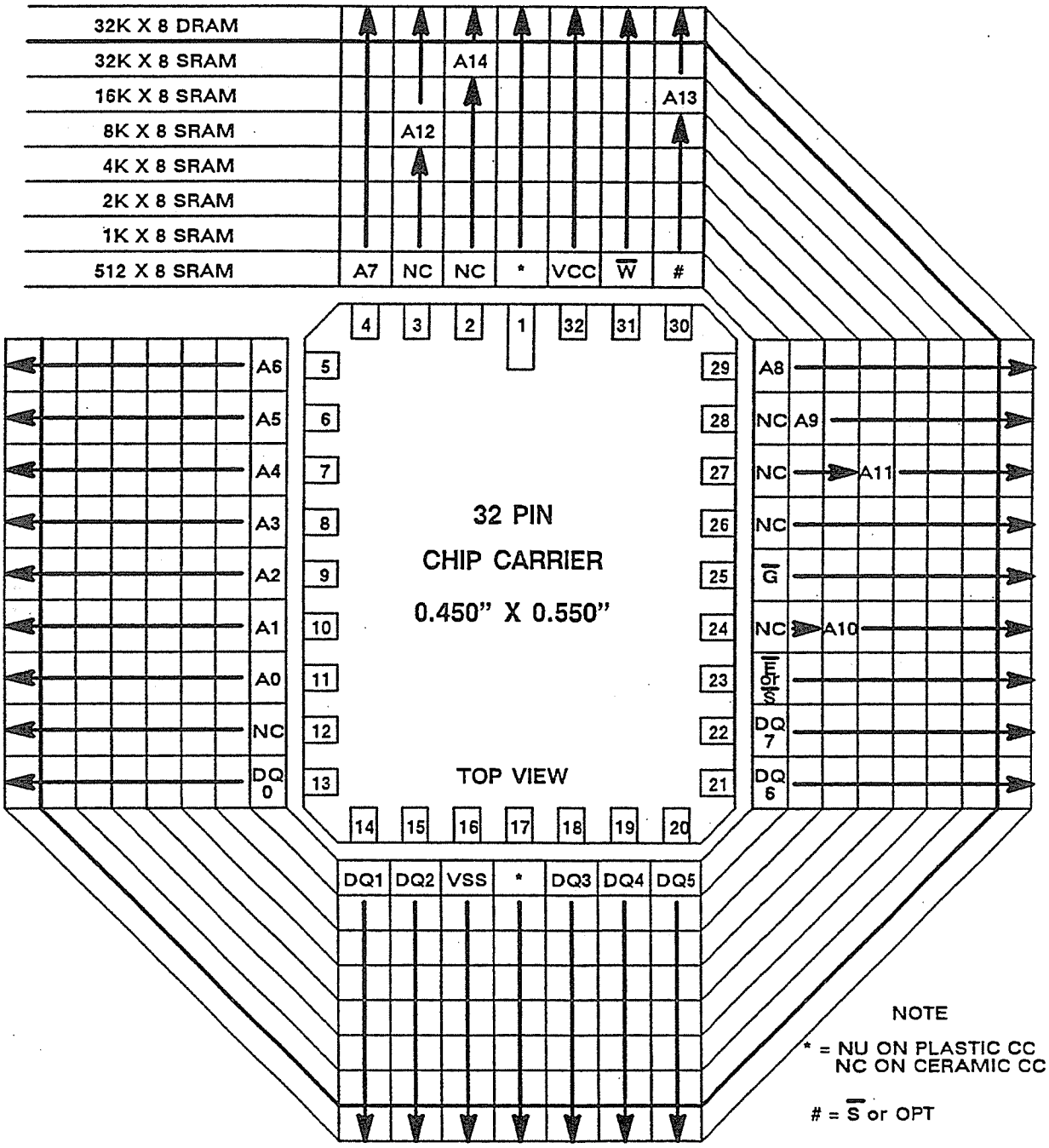
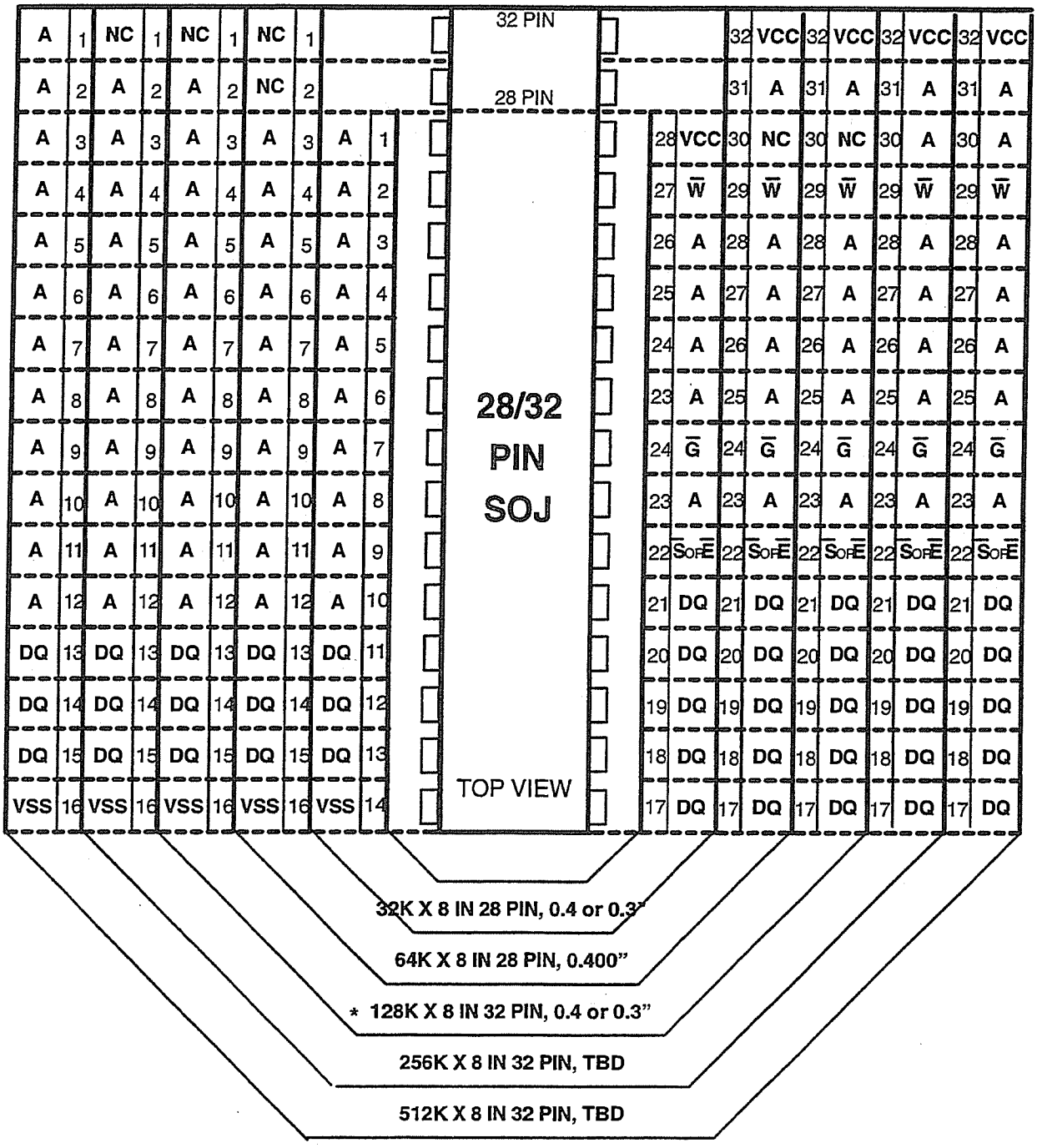


FIGURE 3.7.5-5
.5K TO 32K BY 8 TTL SRAM FAMILY IN RCC



* The 128K X 8 device is also approved for use in 0.300" wide TSOP–2 (PDSO–G) package with a pin pitch of 0.050"

FIGURE 3.7.5–6
32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ

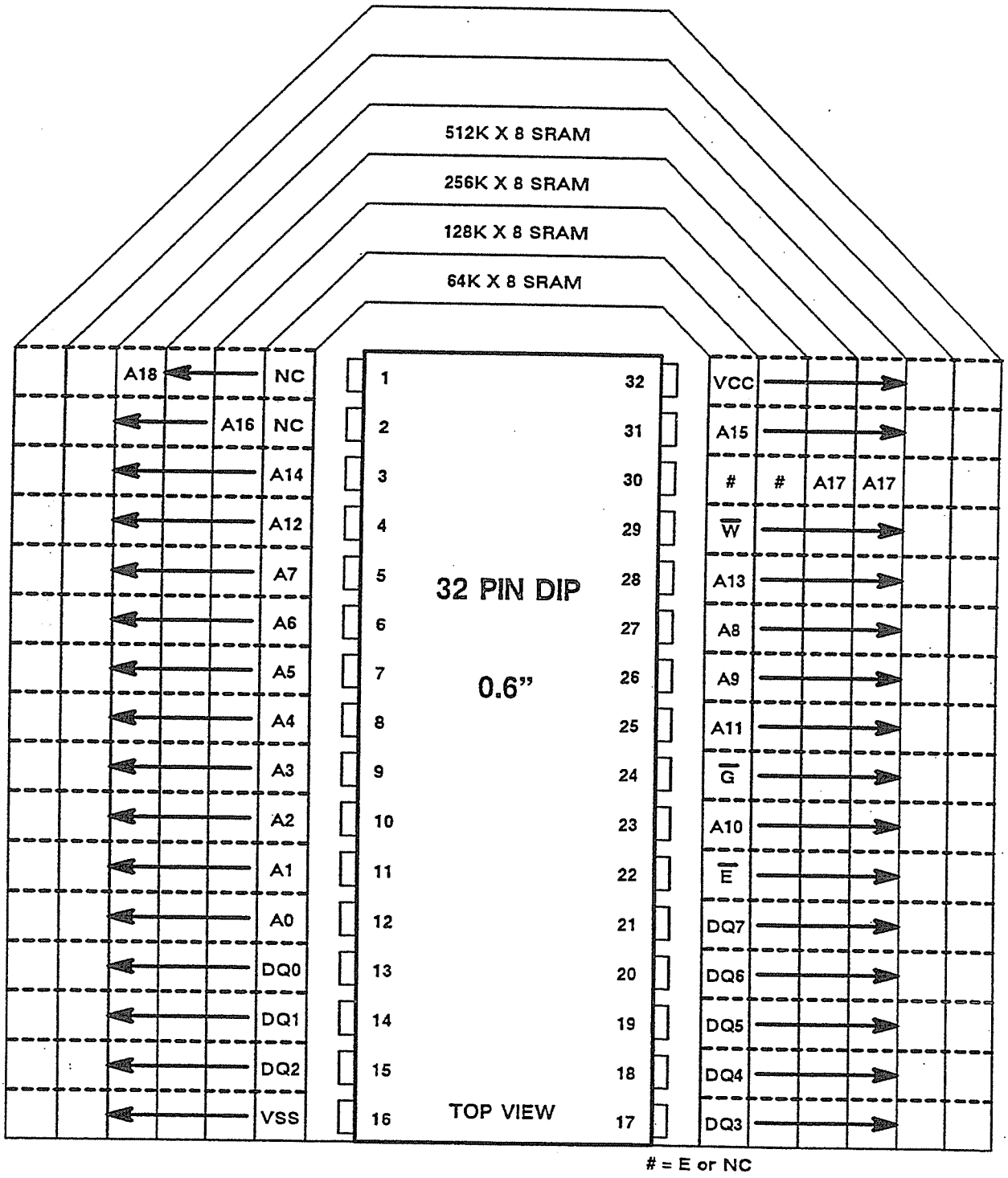
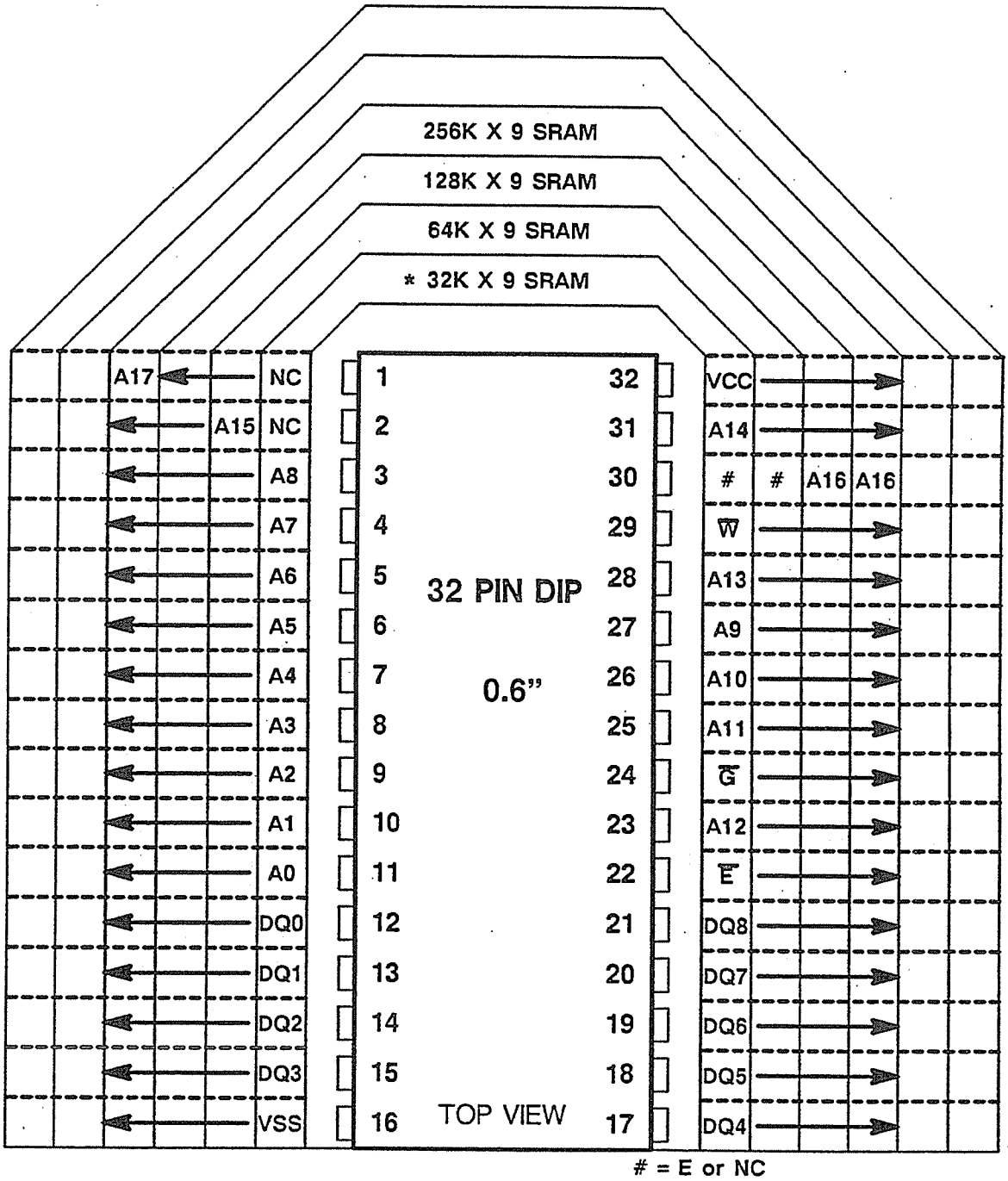


FIGURE 3.7.5-7
64K TO 512K BY 8 TTL SRAM FAMILY IN DIP



= E or NC

* This part is approved also with 0.3" DIP and 0.3" SOJ

FIGURE 3.7.5-8
32K TO 256K BY 9 TTL SRAM FAMILY IN DIP

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
32K X 8	0.3"	0.3"	NA
128K X 8	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
512K X 8/9	0.4"	0.6"	0.4"
2M X 8/9	0.5"	NA	0.5"

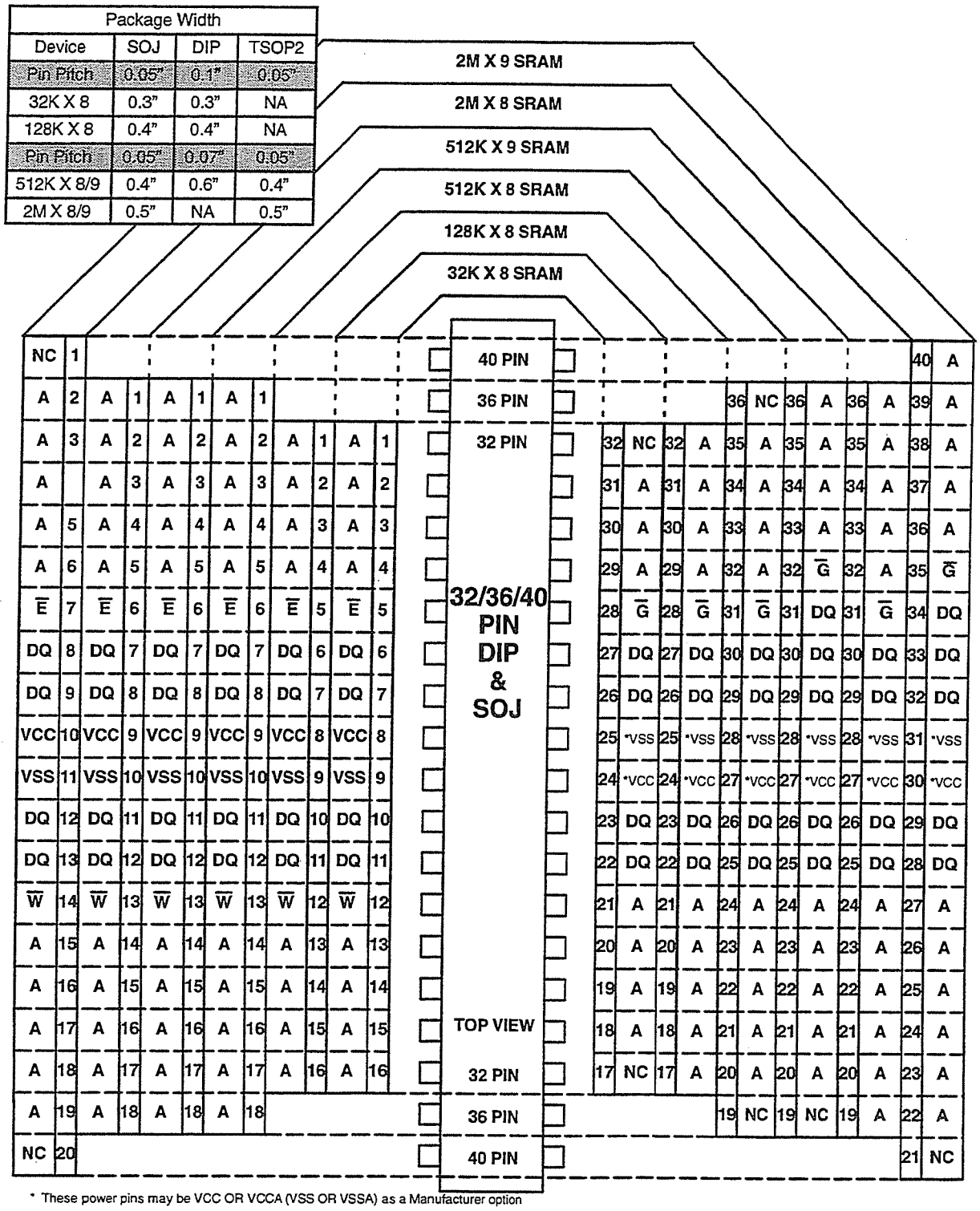
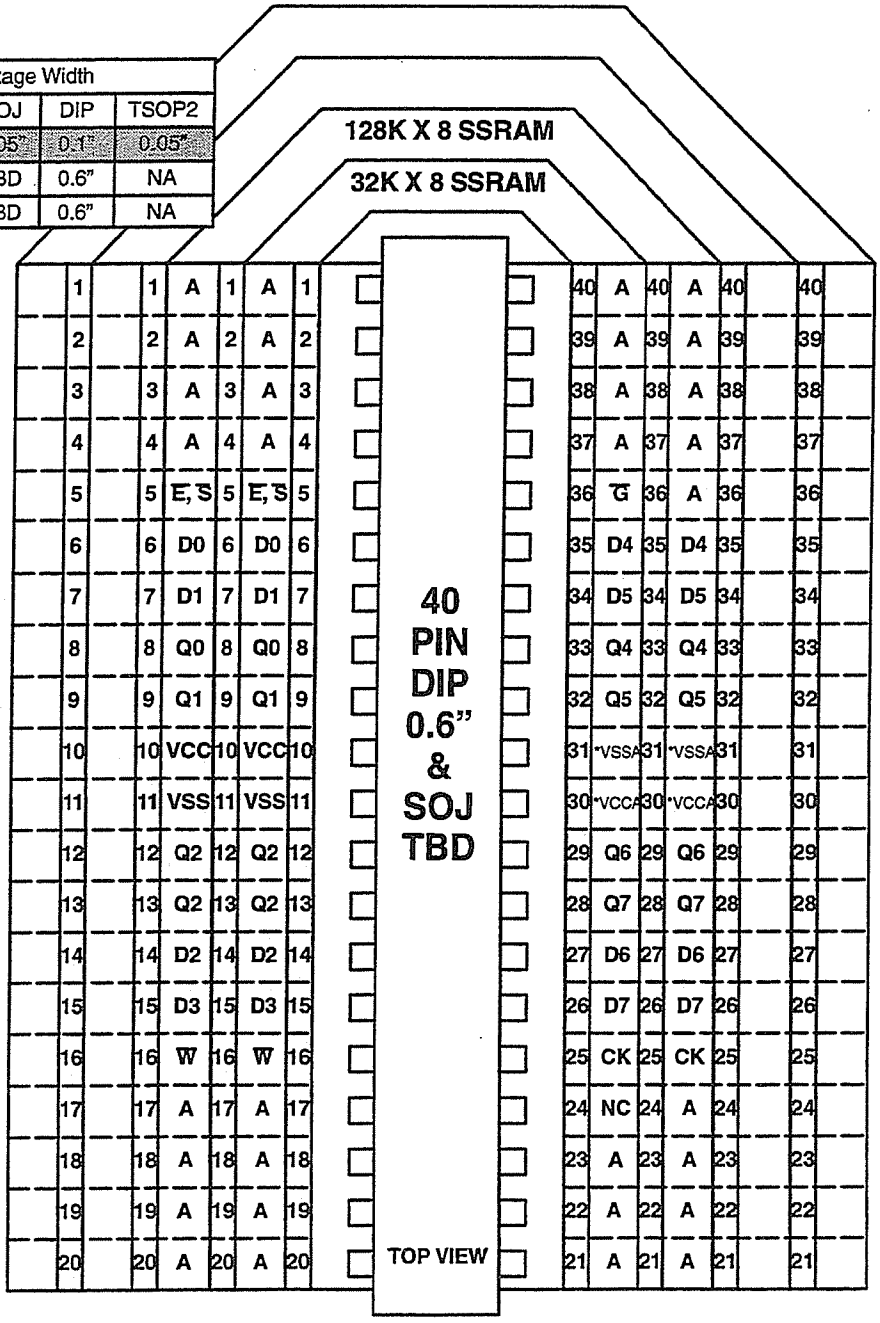


FIGURE 3.7.5–9

32K TO 2M BY 8 AND 9 TTL SRAM FAMILY IN DIP, TSOP2, AND SOJ

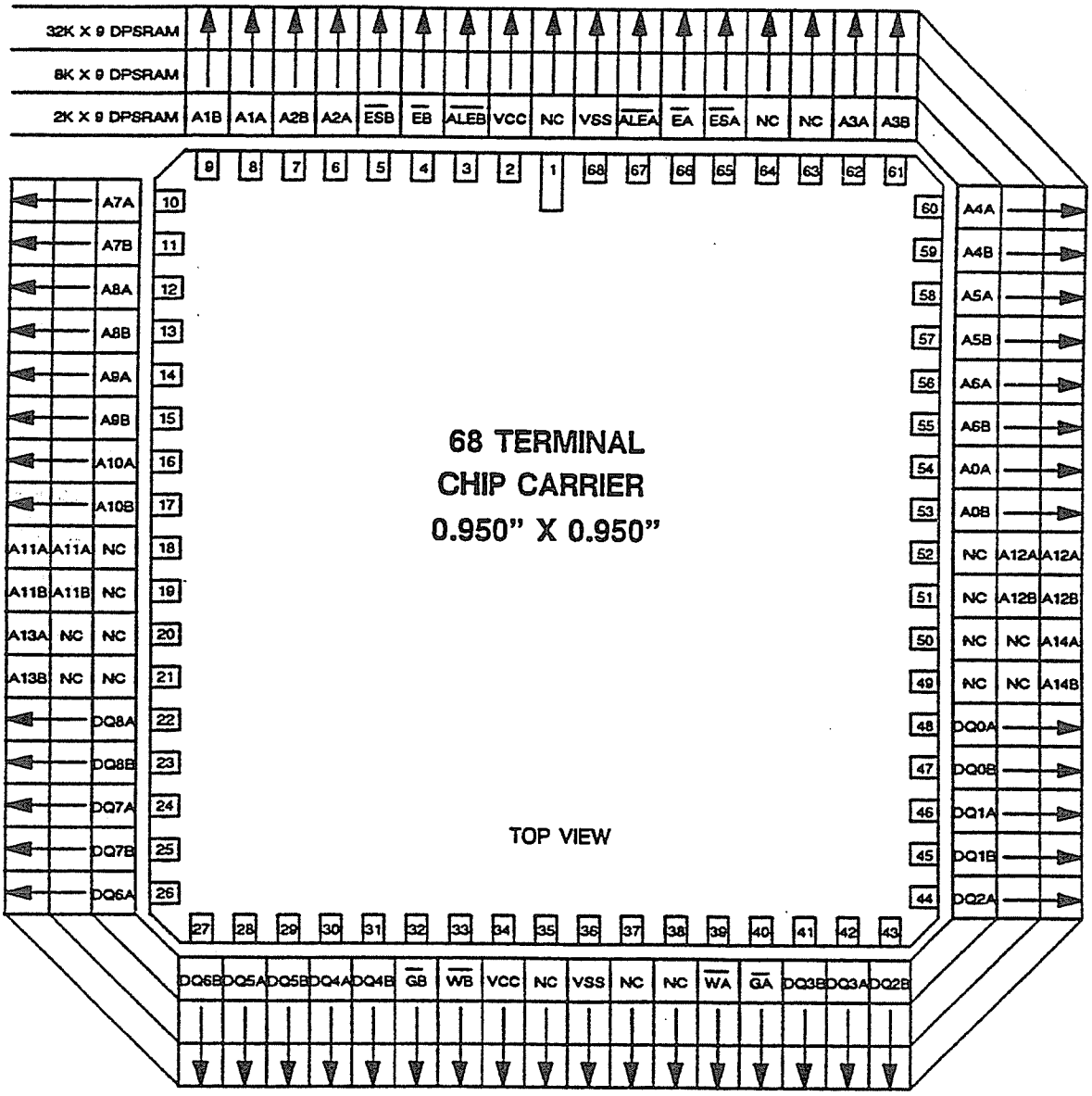
Release 4

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
32K X 8	TBD	0.6"	NA
128K X 8	TBD	0.6"	NA



* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

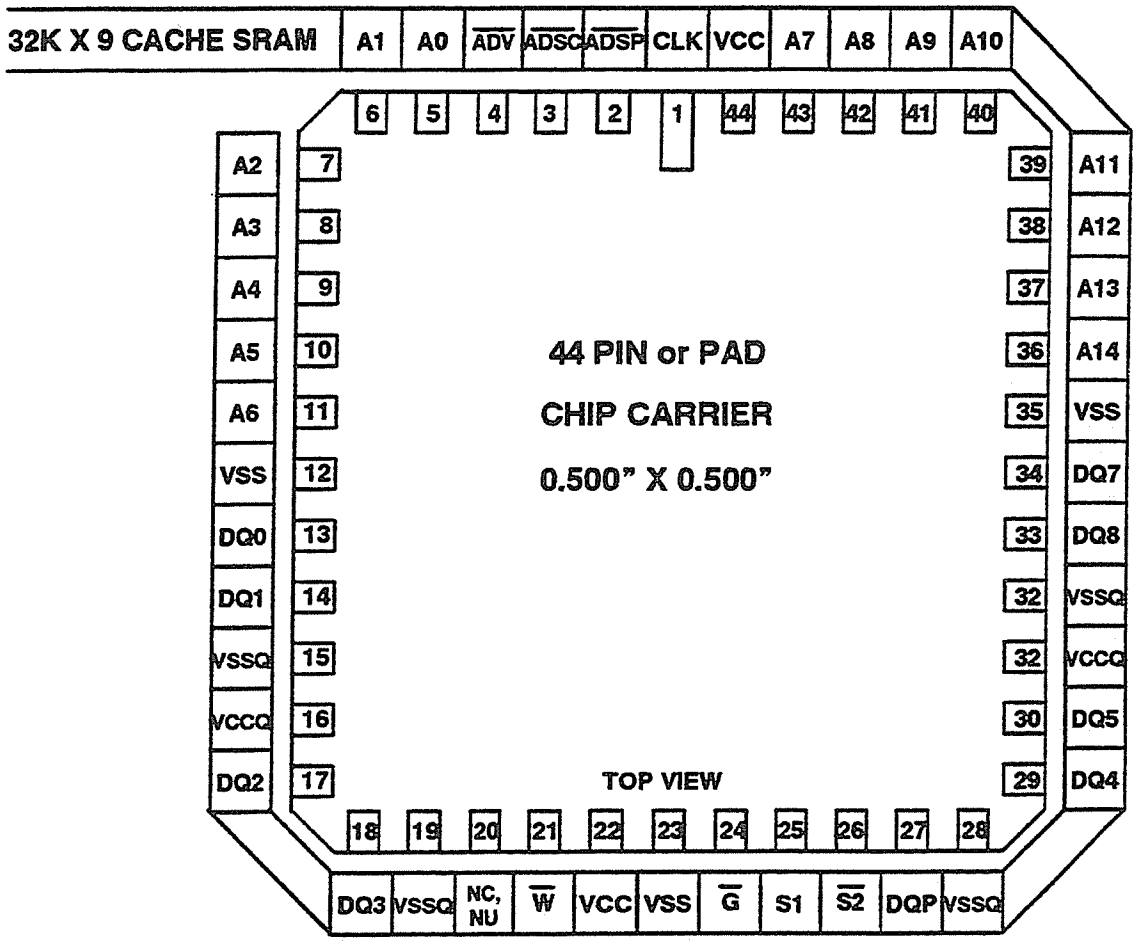
FIGURE 3.7.5–10
32K AND 128K BY 8 TTL SSRAM IN DIP, TSOP2, AND SOJ



THE SIGNALS ASSOCIATED WITH PORT A HAVE THE SUFFIX A ON THE PIN NAME; THOSE ASSOCIATED WITH PORT B HAVE THE SUFFIX B.

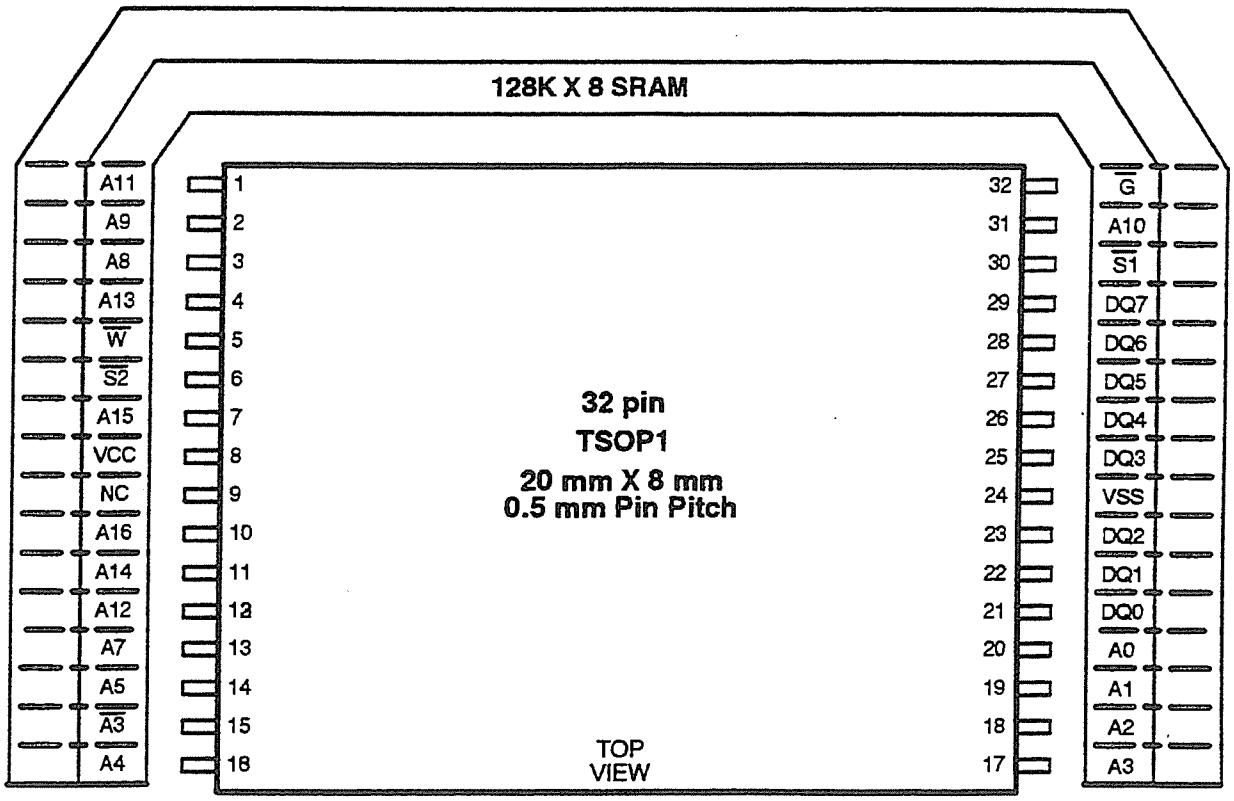
NOTE: Early proposals of this standard showed the pins numbered with Pin 1 in the upper left corner of the package. The pin numbering has been changed to the current version to maintain a uniform numbering convention within Std. 21

FIGURE 3.7.5-11
2K TO 32K BY 9 DPSRAM FAMILY IN SCC



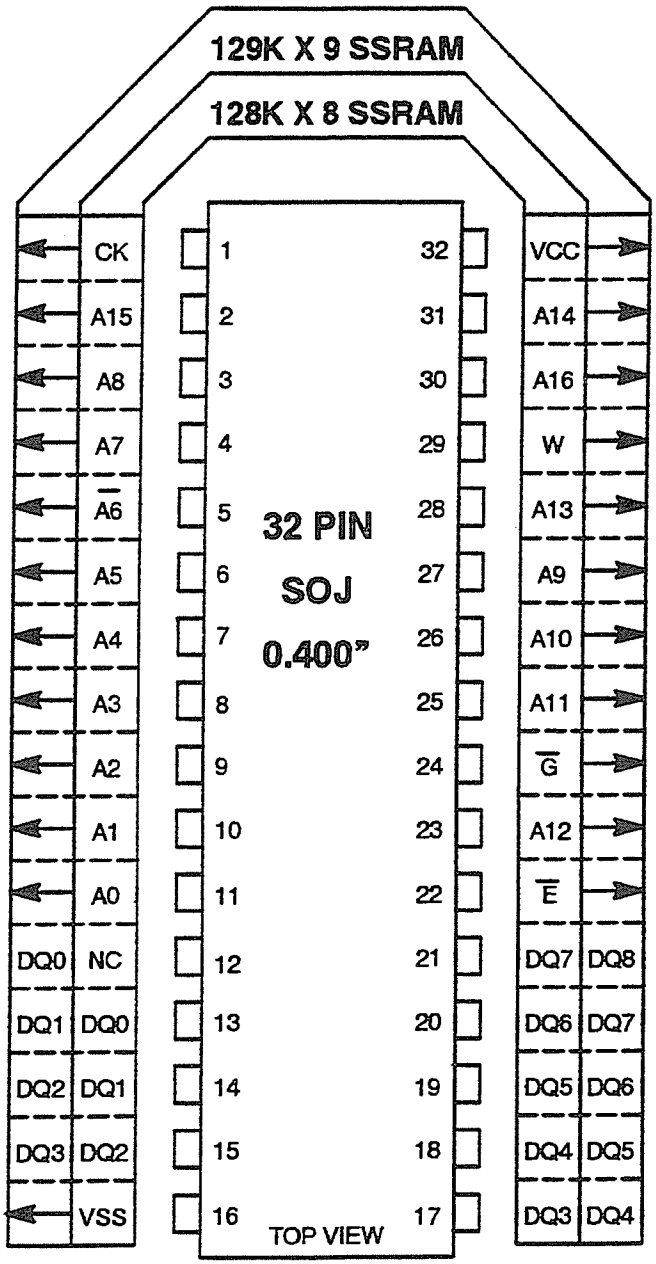
NOTE – ADV, ADSC, & ADSP are specialized inputs which are unique to this part and are not defined in Sec. 2 of this Standard.

FIGURE 3.7.5–12
32K BY 9 CACHE SRAM IN SCC



The JEDEC Std. No 30 designator for the TSOP1 package is PDSO–G

FIGURE 3.7.5–13
128K BY 8 SRAM IN TSOP1



All INPUTS and OUTPUTS can be either registered or latched

FIGURE 3.7.5–14
128K BY 8 & 9 SSRAM IN SOJ

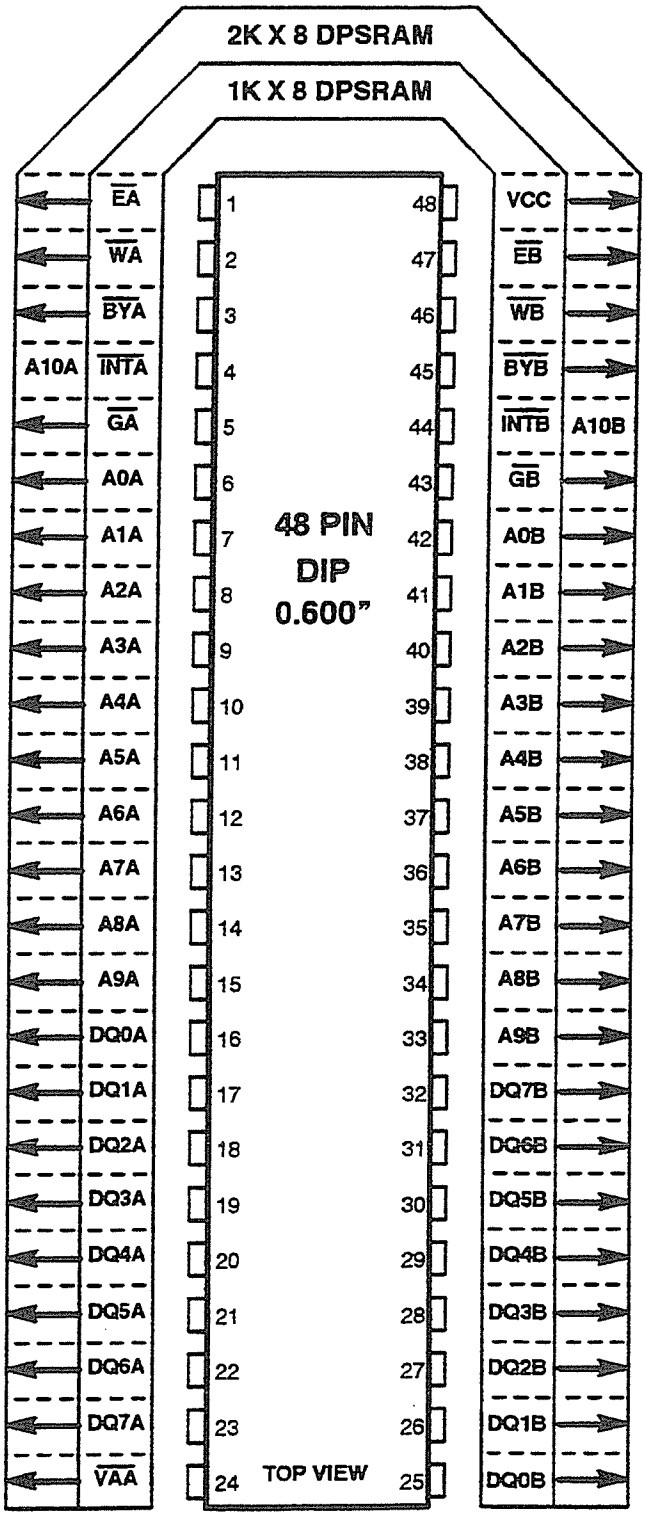


FIGURE 3.7.5–15A
1K AND 2K BY 8 DPSRAM IN DIP

1K & 2K BY 8 DPSRAM TRUTH TABLE

INPUTS EA	EB	A0A–A9A A0B–A9B	BYA When used as an output	BYB When used as an output	FUNCTION
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	h	MATCH	H	H	Normal
L	L	MATCH	L if EA and A0A–A9A Are stable prior to EB and A0B–A9B (2)	L if EB and A0B–A9B are stable prior to EA and A0A–A9A(2)	Write inhibit(3)

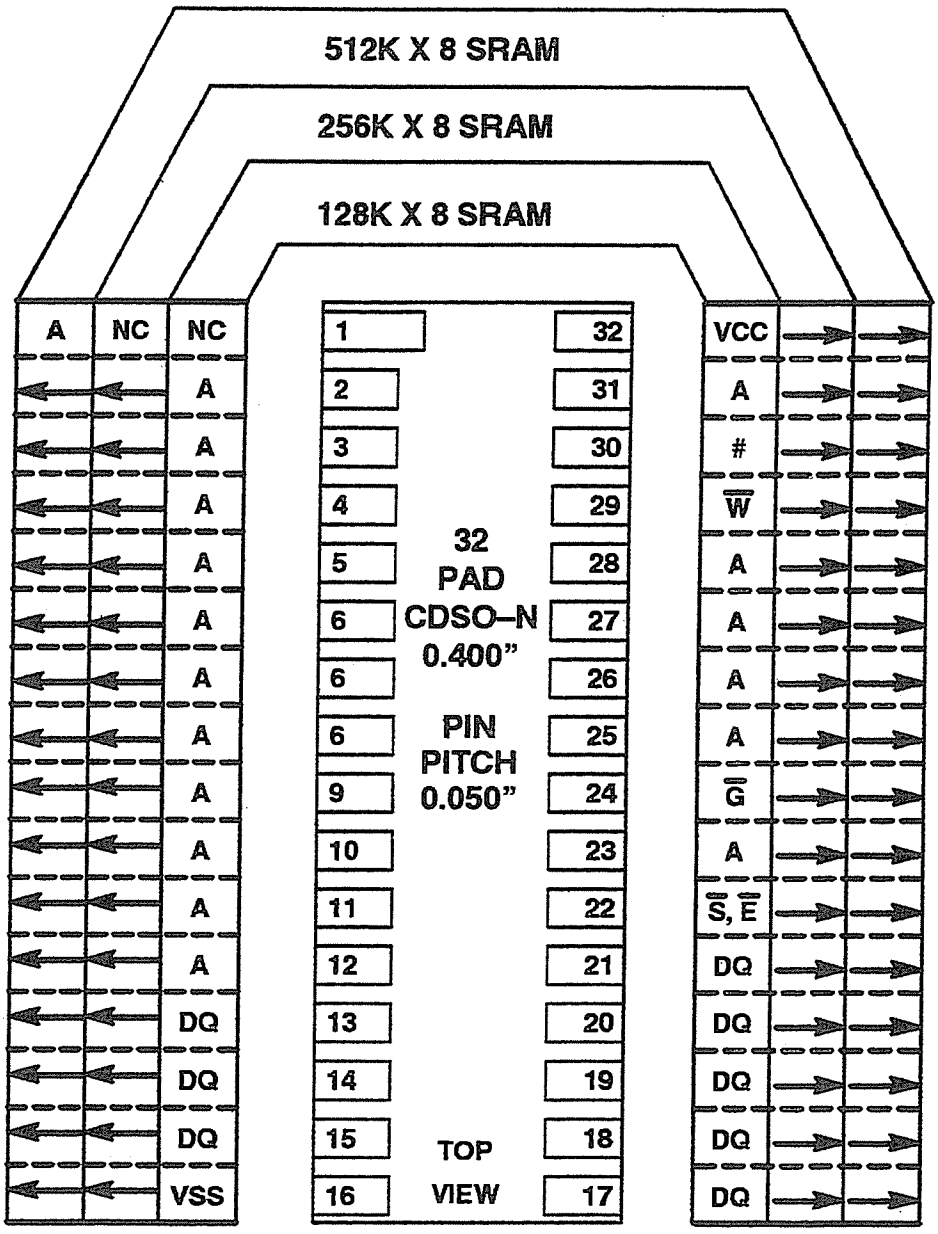
1. Pins BYA and BYB are wither both inputs or both outputs depending on the part type. When used as inputs, BYx gates Wx. Wx internal – Wx OR NOT BYx. BYx outputs are open drain outputs.
2. If the primacy of stable inputs cannot be resolved, either BYA = low or BYB = low, will result. BYA and BYB outputs cannot be low simultaneously.
3. Writes to port A are internally ignored when BYA outputs are driving low regardless of actual logic level on the pin. Writes to port B are internally ignored when BYB outputs are driving low regardless of actual logic level on the pin.

1K BY 8 DPSRAM FUNCTION TABLE

PORT A INPUTS WA	EA	GA	A0A–A9A	PORT B INPUTS WB	EB	GB	A0B A9B	INTA	INTB	FUNCTION
L	L	X	3FF	X	X	X	X	X	L(1)	SET INTB F–F
X	X	X	X	X	L	L	3FF	X	H	RESET INTB F–F
X	X	X	X	L	L	X	3FF	L(1)	X	SET INTA F–F
X	L	L	3FE	X	X	X	X	H	X	RESET INTA F–F

1. Interrupt B will not be set if BYA is low when WA is low. Interrupt A will not be set if BYB is low when WB is low. Interrupt outputs are open drain.

FIGURE 3.7.5–15B
1K AND 2K BY 8 DPSRAM IN DIP



NOTE: CDSO–N is the JEDEC Standard 30 term for a LEADLESS CERAMIC SO Package

FIGURE 3.7.5–16

128K TO 512K BY 8 SRAM IN CDSO–N

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
128K X 8/9	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
512K X 8/9	0.4"	0.6"	0.4"

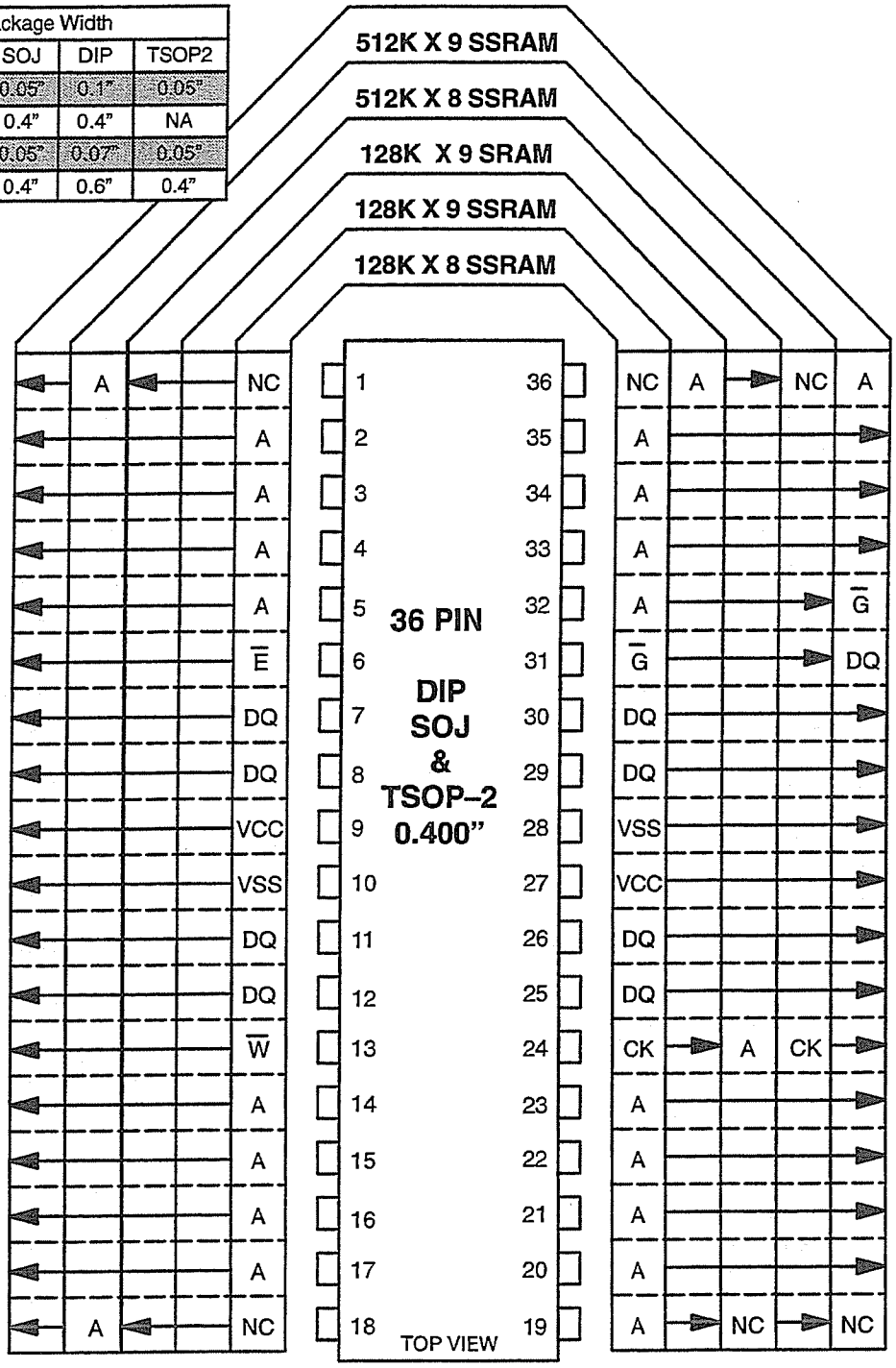


FIGURE 3.7.5–17

128K AND 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN DIP, TSOP2, & SOJ

Release 4

Burst SRAM Ball Grid Array (BGA) Package Bump Assignments, Top View							
X9	1	2	3	4	5	6	7
A	VDDQ	SA	SA	$\overline{SAP}$	SA	SA	VDDQ
B	NC	NC,SE2,SA#	NC, SA⁻	$\overline{SAC}$	NC, SA*	NC,$\overline{SE2}$,SA◇	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	NC	NC	VSS	NC, ZQ	VSS	NC	NC
E	NC	NC	VSS	$\overline{SS}$, $\overline{SE}$	VSS	NC	DQ, NC
F	VDDQ	NC	VSS	$\overline{G}$	VSS	NC	VDDQ
G	NC	DQ	VSS	$\overline{SADV}$	VSS	NC	DQ
H	DQ	NC	VSS	NC	VSS	DQ	NC
J	VDDQ	VDD	VREF, NC	VDD	VREF, NC	VDD	VDDQ
K	NC	DQ	VSS	CK, K	VSS	NC	DQ
L	DQ	NC	VSS	$\overline{CK}$, $\overline{K}$, NC	VSS	DQ	NC
M	VDDQ	NC	VSS	$\overline{SW}$	VSS	NC	VDDQ
N	NC	NC	VSS	SA1	VSS	NC	NC
P	NC	NC	VSS	SA0	VSS	NC	NC
R	NC	SA	$\overline{LBO}$	VDD	$\overline{FT}$	SA	NC
T	NC	SA	SA	SA	SA	SA	ZZ, NC
U	VDDQ	TMS, NC	TDI, NC	TCK, NC	TDO, NC	NC, TRST	VDDQ

Address Assignment and Package Dimension Table		
Density	Address Assignment	Nominal Exterior Package Dimension
1M (128K X 9)	Basic SA	14 mm X 22 mm
2M (256K X 9)	⁻	14 mm X 22 mm
4M (512K X 9)	⁻, *	14 mm X 22 mm
8M (1M X 9)	⁻, *, ◇	TBD
16 M (2M X 9)	⁻, *. ◇, #	TBD

FIGURE 3.7.5-18
128K TO 2M BY 8/9 BURST SRAM IN BGA

Synchronous SRAM Ball Grid Array (BGA) Package Bump Assignments, Top View							
X9	1	2	3	4	5	6	7
A	VDDQ	SA	SA	NC	SA	SA	VDDQ
B	NC	NC,SE2,SA#	NC, SA¯	NC	NC, SA*	NC,$\overline{SE2}$,SA◇	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	NC	NC	VSS	NC, ZQ	VSS	NC	NC
E	NC	NC	VSS	$\overline{SS}$, $\overline{SE}$	VSS	NC	DQ, NC
F	VDDQ	NC	VSS	$\overline{G}$, $\overline{SG}$	VSS	NC	VDDQ
G	NC	DQ	VSS	NC, $\overline{C}$	VSS	NC	DQ
H	DQ	NC	VSS	NC, C	VSS	DQ	NC
J	VDDQ	VDD	VREF, NC	VDD	VREF, NC	VDD	VDDQ
K	NC	DQ	VSS	CK, K	VSS	NC	DQ
L	DQ	NC	VSS	$\overline{CK}$, $\overline{K}$, NC	VSS	DQ	NC
M	VDDQ	NC	VSS	$\overline{SW}$	VSS	NC	VDDQ
N	NC	NC	VSS	SA	VSS	NC	NC
P	NC	NC	VSS	SA	VSS	NC	NC
R	NC	SA	M1, NC	VDD	M2, NC	SA	NC
T	NC	SA	SA	SA	SA	SA	ZZ, NC
U	VDDQ	TMS, NC	TDI, NC	TCK, NC	TDO, NC	NC, TRST	VDDQ

Address Assignment and Package Dimension Table		
Density	**Address Assignment**	**Nominal Exterior Package Dimension**
1M (128K X 9)	Basic SA	14 mm X 22 mm
2M (256K X 9)	¯	14 mm X 22 mm
4M 512K X 9)	¯, *	14 mm X 22 mm
8M (1M X 9)	¯, *, ◇	TBD
16 M (2M X 9)	¯, *. ◇, #	TBD

Mode Truth Table	M1	M2
Single Clock, Register Flow Through	VSS	VSS
Single Clock, Register-Register	VSS	VDD
Single Clock, Register-Latch	VDD	VSS
Dual Clock	VDD	VDD

FIGURE 3.7.5-19
128K TO 2M BY 8/9 SSRAM IN BGA

SSRAM Boundry Scan Order					
X9 Part					
Exit Order	Signal	Bump #		Exit Order	Signal	Bump #
1	M2, NC	5R		22	NC, $\overline{SA}$	3B
2	SA	6T		23	NC, SE2 SA#	2B
3	SA	4P		24	SA	3A
4	SA	4T		25	SA	3C
5	SA	6R		26	SA	2C
6	SA	5T		27	SA	2A
7	NC, ZZ	7T				
8	DQ	6L		28	DQ	2G
9	DQ	7K		29	DQ	1H
10	$\overline{K}$, NC	4L		30	ZQ, NC	4D
11	K	4K		31	$\overline{SS}$	4E
12	$\overline{G}$	4F		32	$\overline{C}$, NC	4G
				33	C, NC	4H
				34	$\overline{SW}$	4M
13	DQ	6H				
14	DQ	7G		35	DQ	2K
				36	DQ	1L
15	DQ, NC	7E				
16	SA	6A				
17	SA	6C		37	SA	3T
18	SA	5C		38	SA	2R
18	SA	5A		39	SA	4N
20	NC, $\overline{SE2}$ SA◇	6B		40	SA	2T
21	NC, SA*	5B		41	M1, NC	3R

FIGURE 3.7.5-20

128K TO 2M BY 8/9 SSRAM IN BGA BOUNDRY SCAN ORDER

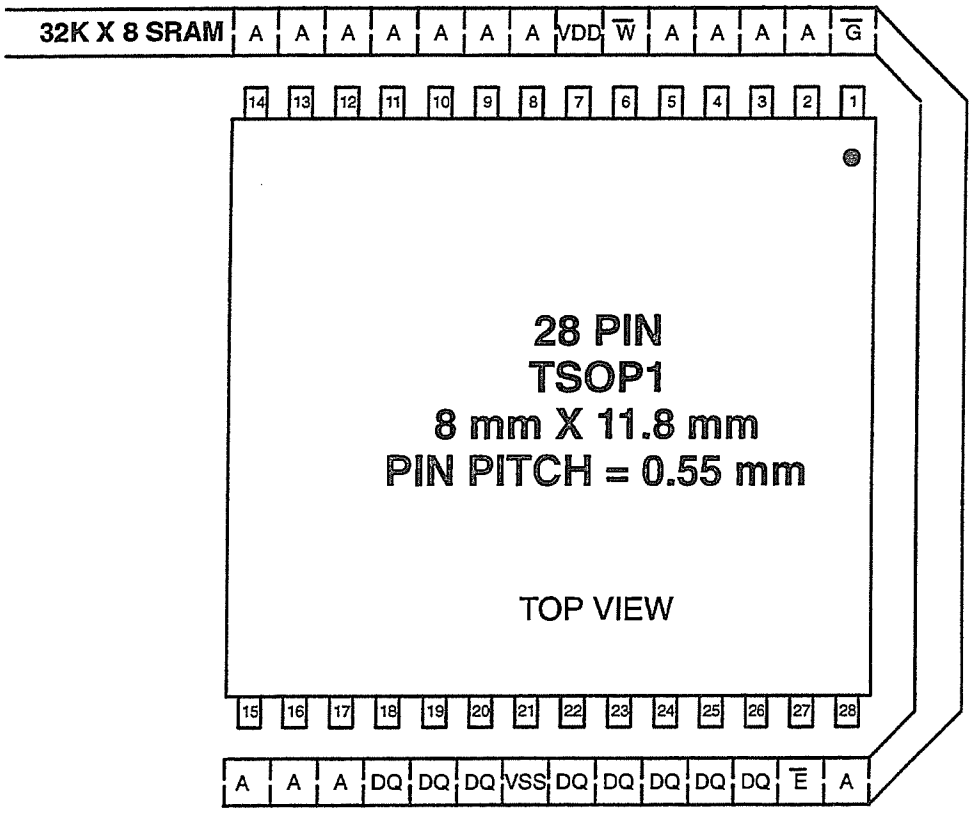


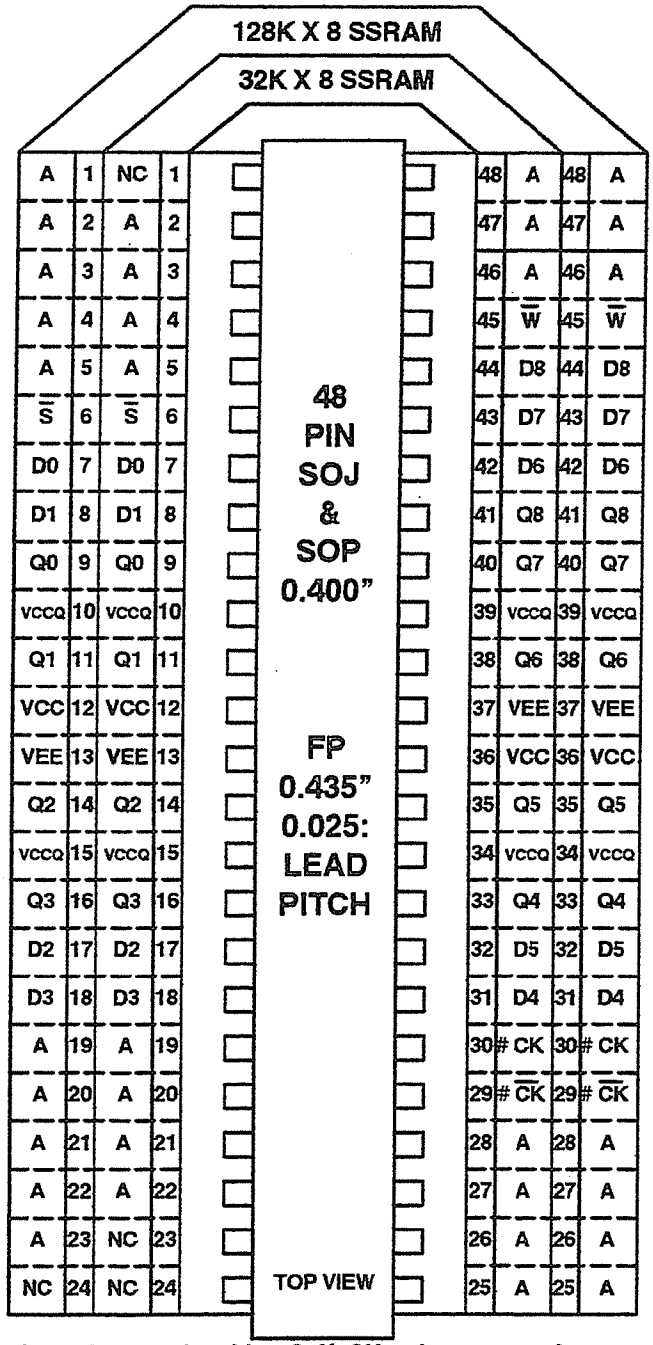
FIGURE 3.7.5–21
32K BY 8 SRAM IN TSOP–1

3.7.6 Byte Wide ECL SRAM

All of the following standards are for devices which operate with ECL interface levels and power voltages.

3.7.6.1 32K and 128K BY 8 ECL SSRAM IN SOJ, SSOP, AND FP

CAPACITY--32K, & 128K WORDS OF 8 BIT
LOGIC FEATURES--SEPARATE DATA INPUT & OUTPUT PINS
PACKAGE--48 PIN SOJ & SSOP, 0.4" wide
--48 PIN FP, 0.435 WIDE, 0.025" LEAD PITCH
SPECIAL FEATURES--MULTIPLE CENTERED POWER PINS AND EXTRA GROUNDS
PIN ASSIGNMENT--Fig. 3.7.6-1



 # The Clock pins may be either C, K, CK or L as a manufacturer option.
These parts are approved for use with 10K, 100K, or 101K interface.

FIGURE 3.7.6–1
32K AND 256K BY 9 ECL SSRAM IN SOJ, SOP, AND FP

3.7.7 Word Wide TTL SRAM

All of the following standards are for devices which operate with TTL interface levels and power voltages.

3.7.7.1 – 4K TO 64K BY 16 TTL SRAM IN DIP

CAPACITY—4K TO 64K WORDS OF 16 BITS,
ELECTRICAL INTERFACE—TTL
PACKAGE—40 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Fig. 3.7.7–1

3.7.7.2 – 4K TO 256K BY 16 TTL SRAM IN SCC

CAPACITY—4K TO 256K WORDS OF 16 BITS,
PACKAGE—44 PAD (PIN) RCC, 0.650" X 0.650"
PIN ASSIGNMENTS—Fig. 3.7.7–2

3.7.7.3 – 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN DIP

CAPACITY—16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES—Address and Data MULTIPLEXED onto common pins.
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Figs. 3.7.7–3

3.7.7.4 – 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN RCC

CAPACITY—16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES—Address and Data MULTIPLEXED onto common pins.
PACKAGE—32 PIN (PAD) RCC, 0.450" X 0.550"
PIN ASSIGNMENTS—Figs. 3.7.7–4

3.7.7.5 – 16K AND 64K BY 18 SRAM IN SCC

CAPACITY—16K, 64K WORDS OF 18 BITS,
LOGIC FEATURES—ASYNCHRONOUS ADDRESS LATCH
—UPPER BYTE AND LOWER BYTE SELECTABLE
PACKAGE—52 TERMINAL SCC, 0.750" X 0.750"
PIN ASSIGNMENTS—Figs. 3.7.7–5

3.7.7.6 – 64K BY 16 & 18 SRAM IN 44 SOJ

CAPACITY—64K WORDS OF 16 OR 18 BITS,
LOGIC FEATURES—ASYNCHRONOUS WITH OPTIONAL ADDRESS LATCH
—UPPER BYTE AND LOWER BYTE SELECTABLE
—COMMON DATA I/O
PACKAGE—44 PIN SOJ, TBD
PIN ASSIGNMENT—Fig. 3.7.5–6

3.7.7.7 – 32K AND 64K BY 16 & 18 SRAM AND SSRAM IN 52 SCC WITH LOGIC FEATURES

CAPACITY—64K WORDS OF 16 OR 18 BITS,
NOTE: These parts are optimized for use as CACHE memory for Microprocessors and come in 5 versions, each with a different set of logic features that are optimized for different environments. In addition, there are features common to all parts.
LOGIC FEATURES—ALL VERSIONS ARE UPPER AND LOWER BYTE SELECTABLE
—ALL VERSIONS HAVE COMMON DATA I/O
—SYNCHRONOUS WITH NO SPECIAL LOGIC FEATURES.
—ASYNCHRONOUS WITH DATA LATCH ENABLE.
—SYNCHRONOUS WITH DATA LATCH ENABLE.
—SYNCHRONOUS WITH BURST MODE.
—SYNCHRONOUS WITH BURST MODE, BASE ADDRESS LATCH(S) AND WRITE CLOCK (KW). SEE FIG. 3.7.7–8 FOR KW TIMING.
PACKAGE—52 TERMINAL SCC, 0.750" X 0.750" WITH A 0.050" LEAD PITCH
PIN ASSIGNMENT—Fig. 3.7.7–7

3.7.7.8 – 64K TO 256K BY 16 & 18 SRAM AND SSRAM FAMILIES IN 100 TQFP

CAPACITY—64K, 128K, OR 256K WORDS OF 16 OR 18 BITS,
LOGIC FEATURES —There are two version of this part available:
—SYNCHRONOUS WITH ADDRESS LATCH OR ASYNCHRONOUS
—UPPER BYTE AND LOWER BYTE SELECTABLE
—COMMON DATA I/O
PACKAGE—100 PIN TQFP, 20 mm v 14 mm
PIN ASSIGNMENT—Fig. 3.7.7-8

3.7.7.9 – 64K TO 1M BY 16/18 BURST SRAM IN BGA

CAPACITY—64K,128K, 256K, 512K, OR 1M WORDS OF 16 OR 18 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.7-9
These parts contain BURST addressing capability.

3.7.7.10 – 64K TO 1M BY 16/18 SSRAM IN BGA

CAPACITY—64K, 128K, 256K, 512K, 1M WORDS OF 16 OR 18 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.7-10
.Included with this standard is a table of the BOUNDRY SCAN ORDER to be used in testing the parts.
BOUNDRY SCAN ORDER TABLE—Fig. 3.7.7-11

3.7.7.11 – 64K TO 256K BY 16/18 BURST SRAM IN QFP OR TQFP

CAPACITY—64K,128K, OR 256K WORDS OF 16 OR 18 BITS,
PACKAGE—100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm Pin Pitch
PIN ASSIGNMENT—Fig. 3.7.7-12
These parts contain BURST addressing capability.

3.7.7.12 – 256K AND 1M BY 16 and 18 SRAM IN TSOP2

CAPACITY—16K, 64K WORDS OF 18 BITS,
LOGIC FEATURES—UPPER BYTE AND LOWER BYTE SELECTABLE
PACKAGE—54 P TSOP2, 10.16 mm or 12.70 mm, 0.8 mm Pin Pitch
PIN ASSIGNMENTS—Figs. 3.7.7-13

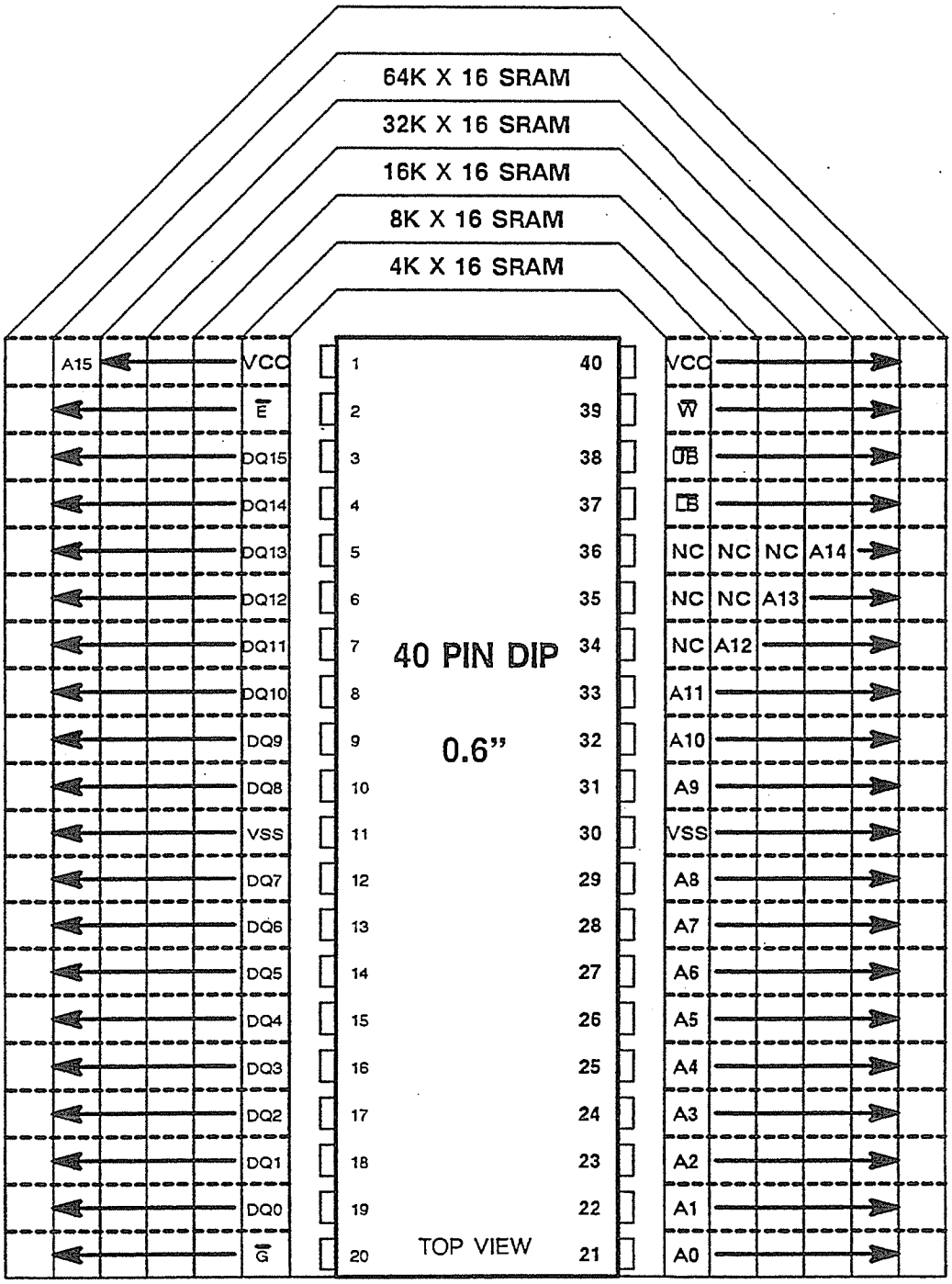


FIGURE 3.7.7-1
4K TO 64K BY 16 TTL SRAM FAMILY IN DIP

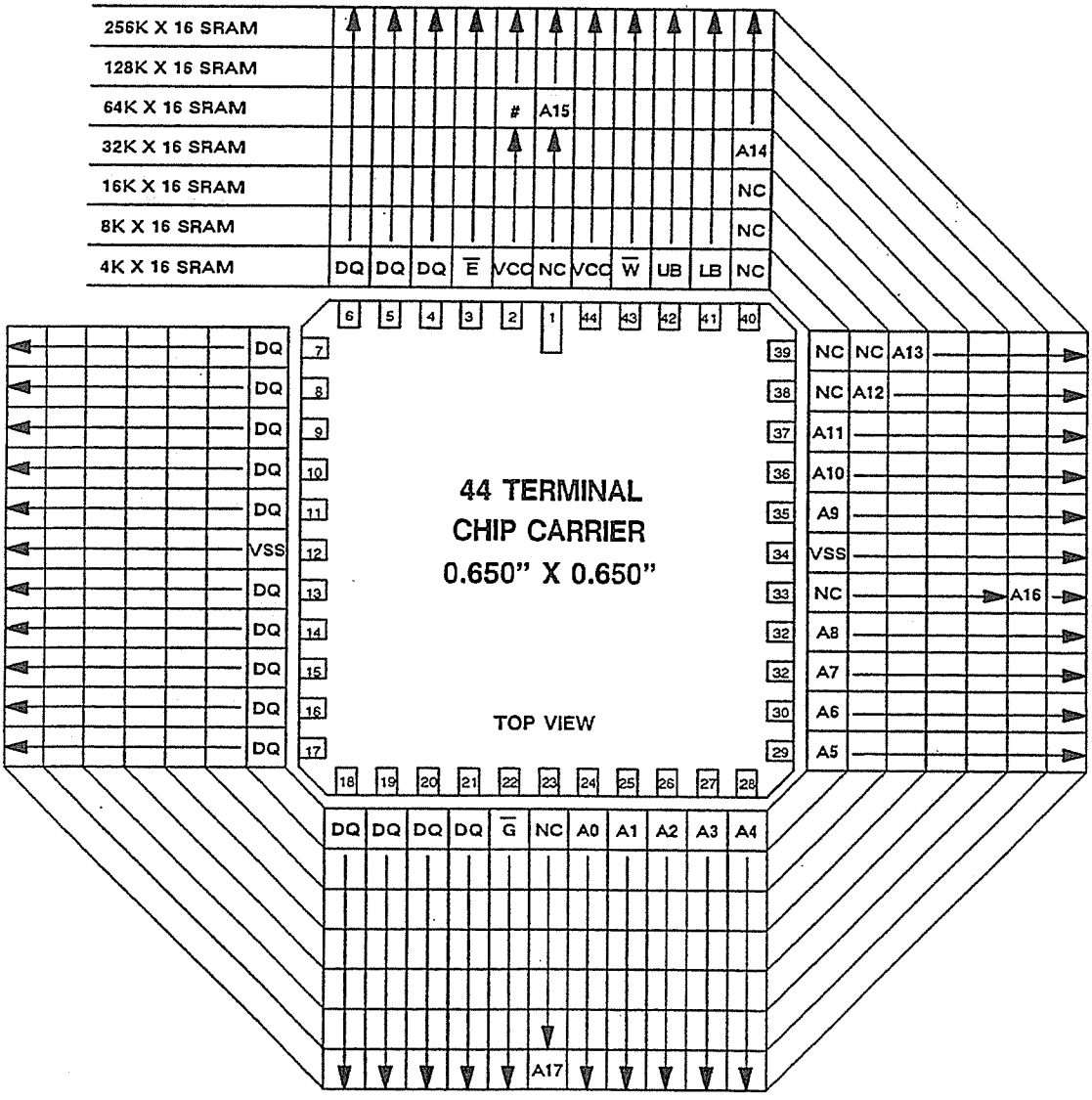
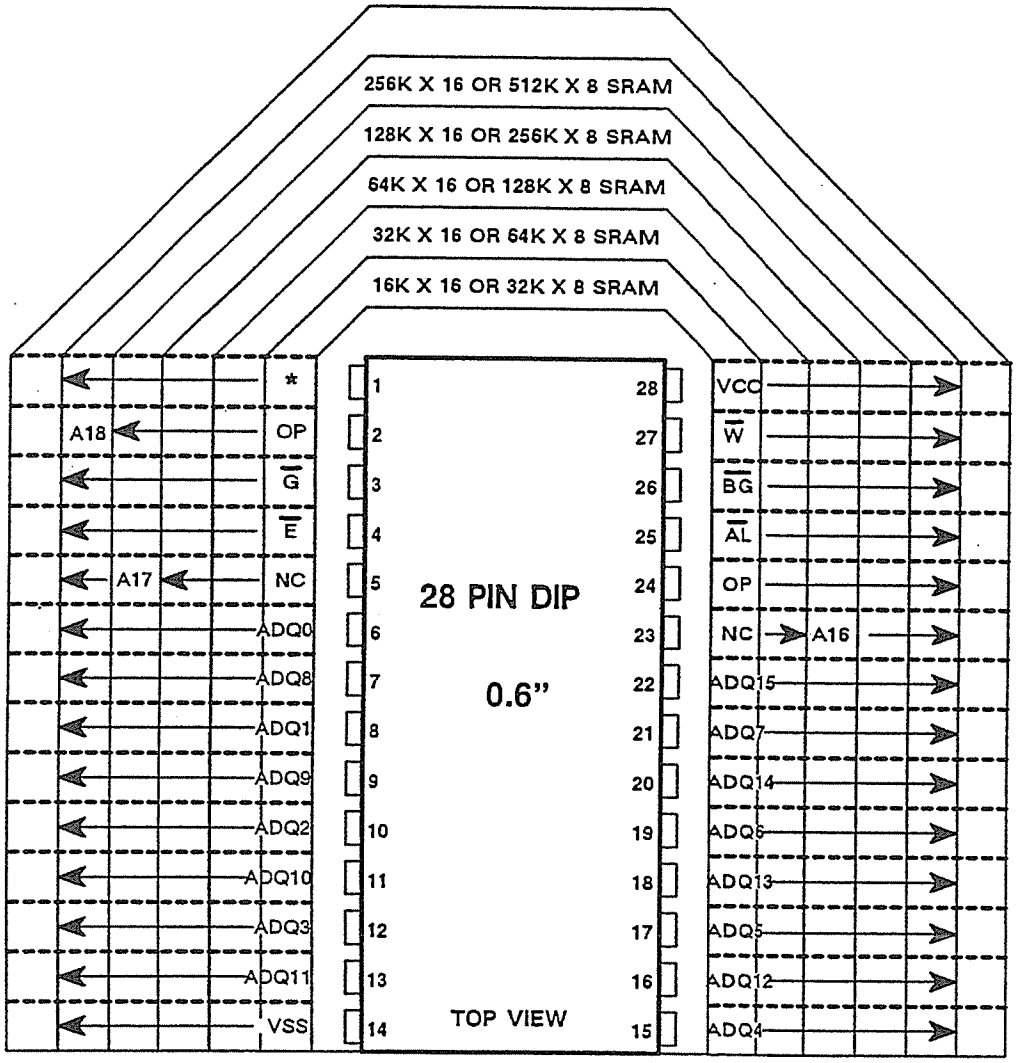


FIGURE 3.7.7-2
4K TO 256K BY 16 TTL SRAM FAMILY IN RCC

$\overline{BG}$	A0	D0–D7	D8–D15	OPERATION
L	L	LOWER BYTE	UPPER BYTE	WORD
L	H		UPPER BYTE	
H	L	LOWER BYTE		BYTE
H	H	UPPER BYTE		BYTE



* NC or VSS

FIGURE 3.7.7-3
16K TO 256K BY 16 ADDRESS/DATA MX SRAM FAMILY IN DIP

$\overline{BG}$	A0	D0–D7	D8–D15	OPERATION
L	L	LOWER BYTE	UPPER BYTE	WORD
L	H		UPPER BYTE	
H	L	LOWER BYTE		BYTE
H	H	UPPER BYTE		BYTE

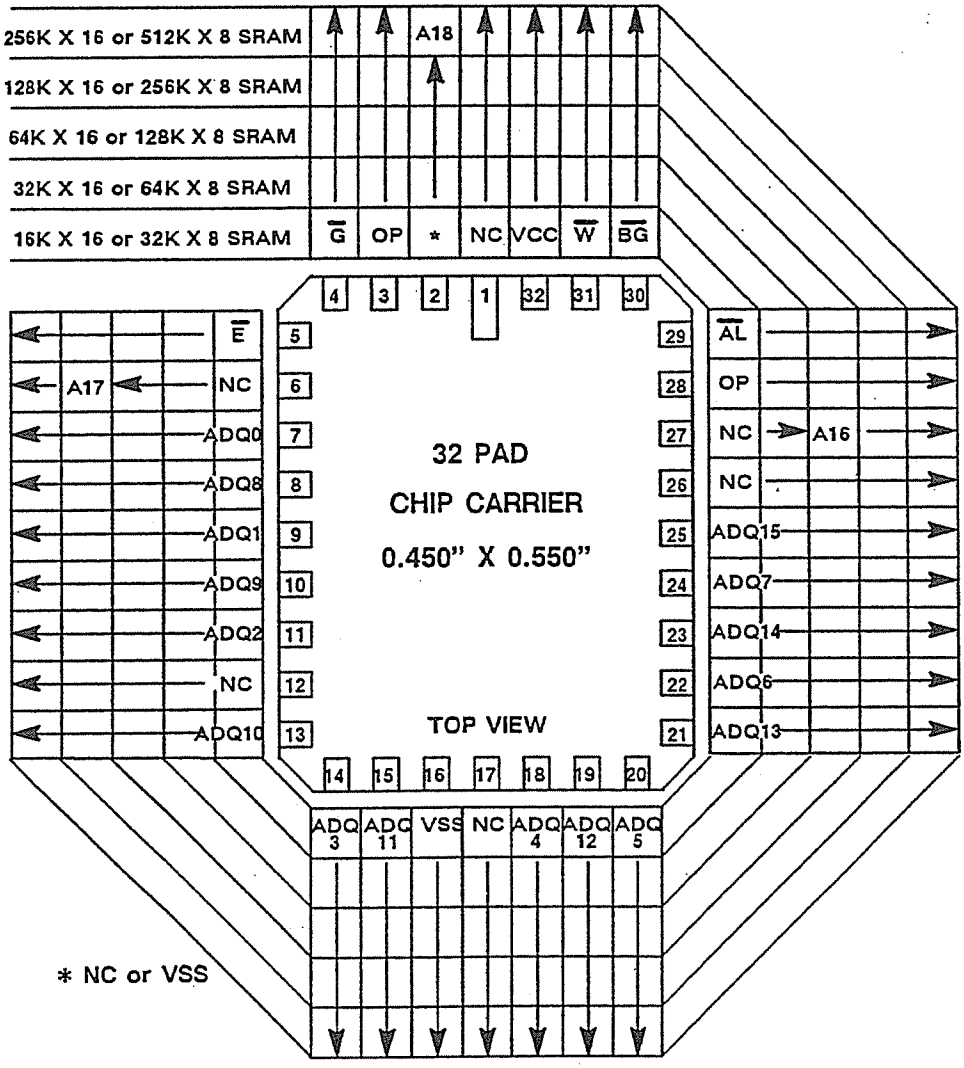
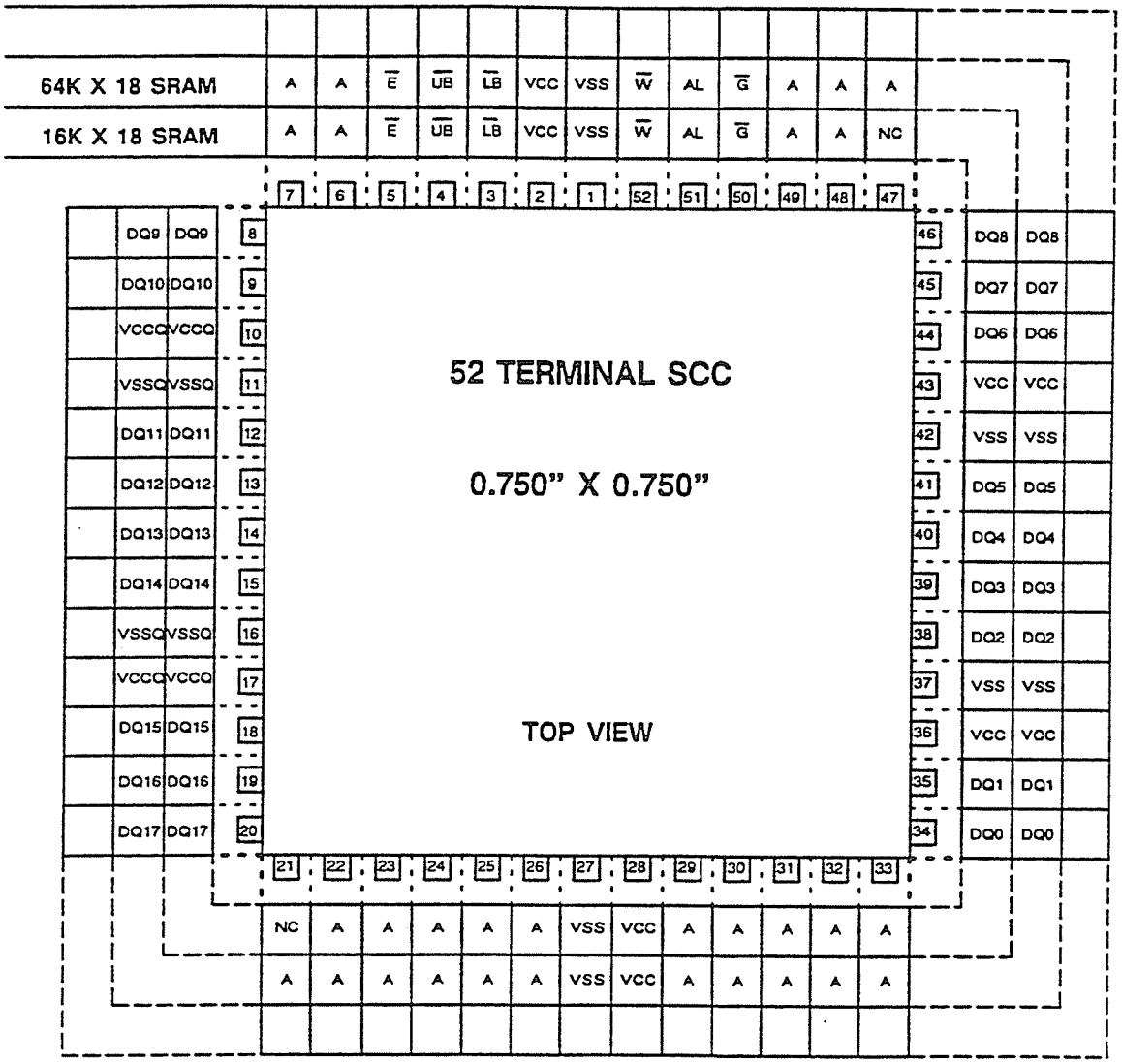
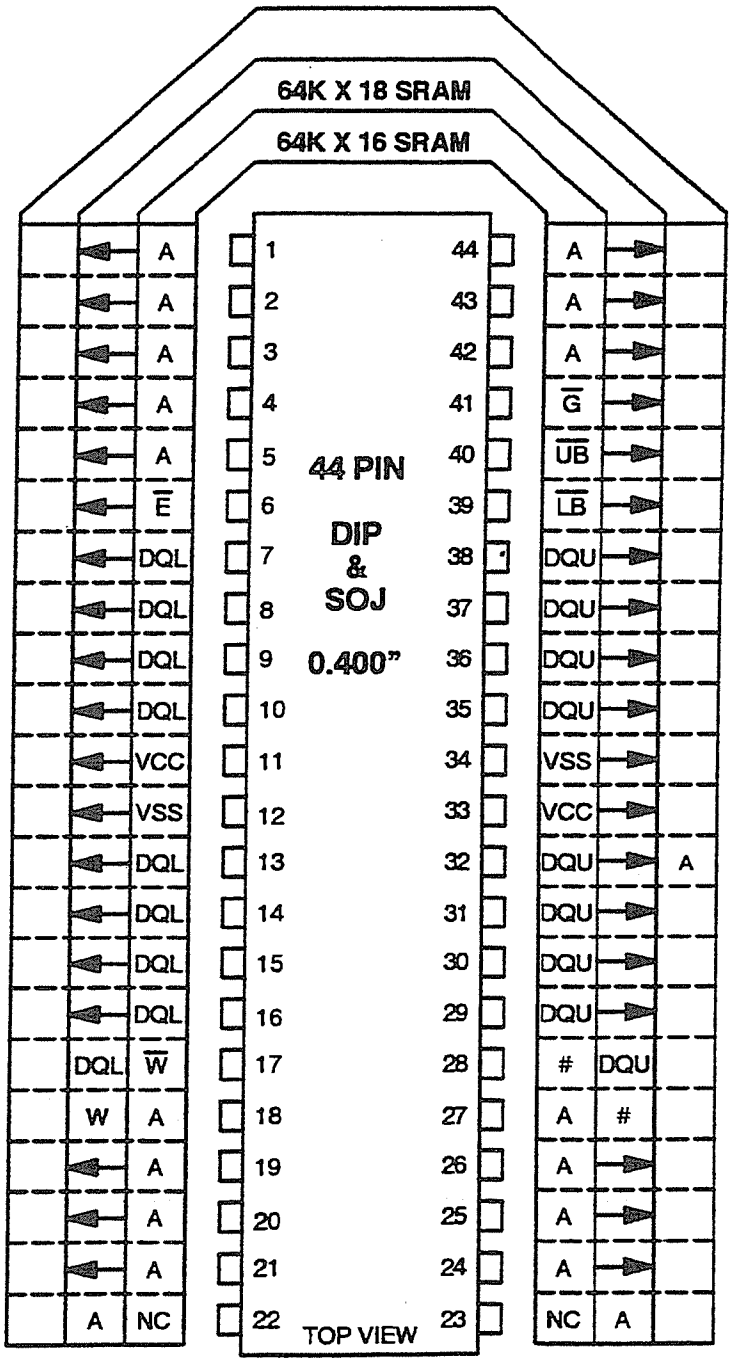


FIGURE 3.7.7-4
16K TO 256K BY 16 ADDRESS/DATA MX SRAM FAMILY IN RCC



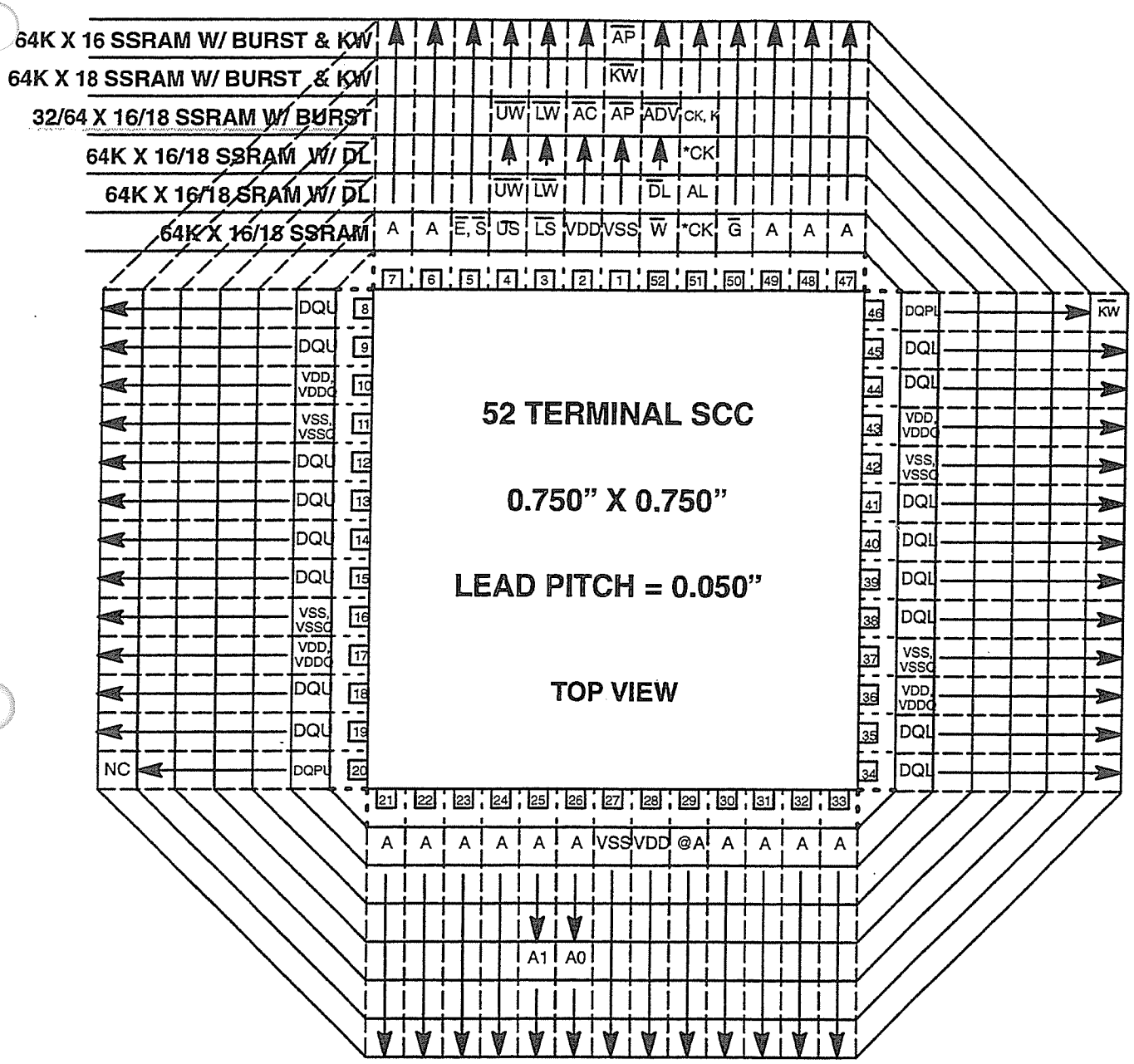
THE POWER CONNECTIONS TO PINS 10, 11, 16, 17, 36, 37, 42, OR 43 MAY BE VSSQ (VCCQ) OR VSS (VCC) AT THE OPTION OF THE MANUFACTURER.

FIGURE 3.7.7-5
16K AND 64K BY 18 SRAM IN SCC



= ALE or NC AT THE MANUFACTURERS OPTION

FIGURE 3.7.7–6
64K BY 16 & 18 SRAM IN DIP & SOJ



1, The suffix U or L on DATA or CONTROL pins designate UPPER or LOWER byte.
2, DQPU or DQPL designate upper and lower BYTE PARITY data pins for X18 devices.
3, *CK – These clock inputs may be I/O (CK), input (C), or output (K) clock.
4, On the X16 version of X16/18 devices, the DQP pins, # 20 & 46, are NC.
5, @A – On the 32K SSRAM with Burst, P 29 is a NC.

NOTE: Some of the pins on these devices have names that are application specific and are not defined in section 2 of this Standard. They are as follows: $\overline{AC}$ is the address strobe from a microprocessor cache controller and latches the base address.
$\overline{AP}$ is the address strobe from a microprocessor and latches the base address.
$\overline{ADV}$ advances the burst address counter.
$\overline{DL}$ is DATA LATCH ENABLE,
$\overline{AL}$ is ADDRESS LATCH ENABLE.
A0 & A1 are specified due to their signficance as burst addresses. If more than two burst address bits are provided, the additional bits are supplied on pins 24 & 25.

FIGURE 3.7.7–7 A

32K & 64K BY 16 & 18 SRAM AND SSRAM WITH LOGIC FEATURES IN SCC

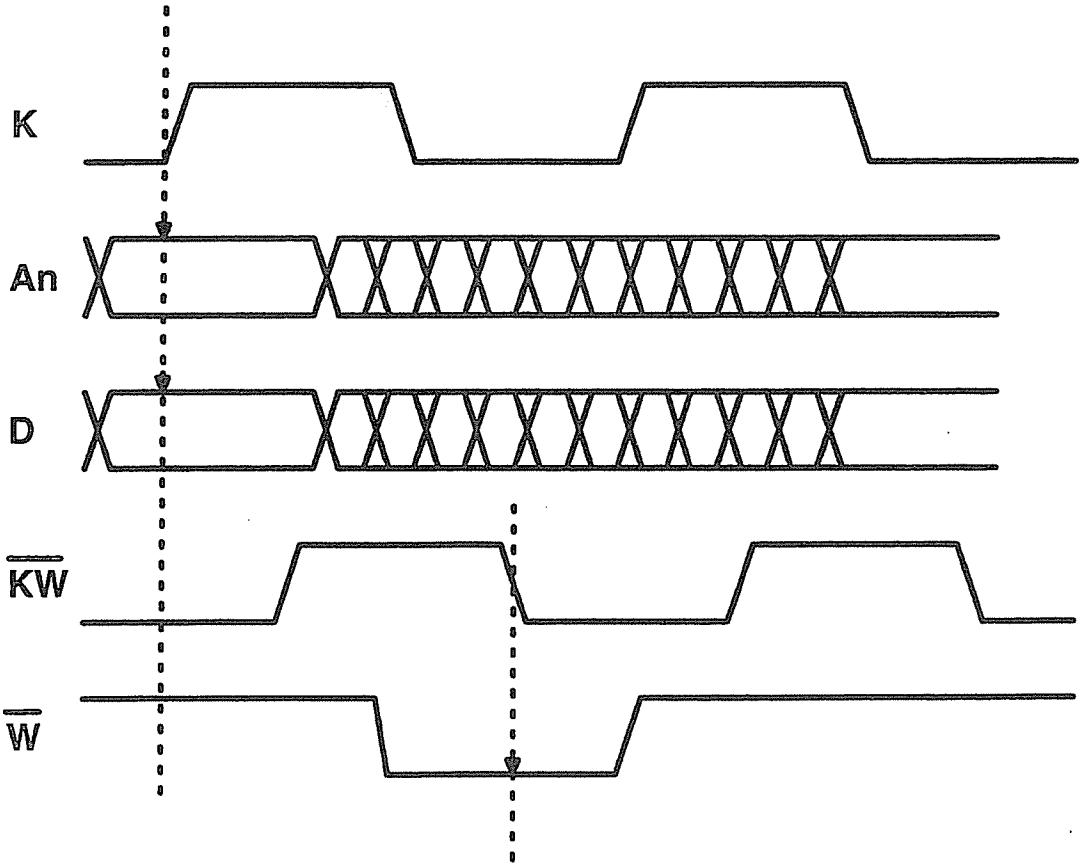
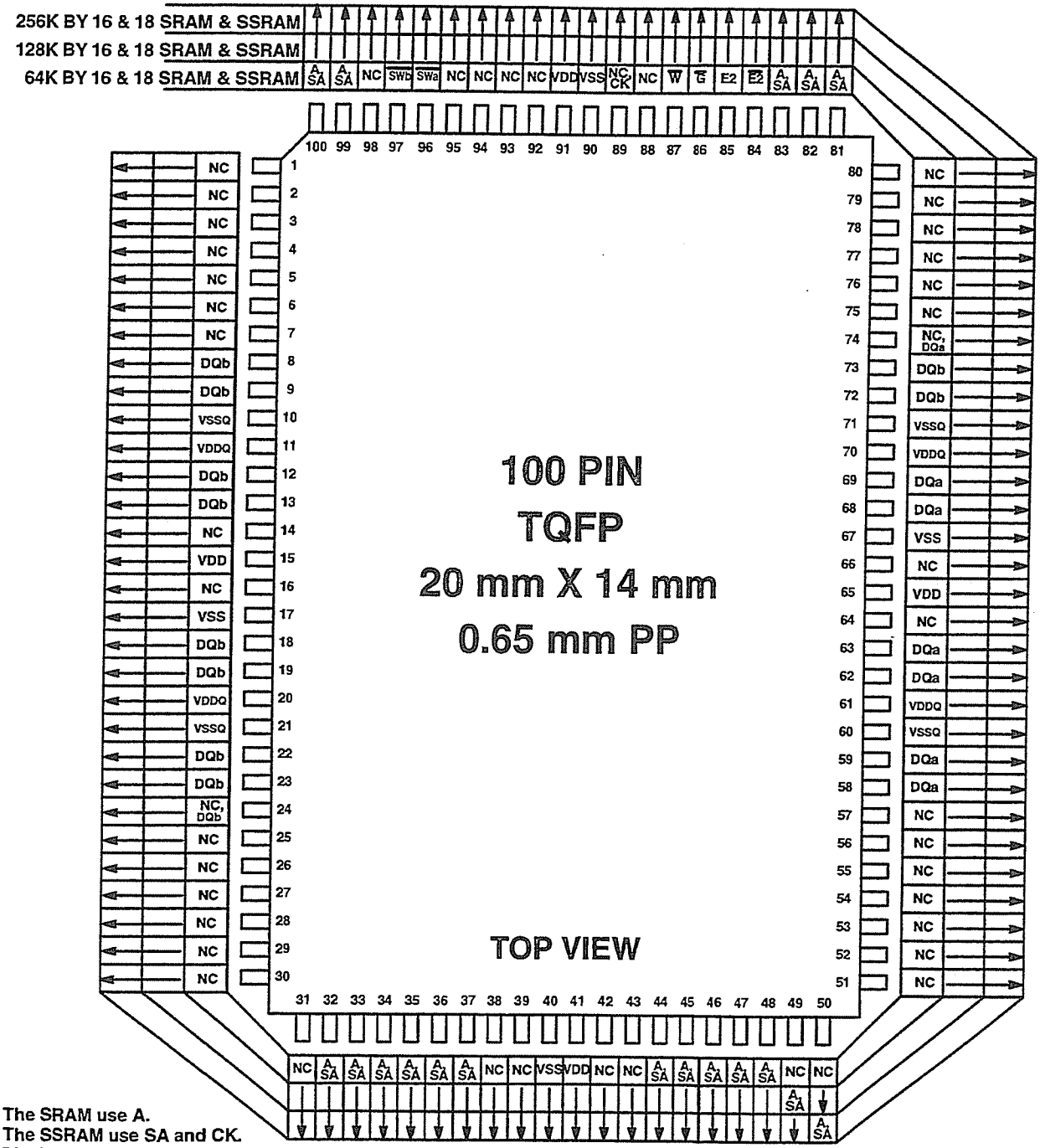


FIGURE 3.7.7–7 B
WRITE CLOCK TIMING FOR SSRAM WITH BURST MODE



The SRAM use A.
The SSRAM use SA and CK.
The PINS labeled "NC, DQx" are intended to be used as parity bits for X18 parts.

FIGURE 3.7.7–8
64K TO 256K BY 16 & 18 SRAM AND SSRAM IN TQFP

Release 5

Burst SRAM Ball Grid Array (BGA) Package Bump Assignments, Top View							
X18	1	2	3	4	5	6	7
A	VDDQ	SA	SA	$\overline{SAP}$	SA	SA	VDDQ
B	NC	NC,SE2,SA#	NC, SA¯	$\overline{SAC}$	NC, SA*	NC,$\overline{SE2}$,SA◇	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	DQb	NC	VSS	NC, ZQ	VSS	DQa, NC	NC
E	NC	DQb	VSS	$\overline{SS}$, $\overline{SE}$	VSS	NC	DQa
F	VDDQ	NC	VSS	$\overline{G}$	VSS	DQa	VDDQ
G	NC	DQb	$\overline{SWb}$, $\overline{SBb}$	$\overline{SADV}$	VSS	NC	DQa
H	DQb	NC	VSS	NC, $\overline{SGW}$	VSS	DQa	NC
J	VDDQ	VDD	VREF, NC	VDD	VREF, NC	VDD	VDDQ
K	NC	DQb	VSS	CK, K	VSS	NC	DQa
L	DQb	NC	VSS	$\overline{CK}$, $\overline{K}$, NC	$\overline{SWa}$, $\overline{SBa}$	DQa	NC
M	VDDQ	DQb	VSS	NC, $\overline{SW}$	VSS	NC	VDDQ
N	DQb	NC	VSS	SA1	VSS	DQa	NC
P	NC	DQb, NC	VSS	SA0	VSS	NC	DQa
R	NC	SA	$\overline{LBO}$	VDD	$\overline{FT}$	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ, NC
U	VDDQ	TMS, NC	TDI, NC	TCK, NC	TDO, NC	NC, TRST	VDDQ

Address Assignment and Package Dimension Table		
Density	**Address Assignment**	**Nominal Exterior Package Dimension**
1M (64K X 18)	Basic SA	14 mm X 22 mm
2M (128K X 18)	¯	14 mm X 22 mm
4M (256K X 18)	¯, *	14 mm X 22 mm
8M (512K X 18)	¯, *, ◇	TBD
16 M (1M X 18)	¯, *. ◇, #	TBD

FIGURE 3.7.7-9
64K TO 1M BY 16 & 18 BURST SRAM IN BGA

Synchronous SRAM Ball Grid Array (BGA) Package Bump Assignments, Top View							
X18	1	2	3	4	5	6	7
A	VDDQ	SA	SA	NC	SA	SA	VDDQ
B	NC	NC,SE2,SA#	NC, SA~	NC	NC, SA*	NC,$\overline{SE2}$,SA◇	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	DQb	NC	VSS	NC, ZQ	VSS	DQa, NC	NC
E	NC	DQb	VSS	$\overline{SS}$, $\overline{SE}$	VSS	NC	DQa
F	VDDQ	NC	VSS	$\overline{G}$, $\overline{SG}$	VSS	DQa	VDDQ
G	NC	DQb	$\overline{SBb}$	NC, $\overline{C}$	VSS	NC	DQa
H	DQb	NC	VSS	NC, C	VSS	DQa	NC
J	VDDQ	VDD	VREF, NC	VDD	VREF, NC	VDD	VDDQ
K	NC	DQb	VSS	CK, K	VSS	NC	DQa
L	DQb	NC	VSS	$\overline{CK}$, $\overline{K}$, NC	$\overline{SBa}$	DQa	NC
M	VDDQ	DQb	VSS	$\overline{SW}$	VSS	NC	VDDQ
N	DQb	NC	VSS	SA	VSS	DQa	NC
P	NC	DQb, NC	VSS	SA	VSS	NC	DQa
R	NC	SA	M1, NC	VDD	M2, NC	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ, NC
U	VDDQ	TMS, NC	TDI, NC	TCK, NC	TDO, NC	NC, TRST	VDDQ

Address Assignment and Package Dimension Table		
Density	**Address Assignment**	**Nominal Exterior Package Dimension**
1M (64K X 18)	Basic SA	14 mm X 22 mm
2M (128K X 18)	~	14 mm X 22 mm
4M (256K X 18)	~, *	14 mm X 22 mm
8M (512K X 18)	~, *, ◇	TBD
16 M (1M X 18)	~, *. ◇, #	TBD

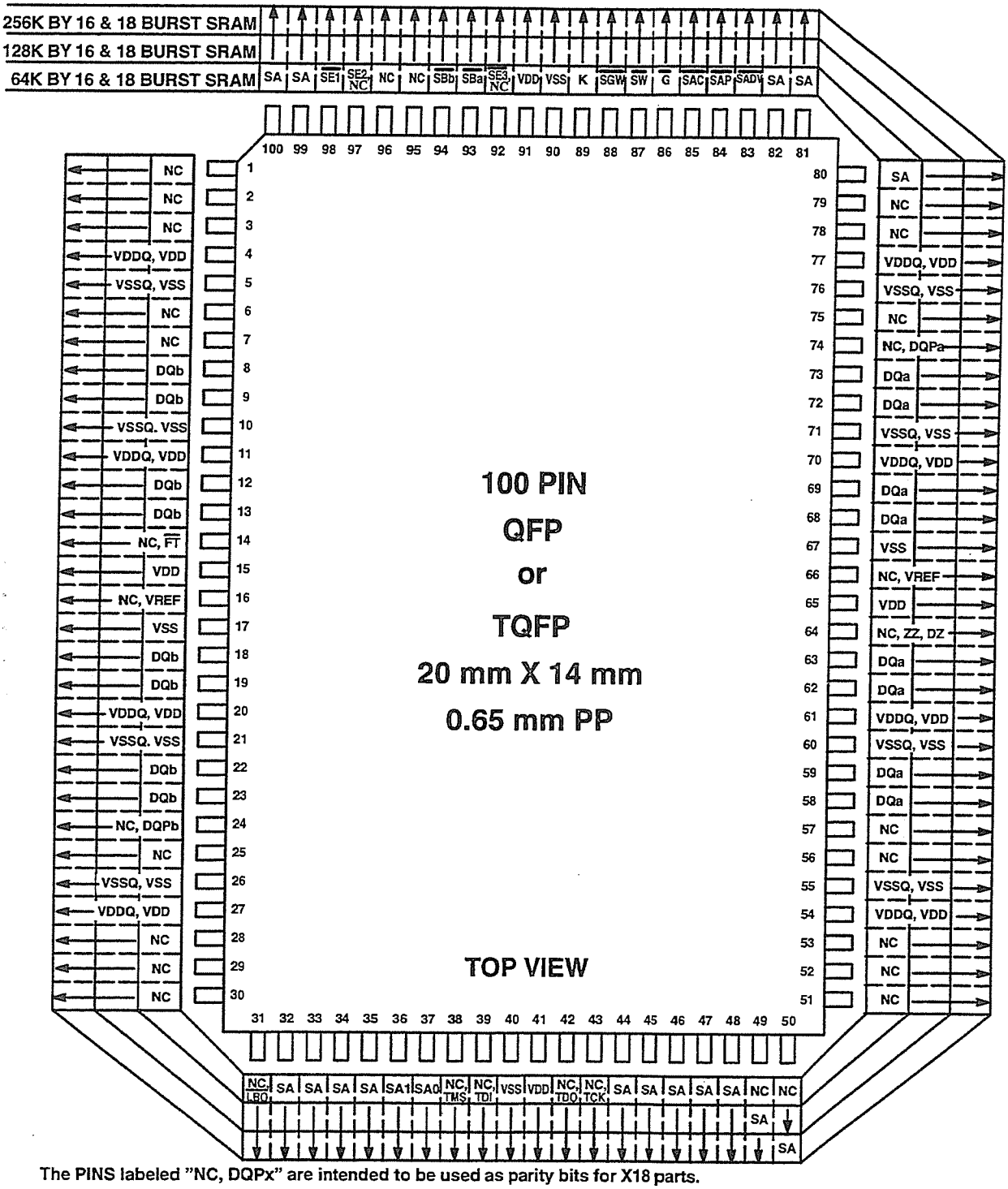
Mode Truth Table	M1	M2
Single Clock, Register Flow Through	VSS	VSS
Single Clock, Register–Register	VSS	VDD
Single Clock, Register–Latch	VDD	VSS
Dual Clock	VDD	VDD

FIGURE 3.7.7–10
64K TO 1M BY 16 & 18 SSRAM IN BGA

SSRAM Boundry Scan Order						
X18 Part						
Exit Order	Signal	Bump #		Exit Order	Signal	Bump #
1	M2, NC	5R		26	NC, SA~	3B
2	SA			27	NC, SE2 SA#	2B
3	SA	6T		28	SA	3A
		4P		29	SA	3C
4	SA	6R		30	SA	2C
5	SA	5T		31	SA	2A
6	NC, ZZ	7T				
				32	DQB	1D
7	DQa	7P		33	DQb	2E
8	DQa	6N				
				34	DQb	2G
9	DQa	6L				
				35	DQb	1H
10	DQa	7K		36	$\overline{SBb}$	3G
11	$\overline{SBa}$	5L		37	ZQ, NC	4D
12	$\overline{K}$, NC	4L		38	$\overline{SS}$	4E
13	K	4K		39	$\overline{C}$, NC	4G
14	G	4F		40	C, NC	4H
				41	$\overline{SW}$	4M
15	DQa	6H				
16	DQa	7G		42	DQb	2K
				43	DQb	1L
17	DQa	6F				
18	DQa	7E		44	DQb	2M
				45	DQb	1N
19	DQa, NC	6D				
20	SA	6A		46	DQb, NC	2P
21	SA	6C		47	SA	3T
22	SA	5C		48	SA	2R
23	SA	5A		49	SA	4N
24	NC, $\overline{SE2}$ SA◇	6B		50	SA	2T
25	NC, SA*	5B		51	M1, NC	3R

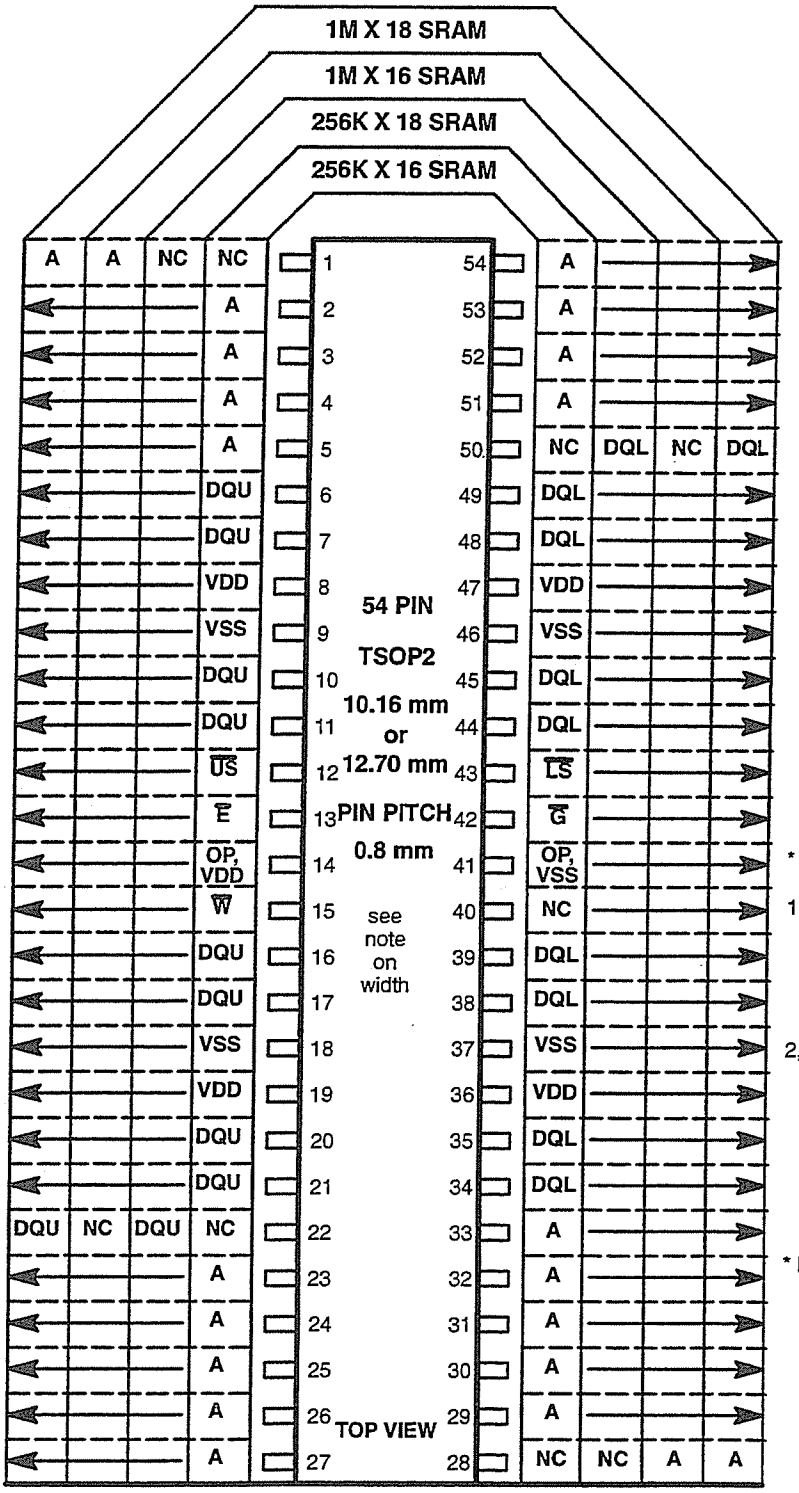
FIGURE 3.7.7–11
64K TO 1M BY 16 & 18 SSRAM IN BGA BOUNDRY SCAN ORDER

Release 5c7



The PINS labeled "NC, DQPx" are intended to be used as parity bits for X18 parts.

FIGURE 3.7.7–12
64K TO 256K BY 16 & 18 BURST SRAM IN TQFP



* NOTES:

1, Pins 14 & 41 that are labeled "OP" are intended to be used for supplier specific options.
If the "OP" functions are unused, set P14 to VDD & P41 to VSS.

2, The I/O pins labeled "DQL" are selected by the "LS" pin and "DQU" are selected by "US"

* PACKAGE NOTES:

The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G

The 256K devices are approved in a 10.16 mm wide package, the 1M devices in a 12.7 mm wide package.

FIGURE 3.7.7–13
256K & 1M BY 16 & 18 SRAM IN TSOP2

3.7.8 Double Word Wide TTL SRAM

All of the following standards are for devices which operate with TTL or any of the lower voltage interface levels and power supply voltages as defined in the individual standards.

3.7.8.1 – 32K TO 128K BY 32 & 36 BURST SSRAM IN TQFP

CAPACITY—32K, 64K, OR 128K, WORDS OF 32 OR 36 BITS,
PACKAGE—100 PIN TQFP, 20 mm X 14 mm WITH 0.65 mm PP
PIN ASSIGNMENT—Fig. 3.7.8–1
These parts combine the features of Synchronous SRAM with BURST addressing capability. This standard modifies the one published previously in Release 5 ab adding new functions and deleting some that were not used.

3.7.8.2 – 32K TO 128K BY 32 & 36 SRAM AND SSRAM FAMILIES IN 100 TQFP

CAPACITY—32K, 64K, OR 128K, WORDS OF 32 OR 36 BITS,
LOGIC FEATURES —There are two version of this part available:
—SYNCHRONOUS WITH ADDRESS LATCH OR ASYNCHRONOUS
—UPPER BYTE AND LOWER BYTE SELECTABLE
—COMMON DATA I/O
PACKAGE—100 PIN TQFP, 20 mm X 14 mm 0.65 mm PP
PIN ASSIGNMENT—Fig. 3.7.8–2

3.7.8.3 – 32K TO 512K BY 32 & 36 BURST SRAM IN BGA

CAPACITY—32K, 64K,128K, 256K, OR 512K WORDS OF 32 OR 36 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.8–3
These parts contain BURST addressing capability.

3.7.8.4 – 32K TO 512K BY 16 & 18 SSRAM IN BGA

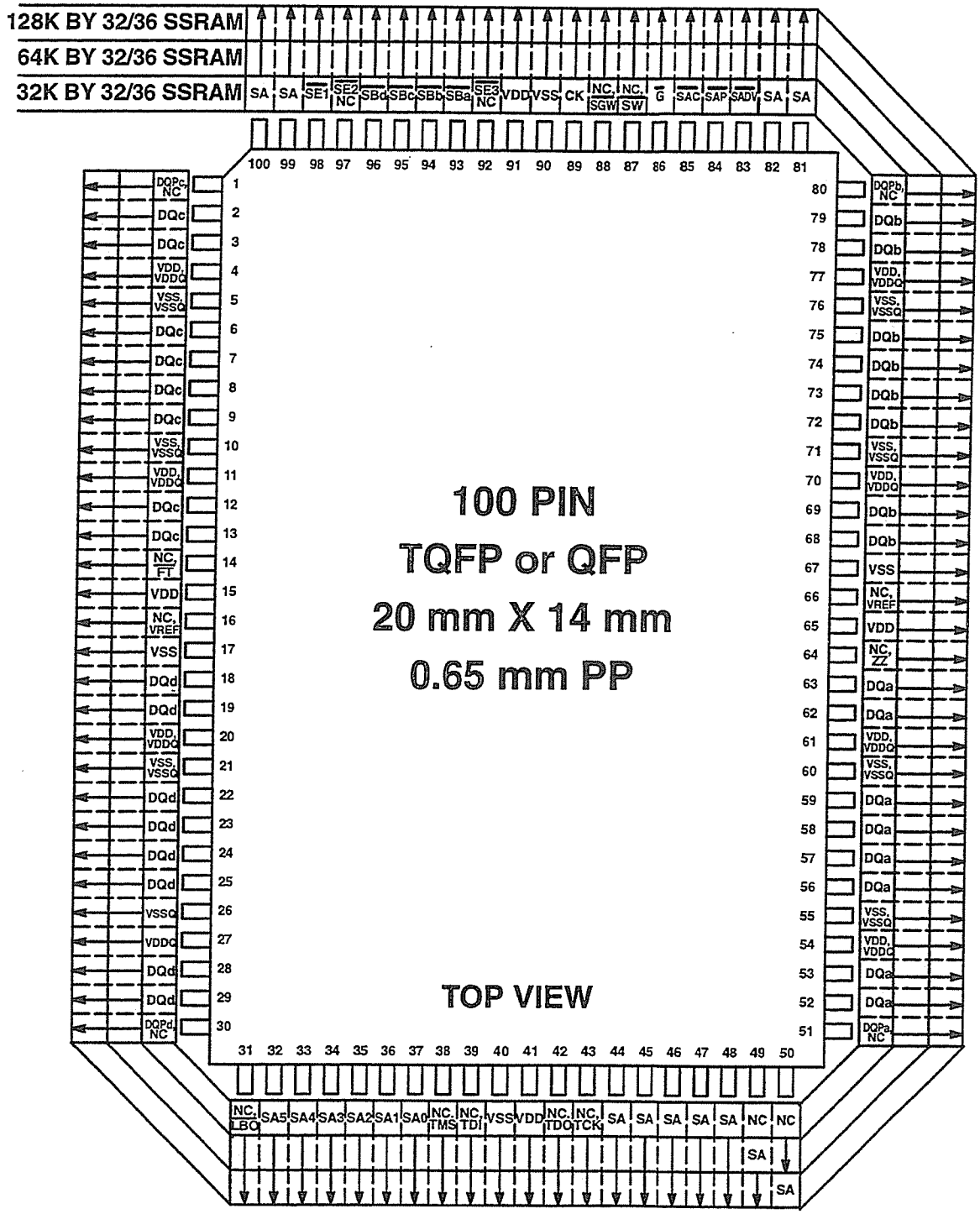
CAPACITY—32K, 64K, 128K, 256K, OR 512K WORDS OF 32 OR 36 BITS,
PACKAGE—7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.8–4
.Included with this standard is a table of the BOUNDRY SCAN ORDER to be used in testing the parts.
BOUNDRY SCAN ORDER TABLE—Fig. 3.7.8–5

3.7.8.5 – 16K TO 64K BY 64 & 72 BURST SSRAM IN QFP

CAPACITY—32K, 64K, OR 128K, WORDS OF 32 OR 36 BITS,
PACKAGE—120 PIN TQFP, 20 mm X 14 mm WITH 0.5 mm PP
PIN ASSIGNMENT—Fig. 3.7.8–6
These parts combine the features of Synchronous SRAM with BURST addressing capability.

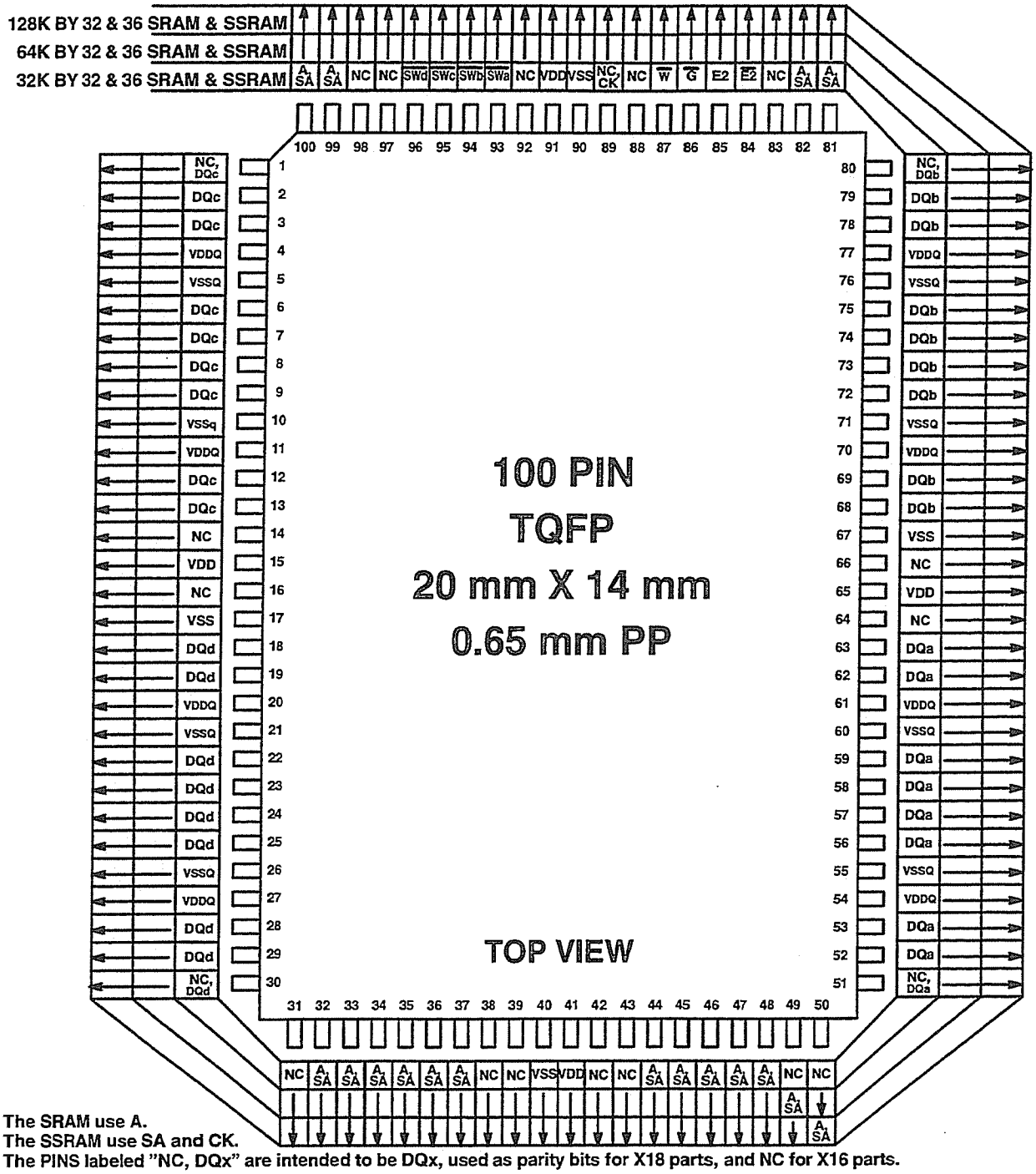
3.7.8.6 – 16K TO 256K BY 64 & 72 BURST SSRAM IN BGA

CAPACITY—16K, 32K, 64K, 128K, OR 256K WORDS OF 64 OR 72 BITS,
PACKAGE—11 X 19 BALL BGA 20 mm X 25 mm OR UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.8–7
These parts combine the features of Synchronous SRAM with BURST addressing capability.



The PINS labeled "NC, DQPx" are intended to be used as parity bits for X36 parts.

FIGURE 3.7.8-1
32K TO 128K BY 32 or 36 BURST SRAM IN TQFP



The SRAM use A.
The SSRAM use SA and CK.
The PINS labeled "NC, DQx" are intended to be DQx, used as parity bits for X18 parts, and NC for X16 parts.

FIGURE 3.7.8–2
32K TO 128K BY 32 & 36 SRAM AND SSRAM IN TQFP

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Burst SRAM Ball Grid Array (BGA) Package Bump Assignments, Top View							
X36	1	2	3	4	5	6	7
A	VDDQ	SA	SA	$\overline{SAP}$	SA	SA	VDDQ
B	NC	NC,$\overline{SE2}$,SA#	NC, SA^{-}	$\overline{SAC}$	NC, SA*	NC,$\overline{SE2}$,SA◇	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	DQc	DQc, NC	VSS	NC, ZQ	VSS	DQb, NC	DQb
E	DQc	DQc	VSS	$\overline{SS}$, $\overline{SE}$	VSS	DQb	DQb
F	VDDQ	DQc	VSS	$\overline{G}$	VSS	DQb	VDDQ
G	DQc	DQc	$\overline{SWc}$, $\overline{SBc}$	$\overline{SADV}$	$\overline{SWb}$, $\overline{SBb}$	DQb	DQb
H	DQc	DQc	VSS	NC, $\overline{SGW}$	VSS	DQb	DQb
J	VDDQ	VDD	VREF, NC	VDD	VREF, NC	VDD	VDDQ
K	DQd	DQd	VSS	CK, K	VSS	DQa	DQa
L	DQd	DQd	$\overline{SWd}$, $\overline{SBd}$	$\overline{CK}$, $\overline{K}$, NC	$\overline{SWa}$, $\overline{SBa}$	DQa	DQa
M	VDDQ	DQd	VSS	NC, $\overline{SW}$	VSS	DQa	VDDQ
N	DQd	DQd	VSS	SA1	VSS	DQa	DQa
P	DQd	DQd, NC	VSS	SA0	VSS	DQa, NC	DQa
R	NC	SA	$\overline{LBO}$	VDD	$\overline{FT}$	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ, NC
U	VDDQ	TMS, NC	TDI, NC	TCK, NC	TDO, NC	NC, TRST	VDDQ

Address Assignment and Package Dimension Table		
Density	**Address Assignment**	**Nominal Exterior Package Dimension**
1M (32K X 36)	Basic SA	14 mm X 22 mm
2M (64K X 36)	$^{-}$	14 mm X 22 mm
4M (128K X 36)	$^{-}$, *	14 mm X 22 mm
8M (256K X 36)	$^{-}$, *, ◇	TBD
16 M (512K X 36)	$^{-}$, *. ◇, #	TBD

FIGURE 3.7.8-3
32K TO 512K BY 32 & 36 BURST SRAM IN BGA

Synchronous SRAM Ball Grid Array (BGA) Package Bump Assignments, Top View							
X36	1	2	3	4	5	6	7
A	VDDQ	SA	SA	NC	SA	SA	VDDQ
B	NC	NC,SE2,SA#	NC, SA¯	NC	NC, SA*	NC,$\overline{SE2}$,SA◇	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	DQc	DQc, NC	VSS	NC, ZQ	VSS	DQb, NC	DQb
E	DQc	DQc	VSS	$\overline{SS}$, $\overline{SE}$	VSS	DQb	DQb
F	VDDQ	DQc	VSS	$\overline{G}$, $\overline{SG}$	VSS	DQb	VDDQ
G	DQc	DQc	$\overline{SBc}$	NC, $\overline{C}$	$\overline{SBb}$	DQb	DQb
H	DQc	DQc	VSS	NC, C	VSS	DQb	DQb
J	VDDQ	VDD	VREF, NC	VDD	VREF, NC	VDD	VDDQ
K	DQd	DQd	VSS	CK, K	VSS	DQa	DQa
L	DQd	DQd	$\overline{SBd}$	$\overline{CK}$, $\overline{K}$, NC	$\overline{SBa}$	DQa	DQa
M	VDDQ	DQd	VSS	$\overline{SW}$	VSS	DQa	VDDQ
N	DQd	DQd	VSS	SA	VSS	DQa	DQa
P	DQd	DQd, NC	VSS	SA	VSS	DQa, NC	DQa
R	NC	SA	M1, NC	VDD	M2, NC	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ, NC
U	VDDQ	TMS, NC	TDI, NC	TCK, NC	TDO, NC	NC, TRST	VDDQ

Address Assignment and Package Dimension Table		
Density	**Address Assignment**	**Nominal Exterior Package Dimension**
1M (32K X 36)	Basic SA	14 mm X 22 mm
2M (64K X 36)	¯	14 mm X 22 mm
4M (128K X 36)	¯, *	14 mm X 22 mm
8M (256K X 36)	¯, *, ◇	TBD
16 M (512K X 36)	¯, *. ◇, #	TBD

Mode Truth Table	M1	M2
Single Clock, Register Flow Through	VSS	VSS
Single Clock, Register–Register	VSS	VDD
Single Clock, Register–Latch	VDD	VSS
Dual Clock	VDD	VDD

FIGURE 3.7.8-4
32K TO 512K BY 32 & 36 SSRAM IN BGA

SSRAM Boundry Scan Order						
X36 Part						
Exit Order	Signal	Bump #		Exit Order	Signal	Bump #
1	M2, NC	5R		36	NC, $\overline{SA}$	3B
				37	NC, SE2 SA#	2B
2	SA	4P		38	SA	3A
3	SA	4T		39	SA	3C
4	SA	6R		40	SA	2C
5	SA	5T		41	SA	2A
6	NC, ZZ	7T		42	DQc,NC	2D
7	DQa, NC	6P		43	DQc	1D
8	DQa	7P		44	DQc	2E
9	DQa	6N		45	DQc	1E
10	DQa	7N		46	DQc	2F
11	DQa	6M		47	DQc	2G
12	DQa	6L		48	DQc	1G
13	DQa	7L		49	DQc	2H
14	DQa	6K		50	DQc	1H
15	DQa	7K		51	$\overline{SBc}$	3G
16	$\overline{SBa}$	5L		52	ZQ, NC	4D
17	$\overline{K}$, NC	4L		53	$\overline{SS}$	4E
18	K	4K		54	$\overline{C}$, NC	4G
19	$\overline{G}$	4F		55	C, NC	4H
20	$\overline{SBb}$	5G		56	$\overline{SW}$	4M
21	DQb	7H		57	$\overline{SBd}$	3L
22	DQb	6H		58	DQd	1K
23	DQb	7G		59	DQd	2K
24	DQb	6G		60	DQd	1L
25	DQb	6F		61	DQd	2L
26	DQb	7E		62	DQd	2M
27	DQb	6E		63	DQd	1N
28	DQb	7D		64	DQd	2N
29	DQb, NC	6D		65	DQd	1P
30	SA	6A		66	DQd, NC	2P
31	SA	6C		67	SA	3T
32	SA	5C		68	SA	2R
33	SA	5A		69	SA	4N
34	NC, $\overline{SE2}$ SA◇	6B				
35	NC, SA*	5B		70	M1, NC	3R

FIGURE 3.7.8-5

32K TO 512K BY 32 & 36 SSRAM IN BGA BOUNDRY SCAN ORDER

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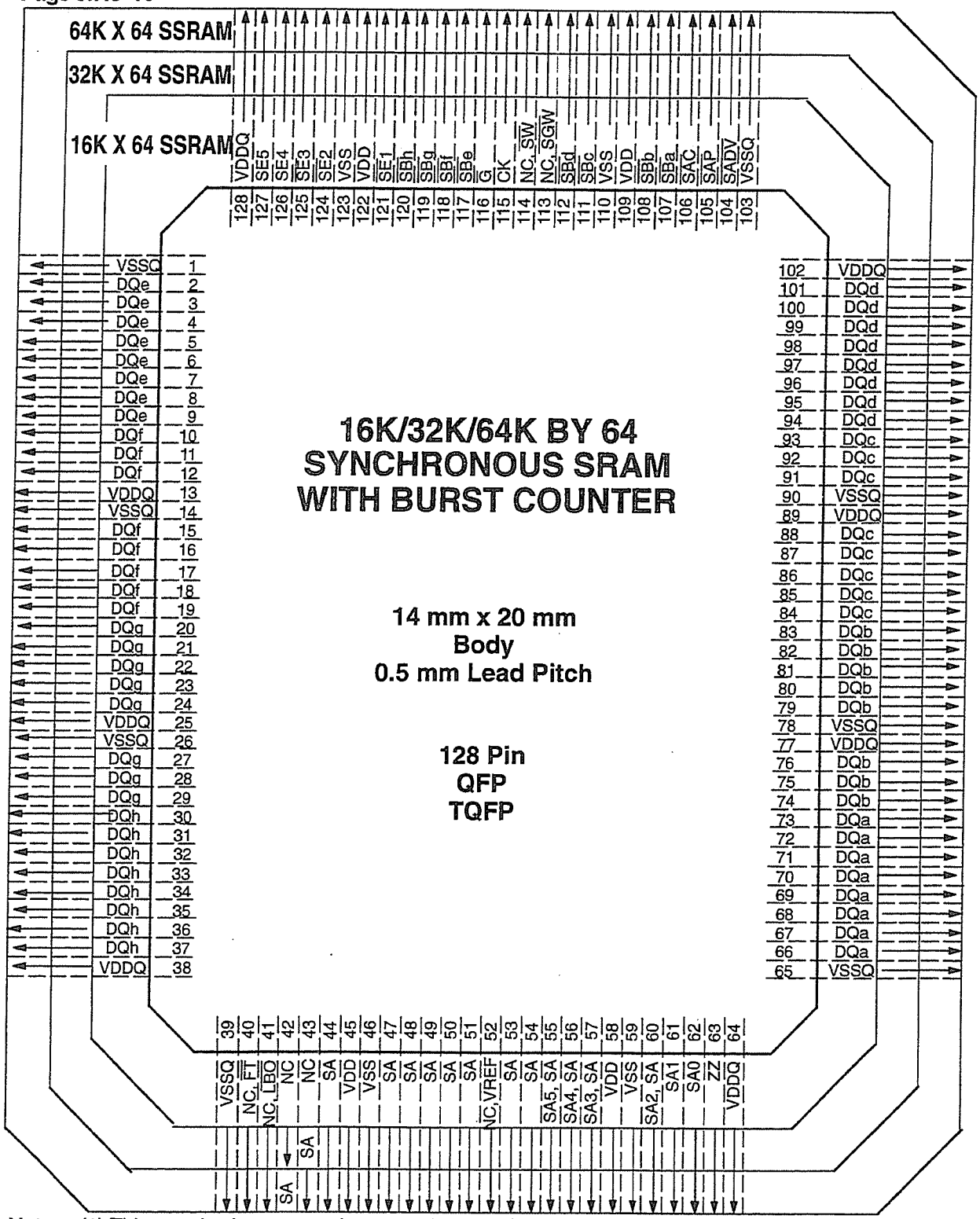


Notes: (1) This standard accommodates synchronous burst address fields ranging from 2 to 6 address b
(2) An 8-word (3 address bits) interleaved burst sequence is currently specified in commercial data sheets

FIGURE 3.7.8–6
16K/32K/64K BY 64 SYNCHRONOUS SRAM WITH BURST COUNTER

Burst SRAM Ball Grid Array (BGA) Package Bump Assignments, Top View											
X72	1	2	3	4	5	6	7	8	9	10	11
A	DQe	DQe	NC, SA#	SA	SA	$\overline{SS}$, $\overline{SE1}$	SA	SA	NC, SA$	DQd	DQd
B	DQe	DQe	NC, SA~	SA	SA	$\overline{G}$	SA	SA	NC, SA◇	DQd	DQd
C	DQe	DQe	NC, SE2	VDD, VDDQ	VDD, VDDQ	ND, $\overline{SGW}$	VDD, VDDQ	VDD, VDDQ	NC, $\overline{SE3}$	DQd	DQd
D	DQe	DQe	VDD, VDDQ	VDD	VSS, VSSQ	$\overline{ADV}$	VSS, VSSQ	VDD	VDD, VDDQ	DQd	DQD
E	DQe, NC	DQf, NC	VDD, VDDQ	VDD	VSS, VSSQ	$\overline{SAC}$	VSS, VSSQ	VDD	VDD, VDDQ	DQc, NC	DQd, NC
F	DQf	DQf	VDD, VDDQ	VDD	VSS, VSSQ	$\overline{SAP}$	VSS, VSSQ	VDD	VDD, VDDQ	DQc	DQc
G	DQf	DQf	VDD, VDDQ	VDD	VSS, VSSQ	VSS, VSSQ	VSS, VSSQ	VDD	VDD, VDDQ	DQc	DQc
H	DQf	DQf	VDD, VDDQ	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	VDD, VDDQ	DQc	DQc
J	DQf	DQf	$\overline{SWe}$, $\overline{SBe}$	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	$\overline{SWd}$, $\overline{SBd}$	DQc	DQc
K	$\overline{SWf}$, $\overline{SBf}$	$\overline{SWg}$, $\overline{SBg}$	NC, VREF	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	NC, VREF	$\overline{SWb}$, $\overline{SBb}$	$\overline{SWc}$, $\overline{SBc}$
L	DQg	DQg	$\overline{SWh}$, $\overline{SBh}$	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	$\overline{SWa}$, $\overline{SBa}$	DQb	DQb
M	DQg	DQg	VDD, VDDQ	VSS, VSSQ	VSS	VSS	VSS	VSS, VSSQ	VDD, VDDQ	DQb	DQb
N	DQg	DQg	VDD, VDDQ	VDD	VSS, VSSQ	VSS, VSSQ	VSS, VSSQ	VDD	VDD, VDDQ	DQb	DQb
P	DQg	DQg	VDD, VDDQ	VDD	VSS, VSSQ	NC, $\overline{CK}$, $\overline{K}$	VSS, VSSQ	VDD	VDD, VDDQ	DQb	DQb
R	DQg, NC	DQh, NC	VDD, VDDQ	VDD	VSS, VSSQ	CK, K	VSS, VSSQ	VDD	VDD, VDDQ	DQa, NC	DQb, NC
T	DQh	DQh	VDD, VDDQ	VDD	VSS, VSSQ	NC, $\overline{SW}$	VSS. VSSQ	VDD	VDD, VDDQ	DQa	DQa
U	DQh	DQh	$\overline{LBO}$, NC	VDD, VDDQ	VDD, VDDQ	SA1	VSS, VSSQ	VDD, VDDQ	NC, $\overline{FT}$	DQa	DQa
V	DQh	DQh	NC	SA	SA	SA0	SA	SA	NC	DQa	DQa
W	DQh	DQh	NC, ZQ	NC, TMS	NC, TDI	NC, TCK	NC, TDO	NC, TRST	NC, ZZ	DQa	DQa

Address Assignment and Package Dimension Table		
Density	**Address Assignment**	**Nominal Exterior Package Dimension**
1M (16K X 64, 72)	Basic SA	21 mm X 25 mm
2M (32K X 64, 74)	~	21 mm X 25 mm
4M (64K X 64, 72)	~, *	21 mm X 25 mm
8M (128K X 64, 72)	~, *, ◇	TBD
16 M (256K X 64, 72)	~, *. ◇, #	TBD

FIGURE 3.7.8–7
16K TO 256K BY 64 & 72 BURST SRAM IN BGA

Release Release 7

3.8 Pseudostatic Random Access Memory (PSRAM)

3.8.1 PSRAM, Byte Wide

3.8.1.1 2K TO 8K BY 8 PSRAM FAMILY IN DIP
CAPACITY–2K, 4K, 8K WORDS OF 8 BITS
PACKAGE–28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT–Fig. 3.8-1

3.8.1.2 2K TO 16K BY 8 PSRAM FAMILY IN RCC
CAPACITY–2K, 4K, 8K, 16K WORDS OF 8 BITS
PACKAGE–32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT–Fig. 3.8-2

3.8.1.3 32K TO 512K BY 8 PSRAM FAMILY IN SOJ
CAPACITY–32K, 128K, 256K, 512K WORDS OF 8 BITS
PACKAGE–28 OR 32 PIN SOJ, 0.4" WIDE OR NOT DEFINED
PIN ASSIGNMENT–Fig. 3.8-3

3.8.2 PSRAM, WORD WIDE

3.8.2.1 4K TO 32K BY 16 PSRAM IN DIP
CAPACITY–4K TO 32K WORDS OF 16 BITS,
PACKAGE–40 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS–Fig. 3.8-4

3.8.2.2 4K TO 256K BY 16 PSRAM IN SCC
CAPACITY–4K TO 256K WORDS OF 16 BITS,
PACKAGE–44 PAD (PIN) RCC, 0.650" X 0.650"
PIN ASSIGNMENTS–Fig. 3.8-5

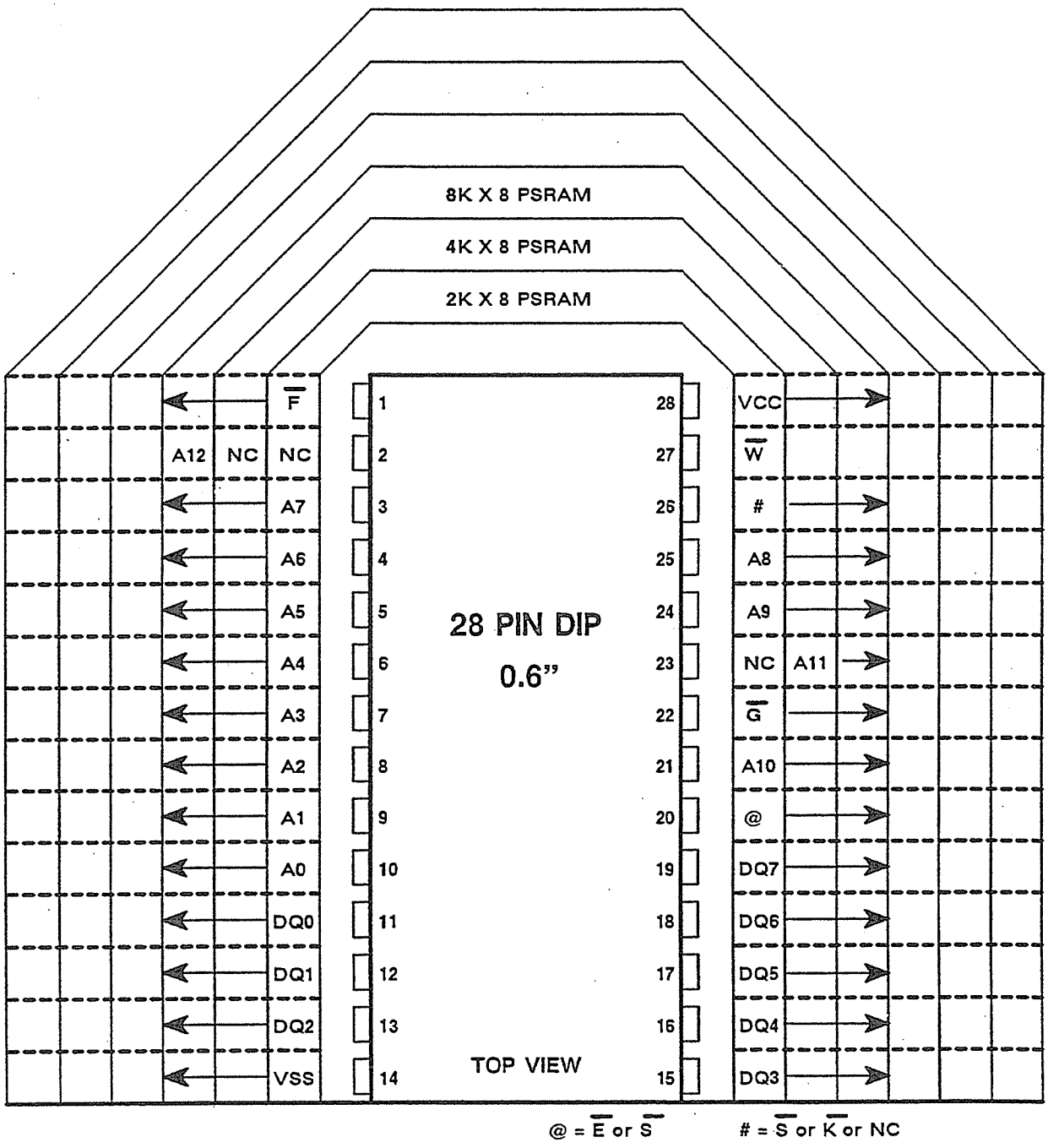


FIGURE 3.8-1
2K TO 8K BY 8 PSRAM FAMILY IN DIP

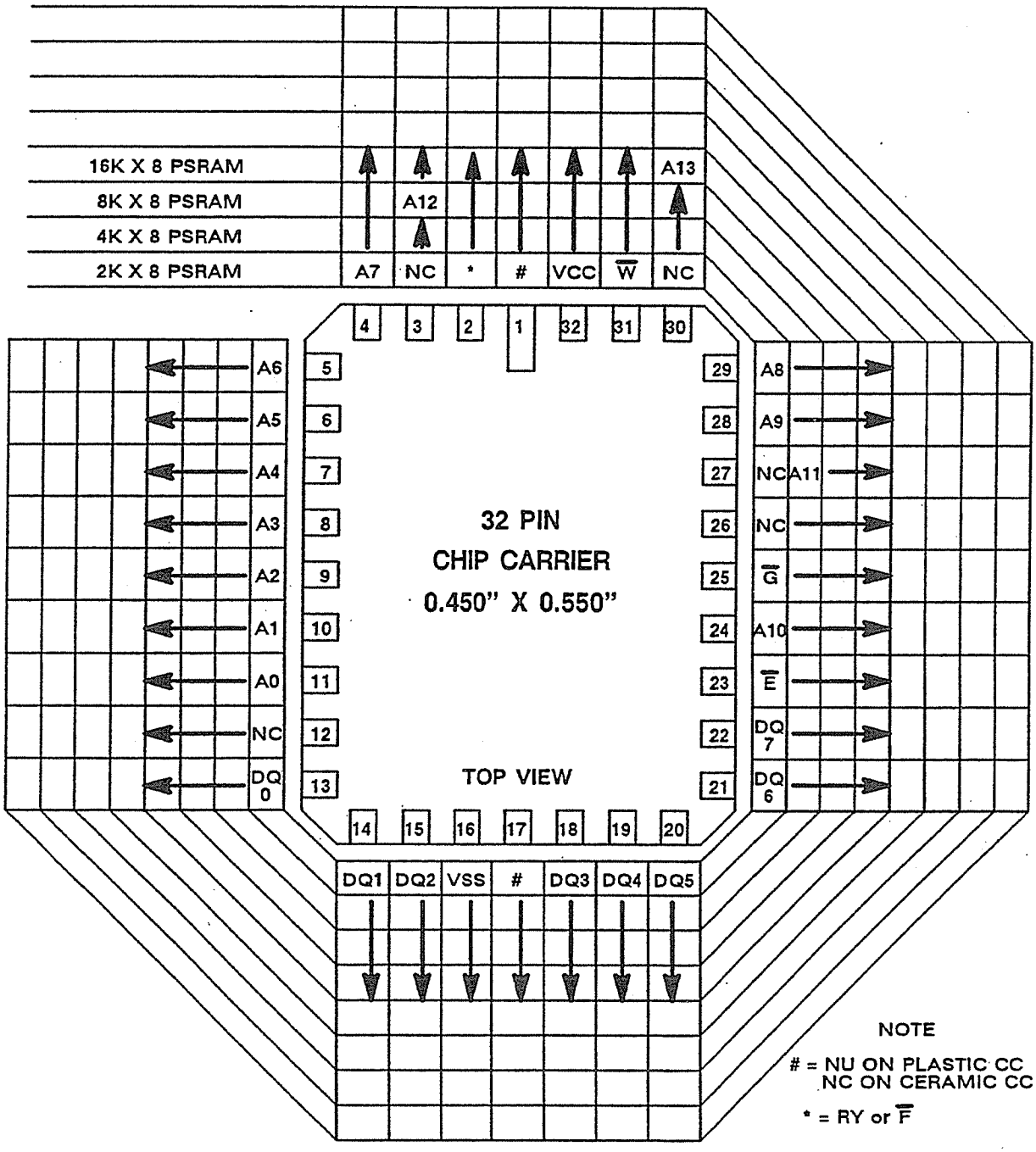


FIGURE 3.8-2
2K TO 16K BY 8 PSRAM FAMILY IN RCC

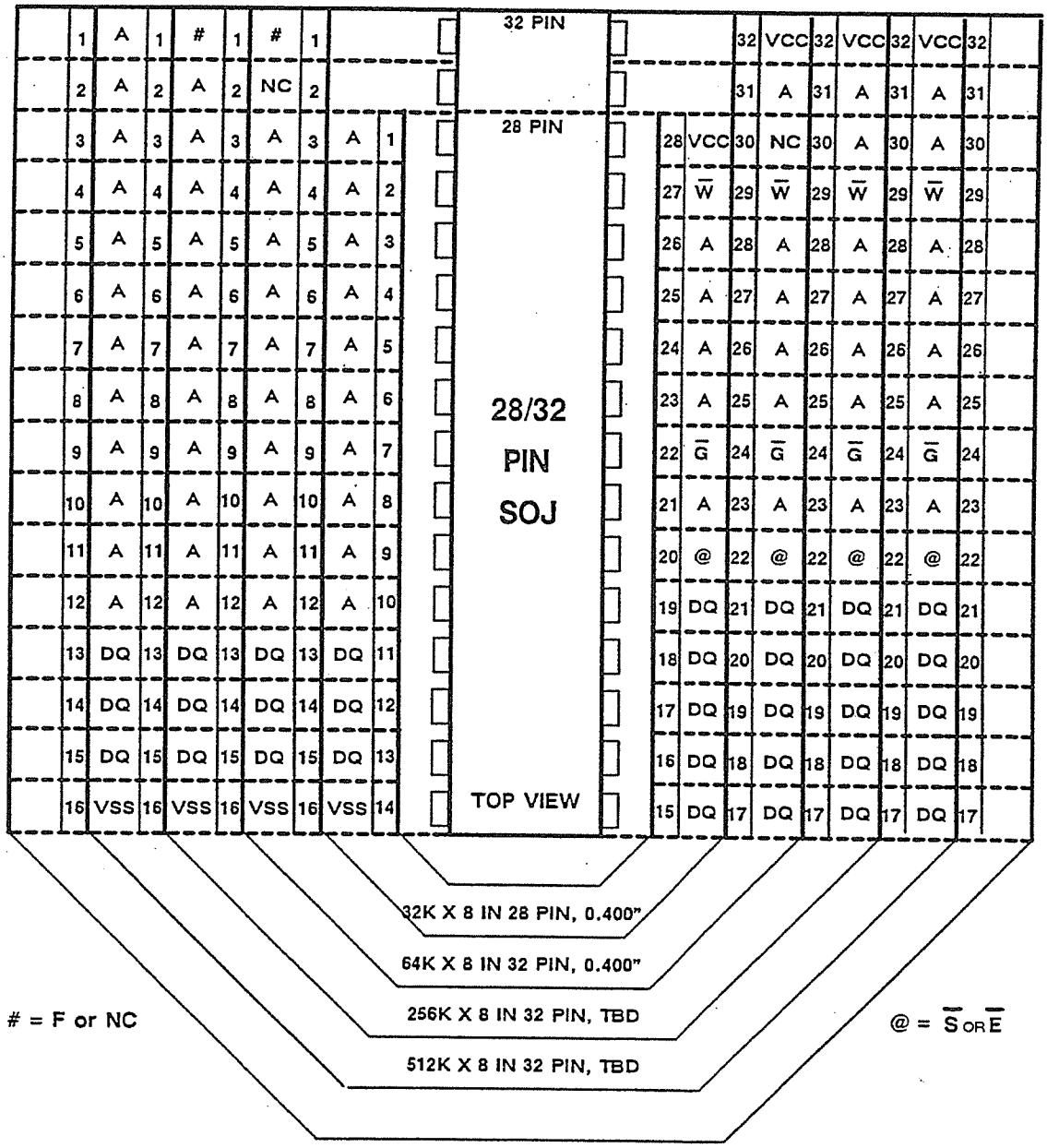


FIGURE 3.8-3
32K TO 512K BY 8 PSRAM FAMILY IN SOJ

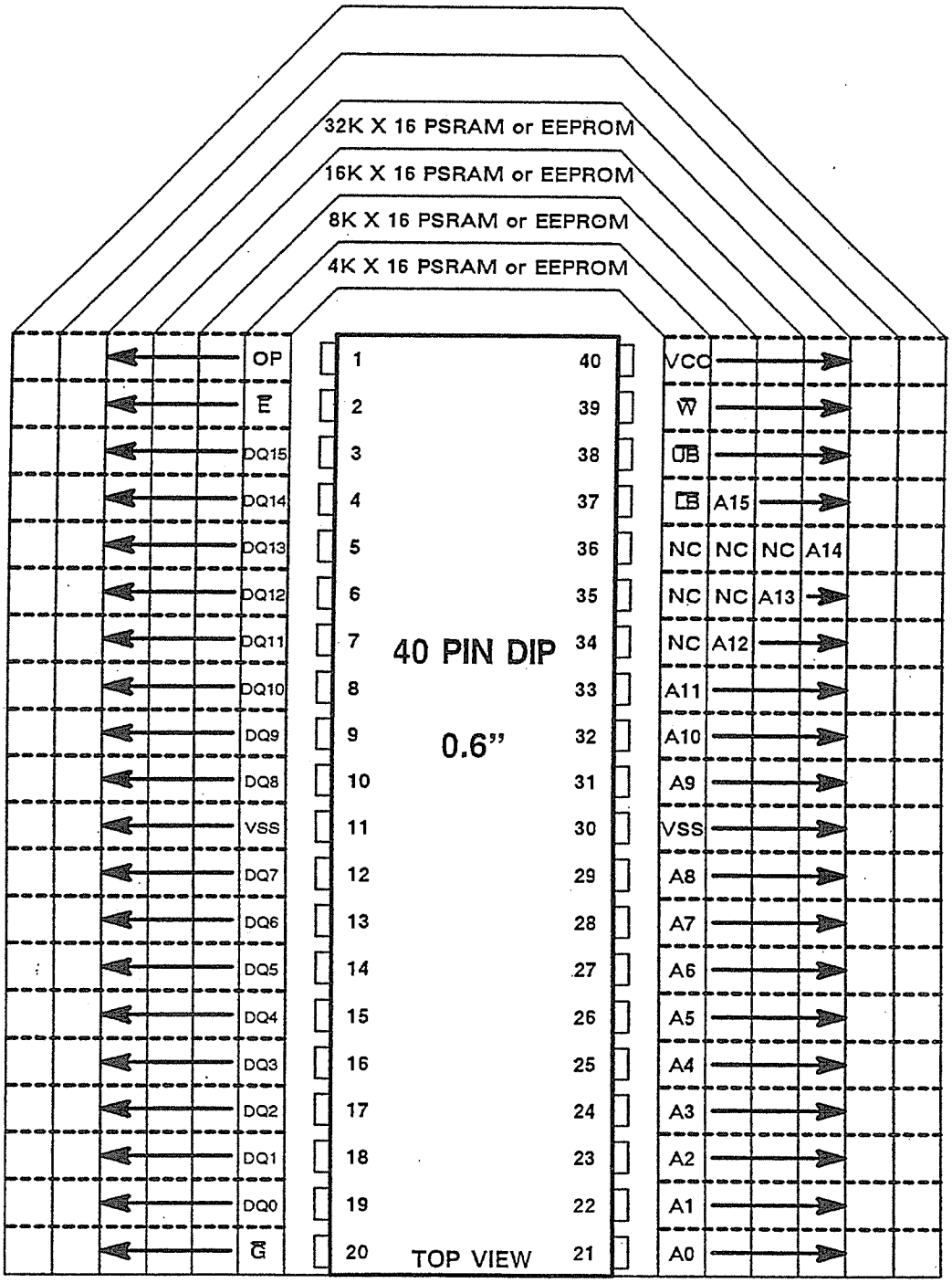


FIGURE 3.8-4
4K TO 32K BY 16 PSRAM FAMILY IN DIP

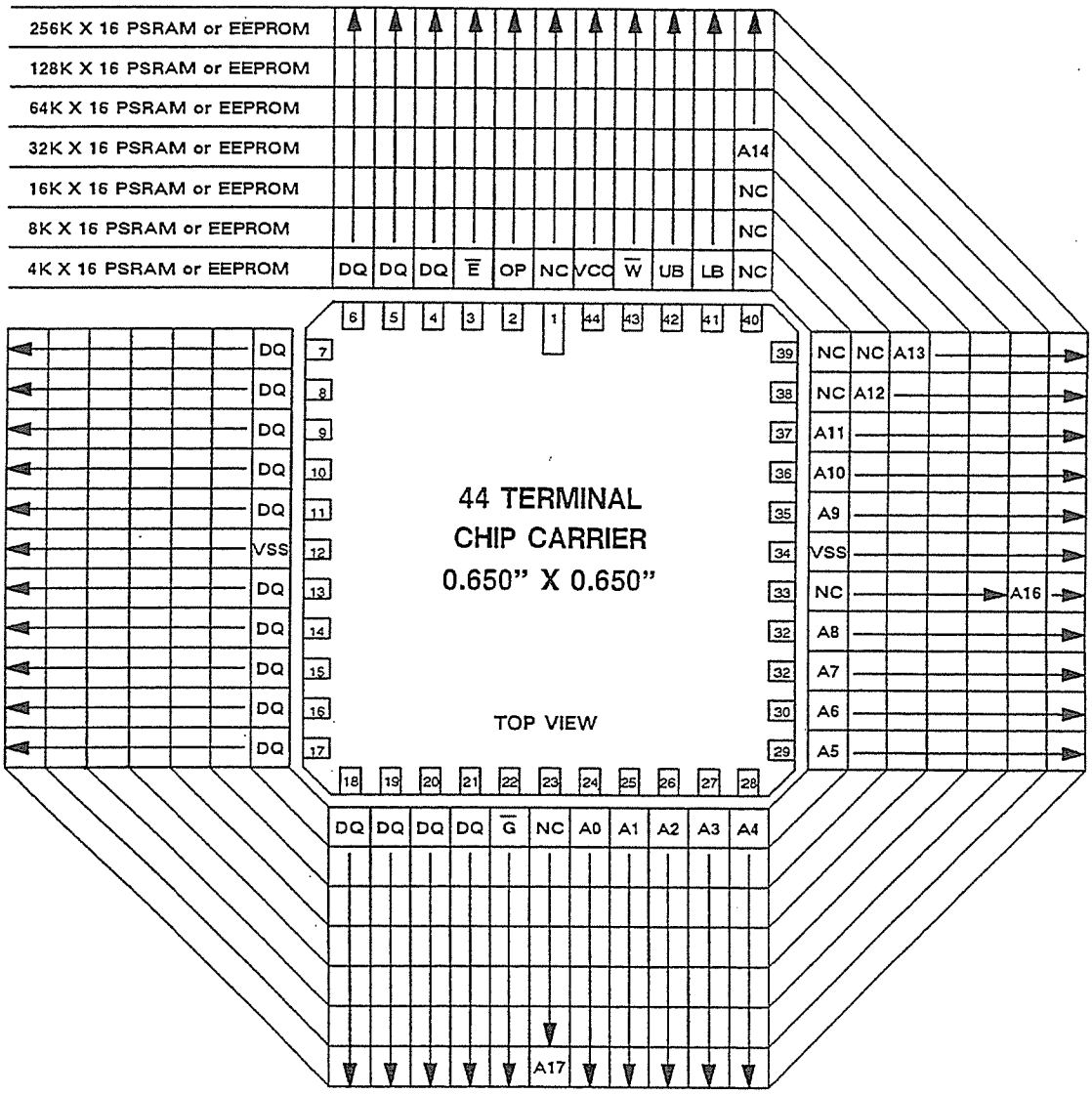


FIGURE 3.8-5
4K TO 256K BY 16 PSRAM FAMILY IN SCC

3.9 Dynamic Random Access Memory (DRAM)

The following DRAM standards were developed by JC-42.3 Committee and have been implemented using MOS technology.

3.9.1 Bit Wide DRAM

3.9.1.1 – 16K BY 1 DRAM IN DIP WITH 3 SUPPLY VOLTAGES

CAPACITY—16K WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—16 PIN DIP, 0.3" wide
POWER VOLTAGES—VDD=+12 V, VCC=+5 V, VBB=–5 V
PIN ASSIGNMENT—Fig. 3.9.1–1

3.9.1.2 – 16K TO 256K BY 1 DRAM FAMILY IN DIP

CAPACITY—16K, 64K, 256K WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—16 PIN DIP, 0.3" wide
PIN ASSIGNMENT—Fig. 3.9.1–1

3.9.1.3 – 16K TO 256K BY 1 DRAM IN RCC

CAPACITY—16K, 64K, 256K WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—18 PAD (PIN) RCC, 0.290" by 0.425" (16K & 64K)
—18 PAD (PIN) RCC, 0.290" by 0.490" (256K)
PIN ASSIGNMENT—Fig. 3.9.1–2

3.9.1.4 – 64K & 256K BY 1 DRAM IN ZIP

CAPACITY—64K, 256K WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—16 PIN ZIP
PIN ASSIGNMENT—Fig. 3.9.1–3

3.9.1.5 – 1M AND 4M BY 1 DRAM FAMILY IN DIP

CAPACITY—1M, & 4M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—18 PIN DIP, Width: 0.3" for 1M, 0.35" for 4M,
PIN ASSIGNMENT—Fig. 3.9.1–4

3.9.1.6 – 1M TO 16M BY 1 DRAM FAMILY IN SOJ OR TSOP2

CAPACITY—1M, 4M, & 16M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—26/20 PIN SOJ: 0.3" by 0.675" for 1M,
— : 0.3" or 0.35" by .675" for 4M
—26/20 PIN TSOP2: 0.3" by 0.675" and 0.050" PIN PITCH for 4M
—26/20 PIN SOJ OR TSOP–2: 0.3" FOR 16M
—28/24 PIN SOJ OR TSOP–2: 0.4" BY 0.725" for 16M
SUPPLY VOLTAGE—The 16M part with an 8K refresh is approved for use with the LVTTL power and interface standard developed by Committee JC–16.
PIN ASSIGNMENT—Fig. 3.9.1–5

3.9.1.7 – 1M TO 16M BY 1 DRAM FAMILY IN ZIP

CAPACITY—1M, 4M, 16M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—20 PIN ZIP, 0.400" WIDE FOR THE 1M & 4M PARTS
PACKAGE—28 PIN ZIP, 0.475" WIDE FOR THE 16M PART
SUPPLY VOLTAGE—The 16M part with an 8K refresh is approved for use with the LVTTL power and interface standard developed by Committee JC–16.
PIN ASSIGNMENT—Fig. 3.9.1–6

3.9.1.8 – 1M TO 16M BY 1 NON–MUX DRAM FAMILY IN SOJ

CAPACITY—1M, 4M, & 16M WORDS OF 1 BIT
LOGIC FEATURES—Non–Multiplexed Address
PACKAGE—28, 32, OR 34 PIN DIP
PIN ASSIGNMENT—Fig. 3.9.1–7

3.9.1.9 – 1M BY 1 DRAM IN TSOP1

CAPACITY—1M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—24/20 PIN TSOP1
PIN ASSIGNMENT—Fig. 3.9.1–8

3.9.1.10 – 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ

CAPACITY—16M WORDS OF 1 BIT or 4M WORDS OF 4 BITS
LOGIC FEATURES—Configurable as a X1 or a X4 part
—The data access mode can be chosen by logic control
PACKAGE—28 PIN SOJ
PIN ASSIGNMENT—Fig. 3.9.1–9

3.9.1.11 – 64M BY 1 DRAM IN SOJ OR TSOP2

CAPACITY—64M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Addresses
This part is available in two package sizes as defined below. The pin rotations of the two are essentially the same with the exception of two NC pins.
PACKAGE—34 PIN SOJ, 0.500" Wide
—34 PIN TSOP2, 0.500" WIDE, 0.050" PP
PIN ASSIGNMENT—Fig. 3.9.1–10
PACKAGE—32 PIN SOJ, 0.400" Wide
—32 PIN TSOP2, 0.400" WIDE, 0.050" PP
PIN ASSIGNMENT—Fig. 3.9.1–12

3.9.1.12 – 2 X 16M BY 1 DRAM IN TSOP2

CAPACITY—32M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Addresses and Two arrays of 16M x1 with common data pins and separate $\overline{RE}$ & $\overline{CE}$ inputs.
PACKAGE—28/24 PIN TSOP2, 0.400" WIDE, 0.050" PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.1–11

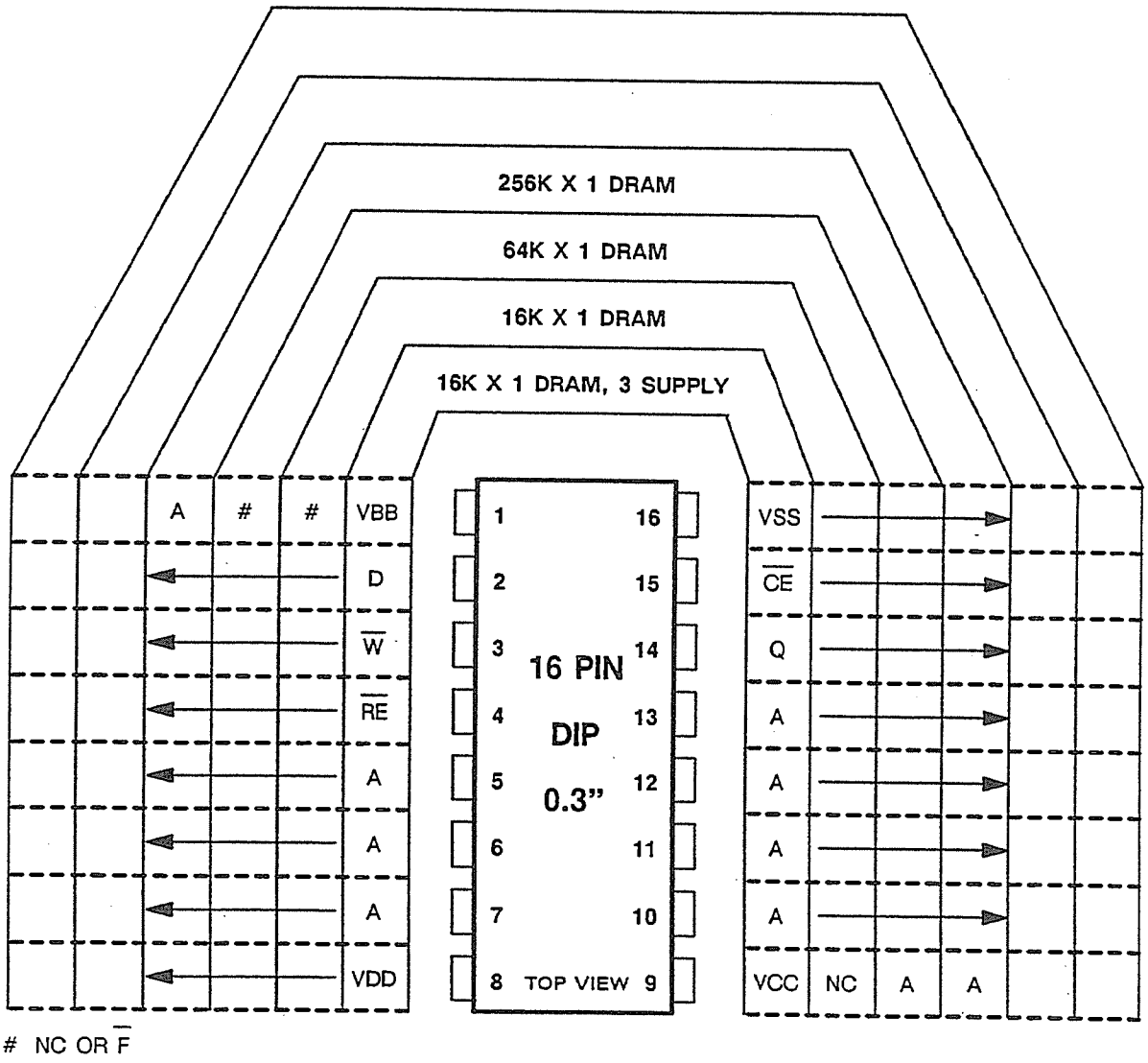


FIGURE 3.9.1-1
16K BY 1 DRAM IN DIP WITH 3 SUPPLY VOLTAGES
16K TO 256K BY 1 DRAM FAMILY IN DIP

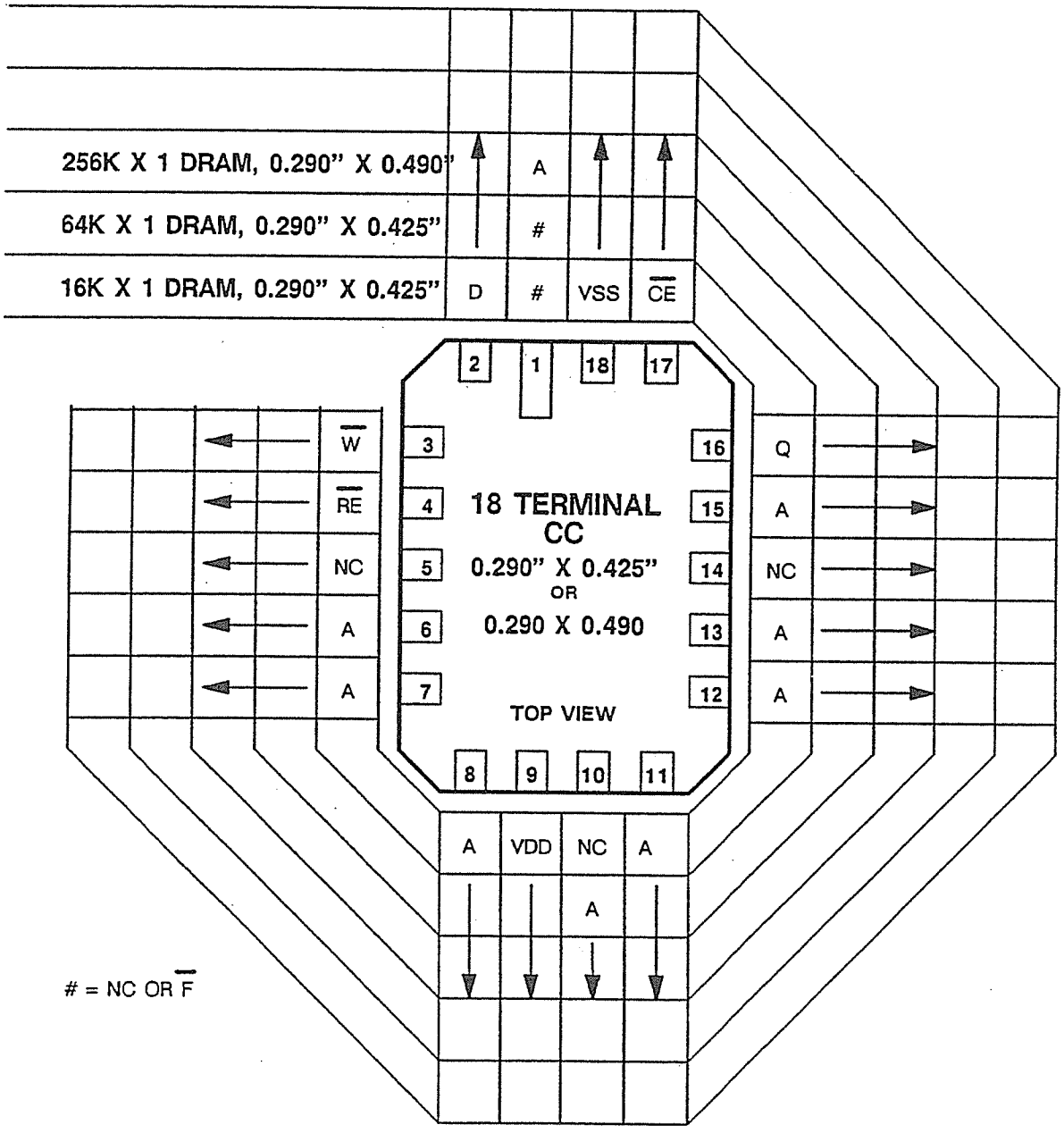


FIGURE 3.9.1-2
16K TO 256K BY 1 DRAM IN RCC

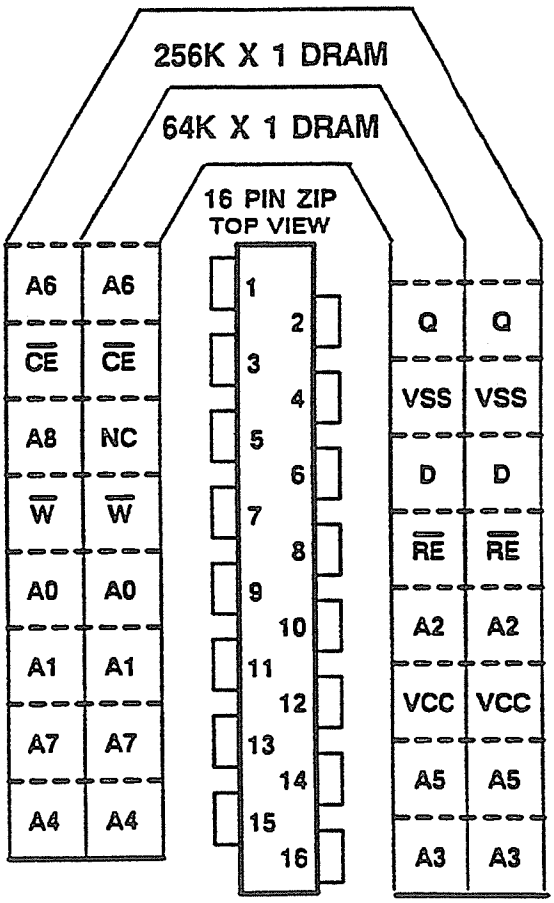
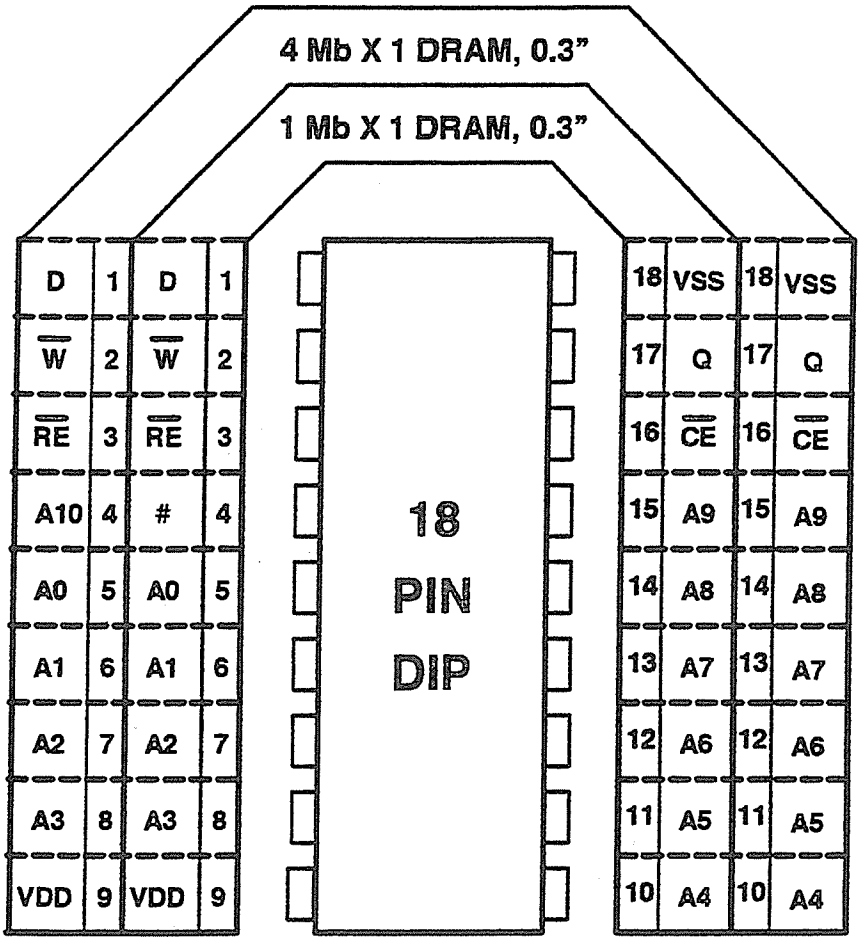


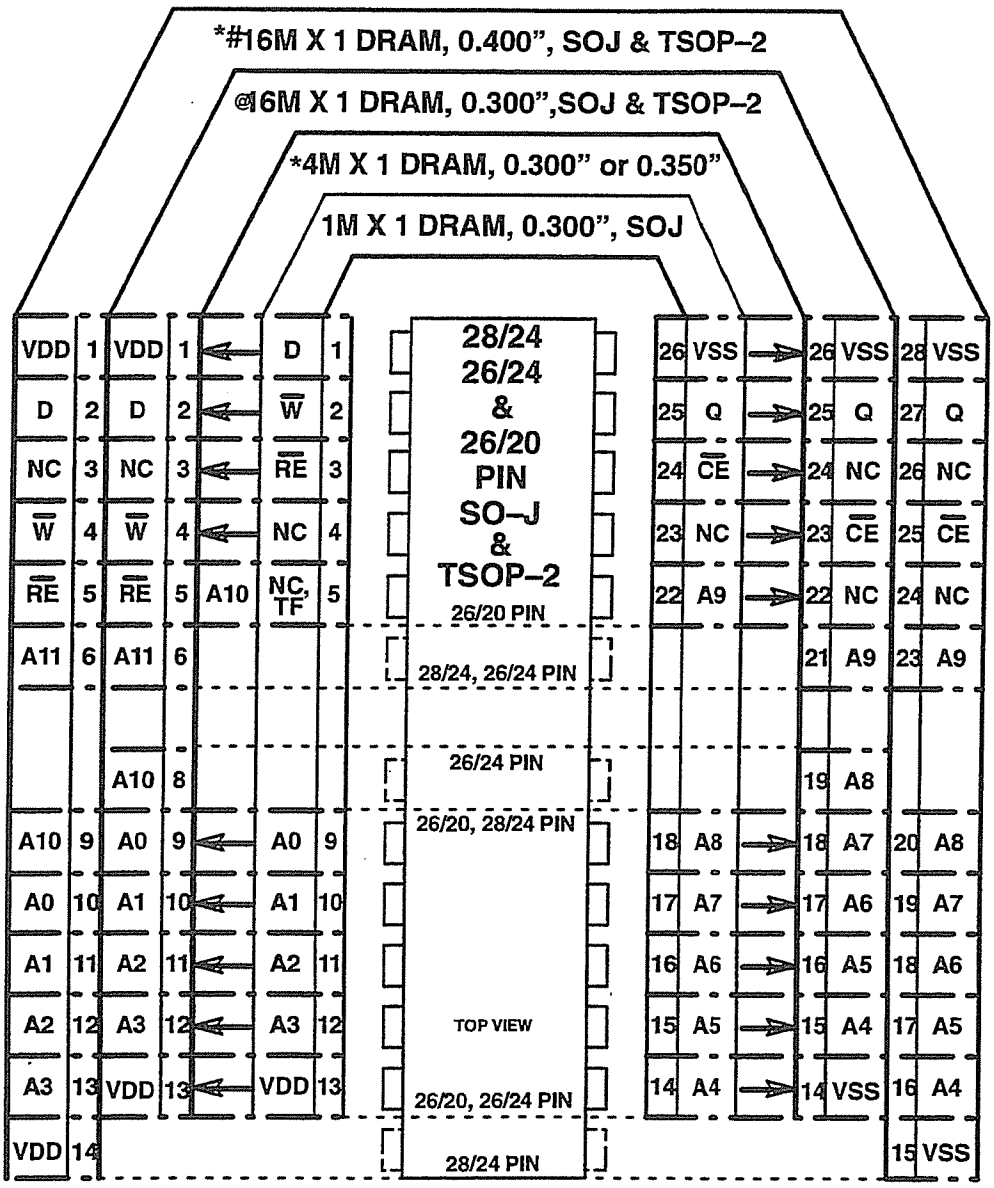
FIGURE 3.9.1-3
64K & 256K BY 1 DRAM IN ZIP



= NC or TF

FIGURE 3.9.1–4

1M & 4M BY 1 ADDRESS MULTIPLEXED DRAM IN DIP



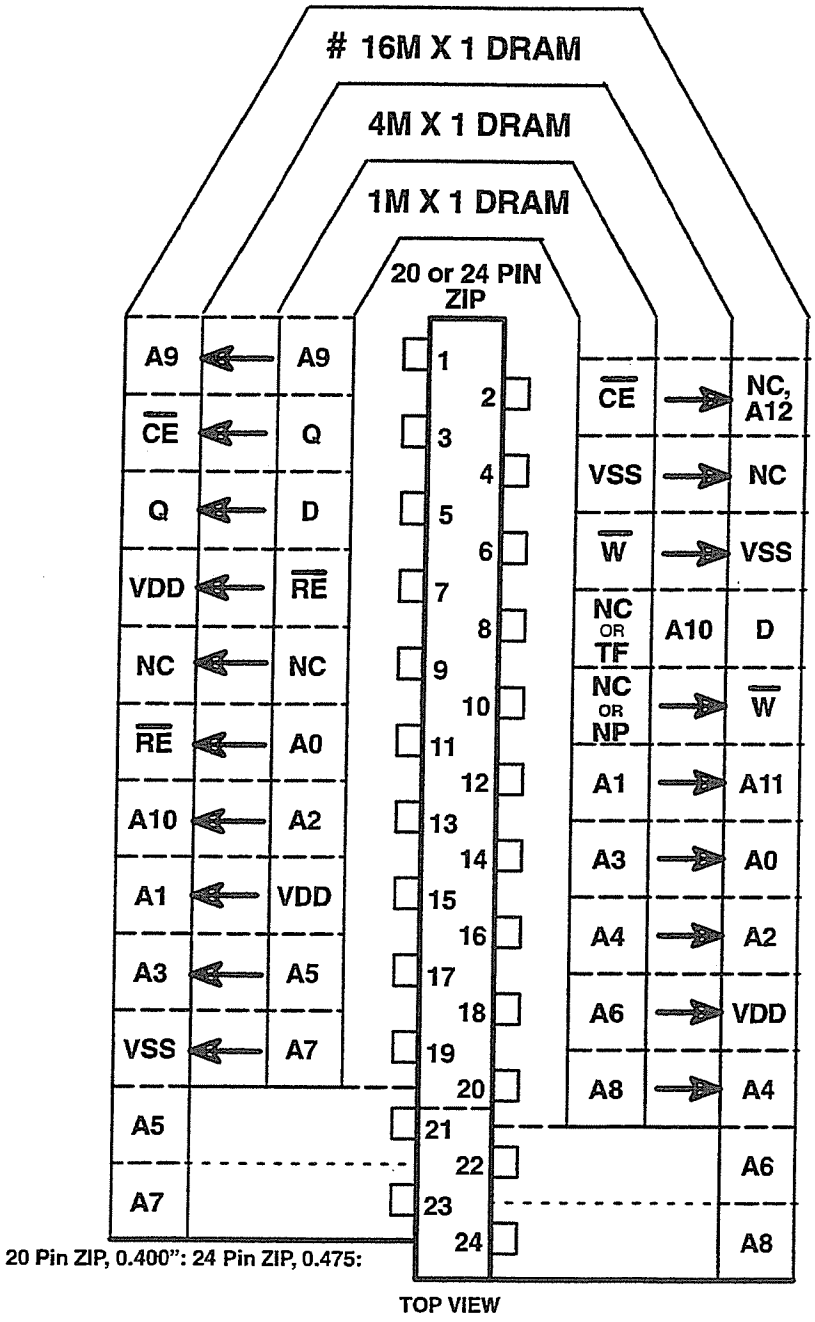
REFRESH, ROW, & COLUMN, ADDRESS CONFIGURATION

DEVICE CONFIGURATION	1M X 1	4M X 1	16M X 1	16M X 1	16M X 1, 3.3V
REFRESH COUNT	512	1K	2K	4K	8K
REFRESH ADDRESSES	A0 to A8	A0 to A9	A0 to A10	A0 to A11	A0 to A12
ROW ADDRESSES	A0 to A9	A0 to A10	A0 to A11	A0 to A11	A0 to A12
COLUMN ADDRESS	A0 to A9	AO to A10	A0 to A11	A0 to A11	A0 to A10

* NOTE – The 4M x 1 part is approved for use in 0.300" TSOP–2 and the 16M x 1 part in 0.400" TSOP–2 (PDSO–G) packages.
# NOTE – The 16M x 1 part with an 8K Refresh is approved for use with a 3.3V VCC.
@ NOTE – The 16M X 1 part in a 26/24 pin package is approved in both SOJ and TSOP–2 (PDSO–G) packages with 4K refresh.

FIGURE 3.9.1–5

1M TO 16M BY 1 DRAM FAMILY IN SOJ and TSOP–2



REFRESH, ROW, & COLUMN, ADDRESS CONFIGURATION

DEVICE CONFIGURATION	1M X 1	4M X 1	16M X 1	16M X 1	16M X 1, 3.3V
REFRESH COUNT	512 Refresh	1K Refresh	2K Refresh	4K Refresh	8K Refresh
REFRESH ADDRESSES	A0 to A8	A0 to A9	A0 to A10	A0 to A11	A0 to A12
ROW ADDRESSES	A0 to A9	A0 to A10	A0 to A11	A0 to A11	A0 to A12
COLUMN ADDRESS	A0 to A9	AO to A10	A0 to A11	A0 to A11	A0 to A10

NOTE – The 16M x 1 part with an 8K Refresh is approved for use with a 3.3V VDD.

FIGURE 3.9.1–6
1M TO 16M BY 1 DRAM FAMILY IN ZIP

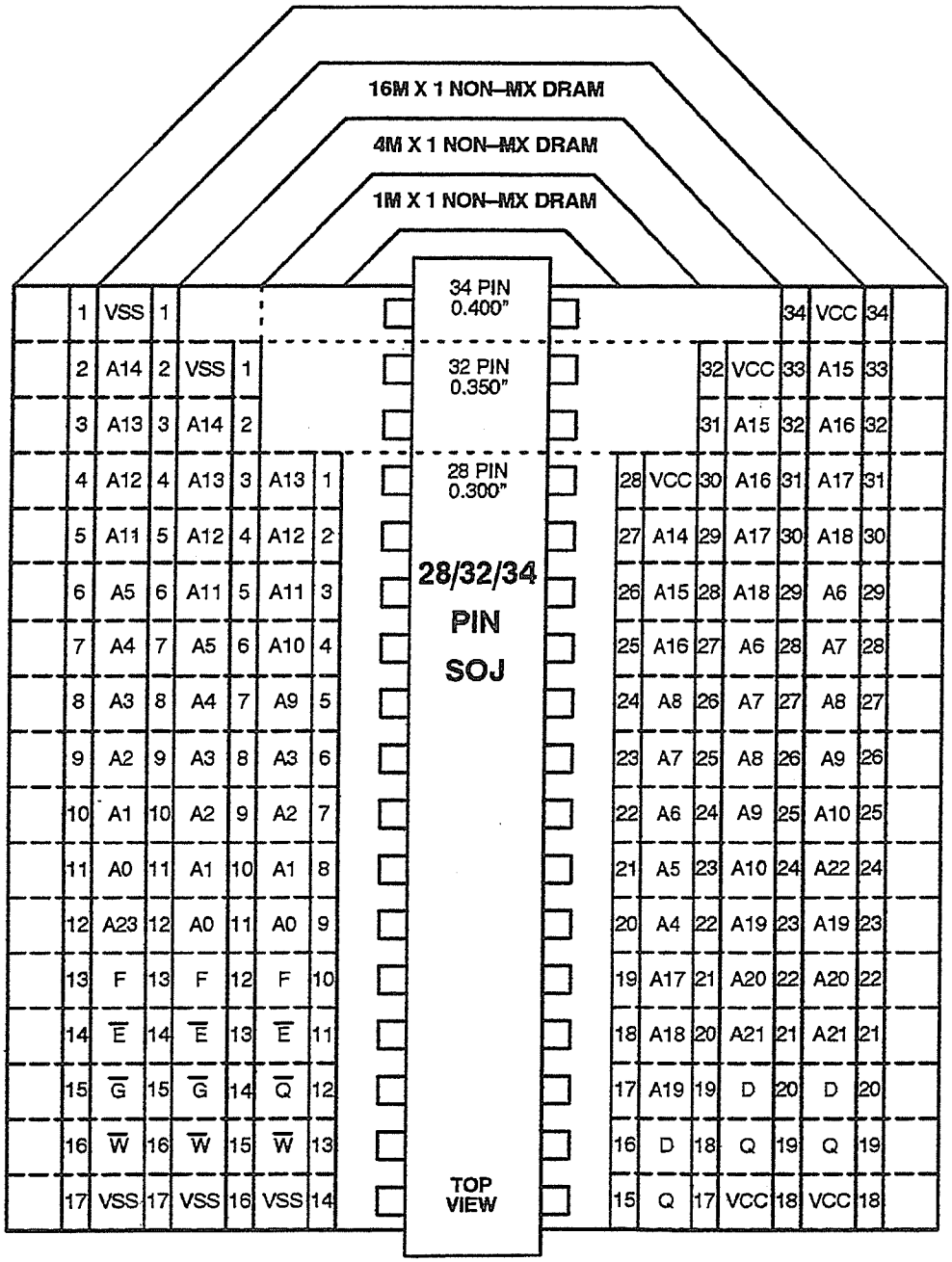
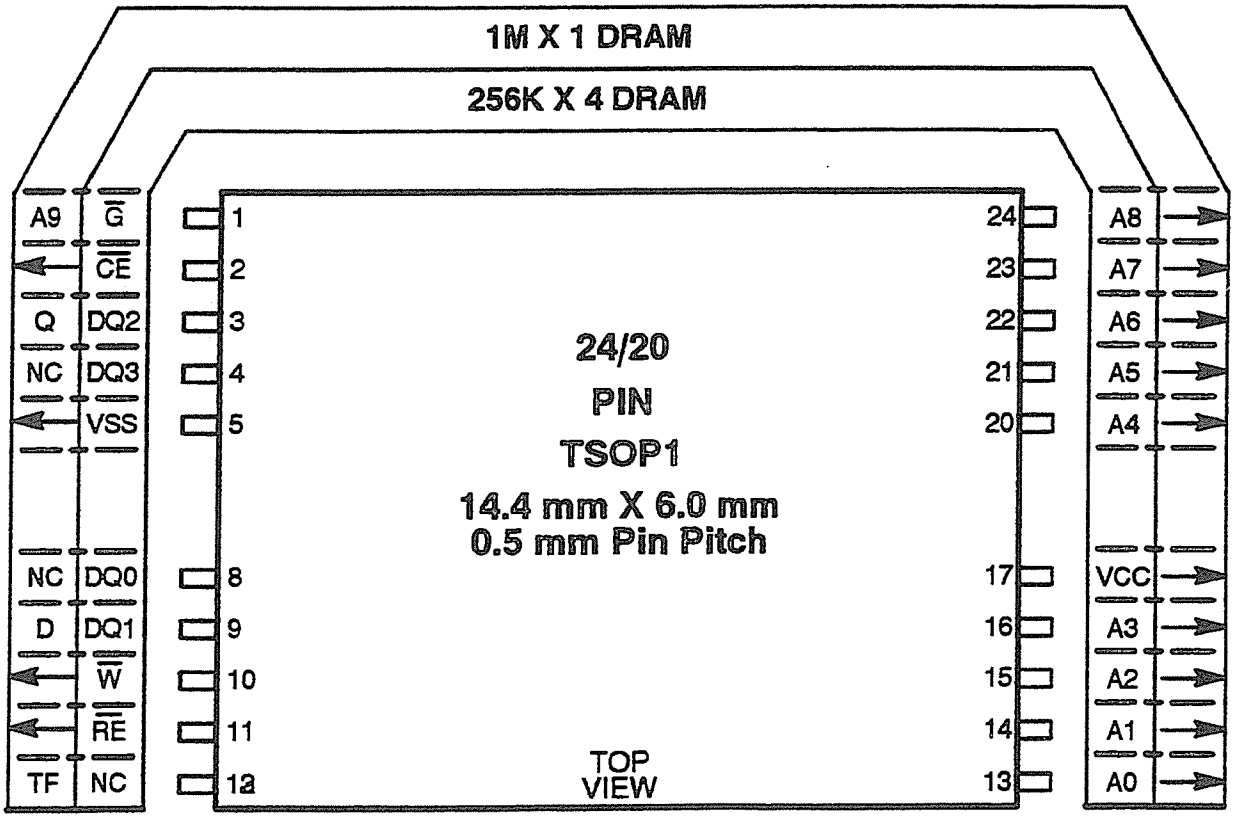


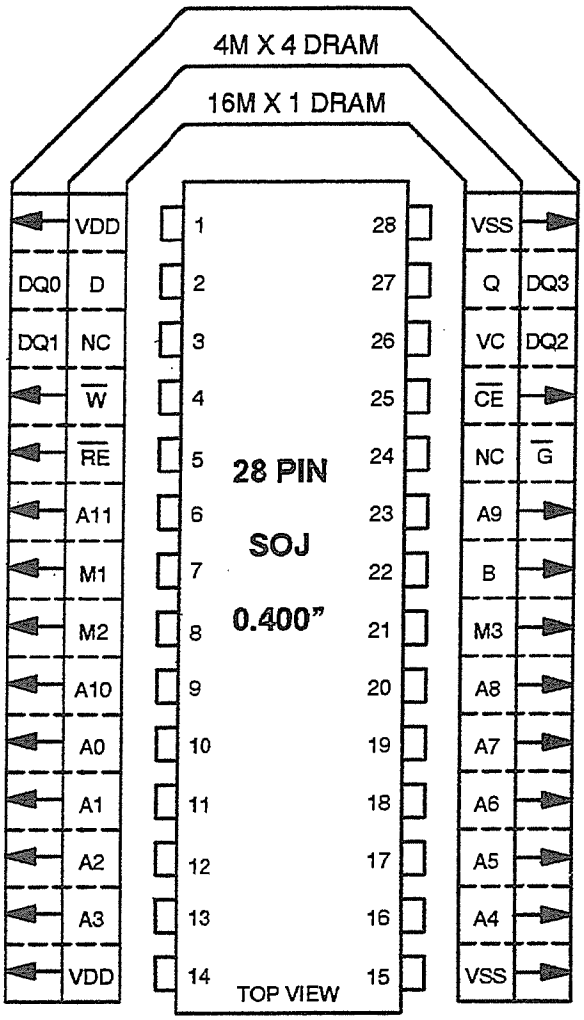
FIGURE 3.9.1–7
1M TO 16M BY 1 NON–MULTIPLEXED DRAM IN SOJ



REFRESH ADDRESS FIELD = A0 to A8

The JEDEC Std. No. 30 designator for the TSOP1 package is PDSO–G.

FIGURE 3.9.1–8
1M BY 4 AND 4M BY 1 DRAM IN TSOP1

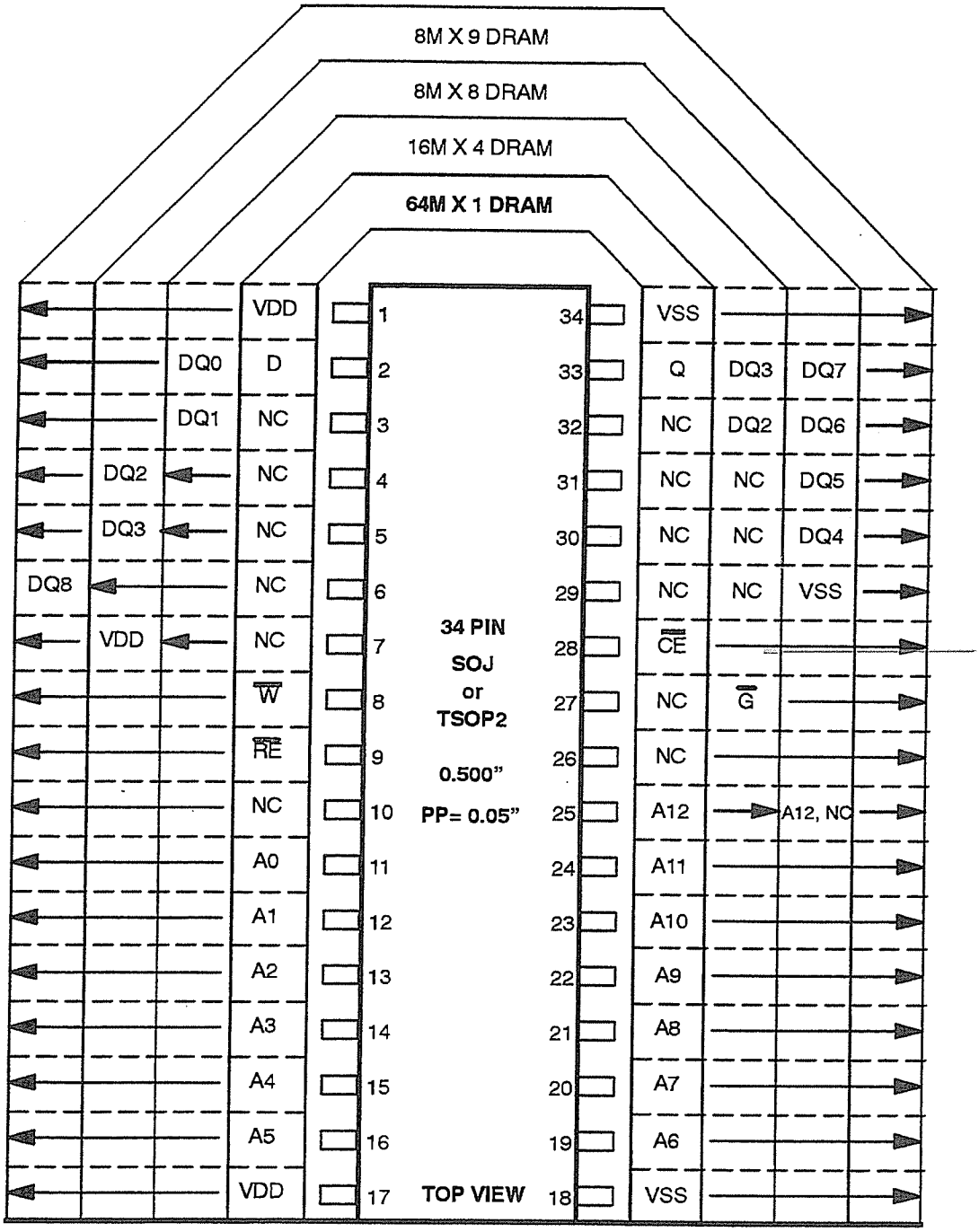


B TRUTH TABLE
DATA INTERFACE CONTROL
B=HI, DATA X1
B=LO, DATA X4

The default state for M1, M2, M3, and B ahould be HI when no external connection is made.

M1/M2/M3 TRUTH TABLE		M1	M2	M3
MANDATORY MODE	FAST PAGE	HI	HI	HI
OPTIONAL MODES	NIBBLE	LO	HI	HI
	BYTE	LO	LO	HI
	BURST	LO	HI	LO
	STATIC COLUMN	HI	LO	HI
	VENDOR SPECIFIC	LO	LO	LO
	VENDOR SPECIFIC	HI	HI	LO
	VENDOR SPECIFIC	HI	LO	LO

FIGURE 3.9.1–9
16M X 1/4M X 4 CONFIGURABLE DRAM IN SOJ



ROW, COLUMN, & REFRESH ADDRESS CONFIGURATIONS

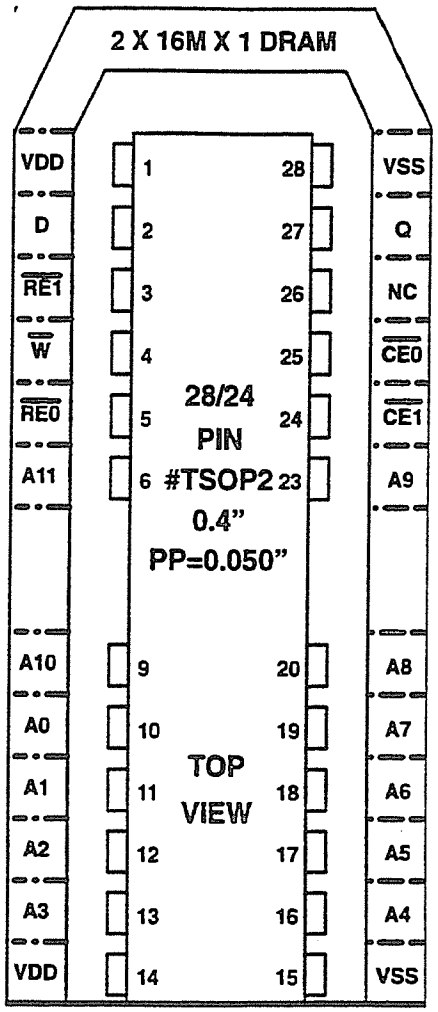
DEVICE CONFIGURATION REFRESH COUNT	64M X 1	16M X 4	8M X 8(9) 4K Refresh	8M X 8(9) 8K Refresh
ROW/REFRESH ADDRESSES COLUMN ADDRESSES	A0 Through A12 A0 Through A12	A0 Through A12 A0 Through A10	A0 Through A11 A0 Through A10	A0 Through A12 A0 Through A9

This standard recognizes that some early deliveries of these parts may have to be in a 0.6" wide package

FIGURE 3.9.1-10

64M BY 1 DRAM IN SOJ & TSOP2

Release 4 a

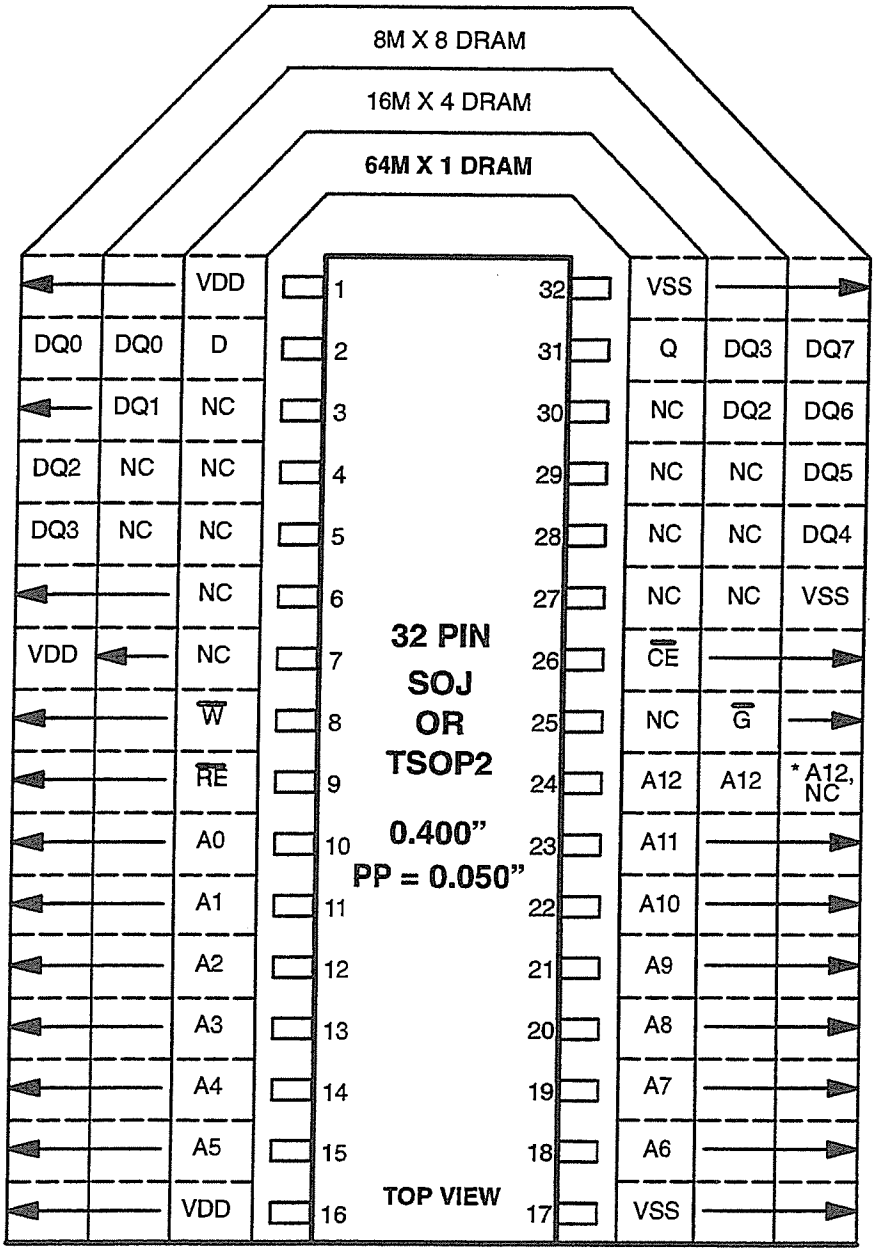


The JEDEC approved term for this package is PDSO–G

ROW, REFRESH, & COLUMN ADDRESS CONFIGURATION

DEVICE CONFIGURATION	2 X 16M X 1	2 X 16M X 1
REFRESH COUNT	2048 Refresh	4096 Refresh
ROW ADDRESS	A0 → A11	A0 → A11
REFRESH ADDRESS	A0 → A10	A0 → A11
COLUMN ADDRESS	A0 → A11	A0 → A11

FIGURE 3.9.1–11
2 X 16M BY 1 DRAM IN TSOP2



* Pin 24 is NC for the 16M X 4 & 8K X 8 parts with a 4K Refresh.

ROW & COLUMN, ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION	64M X 1	16M X 4 4K Rows	16M X 4 8K Rows	8M X 8 4K Rows	8M X 8 8K Rows
ROW COUNT					
ROW ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12
COLUMN ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A10	A0 ⇒ A10	A0 ⇒ A9

FIGURE 3.9.1–12
64M BY 1 DRAM IN SOJ & TSOP2

3.9.2 Nibble Wide DRAM

3.9.2.9 – 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ

CAPACITY—16M WORDS OF 1 BIT or 4M WORDS OF 4 BITS
LOGIC FEATURES—Configurable as a X1 or a X4 part
—The data access mode can be chosen by logic control
PACKAGE—28 PIN SOJ
PIN ASSIGNMENT—Fig. 3.9.2–8

3.9.2.10 – 256K TO 4M BY 4 NON–MUX DRAM FAMILY IN SOJ

CAPACITY—256K, 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—Non–Multiplexed Address
PACKAGE—28, 32, OR 34 PIN SOJ, WIDTH Not yet defined
PIN ASSIGNMENT—Fig. 3.9.2–9

3.9.2.11 – 4M BY 4 DRAM WITH 1 $\overline{CE}$ AND 4 $\overline{CE}$ IN TSOP2

CAPACITY—4M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
—There are two versions of this part, one with 1 $\overline{CE}$ and one with 4 $\overline{CE}$ controlling each of the data bits
PACKAGE—28/24 PIN TSOP2, 0.4" WIDE FOR THE 1 $\overline{CE}$ PART
— 28 PIN TSOP2, 0.4" WIDE FOR THE 4 $\overline{CE}$ PART
PIN ASSIGNMENT—Fig. 3.9.2–10

3.9.2.12 – 16M BY 4 DRAM IN SOJ & TSOP2

CAPACITY—16M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
This part is available in two package sizes as defined below. The pin rotations of the two are essentially the same with the exception of two NC pins.
PACKAGE—34 PIN SOJ, WIDTH: 0.5"
—34PIN TSOP2, WIDTH: 0.5", PIN PITCH: 0.050"
PIN ASSIGNMENT—Fig. 3.9.2–11
PACKAGE—32 PIN SOJ, 0.400" Wide
—32 PIN TSOP2, 0.400" WIDE, 0.050" PP
PIN ASSIGNMENT—Fig. 3.9.1–12

3.9.2.13 – 1M, 2M, & 4M BY 2 DRAM IN SOJ & TSOP2

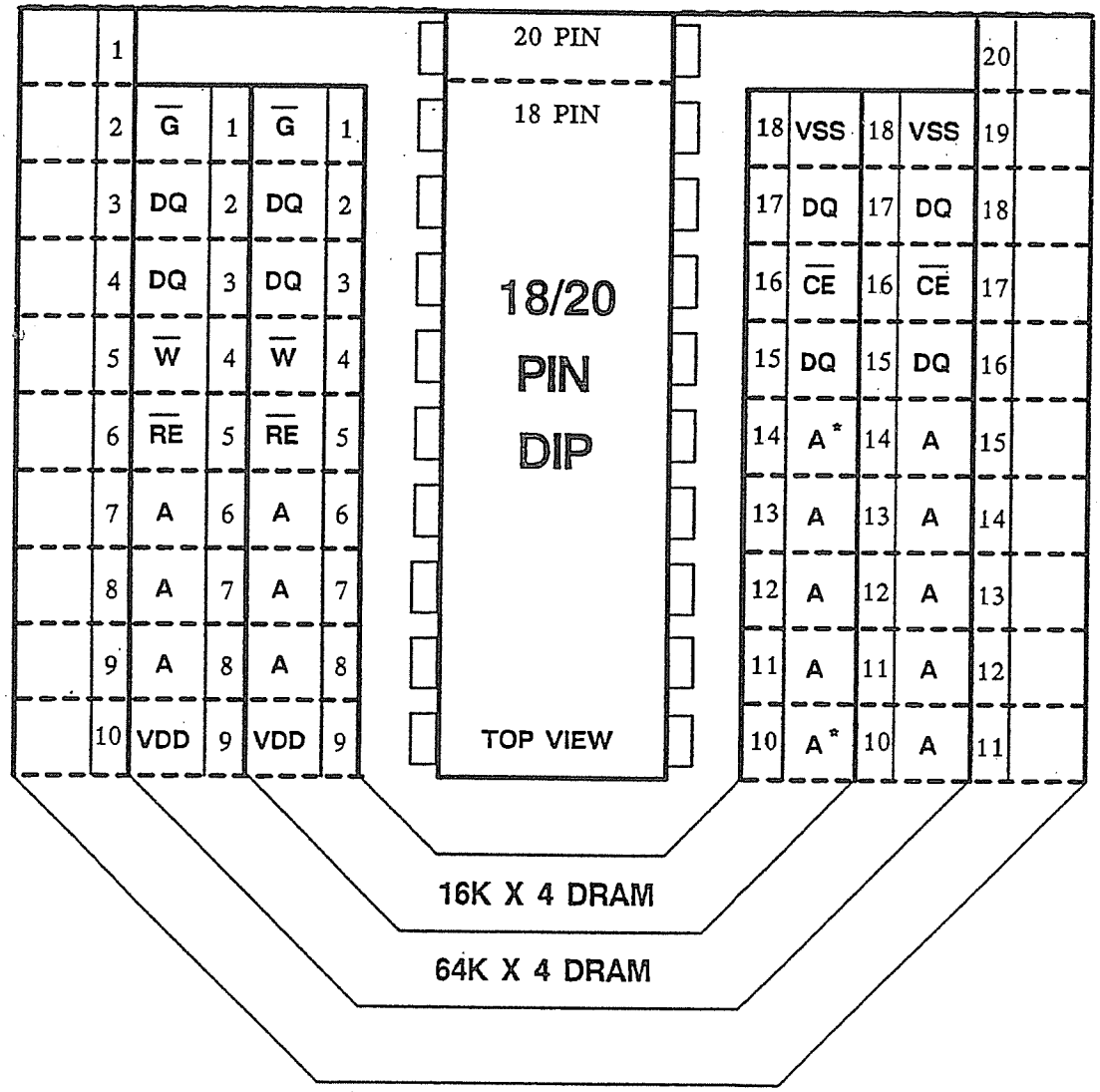
CAPACITY—1M, 2M, & 4M WORDS OF 2 BITS
LOGIC FEATURES—Multiplexed Address and a separate $\overline{CE}$ control for each data bit.
PACKAGE—26/20, 26/24, & 28/24 PIN SOJ or TSOP2, WIDTH: 0.3", PIN PITCH: 0.050"
PIN ASSIGNMENT—Fig. 3.9.2–12

3.9.2.14 – 16M BY 4 DRAM WITH 4 $\overline{CE}$ IN SOJ OR TSOP2

CAPACITY—16M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
—The part, has 4 $\overline{CE}$, one controlling each of the data bits.
PACKAGE— 34 PIN TSOP2, 12.7 mm WIDE, PP = 1.27 mm
— 34 PIN SOJ, 12.7 mm WIDE, PP = 1.27 mm
PIN ASSIGNMENT—Fig. 3.9.2–14
PACKAGE—32 PIN SOJ, 10.16 mm Wide
—32 PIN TSOP2, 10.16 mm Wide, 1.27 mm PP
PIN ASSIGNMENT—Fig. 3.9.2–14

3.9.2.15 – 64M X 4 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 64M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.9.2–15
NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.



* COLUMN ADDRESS NOT SUPPLIED ON PINS 10 & 14 TO 16K PART

FIGURE 3.9.2-1
16K & 64K BY 4 DRAM IN DIP

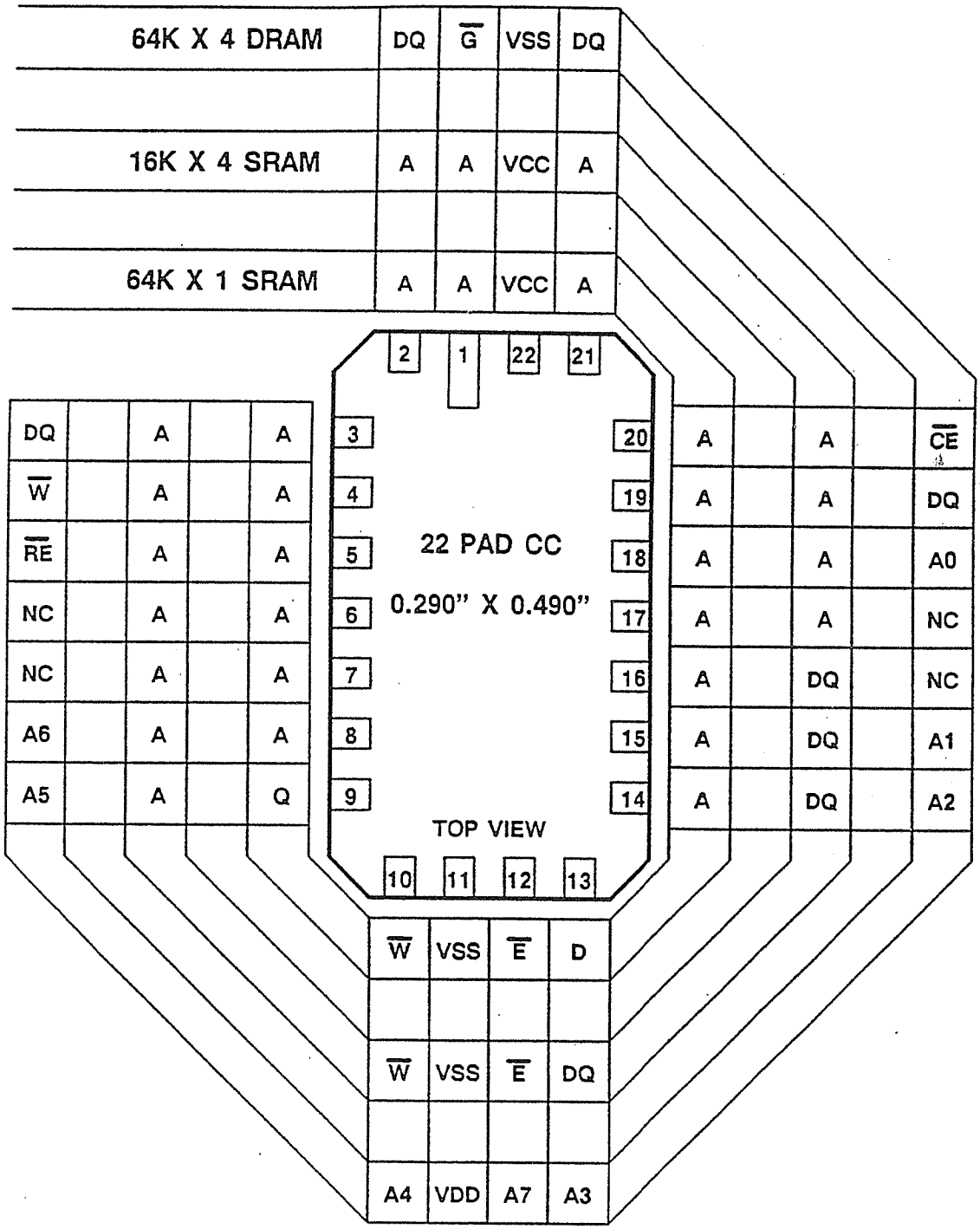


FIGURE 3.9.2-2
16K & 64K BY 4 DRAM IN RCC

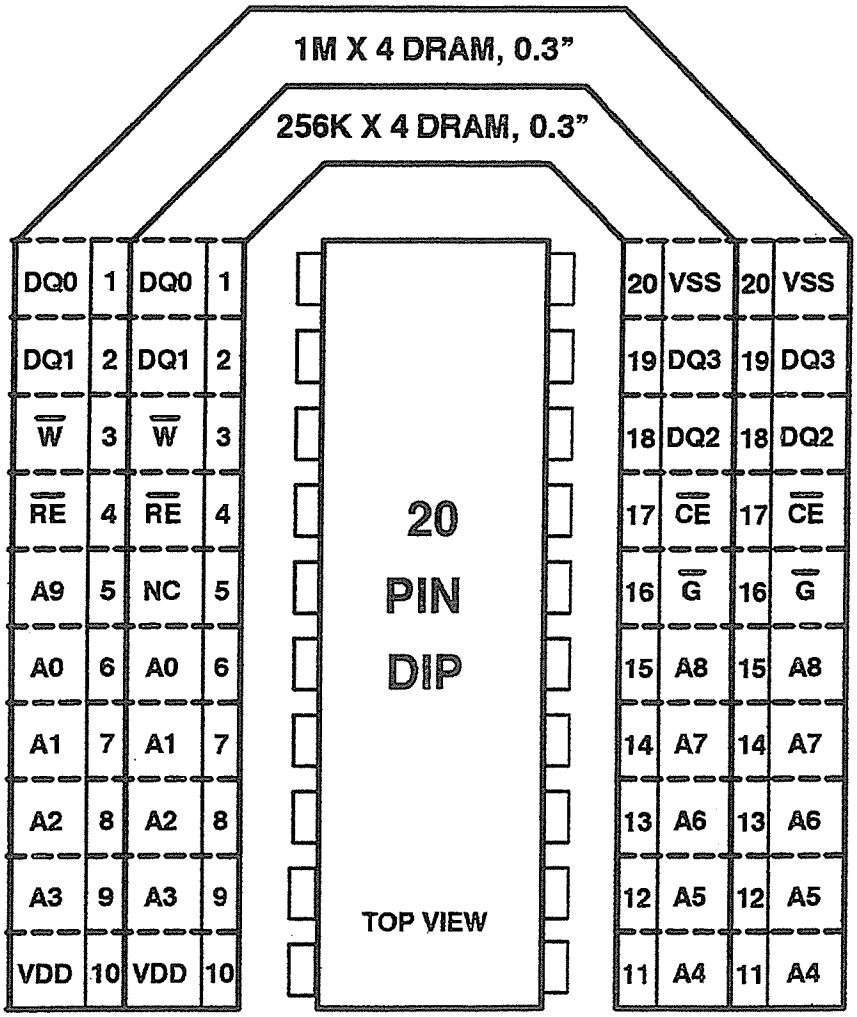
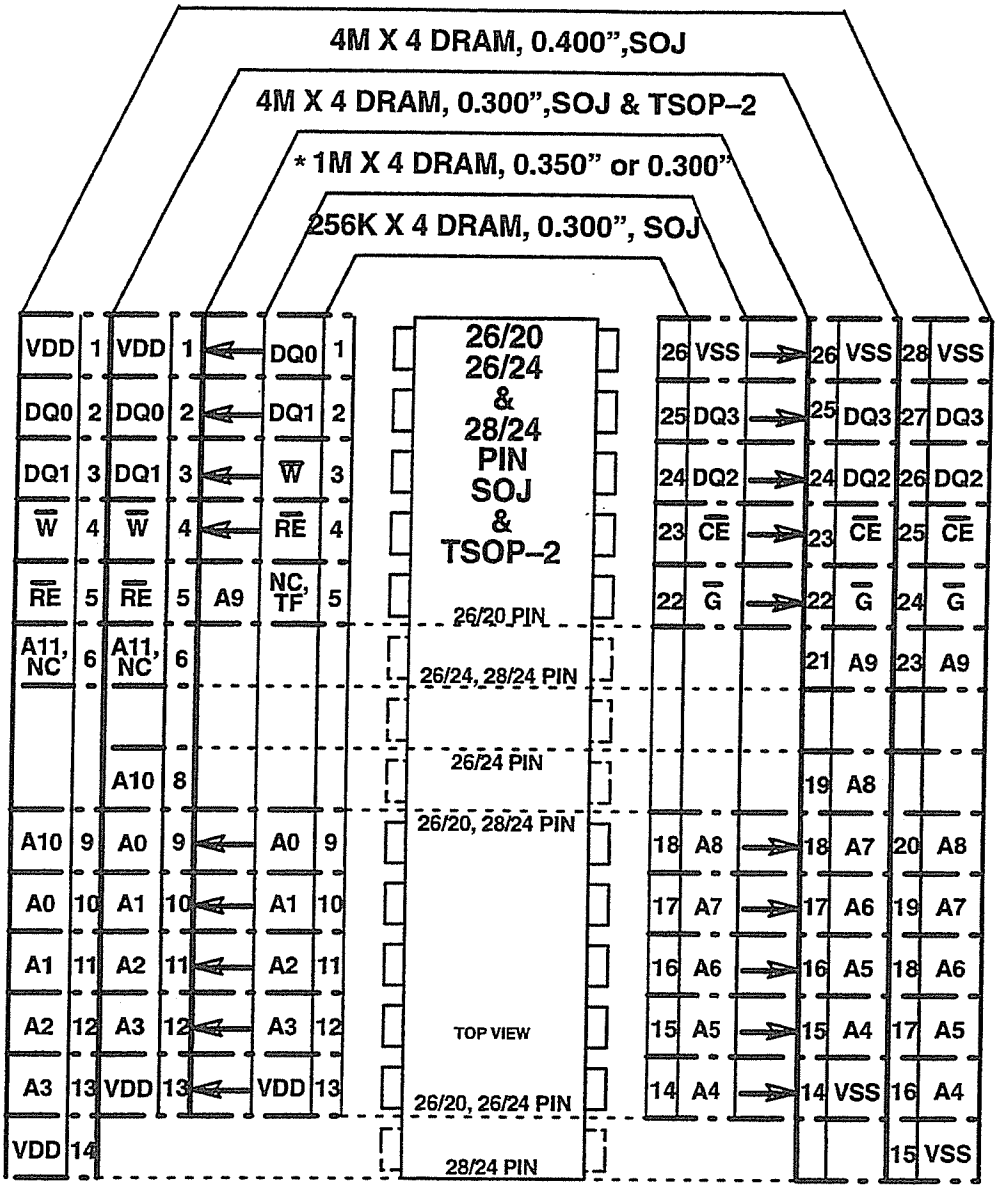


FIGURE 3.9.2–3

256K & 1M BY 4 ADDRESS MULTIPLEXED DRAM IN DIP

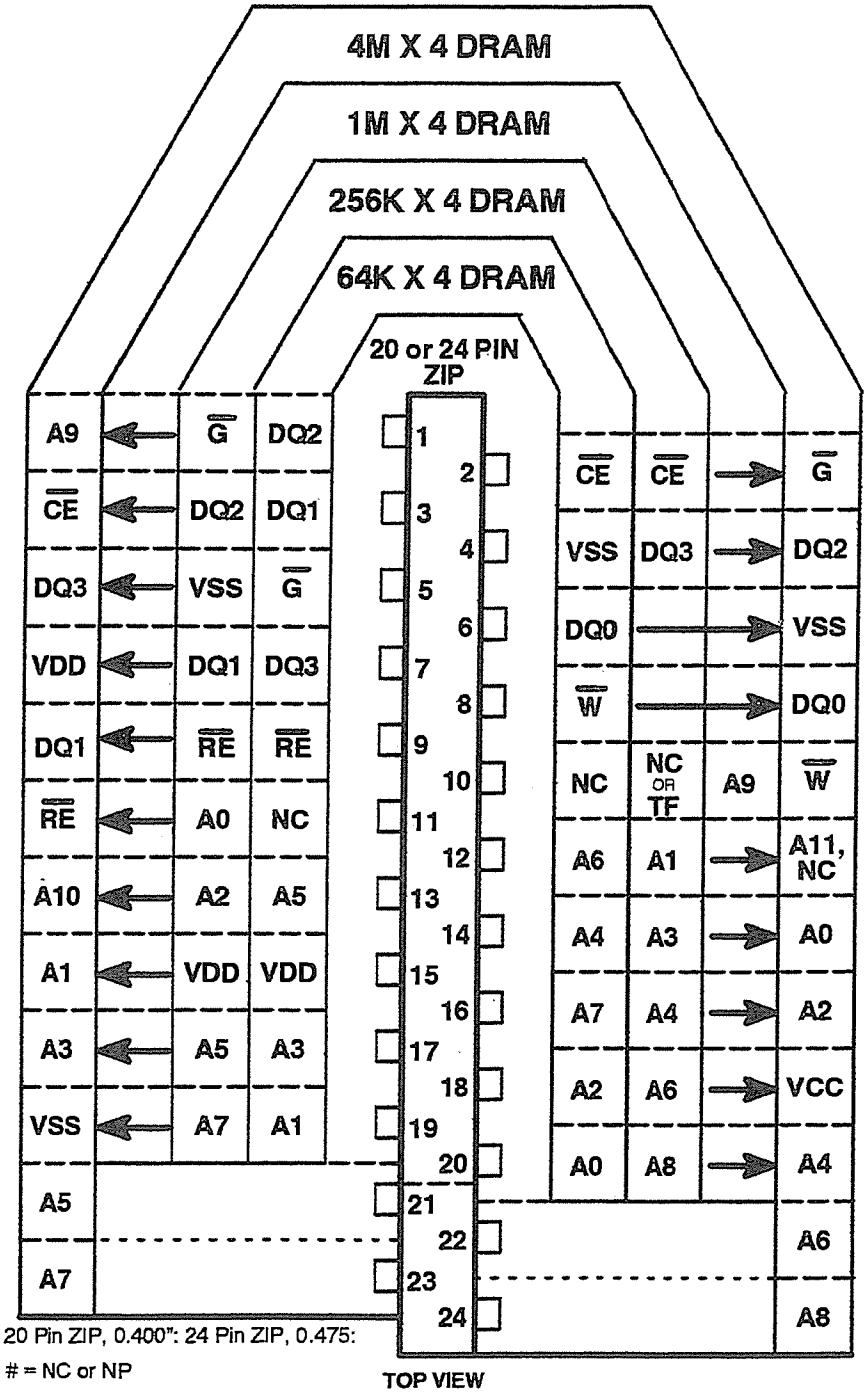


REFRESH, ROW, & COLUMN, ADDRESS CONFIGURATION

DEVICE CONFIGURATION	256K X 4	1M X 4	4M X 4	4M X 4
REFRESH COUNT	512 Refresh	1K Refresh	2K Refresh	4K Refresh
REFRESH ADDRESSES	A0 → A8	A0 → A9	A0 → A10	A0 → A11
ROW ADDRESSES	A0 → A8	A0 → A9	A0 → A10	A0 → A11
COLUMN ADDRESS	A0 → A8	AO → A9	A0 → A10	A0 → A9

* NOTE – The 1M X 4 part is approved for use in a 0.300" TSOP2 package
The JEDEC Std. 30 approved term for the TSOP–2 package is PDSO–G.

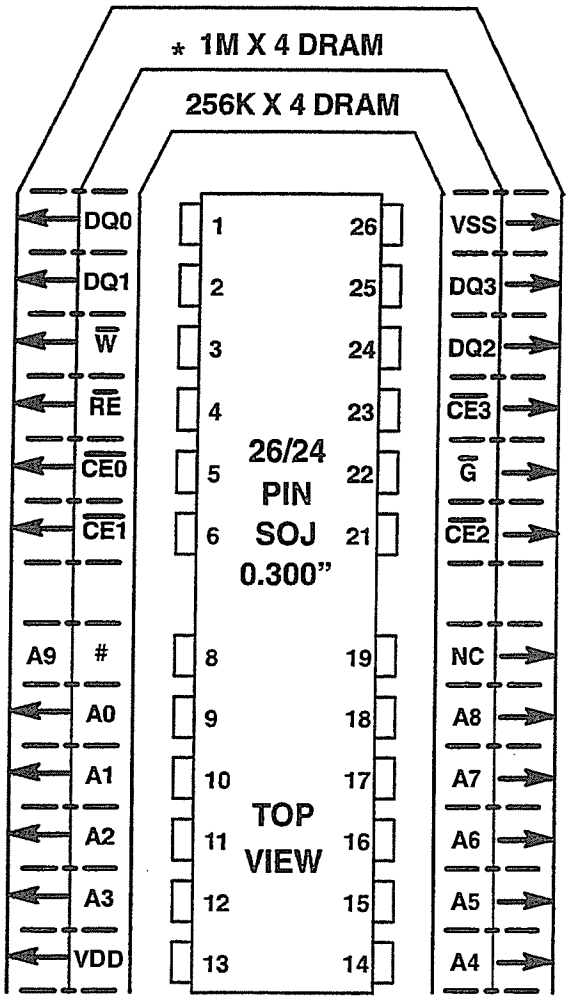
FIGURE 3.9.2–4
256K TO 4M BY 4 DRAM IN SOJ AND TSOP–2



REFRESH, ROW, & COLUMN, ADDRESS CONFIGURATION

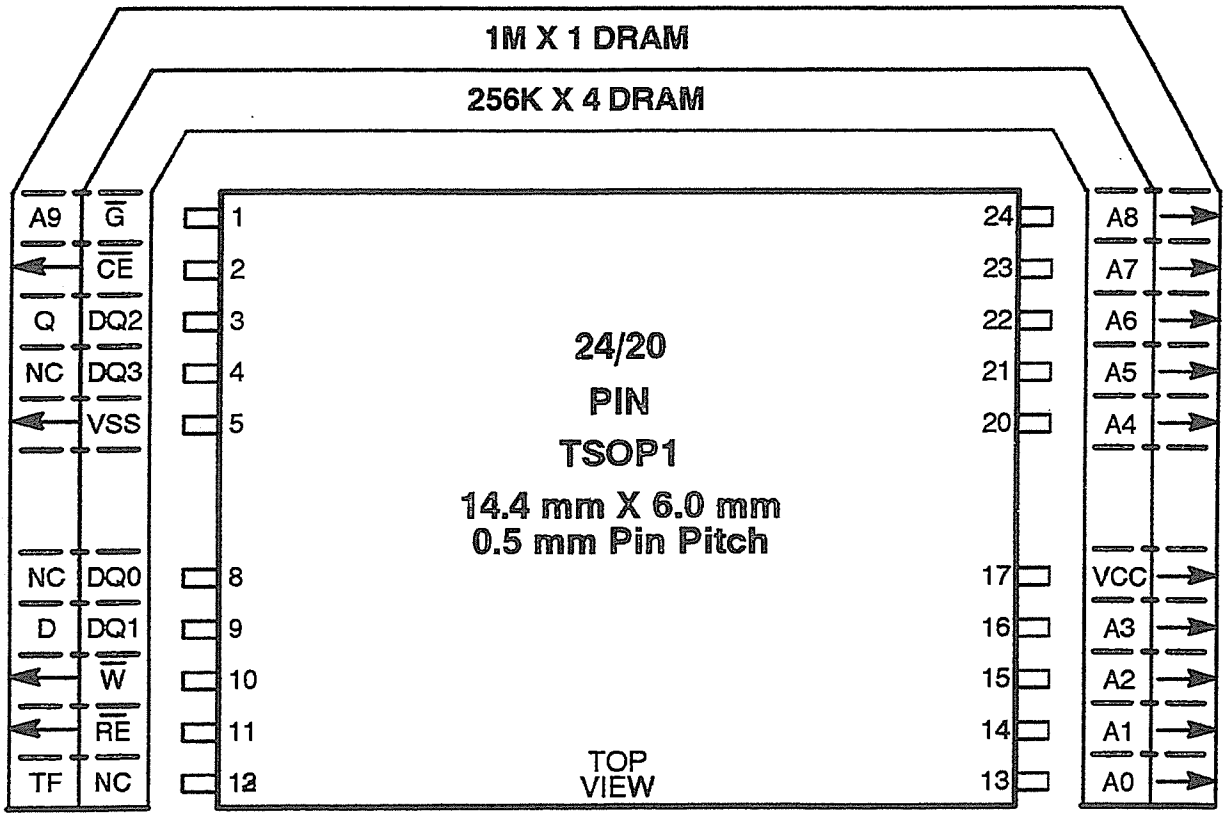
DEVICE CONFIGURATION	64K X 4	256K X 4	1M X 4	4M X 4	4M X 4
REFRESH COUNT	256 Refresh	512 Refresh	1K Refresh	2K Refresh	4K Refresh
REFRESH ADDRESSES	A0 TO A7	A0 TO A7	A0 TO A9	A0 TO A10	A0 TO A11
ROW ADDRESSES	A0 TO A7	A0 TO A7	A0 TO A9	A0 TO A10	A0 TO A11
COLUMN ADDRESS	AO TO A7	A0 TO A7	AO TO A9	A0 TO A10	A0 TO A9

FIGURE 3.9.2–5
64K TO 4M BY 4 DRAM IN ZIP



= NC or TF * THE 1M X 4 PART IS ALSO APPROVED FOR USE IN A TSOP2 PACKAGE WITH A PIN PITCH OF 0.050"

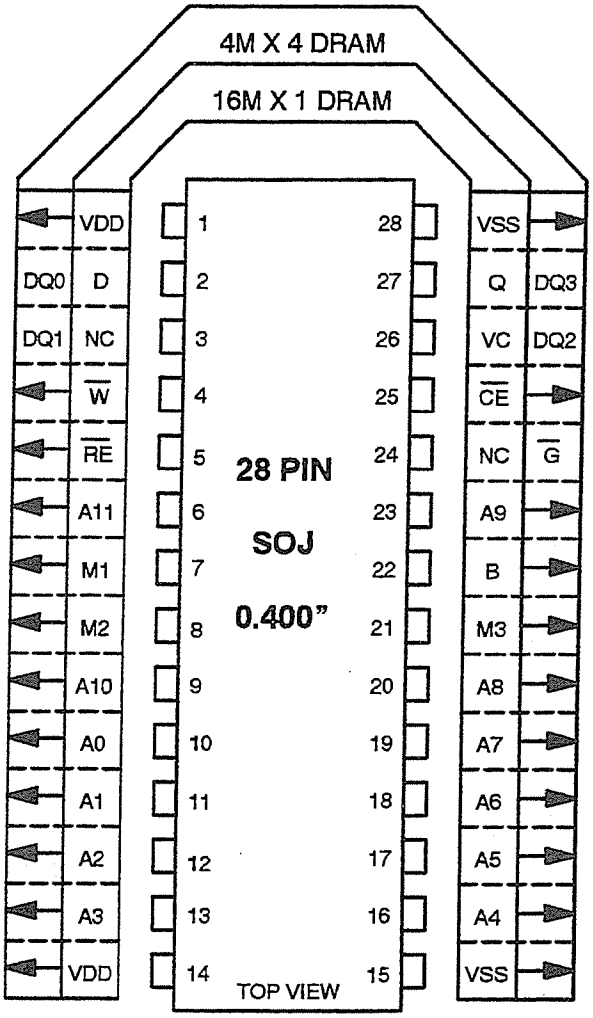
FIGURE 3.9.2–6
256K & 1M BY 4 DRAM WITH 4 $\overline{CE}$ IN SOJ & TSOP2



REFRESH ADDRESS FIELD = A0 to A8

The JEDEC Std. No. 30 designator for the TSOP1 package is PDSO–G.

FIGURE 3.9.2–7
1M BY 4 AND 4M BY 1 DRAM IN TSOP1



B TRUTH TABLE
DATA INTERFACE CONTROL
B=HI, DATA X1
B=LO, DATA X4

The default state for M1, M2, M3, and B ahould be HI when no external connection is made.

M1/M2/M3 TRUTH TABLE		M1	M2	M3
MANDATORY MODE	FAST PAGE	HI	HI	HI
OPTIONAL MODES	NIBBLE	LO	HI	HI
	BYTE	LO	LO	HI
	BURST	LO	HI	LO
	STATIC COLUMN	HI	LO	HI
	VENDOR SPECIFIC	LO	LO	LO
	VENDOR SPECIFIC	HI	HI	LO
	VENDOR SPECIFIC	HI	LO	LO

FIGURE 3.9.2–8
16M X 1/4M X 4 CONFIGURABLE DRAM IN SOJ

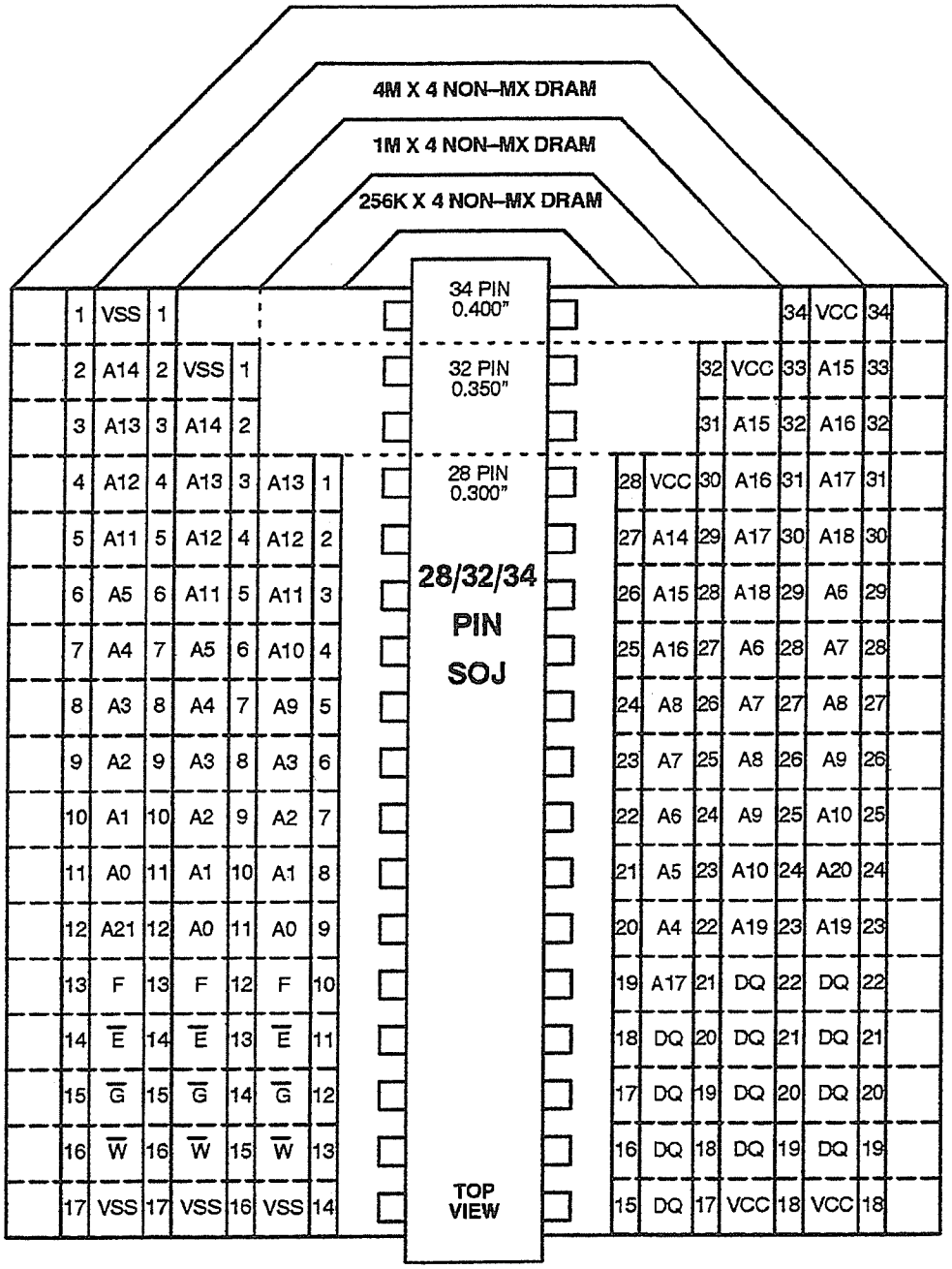
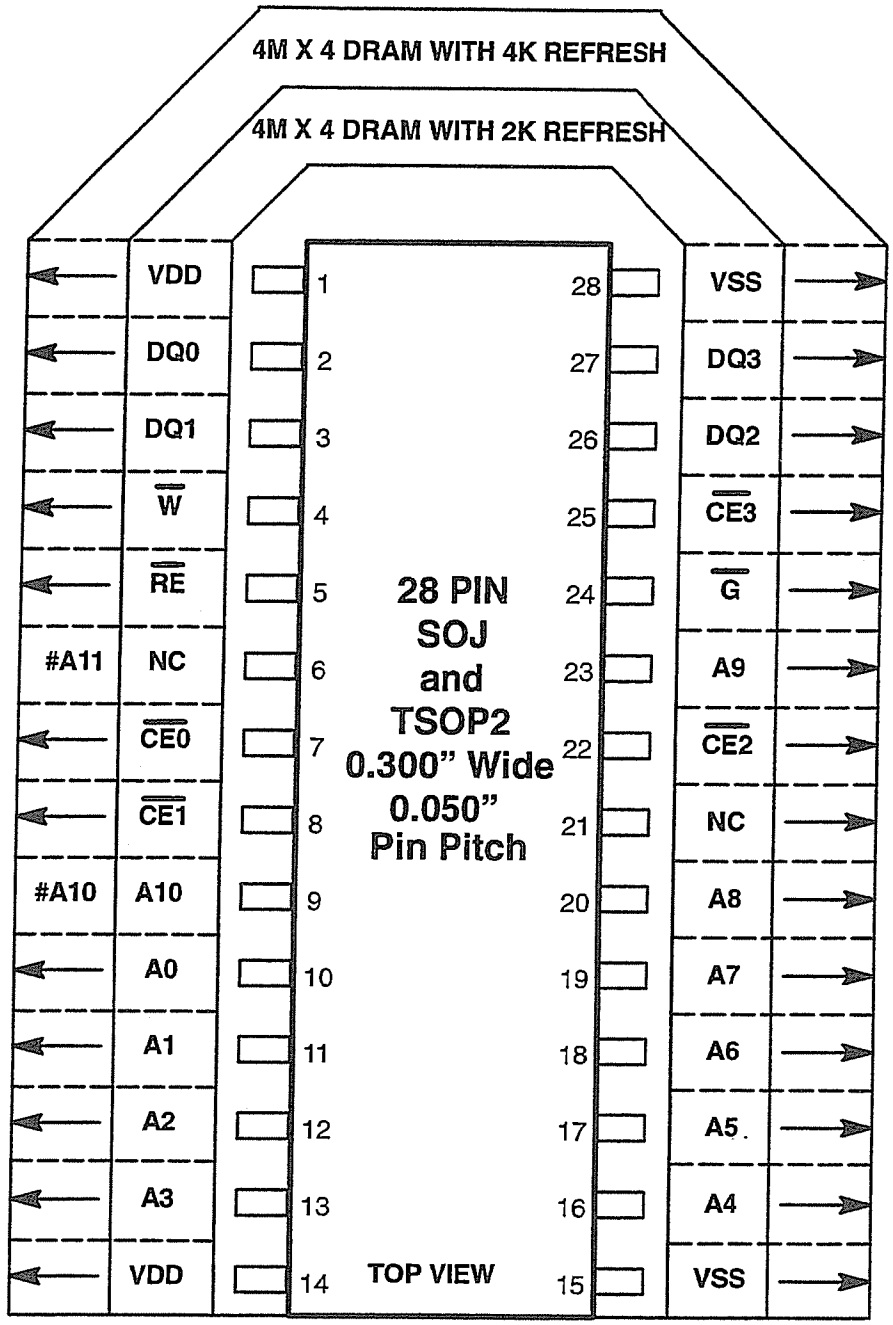


FIGURE 3.9.2–9
256K TO 4M BY 4 NON–MULTIPLEXED DRAM IN SOJ



The JEDEC Std. No 30 designator for the TSOP2 package is PDSO–G
NOTE: A10 & A11 are used as defined in the following table as a function of the refresh count implemented.

Device Configuration	4M X 4,	4M X 4,
Refresh Count	2K	4K
Row/Refresh Address	A0 → A10	A0 → A11
Column Address	A0 → A10	A0 → A9

FIGURE 3.9.2–10
4M BY 4 DRAM WITH 4 $\overline{CE}$ IN SOJ AND TSOP2

3.9.2.1 – 16K & 64K BY 4 DRAM IN DIP

CAPACITY—16K, 64K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—18 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT—Fig. 3.9.2–1

3.9.2.2 – 16K BY 4 DRAM IN DIP

CAPACITY—16K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address, Separate DATA I/O
PACKAGE—20 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT—Fig. 3.9.2–1
NOTE: At the time that this document was published, this standard was in the process of being rescinded by the Committee.

3.9.2.3 – 64K BY 4 DRAM IN RCC

CAPACITY—64K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address with Common DATA I/O
PACKAGE—22 PAD (PIN) RCC, 0.290" X 0.490"
PIN ASSIGNMENT—Fig. 3.9.2–2

3.9.2.4 – 256K & 1M BY 4 DRAM FAMILY IN DIP

CAPACITY—256K, 1M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—20 PIN DIP, Width: 0.3" for 256K & 1M,
PIN ASSIGNMENT—Fig. 3.9.2–3

3.9.2.5 – 256K TO 4M BY 4 DRAM FAMILY IN SOJ & TSOP2

CAPACITY—256K, 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—26/20 PIN SOJ: 0.3" by 0.675" for 256K
—26/20 PIN SOJ or TSOP2: 0.3" or 0.35" by 0.675" for 1M
—26/24 PIN SOJ OR TSOP–2: 0.3" for 4M
—28/24 PIN SOJ: 0.4" by 0.725 for 4M
PIN ASSIGNMENT—Fig. 3.9.2–4

3.9.2.6 – 64K TO 4M BY 4 DRAM IN ZIP

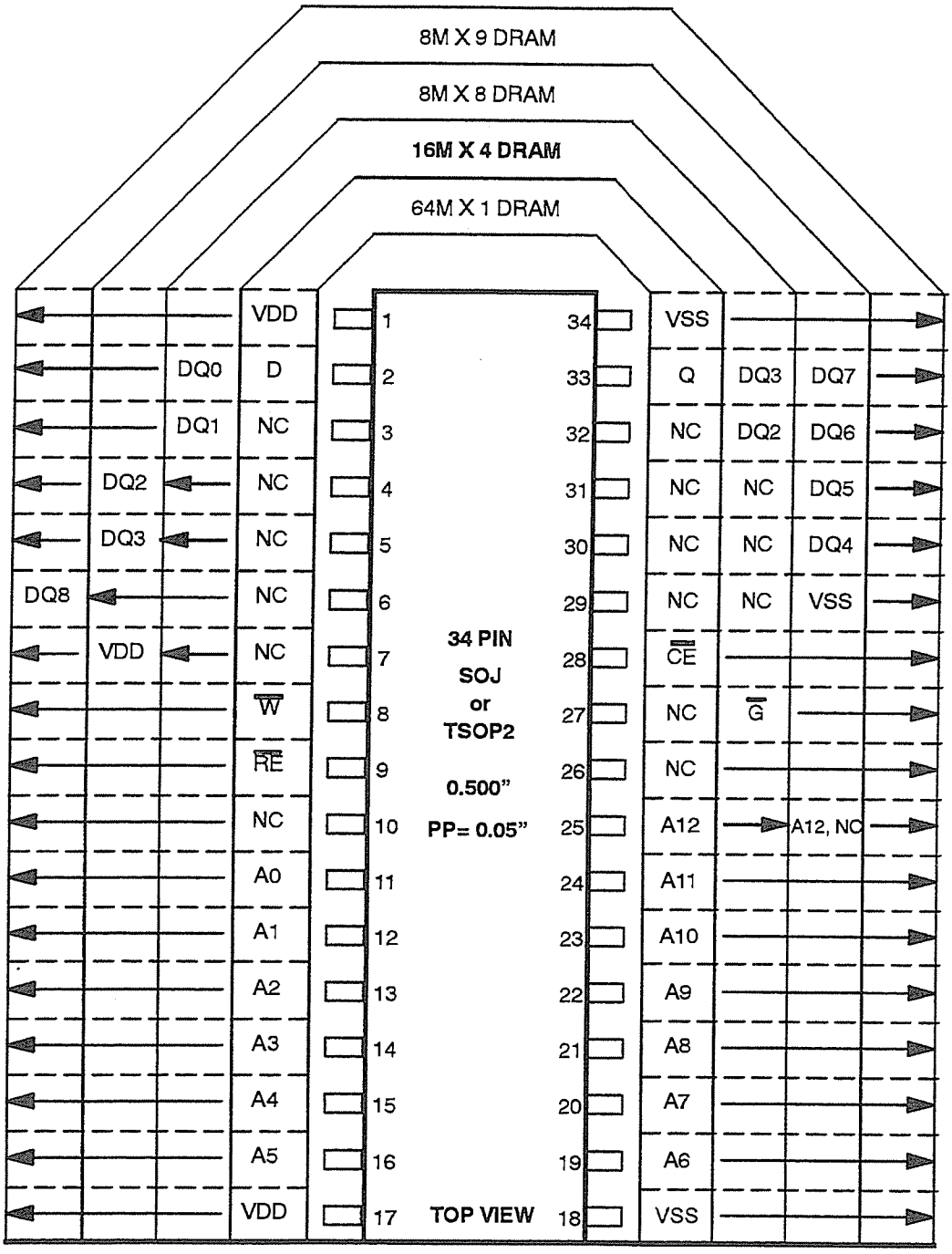
CAPACITY—64K, 256K, 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—20 PIN ZIP, 0.400" WIDE FOR 64K, 256K, & 1M PARTS
—24 PIN ZIP, 0.475" WIDE FOR 4M PART
PIN ASSIGNMENT—Fig. 3.9.2–5

3.9.2.7 – 256K & 1M BY 4 DRAM WITH 4 CE IN SOJ & TSOP2

CAPACITY—256K, 1M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address with 4 CE clocks controlling the 4 data bits
PACKAGE—26/24 PIN SOJ, Width: 0.3"
—26/24 PIN TSOP2, WIDTH: 0.3", PIN PITCH: 0.050"
PIN ASSIGNMENT—Fig. 3.9.2–6

3.9.2.8 – 256K BY 4 DRAM IN TSOP1

CAPACITY—256K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—24/20 PIN TSOP1, 14.4 mm x 6.0 mm, 0.5 mm LEAD PITCH
PIN ASSIGNMENT—Fig. 3.9.2–7



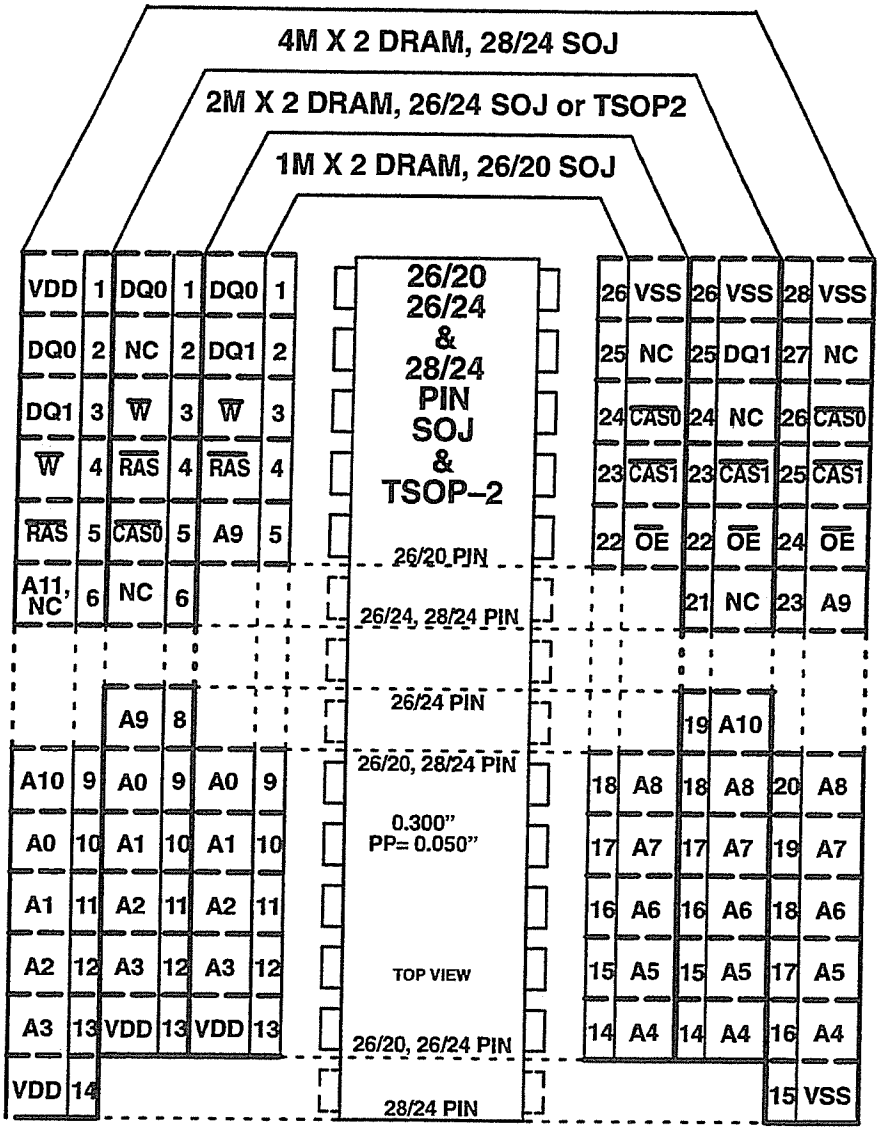
ROW, COLUMN, & REFRESH ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION REFRESH COUNT	64M X 1	16M X 4	8M X 8(9) 4K Refresh	8M X 8(9) 8K Refresh
ROW/REFRESH ADDRESSES COLUMN ADDRESSES	A0 Through A12 A0 Through A12	A0 Through A12 A0 Through A10	A0 Through A11 A0 Through A10	A0 Through A12 A0 Through A9

▌This standard recognizes that some early deliveries of these parts may have to be in a 0.6" wide package

FIGURE 3.9.2-11

16M BY 4 DRAM IN SOJ & TSOP2

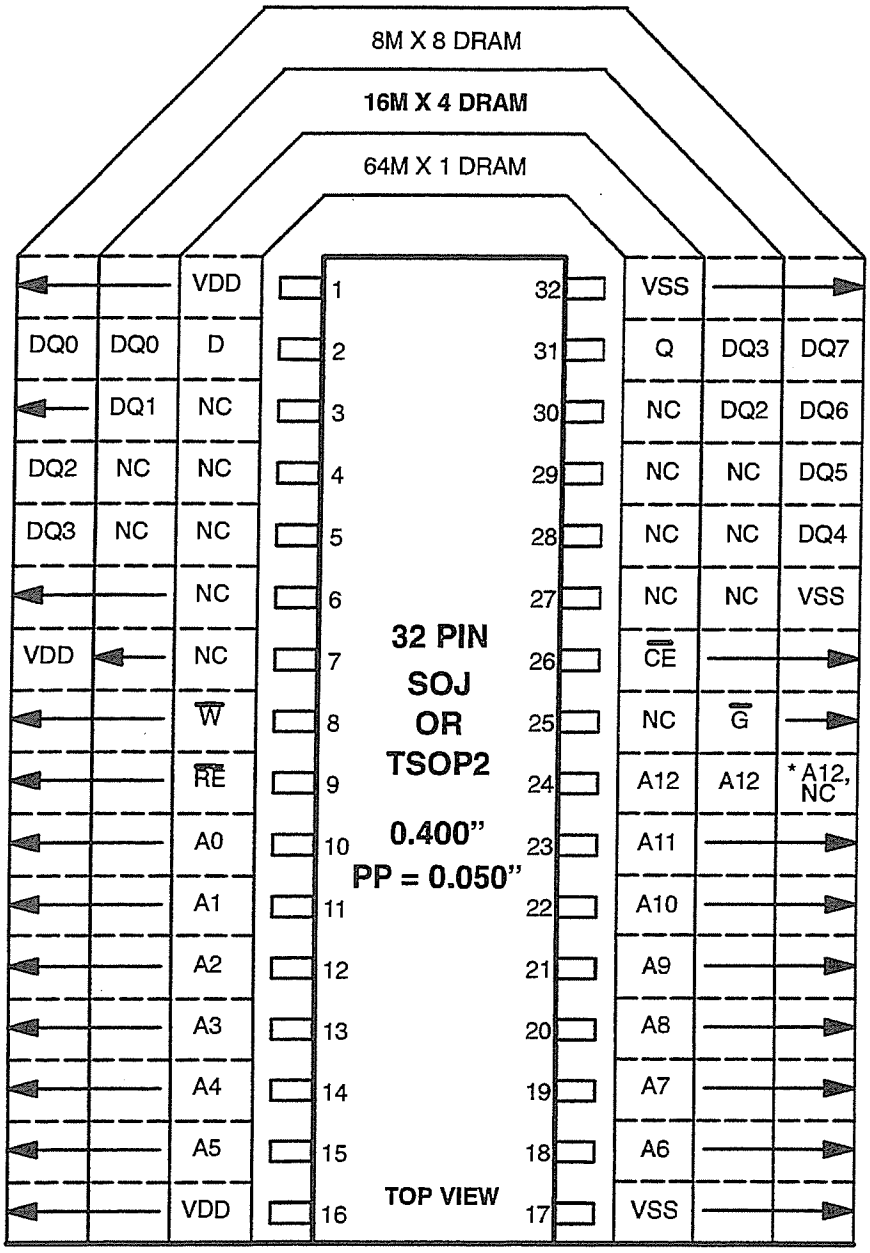


ROW, & COLUMN, ADDRESS CONFIGURATION

DEVICE CONFIGURATION	1M X 2	2M X 2	4M X 2	4M X 2
ROW COUNT	1K Rows	1K Rows	2K Rows	4K Rows
ROW ADDRESSES	A0 → A9	A0 → A10	A0 → A10	A0 → A11
COLUMN ADDRESS	A0 → A9	AO → A9	A0 → A10	A0 → A9

FIGURE 3.9.2–12
1M TO 4M BY 2 DRAM WITH 2 CAS IN SOJ & TSOP2

Release 4r7

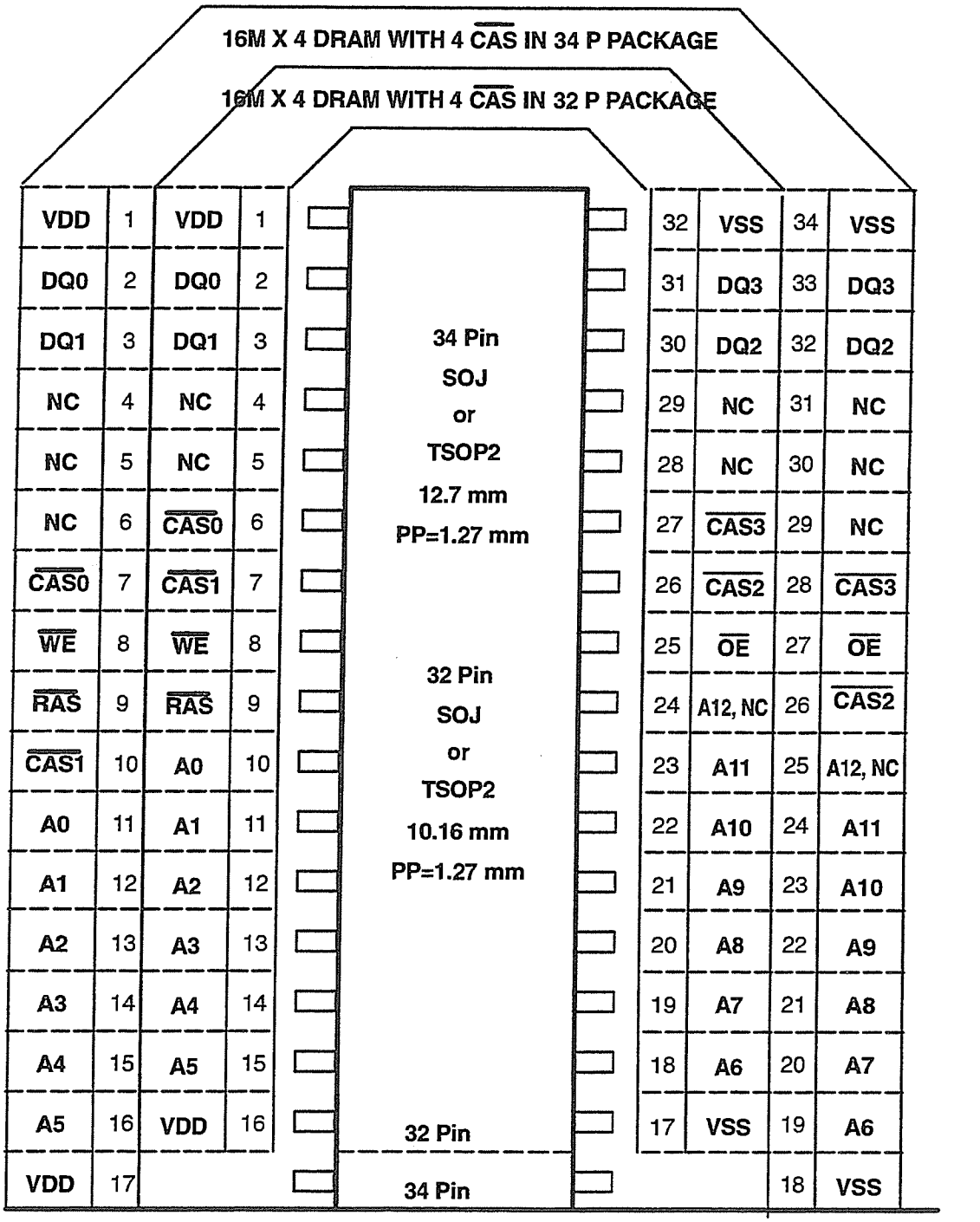


* Pin 24 is NC for the 16M X 4 & 8K X 8 parts with a 4K Refresh.

ROW & COLUMN, ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION	64M X 1	16M X 4	16M X 4	8M X 8	8M X 8
ROW COUNT		4K Rows	8K Rows	4K Rows	8K Rows
ROW ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12
COLUMN ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A10	A0 ⇒ A10	A0 ⇒ A9

FIGURE 3.9.2–13
16M BY 4 DRAM IN SOJ & TSOP2

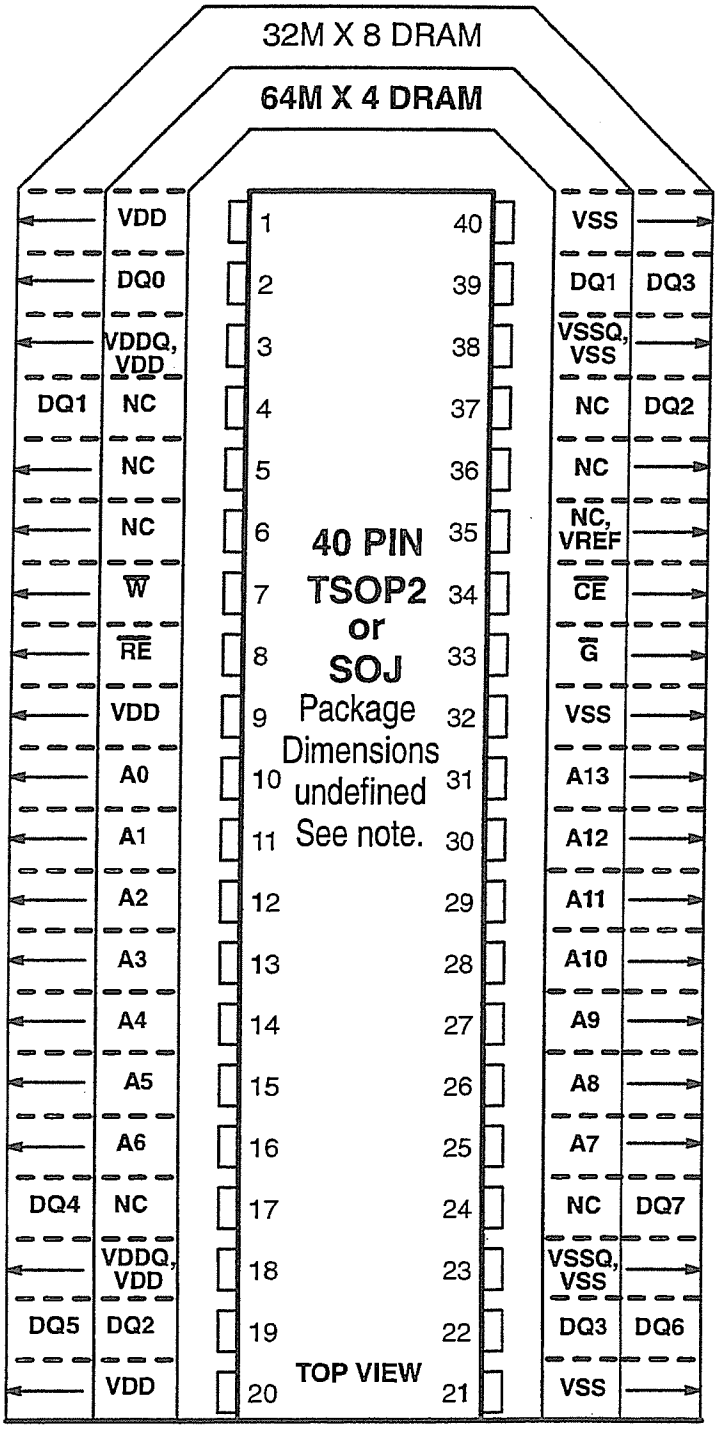


ADDRESS CONFIGURATIONS

ROW COUNT	4K Rows	8K Rows
ROW ADDRESSES	A0 ⇒ A11	A0 ⇒ 12
COLUMN ADDRESSES	A0 ⇒ A11	A0 ⇒ 10

*NOTE: The JESD30 approved term for the TSOP2 package is PDSO–G, for the SOJ is PDSO–J

FIGURE 3.9.2–14
16M BY 4 DRAM WITH 4 CAS IN SOJ & TSOP2



	64M X 4	32M X 8
ROW ADDRESSES	A0 TO A13	A0 TO A13
COLUMN ADDRESSES	A0 TO A11	A0 TO A10

NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. CBR refresh is the only standardized method of refreshing non–synchronous DRAMs with densities of 256Mb and higher.

3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms. (7.8 µs per row with 8K rows, 3.9 µs with 16K rows.

4. (NC, VREF) is VREF on devices that require an external voltage reference.

5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.

6. The VSSQ designator is used when the ground reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS)

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.9.2–15
64M BY 4 DRAM PIN ROTATION IN TSOP2

3.9.3 Byte Wide DRAM

3.9.3.1 – 32K BY 8 DRAM IN DIP

CAPACITY—32K WORDS OF 8 BITS,
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.9.3–1

3.9.3.2 – 32K BY 8 DRAM IN RCC

CAPACITY—32K WORDS OF 8 BITS,
PACKAGE—32 PAD (PIN) RCC, 0.450" X 0.550"
PIN ASSIGNMENT—Fig. 3.9.3–2

3.9.3.3 – 512K BY 8 & BY 9 DRAM IN SOJ, TSOP2, & ZIP

CAPACITY—512K WORDS OF 8 & 9 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
PACKAGE—28 PIN SOJ, 0.400" WIDE
—28 PIN TSOP2, 0.400" WIDE
—28 PIN ZIP, 0.475" WIDE
PIN ASSIGNMENT—SOJ & TSOP2, Fig. 3.9.3–3
—ZIP, Fig. 3.9.3–4

3.9.3.4 – 512K BY 8 & BY 9 NON–MUX DRAM IN SOJ

CAPACITY—512K WORDS OF 8 & 9 BITS,
LOGIC FEATURES—NON–MULTIPLEXED ADDRESS
PACKAGE—36 PIN SOJ, 0.400" WIDE
PIN ASSIGNMENT—Fig. 3.9.3–5

3.9.3.5 – 2M BY 8 & 9 DRAM IN SOJ & TSOP2

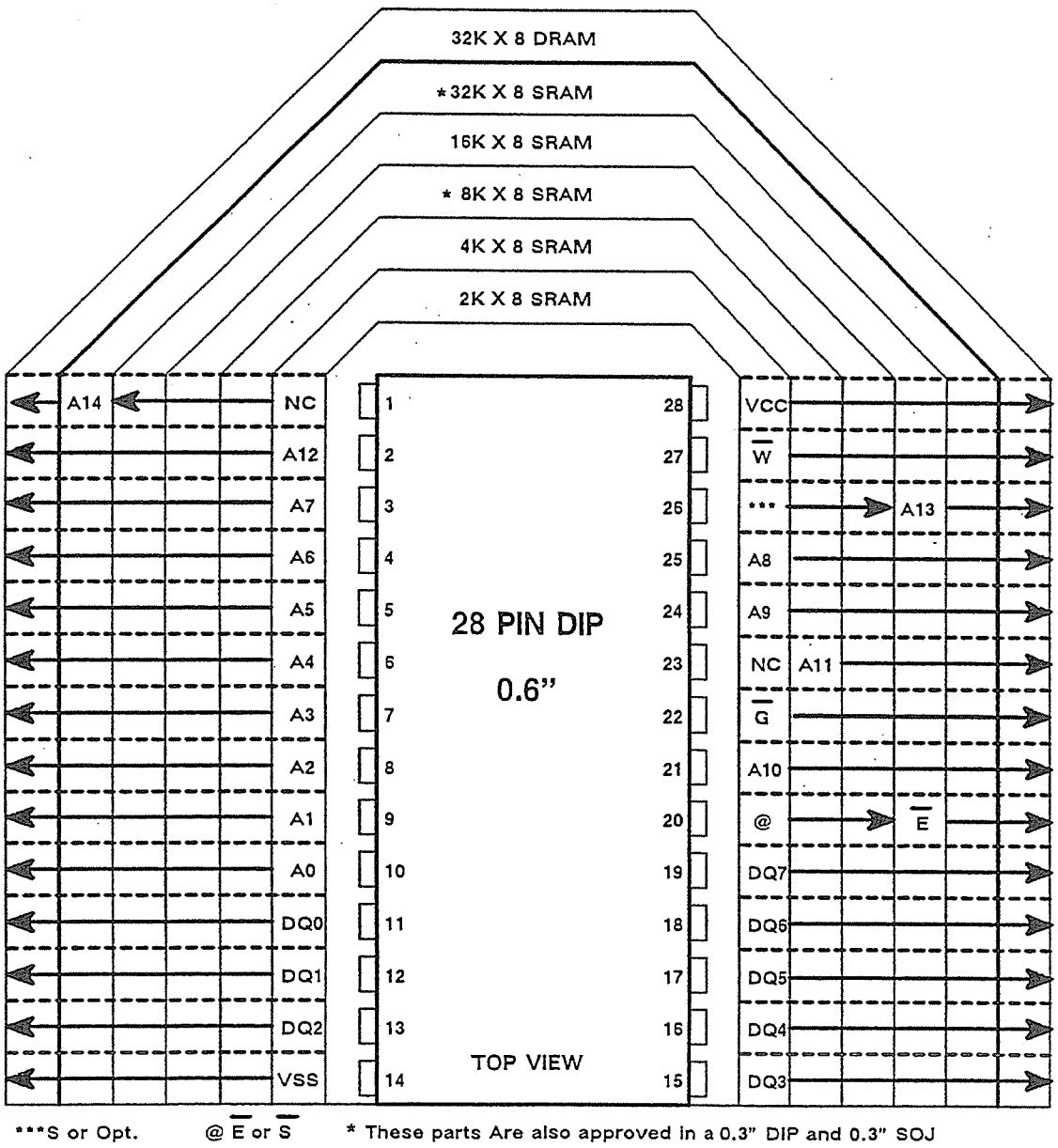
CAPACITY—2M WORDS OF 8 & 9 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
—At the option of the manufacturer, these parts may utilize either 2K or 4K refresh cycles
PACKAGE—28 PIN SOJ or TSOP2, 0.300" or 0.400" WIDE, 0.050" PIN PITCH for 2M BY 8 Part
—32 PIN SOJ or TSOP2, 0.400" WIDE, 0.050" PIN PITCH for 2M BY 8 or 9 Part
PIN ASSIGNMENT—Fig. 3.9.3–6

3.9.3.6 – 8M BY 8 & 9 DRAM IN SOJ & TSOP2

CAPACITY—8M WORDS OF 8 or 9 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
—At the option of the manufacturer, these parts may utilize either 4K or 8K refresh cycles
The X8 part is available in two package sizes as defined below. The pin rotations of the two are essentially the same with the exception of two NC pins.
PACKAGE—34 PIN SOJ, 0.500" WIDE
—34 PIN TSOP2, 0.500" WIDE, 0.025" PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.3–7
PACKAGE—32 PIN SOJ, 0.400" Wide
—32 PIN TSOP2, 0.400" WIDE, 0.050" PP
PIN ASSIGNMENT—Fig. 3.9.1–12

3.9.3.7 – 32M X 8 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 32M WORDS OF 8 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.9.3–9
NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.



***S or Opt. @ $\overline{E}$ or $\overline{S}$ * These parts Are also approved In a 0.3" DIP and 0.3" SOJ

FIGURE 3.9.3-1
32K BY 8 DRAM IN DIP

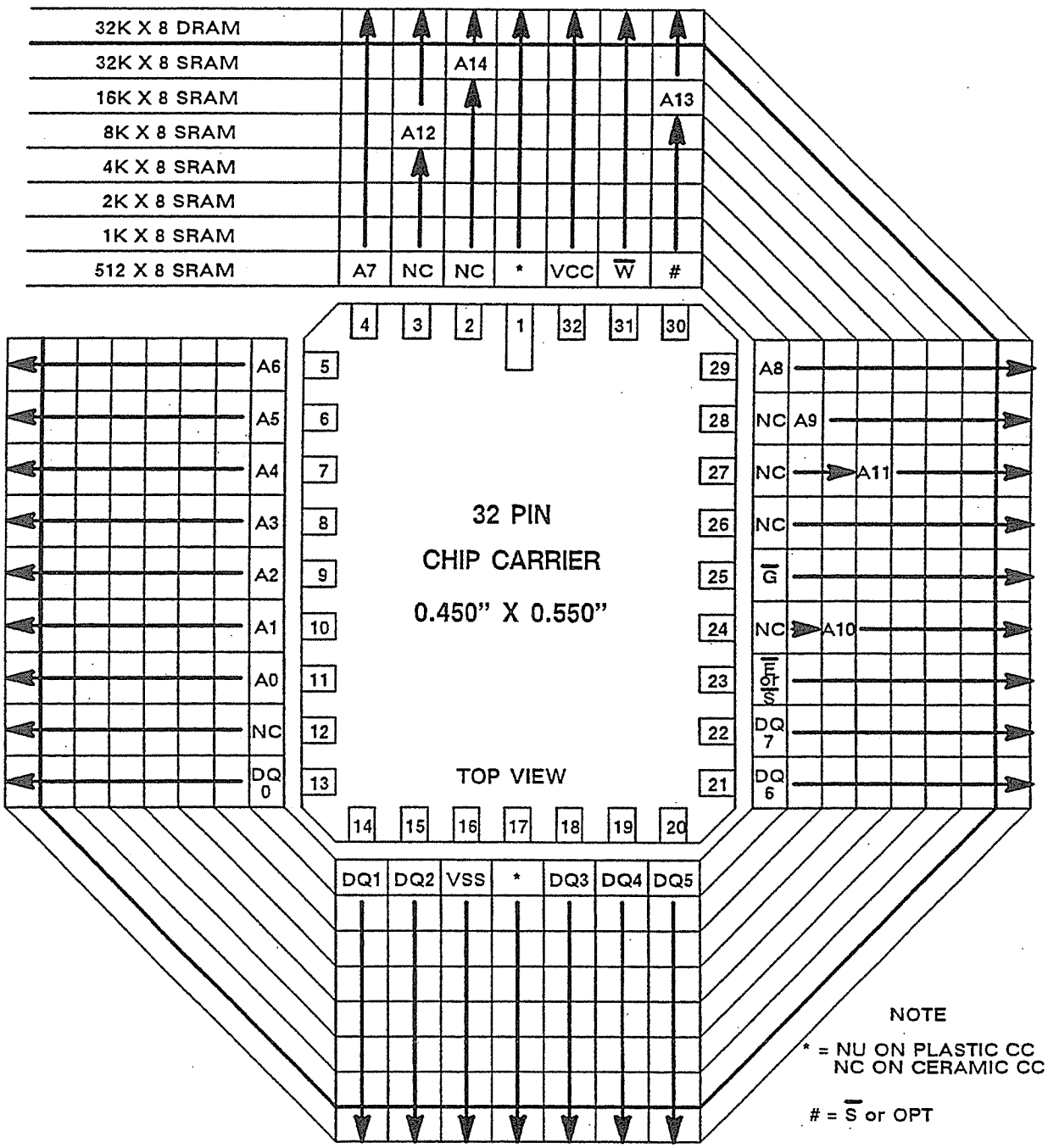
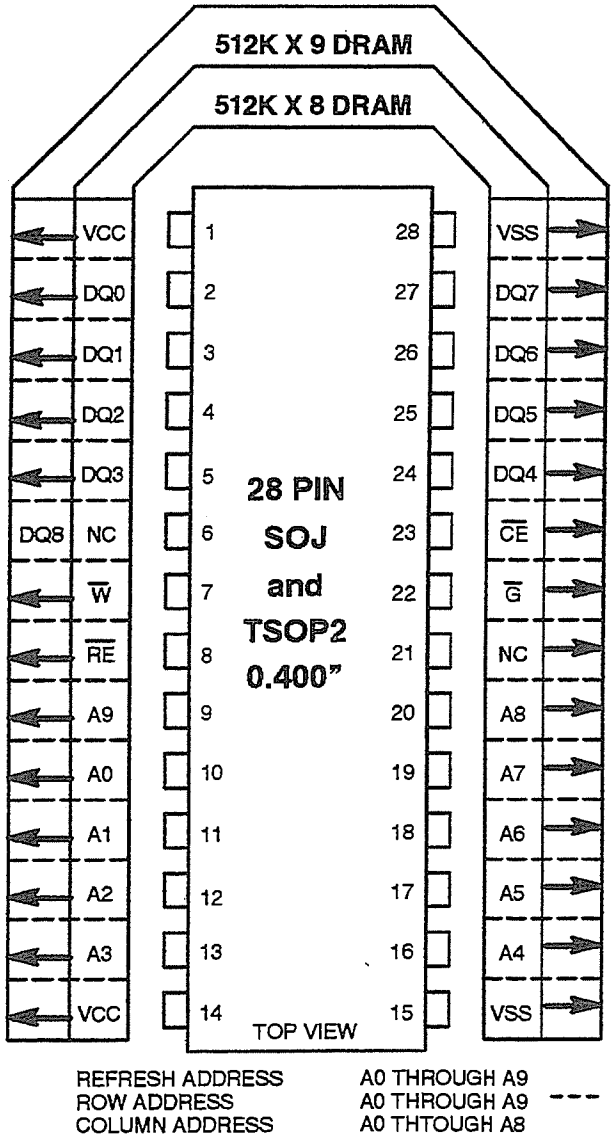


FIGURE 3.9.3-2
32K BY 8 DRAM IN RCC



The JEDEC Std. No 30 designator for the TSOP2 package is PDSO–G

FIGURE 3.9.3–3
512K by 8 and 9 DRAM in SOJ

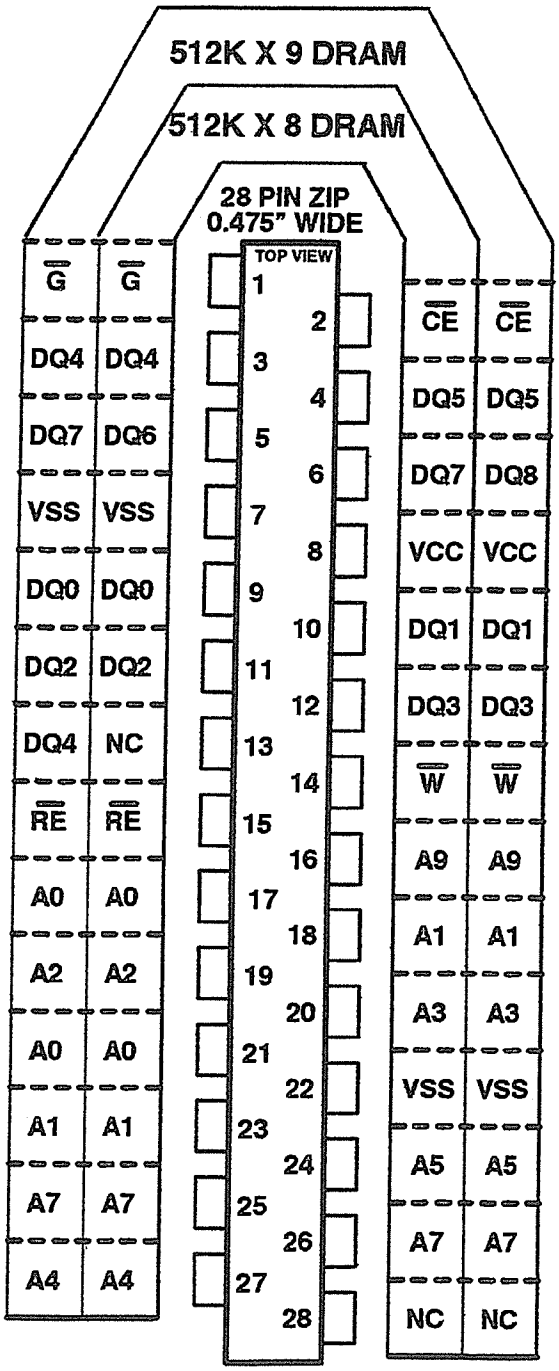
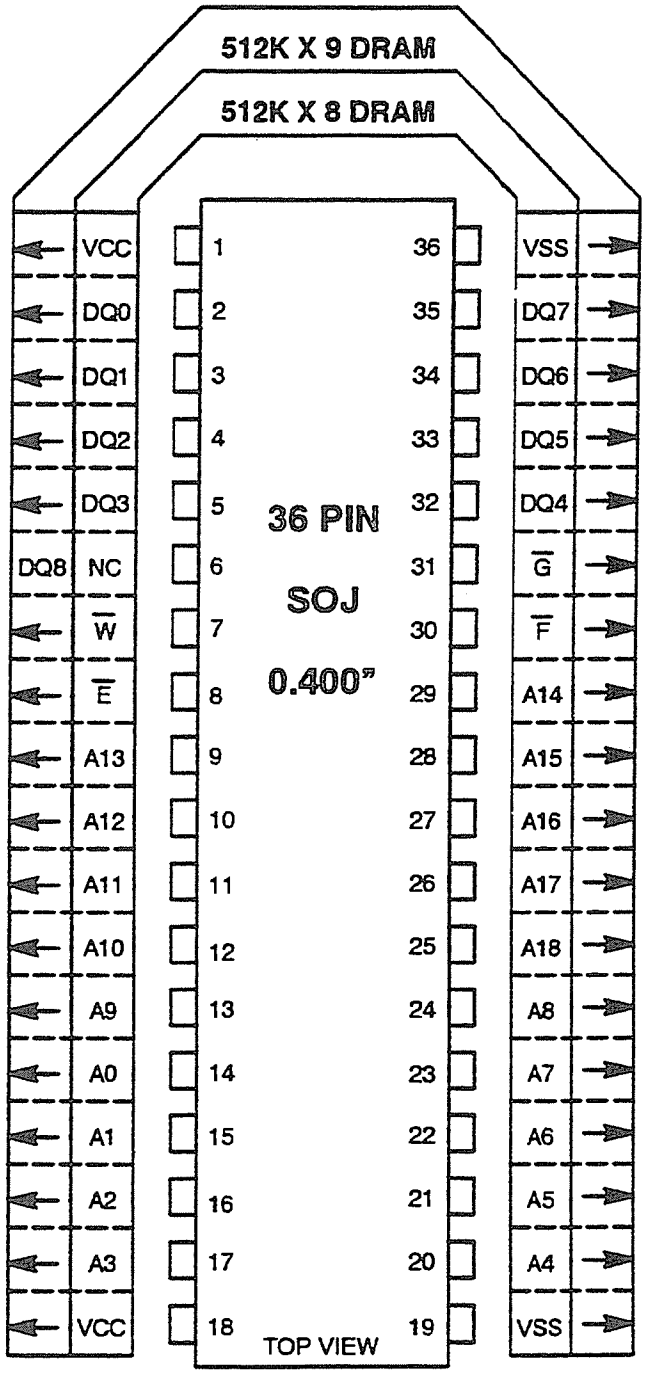


FIGURE 3.9.3–4
512K by 8 and 9 DRAM in ZIP



Refresh address field = A0 THROUGH A9

FIGURE 3.9.3–5
512K by 8 and 9 NON–MULTIPLEXED DRAM in SOJ

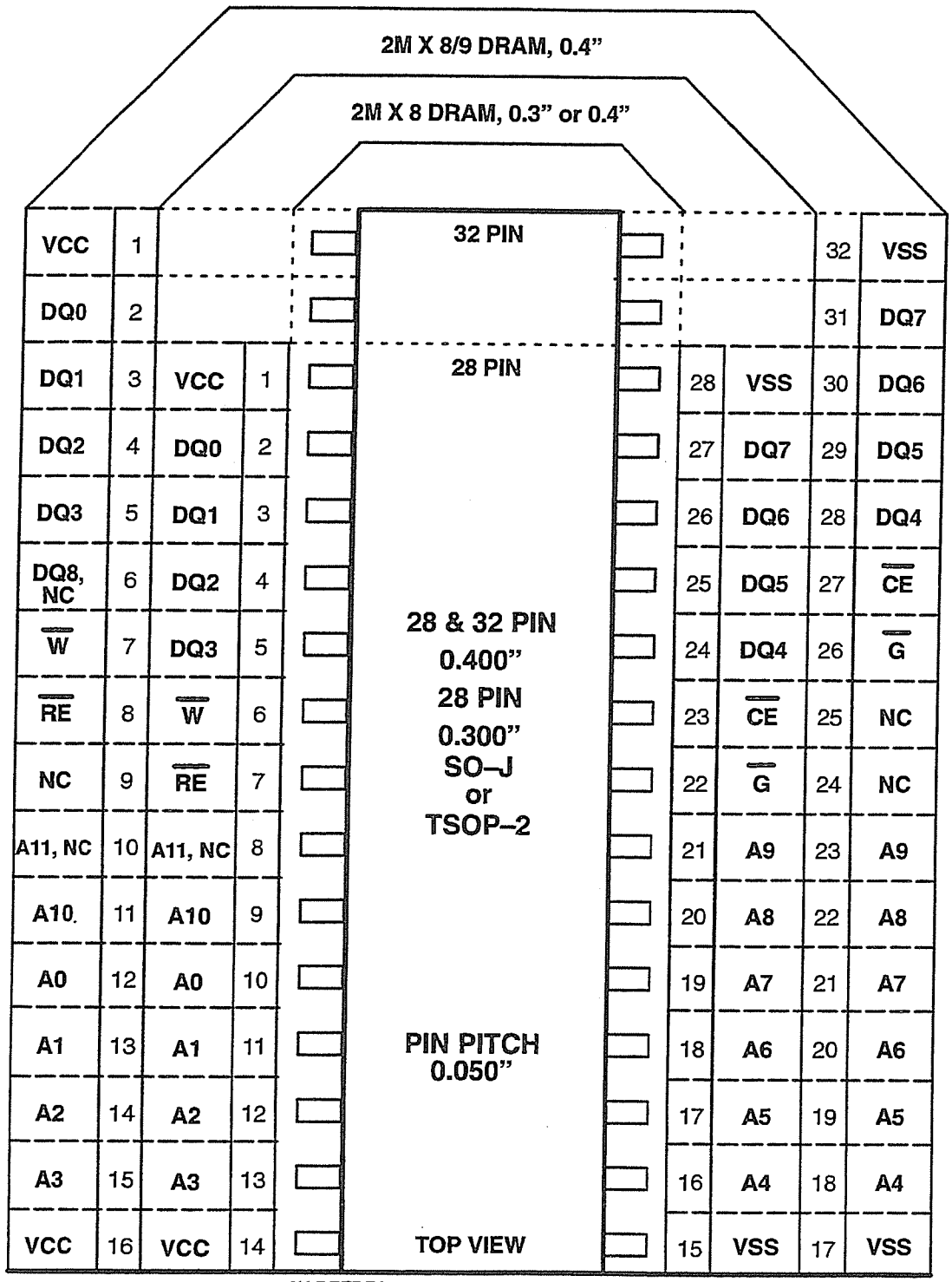
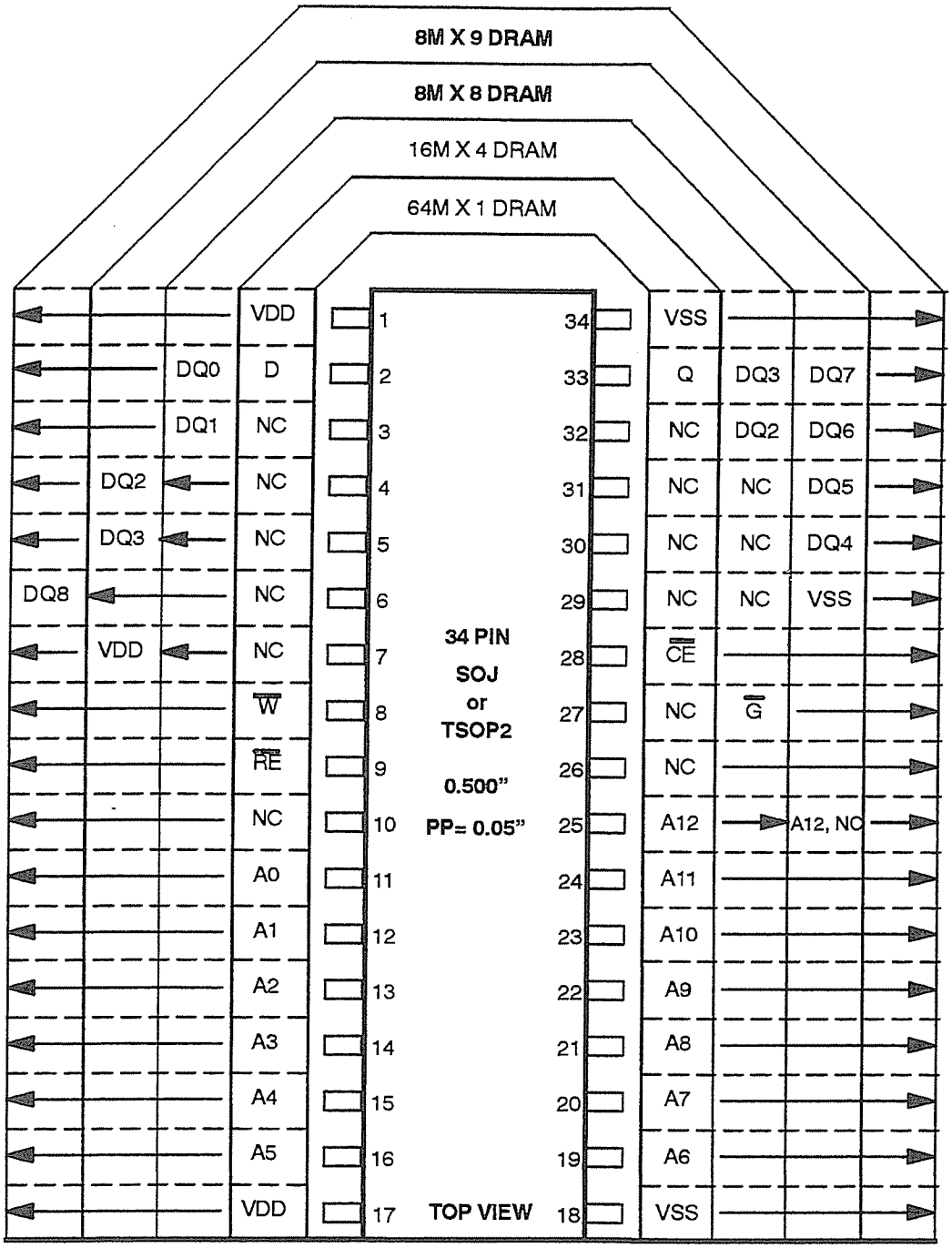


FIGURE 3.9.3–6

2M BY 8 & 9 DRAM IN SOJ & TSOP2



ROW, COLUMN, & REFRESH ADDRESS CONFIGURATIONS

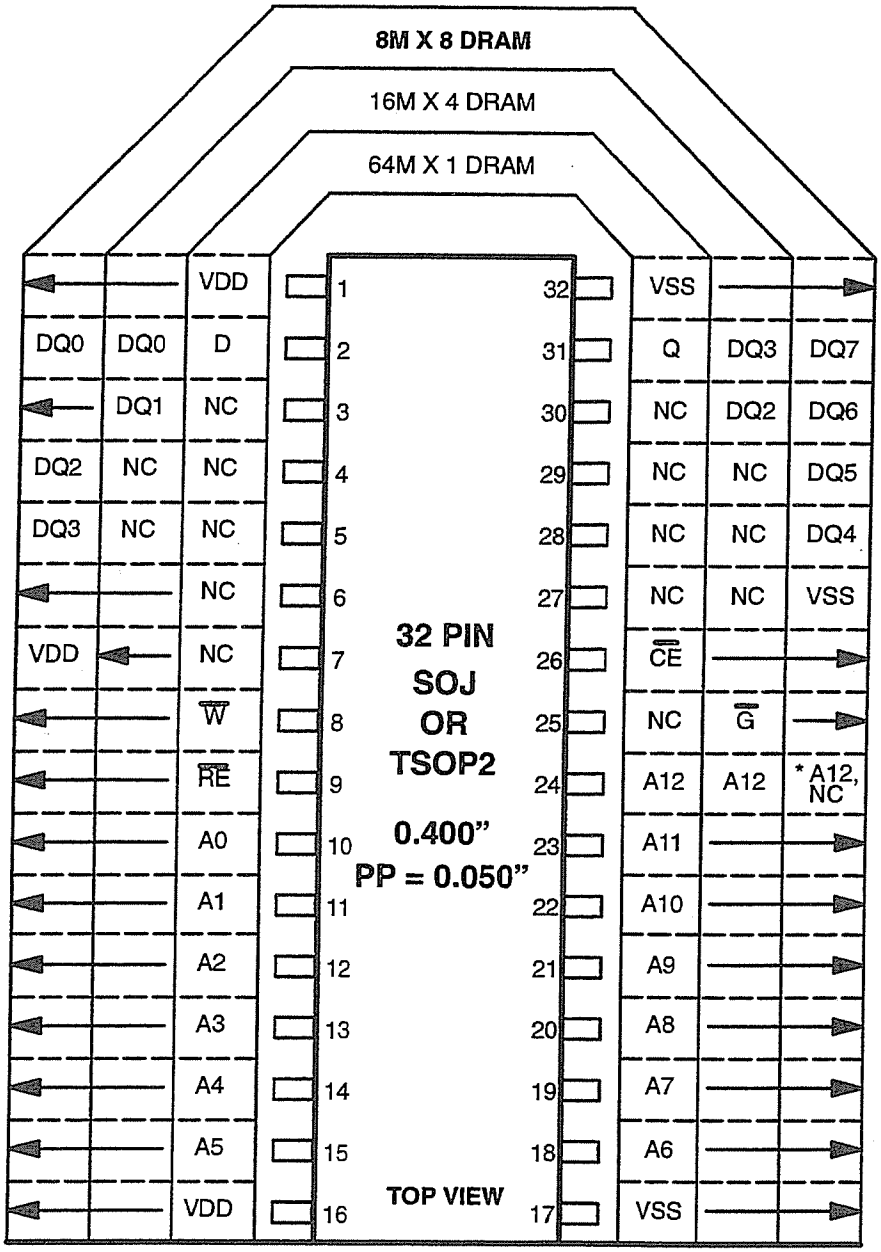
DEVICE CONFIGURATION REFRESH COUNT	64M X 1	16M X 4	8M X 8(9) 4K Refresh	8M X 8(9) 8K Refresh
ROW/REFRESH ADDRESSES	A0 Through A12	A0 Through A12	A0 Through A11	A0 Through A12
COLUMN ADDRESSES	A0 Through A12	A0 Through A10	A0 Through A10	A0 Through A9

This standard recognizes that some early deliveries of these parts may have to be in a 0.6" wide package

FIGURE 3.9.3-7

8M BY 8 & 9 DRAM IN SOJ & TSOP2

Release 4 a

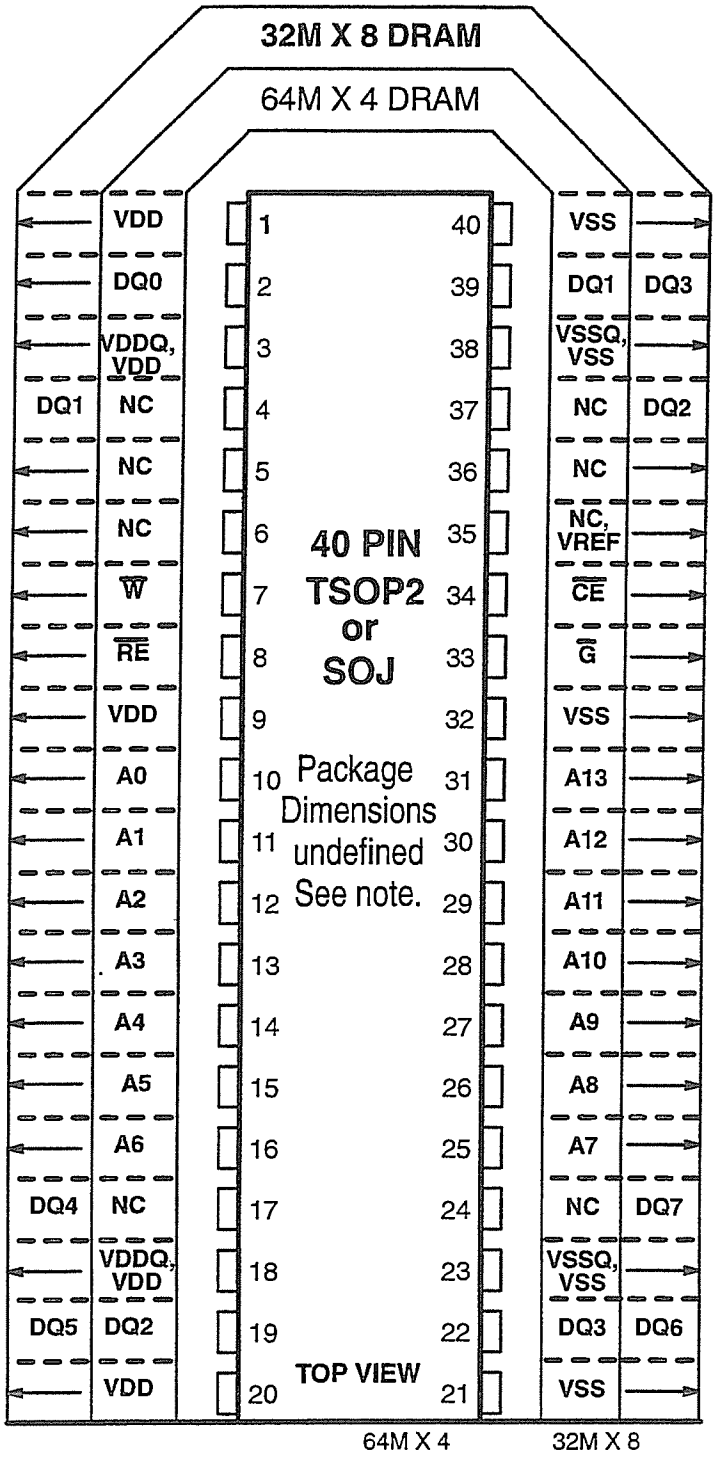


* Pin 24 is NC for the 16M X 4 & 8K X 8 parts with a 4K Refresh.

ROW & COLUMN, ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION	64M X 1	16M X 4	16M X 4	8M X 8	8M X 8
ROW COUNT		4K Rows	8K Rows	4K Rows	8K Rows
ROW ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12
COLUMN ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A10	A0 ⇒ A10	A0 ⇒ A9

FIGURE 3.9.3–8
8M BY 8 DRAM IN SOJ & TSOP2



NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. CBR refresh is the only standardized method of refreshing non–synchronous DRAMs with densities of 256Mb and higher.

3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms. (7.8 µs per row with 8K rows, 3.9 µs with 16K rows.

4. (NC, VREF) is VREF on devices that require an external voltage reference.

5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.

6. The VSSQ designator is used when the ground reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS)

	64M X 4	32M X 8
ROW ADDRESSES	A0 TO A13	A0 TO A13
COLUMN ADDRESSES	A0 TO A11	A0 TO A10

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.9.3–9
32M BY 8 DRAM PIN ROTATION IN TSOP2

3.9.4 Word Wide DRAM

3.9.4.1 – 64K BY 16 DRAM WITH 2 $\overline{W}$ IN SOJ & TSOP2

CAPACITY—64K WORDS OF 16 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
PACKAGE—40 PIN SOJ, 0.400" WIDE
—44/40 PIN TSOP2, 0.400" WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–1 (SOJ)
—Fig. 3.9.4–6 (TSOP2)

3.9.4.2 – 256K & 1M BY 16 & 18 WITH 2 $\overline{CE}$ OR 2 $\overline{W}$ DRAM IN SOJ & TSOP2

CAPACITY—256K, 1M WORDS OF 16 & 18 BITS,
The standard for the 2 $\overline{W}$ versions of the 1M part has been rescinded and removed from Figs. 3.9.4–4 & 3.9.4–5 in Release 5.
LOGIC FEATURES—MULTIPLEXED ADDRESS
—There are two versions of these parts, one with 2 $\overline{W}$ and the other with 2 $\overline{CE}$.
—The two clocks control the LOWER BYTE and UPPER BYTE data bits.
—The 1M part allows the option of the manufacturer to utilize either 1K or 4K refresh cycles
PACKAGE—256K in 40 PIN SOJ, 0.400" WIDE
—256K in 44/40 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH
—1M IN 42 PIN SOJ, 0.400" WIDE
—1M in 50/44 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–2 (256K SOJ)
—Fig. 3.9.4–3 (256K TSOP2)
—Fig. 3.9.4–4 (1M SOJ)
—Fig. 3.9.4–5 (1M TSOP2)

3.9.4.3 – 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ

CAPACITY—256K WORDS OF 16 BITS
LOGIC FEATURES—This part contains multiple logic functions that are similar to those used in MPDRAMS and that are keyed for VIDEO memory applications. All devices meeting this standard must contain all functions which must be implemented as defined in the TRUTH TABLE.
PACKAGE—40 PIN DIP, 0.400" WIDE, 0.100" PIN PITCH
—40 PIN SOJ, 0.400" WIDE, 0.050" PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–7A
FUNCTION TRUTH TABLE—Fig. 3.9.4–7B

3.9.4.4 – 2M BY 16 & 4M BY 16 & 18 DRAM IN TSOP2

CAPACITY—2M & 4M WORDS OF 16 or 4M WORDS OF18 BITS
LOGIC FEATURES—MULTIPLEXED ADDRESS
—These parts utilizes 4K or 8K refresh cycles
PACKAGE—50 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH, X16 parts only
PACKAGE—54 PIN TSOP2, 0.500" WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–8

3.9.4.5 – 128K & 256K BY 16 BURST DRAM WITH 2 CAS IN SOJ, TSOP2, OR ZIP

CAPACITY—128K OR 256K WORDS OF 16 BITS
LOGIC FEATURES—MULTIPLEXED ADDRESS
—These parts have BURST data out capability
PACKAGE—40 PIN SOJ, 10.16 mm WIDE, 1.27 mm PIN PITCH
PACKAGE—44/40 PIN TSOP2, 10.16 mm WIDE, 0.8 mm PIN PITCH
PACKAGE—40 PIN ZIP, 1.27 mm PIN PITCH (256K only)
PIN ASSIGNMENT—SOJ, Fig. 3.9.4–9
PIN ASSIGNMENT—TSOP2, Fig. 3.9.4–10
PIN ASSIGNMENT—ZIP, Fig. 3.9.4–11, (256K ONLY)

3.9.4.6 – 16M X 16 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 16M WORDS OF 16 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.9.4–12
NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

3.9.4.7 – 128K AND 256K BY 32 DRAM WITH 4 $\overline{CE}$ IN SSOP

CAPACITY—128K OR 256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—The part, has 4 $\overline{CE}$, one controlling each group of 8 data bits.
PACKAGE— 64 PIN SSOP, 0.525" WIDE, PP = 0.8 mm
PIN ASSIGNMENT—Fig. 3.9.4–13

3.9.4.8 – 512K & 2M BY 32 & 36 DRAM WITH 4 $\overline{CE}$ IN SOJ & TSOP2

CAPACITY—512K, 2M WORDS OF 32 & 36 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
—The part, has 4 $\overline{CE}$, one controlling each group of 8 or 9 data bits.
—The standard allows the option of the manufacturer to utilize either 1K or 4K refresh cycles
PACKAGE—70 PIN TSOP2, 10.16 mm WIDE, 0.8 mm PP
—70 PIN TSOP2, 10.16 mm WIDE, 0.65 mm PP, 512K only.
—70 PIN SOJ, 10.16 mm WIDE, 0.8 mm PP
PIN ASSIGNMENT—Fig. 3.9.4–14

3.9.4.9 – 8M X 32 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 8M WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.9.4–15
NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

3.9.4.10 – 2M X 32 DRAM IN TSOP2

CAPACITY— 8M WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—86 PIN TSOP2, 10.16 mm WIDE, 0.5 mm PP
PIN ASSIGNMENT—Fig. 3.9.4–16

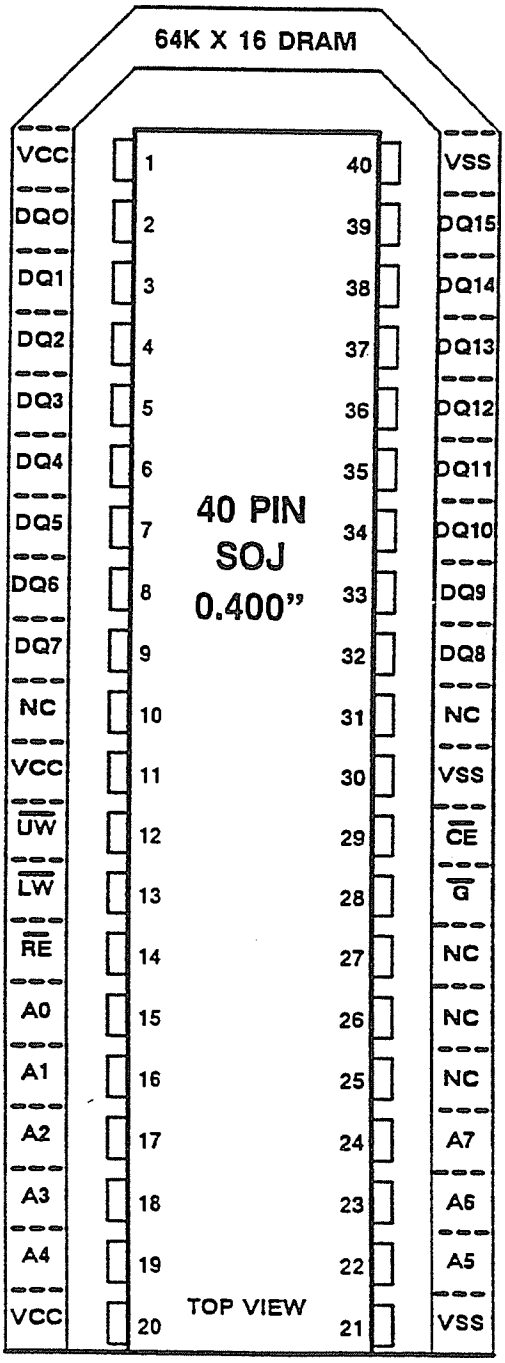


FIGURE 3.9.4-1
64K BY 16 DRAM IN SOJ

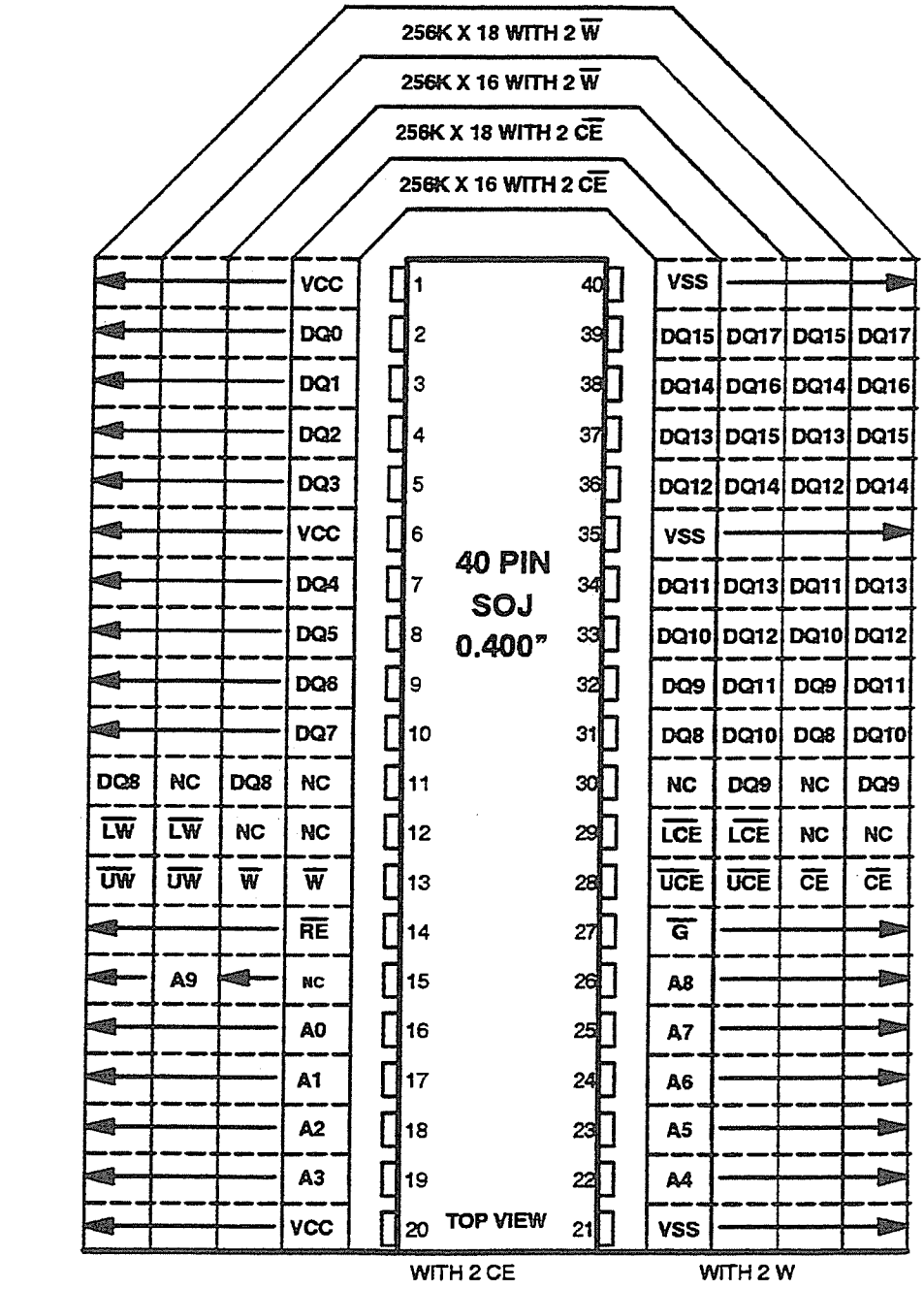
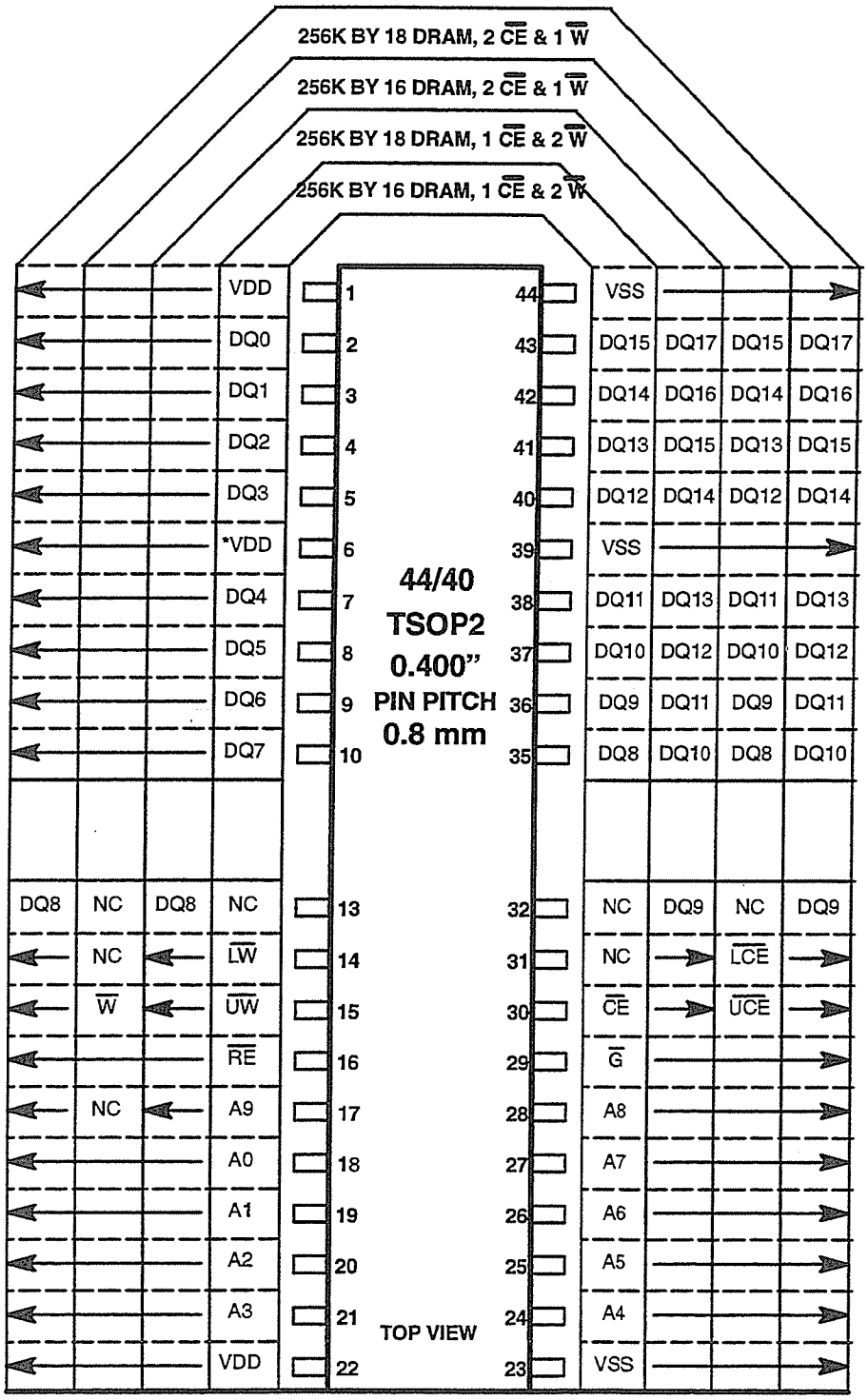


FIGURE 3.9.4–2
256K BY 16 & 18 DRAM WITH 2 $\overline{CE}$ & 2 $\overline{W}$



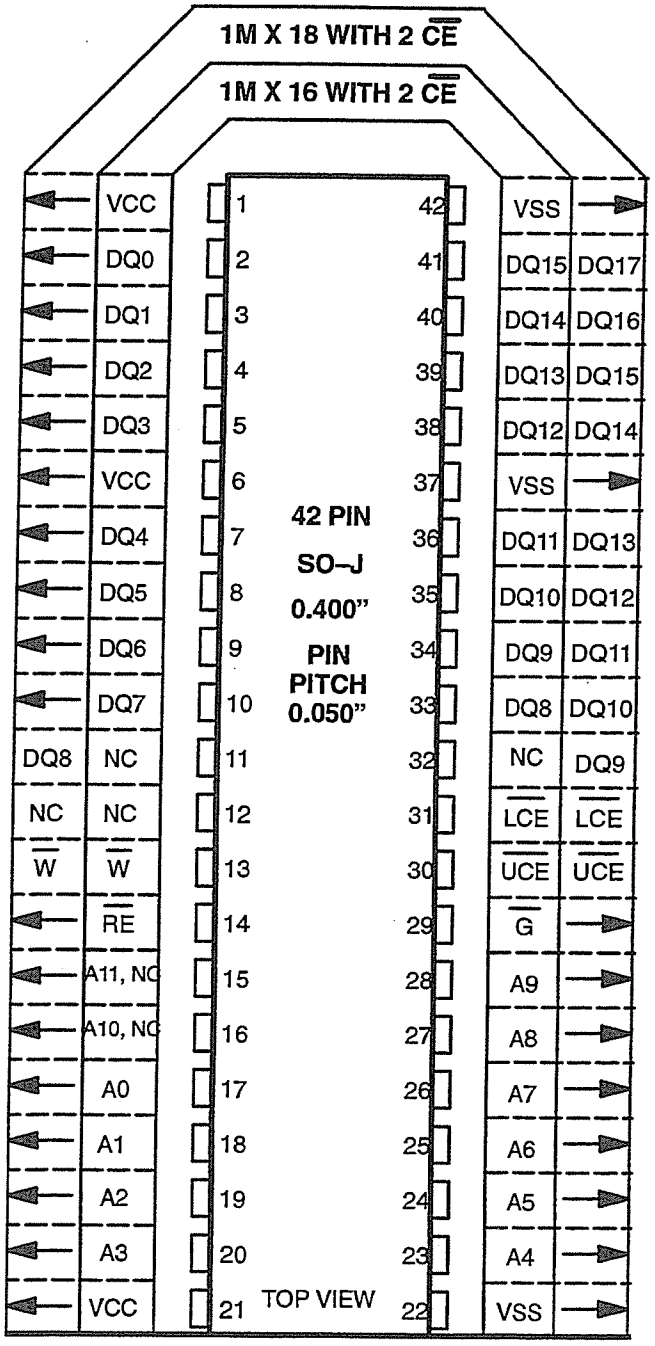
CONFIGURATION	1 $\overline{CE}$, 2 $\overline{W}$	2 $\overline{CE}$, 1 $\overline{W}$
REFRESH COUNT	1024 Cycles	512 Cycles
REFRESH ADDRESS	A0 TO A9	A0 TO A8
ROW ADDRESS	A0 TO A9	A0 TO A8
COLUMN ADDRESS	A0 TO A7	A0 TO A8

The JEDEC Std. No 30 designator for the TSOP2 package is PDSO–G

* NOTE: In the first release of this standard, Pin 6 was a VSS connection. This was in error and this release changes Pin 6 to VDD.

FIGURE 3.9.4–3

256K BY 16 & 18 DRAM WITH 2 $\overline{W}$ OR 2 $\overline{CE}$ IN TSOP2

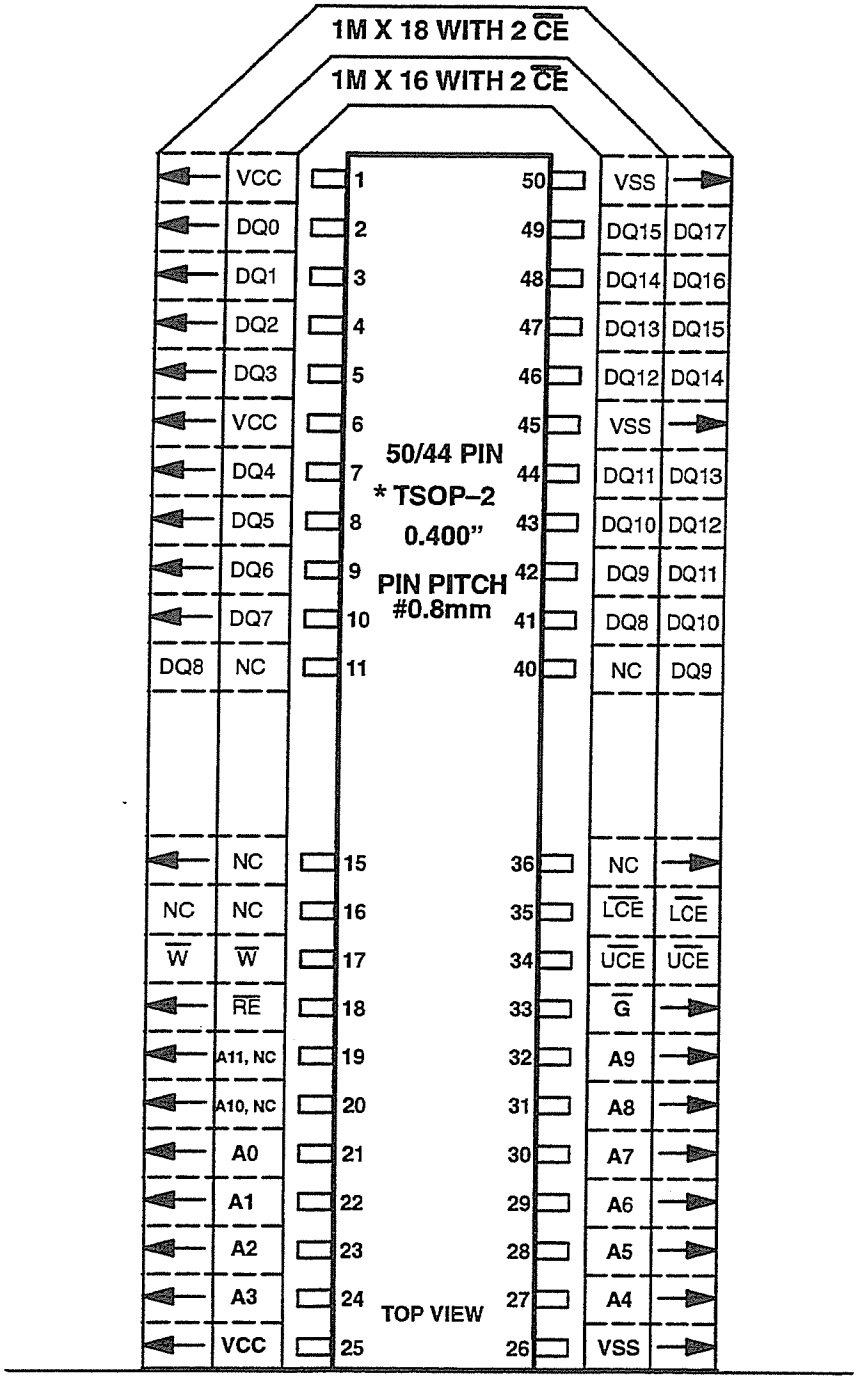


NOTE: The initial publication of this standard in Release 3 contained two devices with 2 $\overline{W}$ inputs. The standard for these devices has been re-scinded.

	1K REFRESH	4K REFRESH
ROW/REFRESH ADDRESSES	A0 THROUGH A9	A0 THROUGH A11
COLUMN ADDRESSES	A0 THROUGH A9	A0 THROUGH A7

FIGURE 3.9.4–4
1M BY 16 & 18 DRAM WITH 2 $\overline{CE}$ IN SOJ

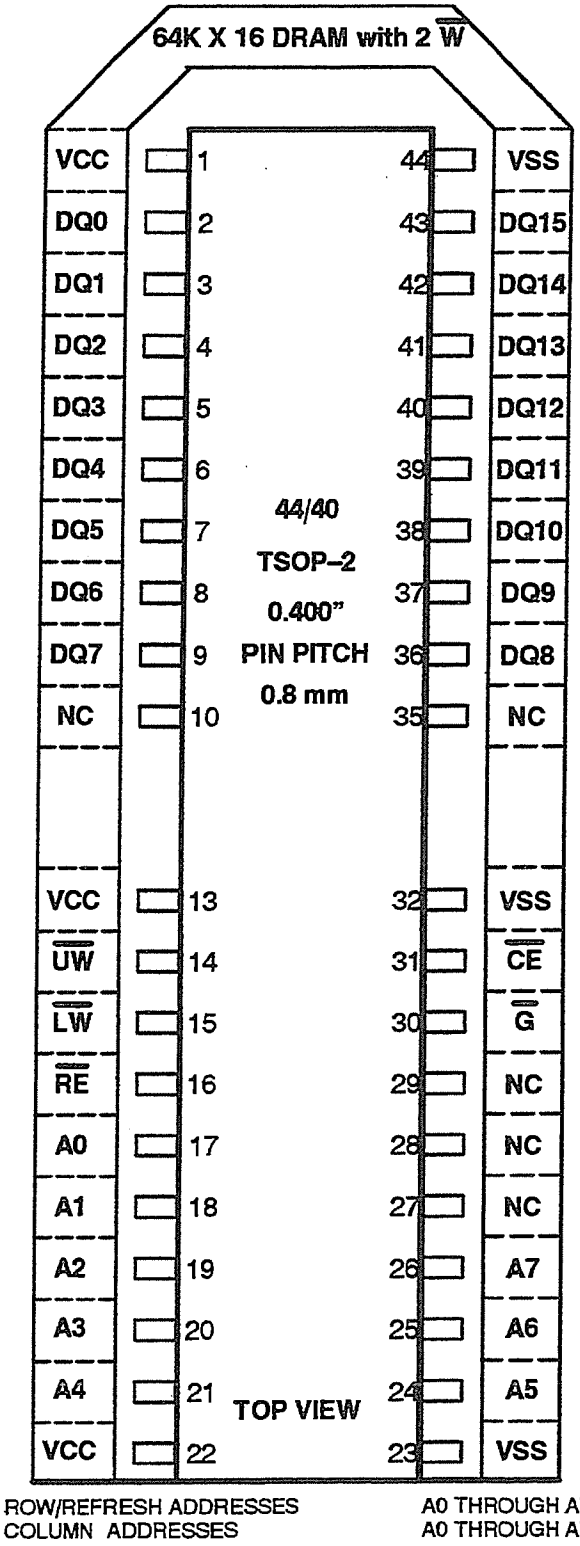
Release 5



Note: The JEDEC Standard 30 term for the TSOP–2 package is PDSO–G

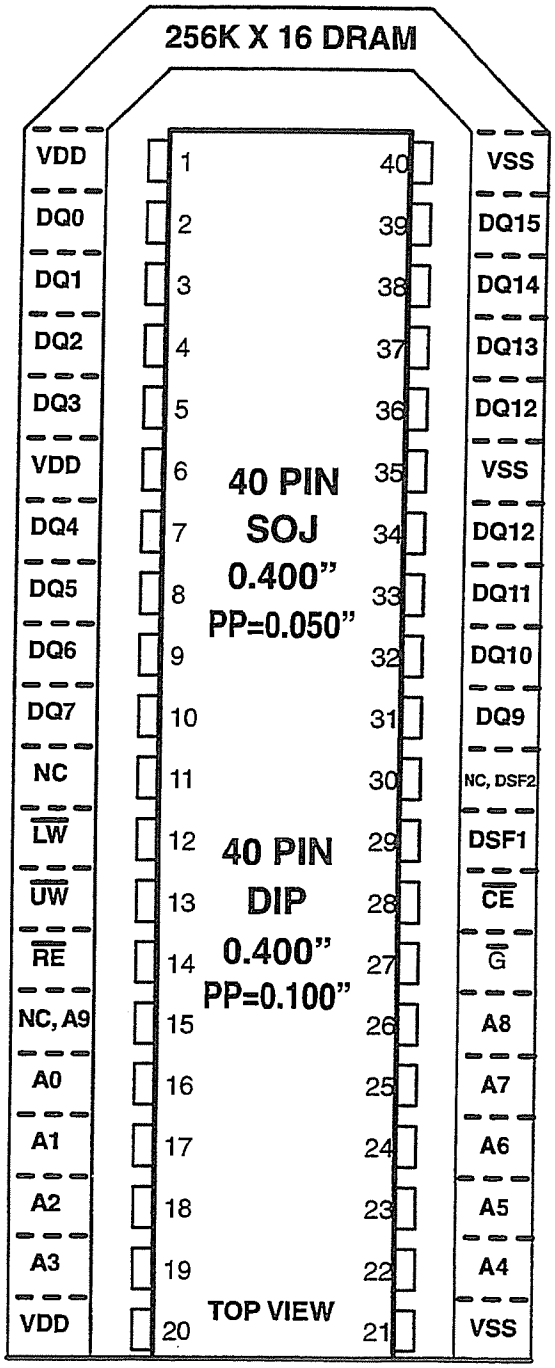
FIGURE 3.9.4–5

1M BY 16 & 18 DRAM WITH 2 $\overline{CE}$ IN TSOP2



* Note: The JEDEC Standard 30 term for the TSOP–2 package is PDSO–G

FIGURE 3.9.4–6
64K BY 16 DRAM WITH 2 W IN TSOP–2



	512 REFRESH	1K REFRESH
ROW/REFRESH ADDRESSES	A0 TO A8	A0 TO A9
COLUMN ADDRESSES	A0 TO A8	A0 TO A7

FIGURE 3.9.4–7 A

256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ

MANDATORY TRUTH TABLE FOR 256K BY 16 DRAM with EXTENDED FUNCTIONS

Mnem.	Function	Valid at RE					Valid at CE
		CE	G	W	DSF(1)	*DSF2	DSF(1)
RW	READ/WRITE	1	1	1	0	0	0
BW	BLOCK WRITE	1	1	1	0	0	1
LMR	LOAD MASK REGISTER	1	1	1	1	0	0
LCR	LOAD COLOR REGISTER	1	1	1	1	0	1
RWM	WRITE, MASKED	1	1	0	0	0	0
BWM	BLOCK WRITE, MASKED	1	1	0	0	0	1
CBR	CBR REFRESH (1)	0	X	1	0	0	X
CBRN	CBR REFRESH (2)	0	X	1	1	0	X
FWT	FLASH WRITE	1	1	0	1	0	X

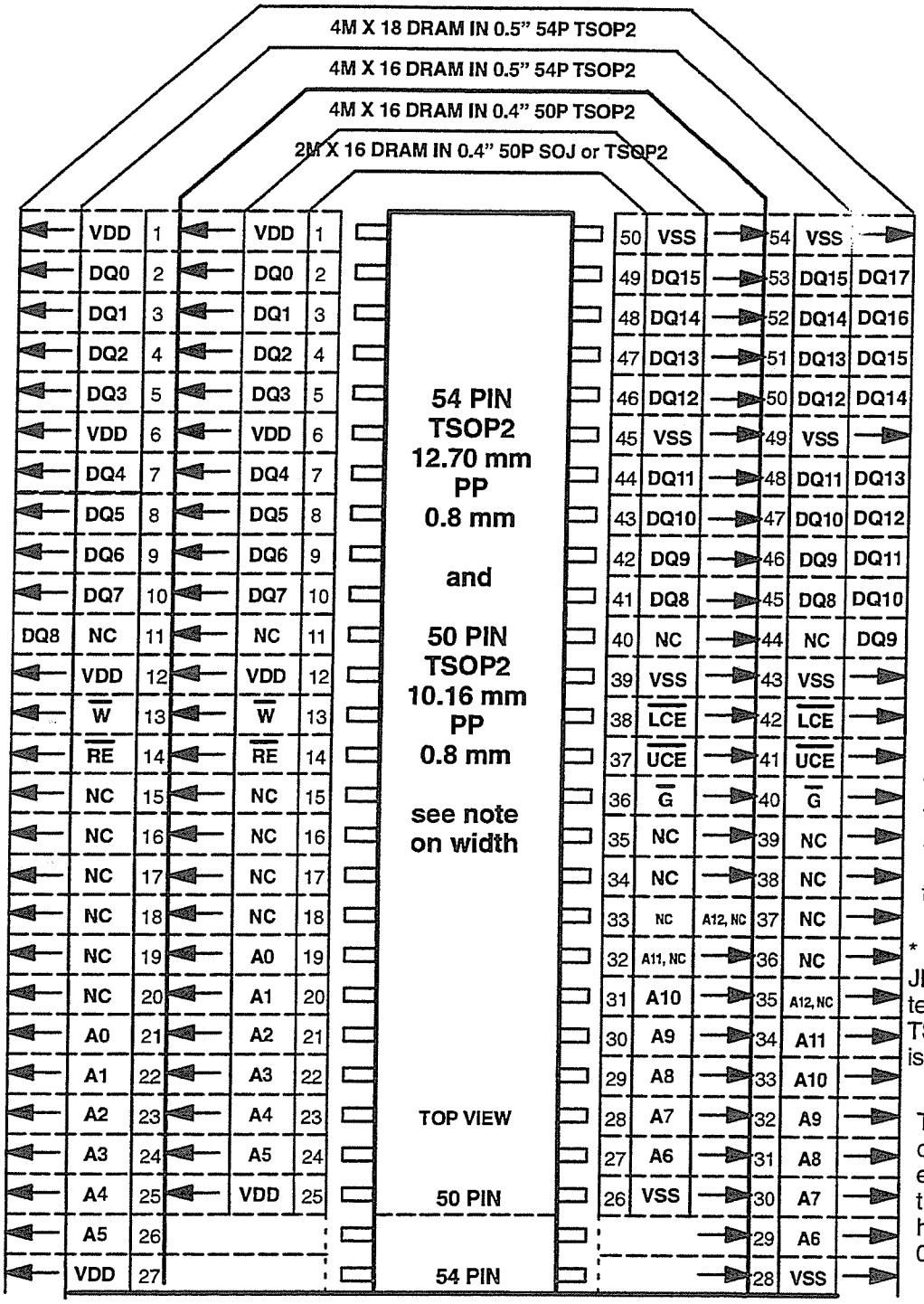
* IF DSF2 IS PRESENT

CBR(1) – All optional modes reset

CBR(2) – Any optional modes remain active

FIGURE 3.9.4–7 B

256K BY 16 DRAM MANDATORY EXTENDED FUNCTION TRUTH TABLE



* NOTES:
For 54P parts, Pin 35 is A12 for 8K rows and NC for 4K rows.

For 50P 4M parts, Pin 33 is A12 for 8K rows and NC for 4K rows. Pin 32 is NC for devices with 11 row & 11 columns and A11 for other Refresh/Address options..

For 50P 2M parts, Pin 32 is A11 for devices with 4K rows and NC for devices with 2K rows.

The use of CBR for Refresh is strongly recommended for these devices.

* NOTE: The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

This standard recognizes that some early deliveries of the 54P parts may have to be in a 0.6"wide package

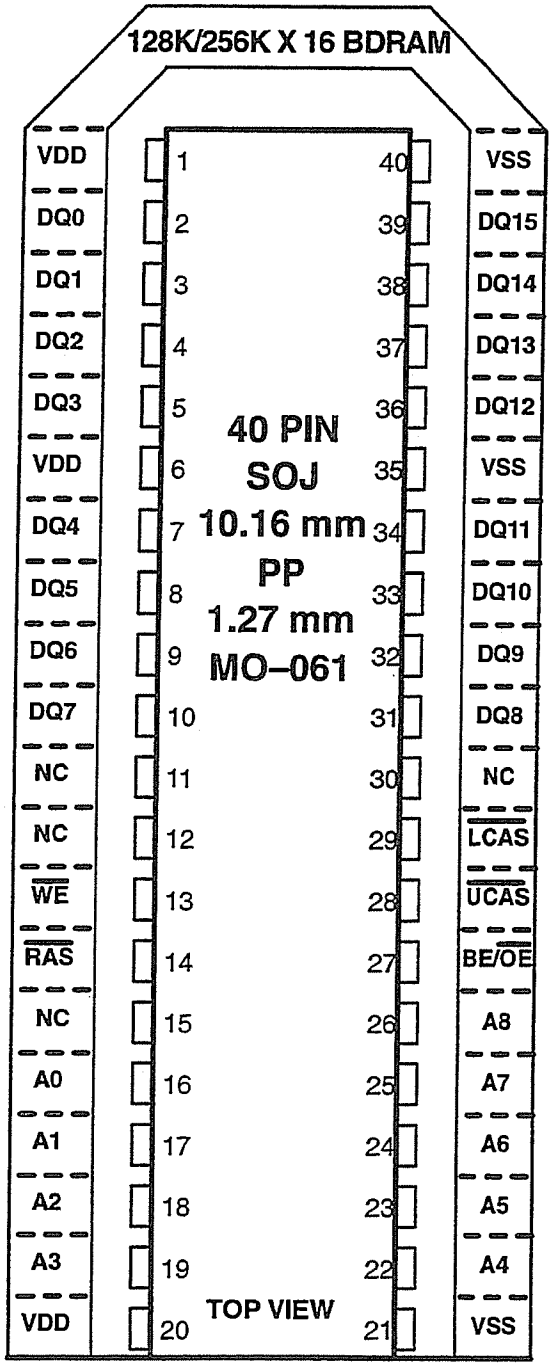
54 P ADDRESS CONFIGURATION

4M X 16/18	4K ROWS	8K ROWS
ROW ADDRESSES	A0 → A11	A0 → A12
COLUMN ADDRESSES	A0 → A9	A0 → A8

50 P ADDRESS CONFIGURATION

2M X 16	2K ROWS	4K ROWS	8K ROWS
ROW ADDRESS	A0 ⇒ A10	A0 ⇒ A11	
COLUMN ADDRESS	A0 ⇒ A9	A0 ⇒ A8	
4M X 16	2K ROWS	4K ROWS	8K ROWS
ROW ADDRESS	A0 ⇒ A10	A0 ⇒ A11	A0 ⇒ A12
COLUMN ADDRESS	A0 ⇒ A10	A0 ⇒ A9	A0 ⇒ A8

FIGURE 3.9.4–8
2M BY 16 & 4M BY 16 & 18 DRAM IN TSOP–2

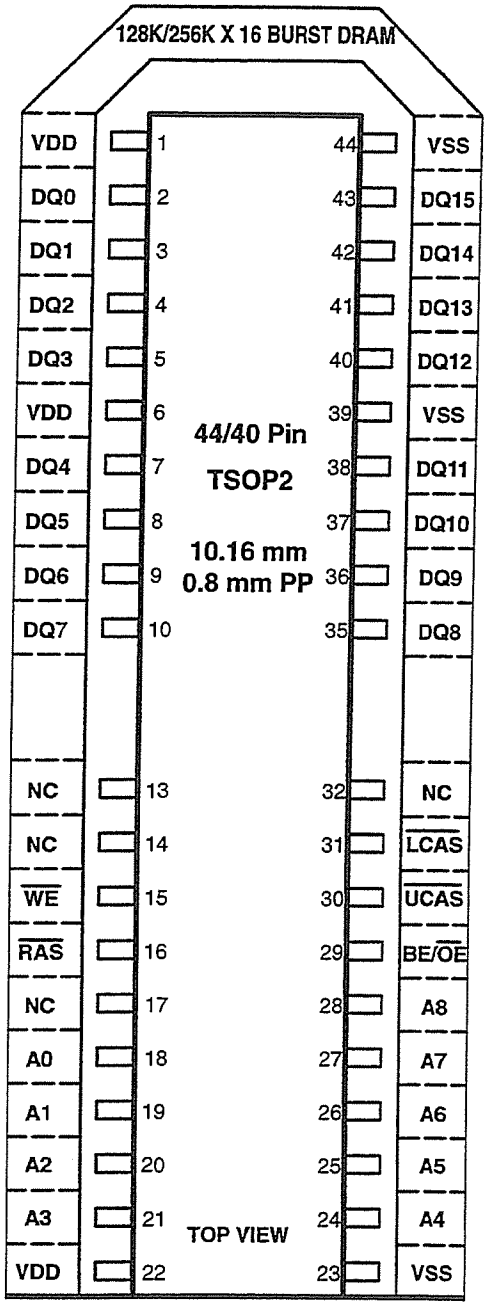


*NOTE: The JESD30 approved term for this package is PDSO–G

ADDRESS CONFIGURATION	128K X 16	256K X 16
ROW ADDRESSES	A0 ⇒ A8	A0 ⇒ A8
COLUMN ADDRESSES	A0 ⇒ A7	A0 ⇒ A8
REFRESH COUNT/PERIOD	512 Cycles/8 ms	512 Cycles/8 ms

FIGURE 3.9.4–9
128K & 256K BY 16 BURST DRAM WITH 2 $\overline{\text{CAS}}$ IN SOJ

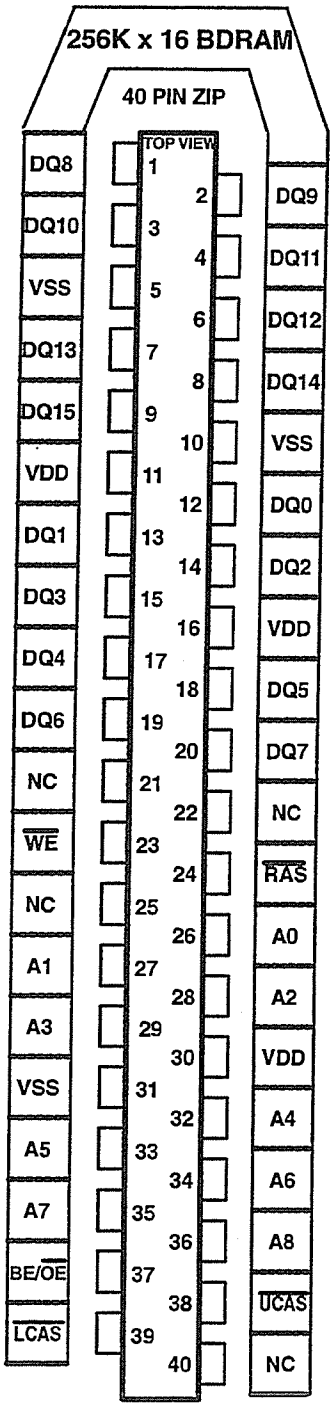
Release 6



*NOTE: The JESD30 approved term for this package is PDSO–G

CONFIGURATION	128K X 16	256K X 16
ROW ADDRESSES	A0 ⇒ A8	A0 ⇒ A8
COLUMN ADDRESS	A0 ⇒ A7	A0 ⇒ A8
REFRESH COUNT/PERIOD	512/8 ms	512/8 ms

FIGURE 3.9.4–10
128K & 256K BY 16 BURST DRAM WITH 2 $\overline{\text{CAS}}$ IN TSOP2



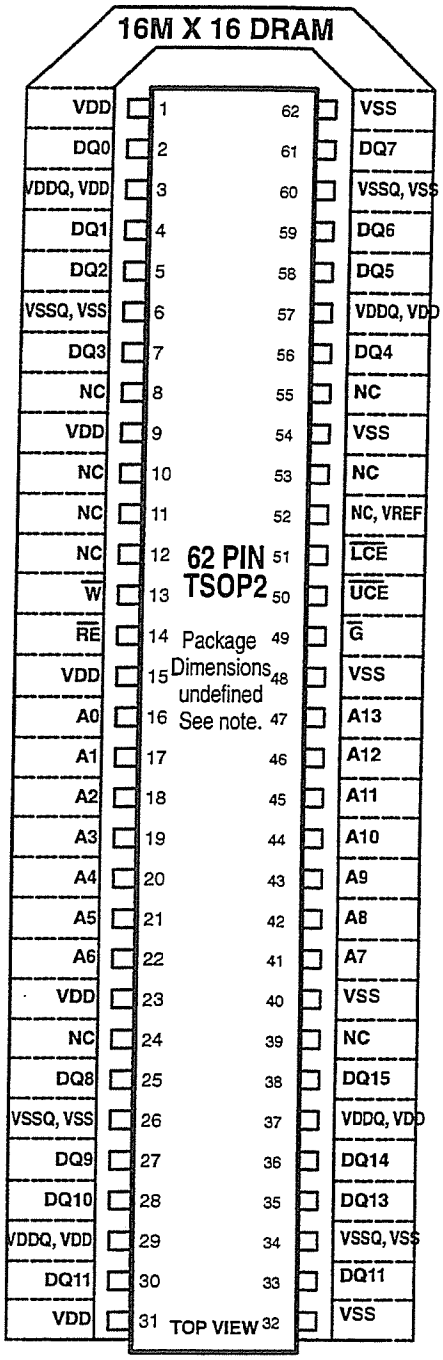
40 Pin ZIP
1206.5 mm
1.27 mm PP

*NOTE: The JESD30 approved term for this package is PSIP–P

ADDRESS CONFIGURATION

ROW ADDRESSES	A0 ⇒ A8
COLUMN ADDRESSES	A0 ⇒ A8
REFRESH COUNT/PERIOD	512 Cycles/8 ms

FIGURE 3.9.4–11
256K BY 16 BURST DRAM WITH 2 $\overline{\text{CAS}}$ IN ZIP



Configuration	16M X 16
ROW ADDRESS	A0–A13
COLUMN ADDRESS	A0–A9

NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. CBR refresh is the only standardized method of refreshing non–synchronous DRAMs with densities of 256Mb and higher.

3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms. (7.8 µs per row with 8K rows, 3.9 µs with 16K rows.

4. (NC, VREF) is VREF on devices that require an external voltage reference.

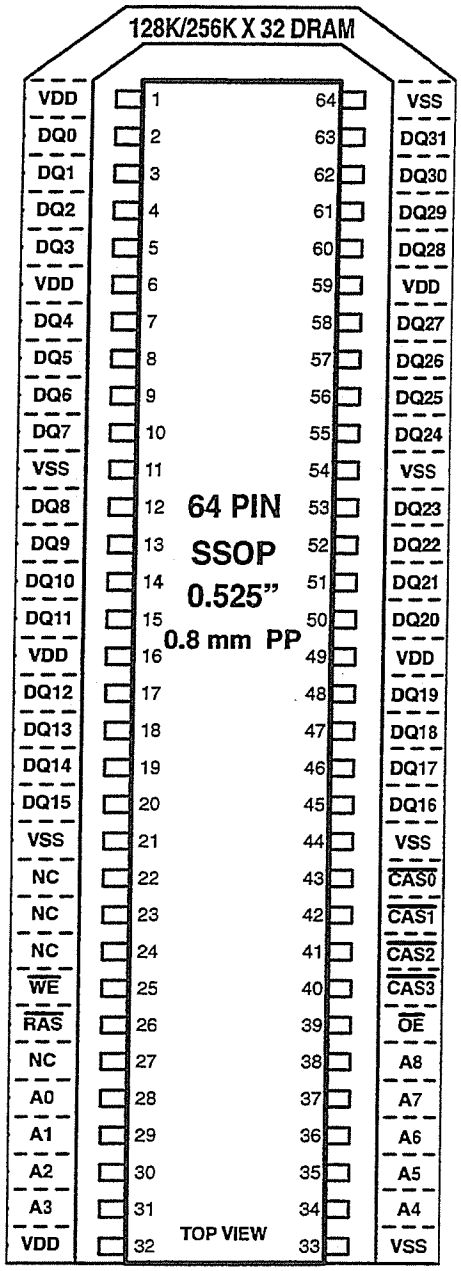
5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.

6. The VSSQ designator is used when the ground reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS)

* NOTE: The JEDEC Std. 0 term for the TSOP–2 package is PDSO–G.

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.9.4–12
16M BY 16 DRAM PIN ROTATION IN TSOP2

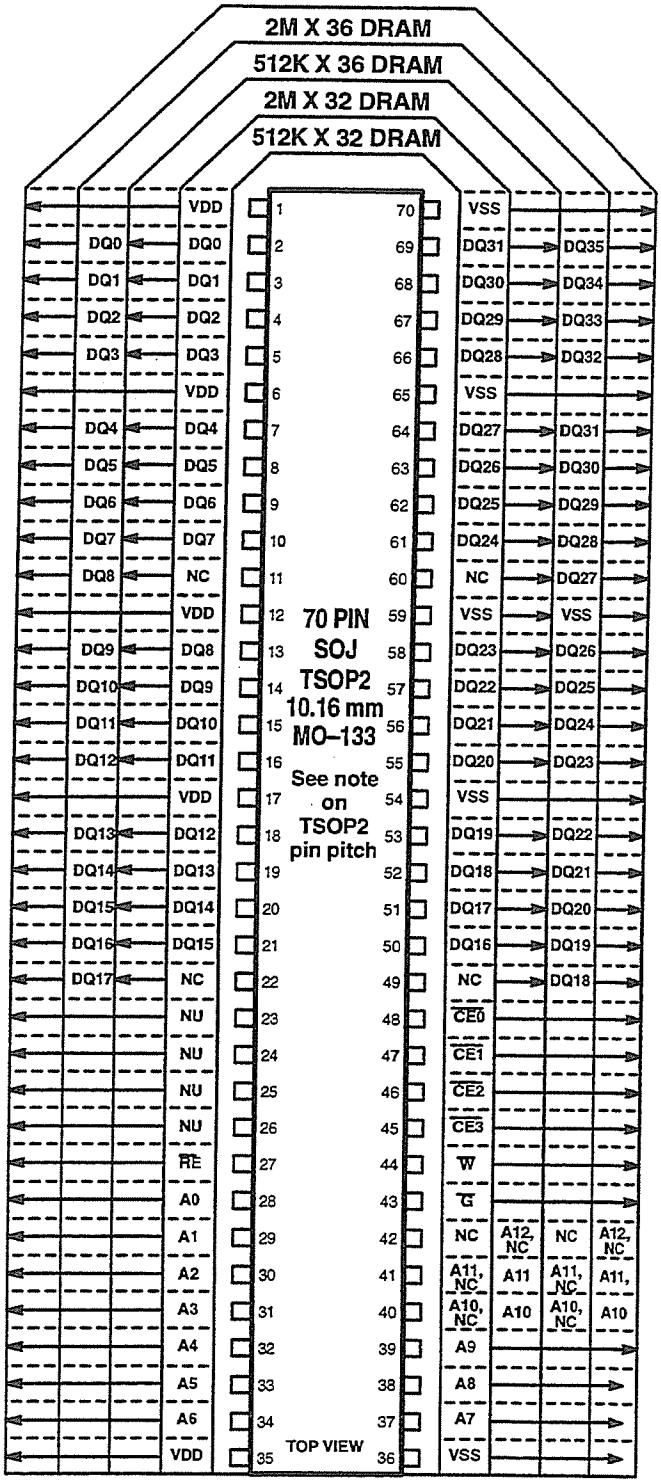


*NOTE: The JESD30 approved term for this package is PDSO–G

ADDRESS STRUCTURE	128K X 32	256K X 32
ROW Address	A0 ⇒A8	A0 ⇒A8
Column Address	A0 ⇒A7	A0 ⇒A8
Refresh Cycles/Period	512 Cycles/8 ms	512 Cycles/8 ms

FIGURE 3.9.4–13
128K & 256K BY 32 DRAM WITH 4 $\overline{\text{CAS}}$ IN SSOP

Release 6

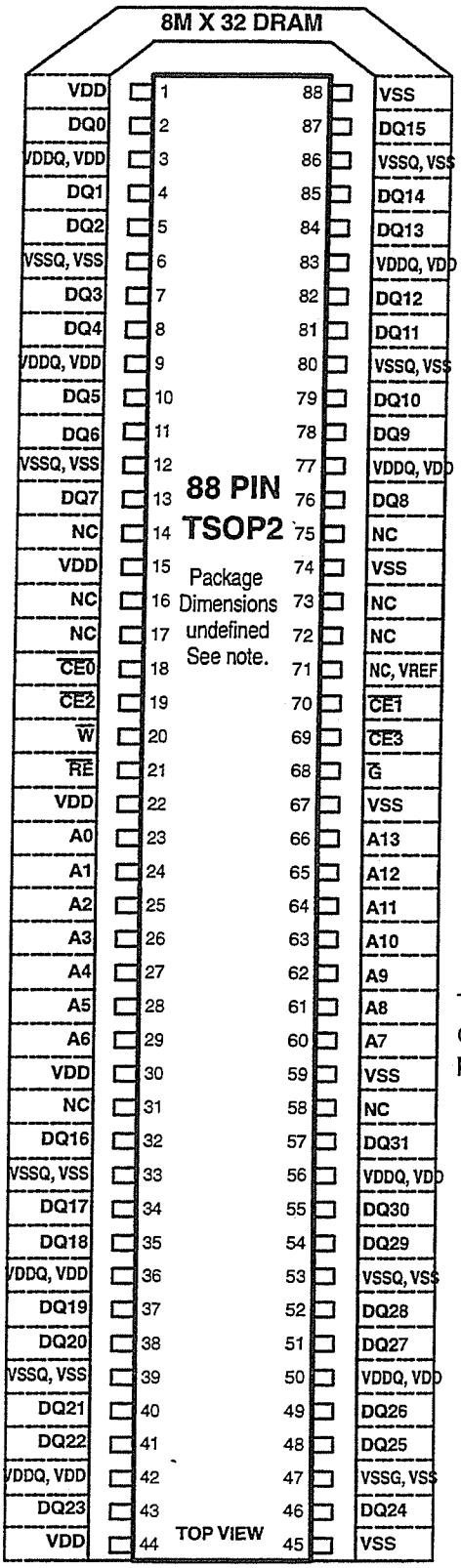


The 512K parts are approved with a TSOP2 package that has a pin pitch of either 0.8 mm or 0.65 mm . The 2M parts are approved with 0.8 mm only.

* NOTE: The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

CAPACITY	512K		2M	
ADDRESS FIELD	**1K REFRESH**	**4K REFRESH**	**4K REFRESH**	**8K REFRESH**
ROW ADDRESS	A0–A9	A0–A11	A0–A11	A0–A12
COLUMN ADDRESS	A0–A8	A0–A6	A0–A8	A0–A7

FIGURE 3.9.4–14
512K & 2M BY 32 & 36 DRAM IN SOJ & TSOP2



NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. CBR refresh is the only standardized method of refreshing non–synchronous DRAMs with densities of 256Mb and higher.

3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms. (7.8 µs per row with 8K rows, 3.9 µs with 16K rows.

4. (NC, VREF) is VREF on devices that require an external voltage reference.

5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.

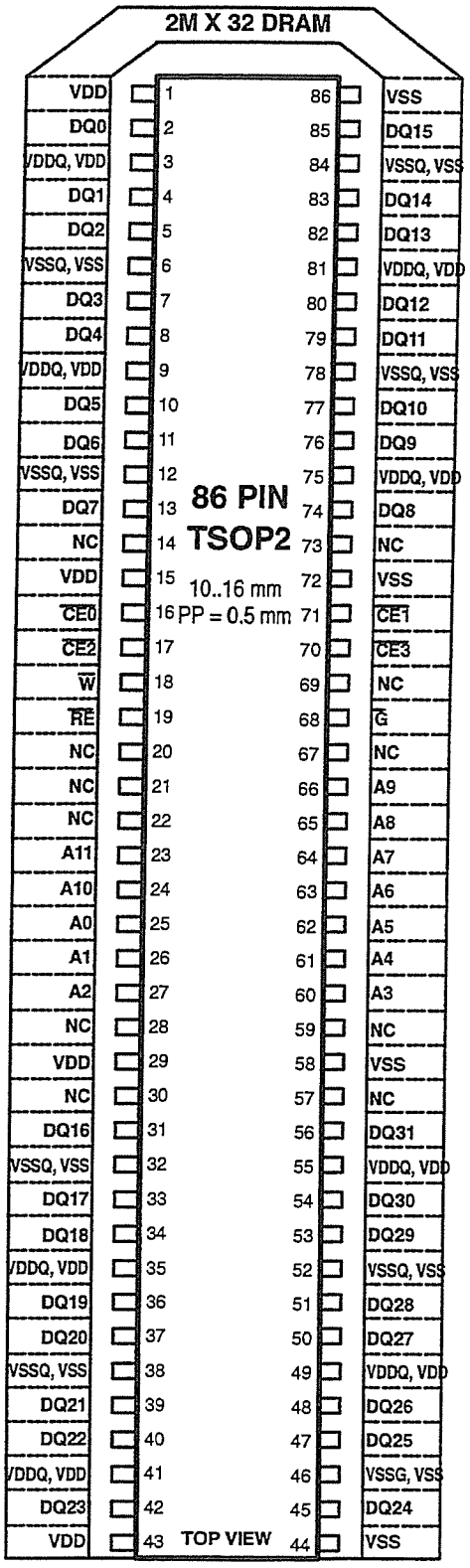
6. The VSSQ designator is used when the ground reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS)

The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO–G

Configuration	16M X 16
ROW ADDRESS	A0–A12
COLUMN ADDRESS	A0–A8

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.9.4–15
8M BY 32 DRAM PIN ROTATION IN TSOP2



NOTES
1. The standard refresh period is 64 ms.
2. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally DC isolated from the VDD power supply pins.
3. The VSSQ designator is used when the ground reference pins

The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO–G

Configuration	2M X 32
ROW COUNT	4K Rows
ROW ADDRESS	A0 ⇒ A11
COLUMN ADDRESS	A0 ⇒ A8

FIGURE 3.9.4–16
2M BY 32 DRAM IN TSOP2

3.9.5 DRAM Optional Features

3.9.5.1 – OPTIONAL OPERATIONAL MODES AND CYCLES FOR DRAM

The definitions for serial data access, bit write, and refresh control included in Release 1 of this standard have been replaced by the more general definitions of Optional Operational Modes and Cycles beginning on page 3.9.5–11

3.9.5.2 – 1M DRAM BUILT IN TEST FUNCTION

An approved option for 1M DRAM (1M X 1 or 256K X 4) is the inclusion of a built in manufacturer defined "Test Mode". This mode is enabled using a dedicated pin which is optional NC or TF. When the optional mode is implemented, the manufacturer should include notes on his data sheet as follows:

(A) Normal operation requires the "TF" pin be connected to a VSS or logic low level or left unconnected.

(B) When the "TF" pin is connected to the manufacturer defined positive voltage, the internal test mode will be actuated. Contact the manufacturer for specific operational details of the Test Mode.

3.9.5.3 – ON–CHIP REFRESH CONTROL FOR X8 DRAM

This standard describes an optional feature that is applicable to the non–address multiplexed byte wide dynamic RAMs described in this publication. The standard establishes the clock timing sequence needed to invoke an on–chip refresh feature.

3.9.5.4 – $\overline{G}$ BEFORE $\overline{E}$ REFRESH

If G is low when E falls, a refresh cycle is executed. During this type of refresh cycle, an internal counter/register provides the refresh address and the external address is ignored

3.9.5.5 – DRAM SPECIAL TEST AND OPERATIONAL MODES

This standard defines a scheme for controlling a series of special operational modes for address multiplexed DRAM. The standard defines the logic interface required to enter, control and exit from the special modes. In addition, it defines a basic test mode plus a series of other special test and operational modes. The details of this standard are given on pages 3.9.5–7 through 3.9.5–10.

3.9.5.6 – NON–MULTIPLEXED DRAM OPERATION

This standard defines multiple aspects of the address and clock relationships for DRAMs that have a non–multiplexed address architecture. It also defines the relationships between the address bits of multiplexed and non–multiplexed devices. The details of the standard are given on page 3.9.5–13

3.9.5.7 – DRAM EXTENDED DATA OUT

This standard defines the output characteristics of Extended Data Out (EDO) feature for DRAMs. Any part encorporating "EDO" must satisfy all of the following criteria to conform to the Standard. The details of the EDO standard are given on P 3.9.5–14

3.9.5.8 – 256M DRAM TEST MODE DATA AND ADDRESS COMPRESSION

This standard defines the algorithms for data and address compression when 256M DRAMs are operated in the built in special test mode. The detaild of the Compression standard are given on P 3.9.5–15

3.9.5.9 – PIPELINED NIBBLE MODE DEFINITION

This standard defines the output characteristics of the Pipelined Nibble Mode feature for DRAMs. Any part encorporating Pipelined Nibble Mode must satisfy all of the following criteria to conform to the Standard. The details of the standard are given on P 3.9.5–16

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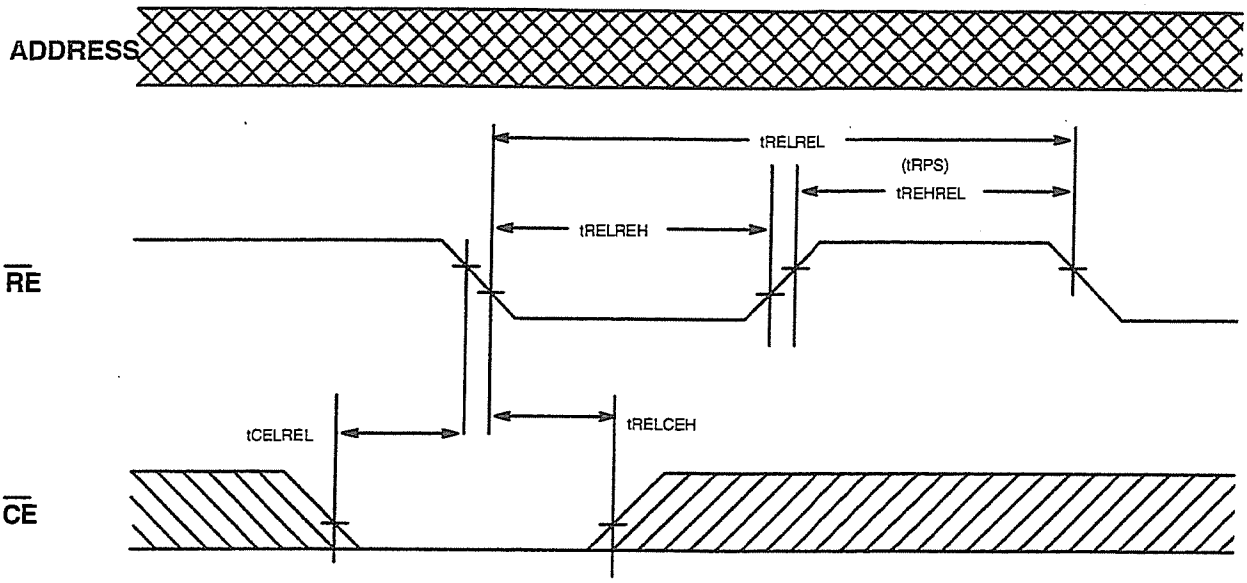
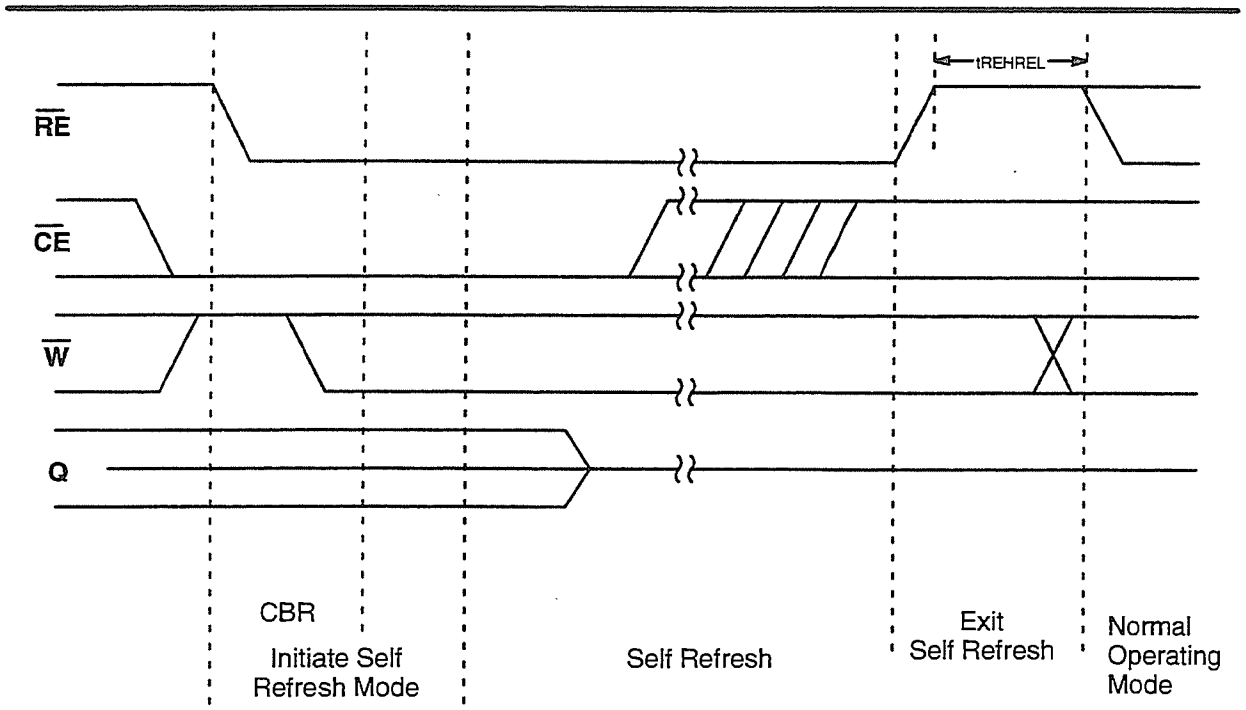


FIGURE 3.9.5–1A
DRAM ON CHIP REFRESH TIMING



Data Out may be either Tristate or Active depending on the state of CE\ when the cycle is entered.

FIGURE 3.9.5–1 B
DRAM SELF REFRESH MODE TIMING

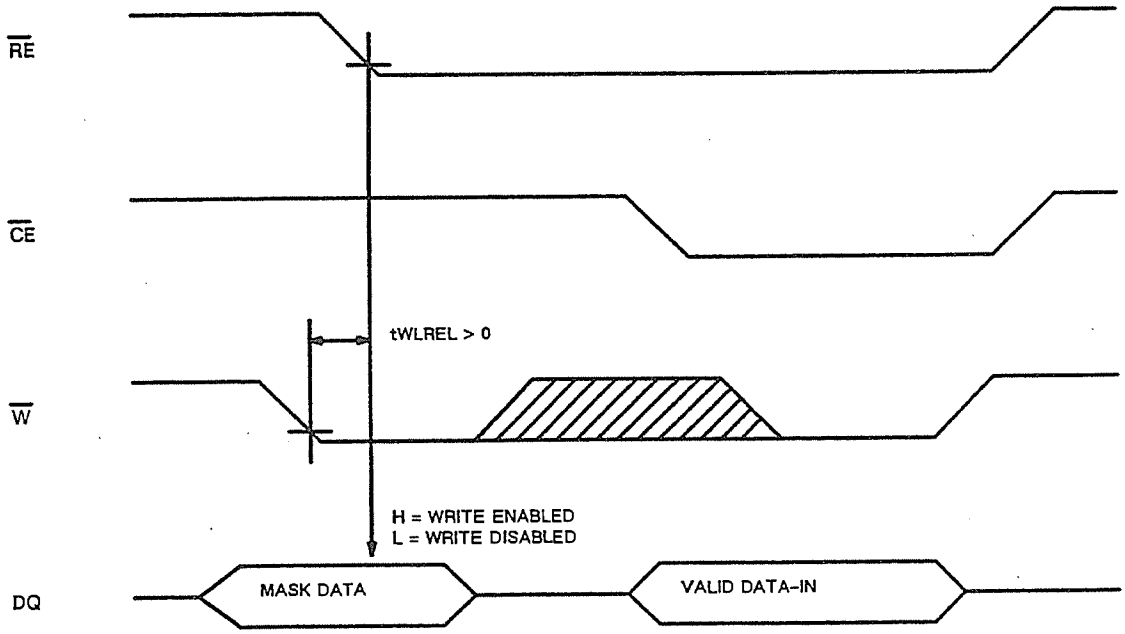


FIGURE 3.9.5-2
DRAM BIT WRITE TIMING

DRAM SPECIAL TEST AND OPERATIONAL MODES

1 PURPOSE

This standard defines a scheme for controlling a series of special modes for address multiplexed DRAM. The standard defines the logic interface required to enter, control, and exit from the special modes. In addition, it defines a basic special test mode plus a series of other special test and operational modes.

2 SPECIAL MODE INITIATE

The special modes will be initiated by the W\ AND CE\ BEFORE RE\ clock sequence shown in Fig.A2–1. This sequence is called "Write Enable and CAS before RAS" or "WCBR". When this clock sequence is generated, the state of the 8 low order Row Address bits (address key) will define the mode to be selected (see Par. 4) if optional modes are implemented. This mode will be latched and remain in effect until a special release cycle is generated or a new initiate cycle defining some other special mode is generated.

Following the initiate cycle, all subsequent cycles except refresh cycles (see pars. 3 & 5), will be operating cycles as allowed by the special mode selected.

3 MODE EXIT

A special mode will be cleared and the memory device returned to its normal operational state by the application of any normal REFRESH cycle, "RAS only refresh", (ROR) or "CAS before RAS refresh" (CBRR).

4 MODE SELECTION

Devices meeting this standard must have an implementation of the BASIC TEST MODE (see par 6) but also may contain other modes as options. When optional special modes are implemented, they will be selected by the state of the 8 least significant ROW Address bits at the time that INITIATE clock sequence is provided. The address space for the mode selection is defined as follows.

The special modes as selected by the 8–bit Address Key will be partitioned into four (4) subsets as follows:

1 – JEDEC Registered Modes

2 – Reserved for future expansion

3 – Vendor Specific Modes

4 – Customer Specific Modes

4.1 MODE PARTITIONING

These modes and their partitioning will be as diagrammed in Table A2–2. Additional address bits above A7 can be used to select additional pages of MODE definition (see par.4.3). Mode subgroups 1 and 2 will be further subdivided into "Test" and "Operational" modes as follows:

TEST MODES are those that implement some special test or measurement function or algorithm designed to enhance the ability of the Vendor or User to determine the integrity of, or to characterize, the part.

OPERATIONAL MODES are those that alter the operational characteristics of the part but do not interfere with its function as a storage device and are intended to be used in system operation.

4.2 MODE CHANGES

The special mode can be changed at any time by the application of a mode initiate clock sequence with the appropriate address key to define the new mode.

4.3 ADDITIONAL MODES

The additional address bits above A7 can be used as needed to define additional pages of MODE definitions.

5 JEDEC REGISTERED SPECIAL MODE REFRESH

–Refresh can be performed while in a special mode by the following means.

(1) – An initiate cycle is generated (W\ and CE\ before RE\) with the address key used to select the mode currently in effect.
(2) – Any normal read or write cycle will perform REFRESH.

–The Initiate Special Mode clock sequence will always perform an on–chip refresh cycle even when the MODE is being changed.

–This refresh applies to JEDEC Special Registered Modes only

6 BASIC TEST MODE DATA ALGORITHM

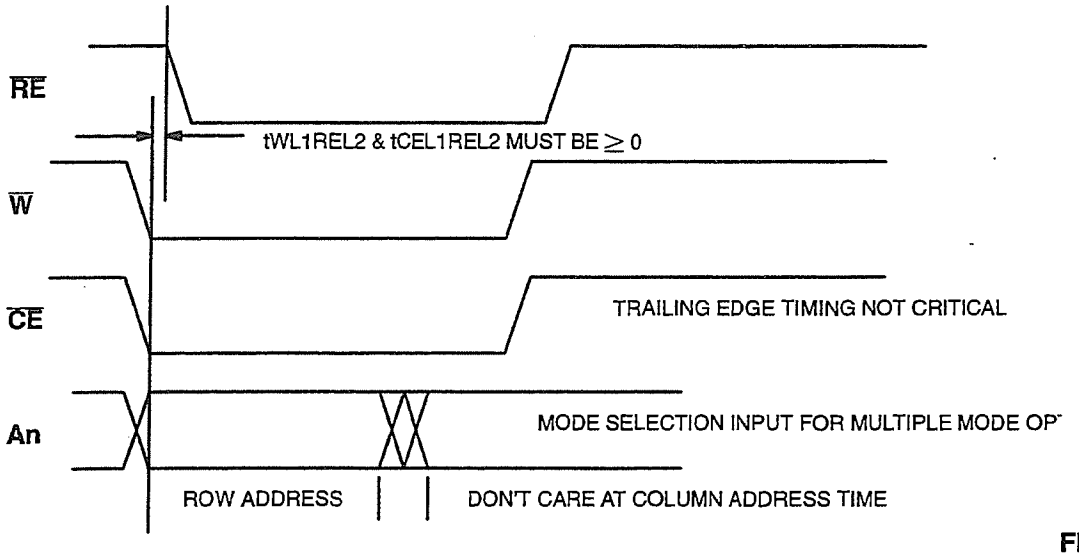
Any memory device that implements the JEDEC Registered modes must implement the "Basic Test Mode" as a minimum. Any other of the special modes which are registered and listed in Table A2–3, may be implemented at the option of the manufacturer. Additional MODES and test algorithms may be registered as needed.

When a memory device is operating in the Basic Test Mode, data that are presented to be written into the memory will be written into multiple locations depending upon the internal device organization and the number of parallel bits in the internal data bus (4, 8, 16, or other) (see par. 7). When a Read Operation is done, the data recovered will include the same set of data bits on the parallel data bus. The internal logic of the memory device will compare the states of all bits of the internal data bus. If all internal bits are equal, the "Q" pin will take the state equal to "1". If any internal data bits are not equal , then "Q" will equal "0". This is called the "1/0/=" test algorithm.

The BASIC TEST MODE is assigned the address keys, "All 1's" and all subsets of this key from 2 low order 1's to all 1's (see Appendix 2). It is acceptable for a device which implements the BASIC TEST MODE and optional test modes to sense a low order subset of the key address field but it is recomended that at least 3 bits be used to minimize the chances of ambiguities in the mode selection.

7 ADDRESS SPACE COMPRESSION CONTROL

Any Standard or Registered test algorithm in which the address space of the device is compressed by test operations on multiple internal data bits will have the address bits which control the internal data bits as defined in Table A2–1. In any test operations, the state of these bits will be "don't care".



FIG

A2–1 SPECIAL OPERATIONAL MODE INITIATE CYCLE

NOTE: The timing parameters of the pulses are not specified in this standard but care must be taken in the device specification to define minimum and maximum pulse durations to insure that noise pulses will be rejected and that intentional control sequencies will be recognized.

Table A2–1–A, 1M TO 16M DRAM ADDRESS COMPRESSION CONTROL BITS

Data Bus Width (# bits)	Control Address Bits	
	X1 DATA INTERFACE	X4 DATA INTERFACE
2		CA0
4	RA(MSB), CA(MSB)	CA0, CA1
8	RA(MSB), CA(MSB), CA0	
16	RA(MSB), CA(MSB), CA0, CA1	(MSB = Most Significant Bit)

Table A2–1–B 64M DRAM ADDRESS COMPRESSION CONTROL BITS

Compression Address = CA(MSB), CA(MSB–1), ...,CA(MSB–n)
where 2n–1 = the number of internal parallel data test bits = Compression factor

PARALLEL TEST BITS	64M X 1	16M X 4	8M X 8	4M X 16
32(n=4)	CA12>CA8			
8(n=2)		CA10>CA8		
4(n=1)			CA10>CA9(4K)	
2(n=0)				CA9(4K)

TABLE A2–1–C 64M DRAM ADDRESS ASSIGNMENT TABLE

Test Bits	DEVICE	RFSH CYCLES	Address Assignments												
32	64M X 1	–													
32	64M X 1	8K	0/0	1/1	2/2	3/3	4/4	5/5	6/6	7/7	8/(8)	9/(9)	10/(10)	11/(11)	12/(12)
8	16M X 4	–													
8	16M X 4	8K	0/0	1/1	2/2	3/3	4/4	5/5	6/6	7/7	8/(8)	9/(9)	10/(10)	11	12
4	8M X 8	4K	0/0	1/1	2/2	3/3	4/4	5/5	6/6	7/7	8/8	9/(9)	10/(10)	11	12
4	8M X 8	8K	0/0	1/1	2/2	3/3	4/4	5/5	6/6	7/7	8/(8)	9/(9)	10	11	12
2	4M X 16	4K	0/0	1/1	2/2	3/3	4/4	5/5	6/6	7/7	8/8	9/(9)	10	11	12
2	4M X 16	8K	0/0	1/1	2/2	3/3	4/4	5/5	6/6	7/7	8/(8)	9	10	11	12
1	2M X 32	4K	0/0	1/1	2/2	3/3	4/4	5/5	6/6	7/7	8	9	10	11	12
1	2M X 32	8K	0/0	1/1	2/2	3/3	4/4	5/5	6/6	7/	8	9	10	11	12

These addresses can be used as common addresses for 64M X 1, 16M X 4, 8M X 8, & 16M X 32 devices

(n) = compression address
n/n = RAn/CAn

TABLE A2–2 SPECIAL MODE ADDRESS KEY SPACE

The SPECIAL MODE Address Key space will be as shown in the following Karnaugh map with the exception of those codes reserved for the BASIC TEST MODE:

$\overline{A6}$	$\overline{A5}$	JEDEC Registered Modes	Reserved for Expansion	TEST
	A5			OPERATION
A6	$\overline{A5}$	Vendor Specific Modes	Customer Specific Modes	
	A5			
		$\overline{A7}$	A7	

A0 – A4 define individual modes within a block

JEDEC REGISTERED MODES – These are the modes that are defined in detail in registration documents. The function(s) shall be performed as defined with no variations (see Appendix 2 for list of registered modes).

VENDOR SPECIFIC MODES – These are those modes that are implemented by a Vendor for his own in–house use. The details will be revealed only at the discretion of the Vendor. The code assignments will have no standardization from vendor to vendor except at their discretion.

CUSTOMER SPECIFIC MODES – These modes are implemented by a vendor at the request of a specific customer. The information on these modes is not revealed except at their discretion.

TABLE A2–3

REGISTERED MODE ASSIGNMENT PAGE 0 TABLE

ROW ADDRESS BIT	FUNCTION
7, 6, 5, 4, 3, 2, 1, 0	
0, 0, 0, 0, 0, 0, 0, 0	NOT ASSIGNED
0, 0, 0, 0, 0, 0, 1, 1	BASIC TEST MODE, 1/0/=
0, 0, 0, 0, 0, 1, 1, 1	BASIC TEST MODE, 1/0/=
0, 0, 0, 0, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=
0, 0, 0, 1, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=
0, 0, 1, 1, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=
* 0, 1, 1, 1, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=
* 1, 1, 1, 1, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=

Additional address bits above A7 can be used to select additional pages of MODE definition.

* It should be noted that these pre–assigned address codes do not fall into the address space assigned to JEDEC Registered Modes.

NOTE:: A table of registered optional modes along with definitions will be compiled by the Committee and published periodically.

OPTIONAL DRAM OPERATIONAL MODES AND CYCLES

This standard defines a series of optional serial and random READ, WRITE, and REFRESH operational modes for address multiplexed DRAMs.

1 RANDOM ACCESS MODES

The following sections define the timing sequence required to operate a variety of optional random access data modes for address multiplexed DRAMs.

1.1 PAGE MODE

Page Mode is initiated with the row (word) address strobed by the falling edge of $\overline{RE}$. While $\overline{RE}$ remains asserted any combination of successive read or write operations on randomly selected column (bit) addresses may be initiated by the falling edge of $\overline{CE}$. During a read cycle, data out (Q) is terminated (high impedance) when $\overline{CE}$ goes inactive. A write cycle is initiated, and data-in sampled, at the concurrence of $\overline{CE}$ and $\overline{W}$ active. Page mode is terminated by $\overline{RE}$ going inactive.

1.2 STATIC COLUMN MODE

Static Column Mode features a static "ripple through" column address decoder. While $\overline{RE}$ remains asserted, successive reads or writes of randomly selected column addresses of the currently selected row are initiated by an address transition. A write operation is initiated, and data-in sampled, at the concurrence of $\overline{W}$ and $\overline{CE}$ active. Note that $\overline{CE}$ may function as an output enable rather than a column address strobe. Static Column operation is terminated by $\overline{RE}$ going inactive.

1.3 FAST PAGE MODE

Fast Page Mode is a latched Static Column operation. It is initiated with a row address strobed by the falling edge of $\overline{RE}$. While $\overline{RE}$ remains asserted, successive read or write operations on randomly selected column addresses are controlled by $\overline{CE}$. The mode is similar to that of Static Column with the addition of a "flow-through" address latch that is controlled by $\overline{CE}$.

open with $\overline{RE}$ active and $\overline{CE}$ inactive

latched with $\overline{RE}$ active and $\overline{CE}$ active

During a read operation, $\overline{CE}$ going active will also enable data out and $\overline{CE}$ going inactive will also place the output terminals into a high impedance state. Note that read cycle access times in Fast Page mode are often measured from the point where $\overline{CE}$ is inactive with a valid address. Data-in for a write operation is sampled at the concurrence of $\overline{CE}$ and $\overline{W}$ active. Fast Page mode is terminated by $\overline{RE}$ going inactive.

1.4 EXTENDED DATA OUT FAST PAGE MODE

In this variation of Fast Page Mode, in a read operation, the low to high transition of $\overline{CE}$ with $\overline{RE}$ active will not place the data out terminals into a high impedance state. Data-out will remain valid. During sequential read operations the data out terminals will transition from old to new data. The data out terminals will not go to the high impedance state until both $\overline{RE}$ and $\overline{CE}$ are inactive.

2 SERIAL ACCESS MODES

The following sections define the timing sequence required to operate a variety of serial access data modes for address multiplexed DRAMs.

2.1 NIBBLE MODE

Nibble mode provides high speed serial access of 4 sequential address locations. A Nibble Mode cycle is initiated with the row address strobed by the falling edge of $\overline{RE}$. An initial, randomly selected, column address is strobed by the falling edge of $\overline{CE}$. While $\overline{RE}$ remains asserted, reads or writes of sequential column addresses (modulo 4) can be performed by cycling $\overline{CE}$. The column address is internally incremented by +1 and wraps around. (4n+2, 4n+3, 4n, 4n+1, 4n+2, ...)

Nibble mode is terminated by the rising edge of $\overline{RE}$.

2.2 BYTE MODE

Byte Mode is an extension of the Nibble Mode operation to modulo 8. As in Nibble Mode, the initial column address may be randomly selected, and is automatically incremented by +1 at each cycle of $\overline{CE}$. The column address accessed is modulo 8 and wraps around (8n+6, 8n+7, 8n, 8n+1 ...).

2.3 BURST MODE

Burst Mode provides high speed serial access to all column addresses along a single row. Burst mode is initiated with a row address strobed at the falling edge of $\overline{RE}$. An initial, randomly selected column address is strobed at the falling edge of $\overline{CE}$. While $\overline{RE}$ remains asserted, read or write operations on sequential column addresses can be performed by cycling $\overline{CE}$. Like Nibble and Byte Modes, the column address is incremented by +1 and wraps around. (N-3, N-2, N-1, 0, 1, ...) Burst mode operation is terminated by $\overline{RE}$ going inactive.

2.4 STREAMING MODE

Streaming Mode is an extension of Burst Mode. In addition to being modulo N in the column direction, the row address is also incremented by +1 when the column address wraps from N-1 to 0. At the maximum row and maximum column addresses, both will wrap around to row 0, column 0, at the next cycle of $\overline{CE}$.

3 REFRESHMODES

The following sections define the timing sequence required to operate a variety of modes which refresh the data in address multlipexed DRAMs.

3.1 RAS ONLY REFRESH

A cycle with $\overline{RE}$ active and $\overline{CE}$ inactive is a RAS Only Refresh cycle. The address of the row to be refreshed is externally provided.

3.2 INTERNAL REFRESH (CAS BEFORE RAS REFRESH, CBRR)

A CBR refresh will occur if any $\overline{CE}$ is active and $\overline{W}$ is inactive when $\overline{RE}$ falls. External addresses are ignored; an internal refresh address counter supplies the address of the row to be refreshed. The refresh counter is incremented during each CBR cycle. Figure 3.9.5-2 shows the timing relationships which must be maintained to perform an internal refresh cycle

3.3 HIDDEN REFRESH

A Hidden Refresh occurs when $\overline{RE}$ is cycled while $\overline{CE}$ remains active. If data out (Q) was valid at the start of the refresh cycle, it will remain valid for the duration of $\overline{CE}$ active. For devices with CBR, the internal refresh address counter supplies the refresh address and is incremented during the cycle. Devices without CBR that support Hidden Refresh require the refresh address to be supplied externally.

3.4 SELF REFRESH

Self Refresh occurs when a CBR cycle is initiated following which $\overline{RE}$ and $\overline{CE}$ are kept active for an indefinite time that exceeds the DRAM active specification. The part then will internally cycle through all refresh addresses at a rate defined by the internal design of the part. The mode is exited by $\overline{RE}$ going inactive. The required timing relationships are shown in Figure 3.9.5-1B

4 WRITE MODES

The following sections describe the various WRITE modes which can be used with address multiplexed DRAMs

4.1 EARLY WRITE

$\overline{W}$ has transitioned to the active state, and data in is valid, prior to $\overline{CE}$ transitioning from high to low. Additional high to low transitions of $\overline{W}$ while $\overline{CE}$ remains active are not interpreted as write cycles. Data-out (Q) remains in a high impedance state for the duration of the cycle.

Note: Multiple Early Write cycles can be performed within a single $\overline{RE}$ cycle.

4.2 LATE WRITE

During a $\overline{RE}$/$\overline{CE}$ cycle, $\overline{W}$ is inactive when $\overline{CE}$ transitions from high to low. $\overline{W}$ will be asserted after $\overline{CE}$ transitions from high to low. Data-in will be sampled and the write operation initiated by $\overline{W}$ going active.

Note: Multiple Late Write cycles can be performed at several column addresses during a single $\overline{RE}$ cycle.

Note: For devices with bidirectional (DQ) input/outputs, the output drivers should be disabled by $\overline{G}$ (and the data-in provided), prior to the the falling edge of $\overline{W}$.

4.3 READ WRITE

This is a late write cycle at a single address for memory devices with independent data-in (D) and data-out (Q) terminals. During a $\overline{RE}$/$\overline{CE}$ cycle $\overline{W}$ is inactive when $\overline{CE}$ transitions from high to low. $\overline{W}$ will be asserted prior to the data access time of the memory. The memory will start a write operation with new data-in in parallel with the access of the previously stored information.

4.4 READ MODIFY WRITE

This is a late write cycle at a single address where the state of $\overline{W}$ remains inactive until after the access time of the memory and then goes active. (As data has been read out of the memory prior to writing, the data to be written could be the modified data out.)

4.5 BIT WRITE

A write cycle for a n bit wide memory in which the data bits that are to be written are controlled by a write mask. Write per Bit is selected by $\overline{W}$ active and $\overline{CE}$ inactive as $\overline{RE}$ transitions to the active state. The mask is supplied at the beginning of the write cycle on the data-in terminals. A high mask bit enables the write function for that bit. A low mask bit leaves the previously stored data unaltered. Figure 3.9.5-1 shows the riming relationships which must be maintained for a bit write cycle.

4.6 FLASH WRITE

This is a write cycle in which the contents of an entire row of the memory array can be selectively set to a stated value. For an n bit wide memory, the write per bit register determines which bits of the word are to be altered.

4.7 BLOCK WRITE

A write cycle in which n sequential column addresses, modulo n, are written in a single operation. The n locations are controlled by the LSB of the column address.

NON–MULTIPLEXED ADDRESS DRAM OPERATIONAL REQUIREMENTS

All DRAMs that do not utilize address multiplexing must have internal architecture that allows them to operate with the following characteristics:

NON–MULTIPLEXED ADDRESS DRAM with PAGING

Non–Multiplexed DRAMs require that all addresses be valid at RE time; however CE\ is still needed for control of other standard DRAM modes & features. A Non–Muxed DRAM is the same as a multiplexed DRAM except for the four items listed below:

1 ALL Refresh modes are supported, but "RAS–Only" is not recommended;

2 All addresses are provided valid at RE\ (RAS) time;

3. 1st CE\ is Non–Critical; it is used only to enable the output(s);

4. Subsequent CE\s (with Low–Order Addresses) or only the Low–Order Addresses provide the various DRAM column operations such as Page Mode, Static Column Mode, Nibble Mode, etc. The length of a column is limited by the number of Low–Order Addresses, which is manufacturer defined.

Non–Muxed to Muxed address equivalents

ADDRESSES: Non–Multiplexed Part (High to Low Order)
High Low

RA(N).....RA(1), RA(0), CA(N).....CA(1), CA(0)
(_____)(_____)

ROW Column
(Multiplexed Address Part)

Extended Data Out Standard

This Standard defines the output characteristics of Extended Data Out (EDO) feature for DRAMs. Any part encorporating "EDO" must satisfy all of the following criteria to conform to the Standard.

1. Data out remains valid when $\overline{RAS}$ is active, $\overline{CAS}$ is inactive, and $\overline{WE}$ is inactive, and $\overline{OE}$ is active. In this case, either $\overline{WE}$ going active, or $\overline{OE}$ going inactive will cause the output to go high Z
2. Data output becomes high Z when both $\overline{CAS}$ and $\overline{RAS}$ are inactive.
3. When $\overline{RAS}$ and $\overline{CAS}$ are active and $\overline{WE}$ is inactive, output is controlled (turned on or turned off) as a static function of $\overline{OE}$. In an active Read cycle with $\overline{RAS}$ and $\overline{CAS}$ low, a change in state of $\overline{WE}$ to active low. is illegal.
4. If the output is high z when $\overline{CAS}$ goes inactive, the output will remain in high Z with G either active or inactive.
5. When $\overline{RAS}$ is active and the output from a read cycle is turned off by $\overline{WE}$ going active, the output will remain in a high Z state until a subsequent read is executed.
6. If output transitions from low Z (output turned on) to high Z (output turned off) while $\overline{CAS}$ is inactive, the output will remain high Z until a subsequent read cycle is executed.
7. Data from a read cycle will remain valid when $\overline{RAS}$ goes inactive as long as both $\overline{CAS}$ and $\overline{OE}$ will remain active. After $\overline{RAS}$ goes inactive, $\overline{WE}$ becomes a "don't care" and has no influence on the output.
8. When the output is high Z and $\overline{RAS}$ is inactive, the output will remain high Z, independent of the levels on $\overline{CAS}$ or $\overline{OE}$, until a $\overline{RAS}$ active read cycle is executed.

Definitions of terms used in EDO description:

High Z: An output logic state that presents a high impedence (neither sourcing or sinking) to any driving device.

Low Z: An output logic state that presents a low inpedence (either sourcing or sinking current) to any driving device.

Active Low: (low true) A logic description where a low signal represents a logical "active" condition. Note: All input signals included in this specification of EDO are "low true".

Read Cycle: A memory cycle for which the control signals are applied in the appropriate sequence to have data read from the device and presented on the output terminals.

256M DRAM Address Compression for Test–Mode

Devices		16K Refresh cycles (RA0–RA13)			8K Refresh cycles (RA0–RA12)		
		Normal Mode Input Addr.	Test Mode		Normal Mode Input Addr.	Test Mode	
			Input Address	Compress. Address		Input Address	Compress. Address
256M	64M X 4	RA0–RA13 CA0–CA11	RA0–RA13 CA0–CA7	CA8–11	RA0–RA12 CA0–CA12	RA0–RA12 CA0–CA8	CA9–12
	32M X 8	RA0–RA13 CA0–CA11	RA0–RA13 CA0–CA7	CA8–10	RA0–RA12 CA0–CA11	RA0–RA12 CA0–CA8	CA9–11
	16M X 16	RA0–RA13 CA0–CA9	RA0–RA13 CA0–CA7	CA8–9	RA0–RA12 CA0–CA10	RA0–RA12 CA0–CA8	CA9–10
	8M X 32	RA0–RA13 CA0–CA8	RA0–RA13 CA0–CA7	CA8	RA0–RA12 CA0–CA9	RA0–RA12 CA0–CA8	CA9

256M DRAM Data Space Compression for Test–Mode

When the memory device is operating in the compression mode, the data space is compressed with four DQn circuits supplying test data and receiving test results as defined in the following table.

Devices		Normal Mode Data Interface	Test Mode Data Interface	
			Active Data Bits	Data Bits Served
256M	64M X 4	DQ0–DQ3	DQ0	DQ0
			DQ1	DQ1
			DQ2	DQ2
			DQ3	DQ3
	32M X 8	DQ0–DQ7	DQ0	DQ0, DQ1
			DQ3	DQ2, DQ3
			DQ5	DQ4, DQ5
			DQ6	DQ6, DQ7
	16M X 16	DQ0–DQ15	DQ0	DQ0⇒DQ3
			DQ7	DQ4⇒DQ7
			DQ11	DQ8⇒DQ11
			DQ12	DQ12⇒DQ15
	8M X 32	DQ0–DQ31	DQ0	DQ0⇒DQ7
			DQ15	DQ8⇒DQ15
			DQ23	DQ16⇒DQ23
			DQ24	DQ24⇒DQ31

256M DRAM ADDRESS AND DATA SPACE COMPRESSION FOR TEST MODE

Release 7

Pipelined Nibble Mode Definition

Devices that operate in the Pipelined Nibble Mode are required to meet the following criteria to conform to this Standard.

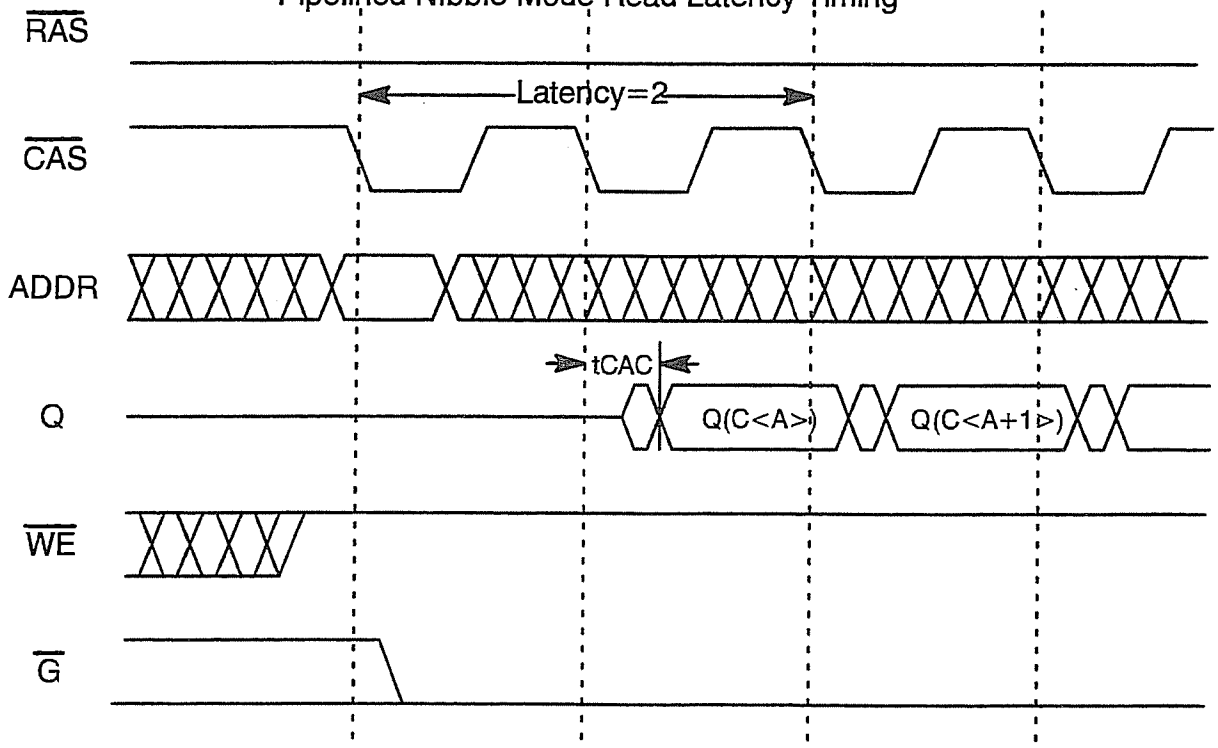
1. Burst Length shall be 4
2. Read Latency shall be 2 (refer to attached timing diagram for clarification)
3. Write Latency shall be 0
4. A WCBR, with the address keys shown below, is used to program the burst sequence. It is persistant until it is reprogrammed.

Address Sequence	A0	A1	A2	A3	A4	A5	A6	A7
Linear	0	0	0	0	0	1	0	0
Interleaved	1	0	0	0	0	1	0	0

5. $\overline{WE}$ transition during $\overline{CAS}$ precharge time causes burst to terminate
6. $\overline{WE}$ transition during $\overline{CAS}$ low, which remains through the $\overline{CAS}$ rising edge, causes burst to terminate.
7. $\overline{WE}$ pulse which is fully enclosed by a $\overline{CAS}$ low will be ignored and not cause a burst terminate.
8. Same output enable function as in EDO definition.
9. Read–modify–write cycle within $\overline{CAS}$ active cycle is not supported.
10. A Pipelined Nibble Mode device may not be reconfigured by the user to operate in the standard EDO (non–burst) mode.

FOR REFERENCE ONLY

Pipelined Nibble Mode Read Latency Timing



3.10 Multiport Dynamic RAM (MPDRAM)

The following MPDRAM standards were developed by JC-42.3 Committee and have been implemented using MOS technology.

3.10.1 Nibble Wide MPDRAM

3.10.1.1 64K BY 4 MPDRAM IN DIP, SOJ, & ZIP

CAPACITY--64K WORDS OF 4 BITS
LOGIC FEATURES--Multiplexed Address and
--SERIAL and RAM data ports
There are three versions of this part: in DIP, SOJ, and in ZIP
PACKAGE--24 PIN DIP, 0.400" WIDE
PIN ASSIGNMENTS--FIG. 3.10.1-1
PACKAGE--24 PIN SOJ, 0.300" WIDE
PIN ASSIGNMENTS--FIG. 3.10.1-1
PACKAGE--24 PIN ZIP
PIN ASSIGNMENT--Fig. 3.10.1-2

3.10.1.2 256K BY 4 MPDRAM IN DIP, SOJ, TSOP2, & ZIP

CAPACITY--256K WORDS OF 4 BITS
LOGIC FEATURES--Multiplexed Address and
--SERIAL and RAM data ports
There are three versions of this part: in DIP, SOJ, and in ZIP
PACKAGE--28 PIN DIP, 0.400" WIDE
PIN ASSIGNMENTS--FIG. 3.10.1-3
PACKAGE--28 PIN SOJ or TSOP2, 0.400" WIDE, 0.050" PIN PITCH
PIN ASSIGNMENTS--FIG. 3.10.1-3
PACKAGE--28 PIN ZIP
PIN ASSIGNMENT--Fig. 3.10.1-4

3.10.1.3 256K BY 4 TPDRAM IN SOJ

CAPACITY--256K WORDS OF 4 BITS
LOGIC FEATURES--Multiplexed Address and
--TWO SERIAL and ONE RAM data ports
PACKAGE--40 PIN SOJ, 0.400" WIDE
PIN ASSIGNMENTS--FIG. 3.10.1-5

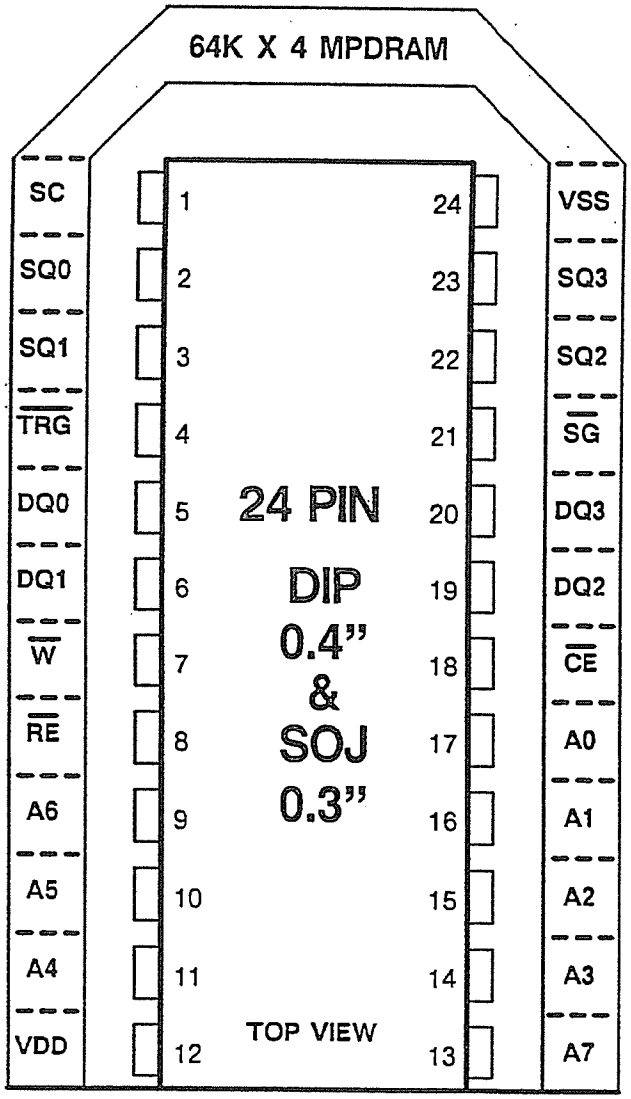


FIGURE 3.10.1-1
64K BY 4 MPDRAM IN DIP & SOJ

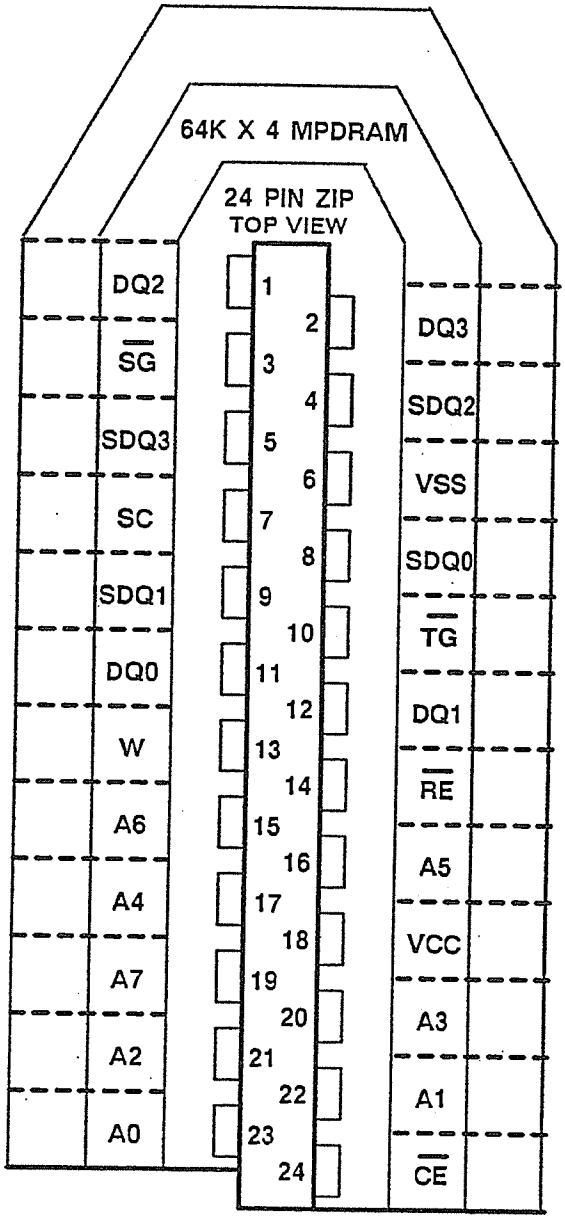


FIGURE 3.10.1-2
64K BY 4 MPDRAM IN ZIP

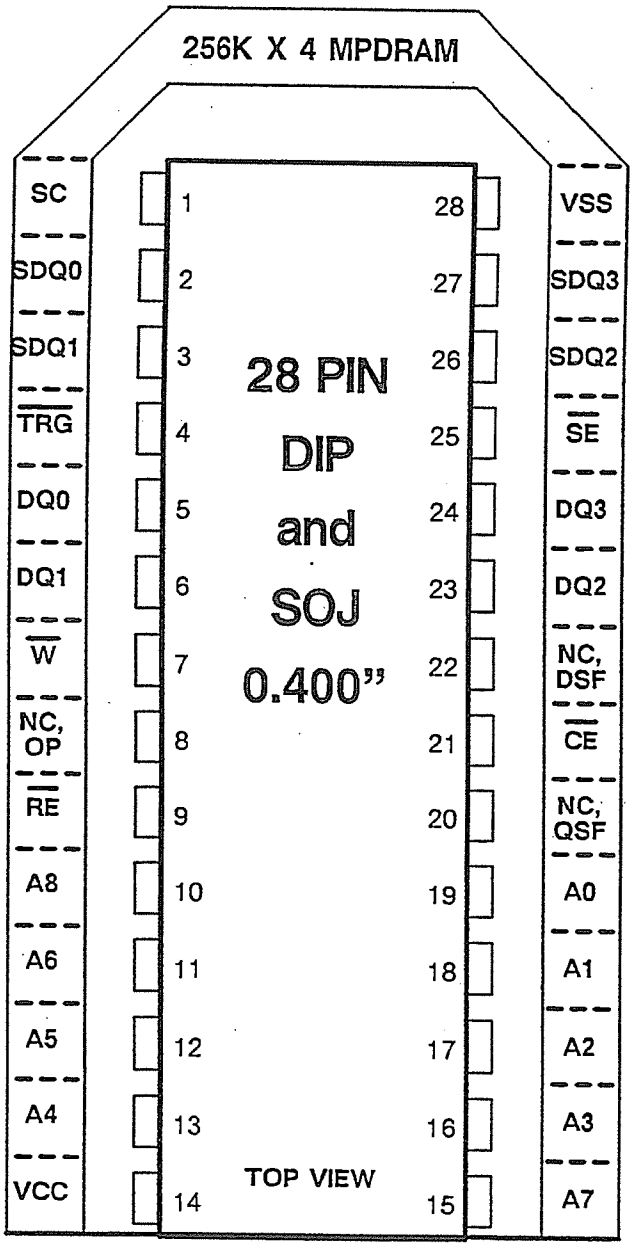


FIGURE 3.10.1-3
256K BY 4 MPDRAM IN DIP & SOJ

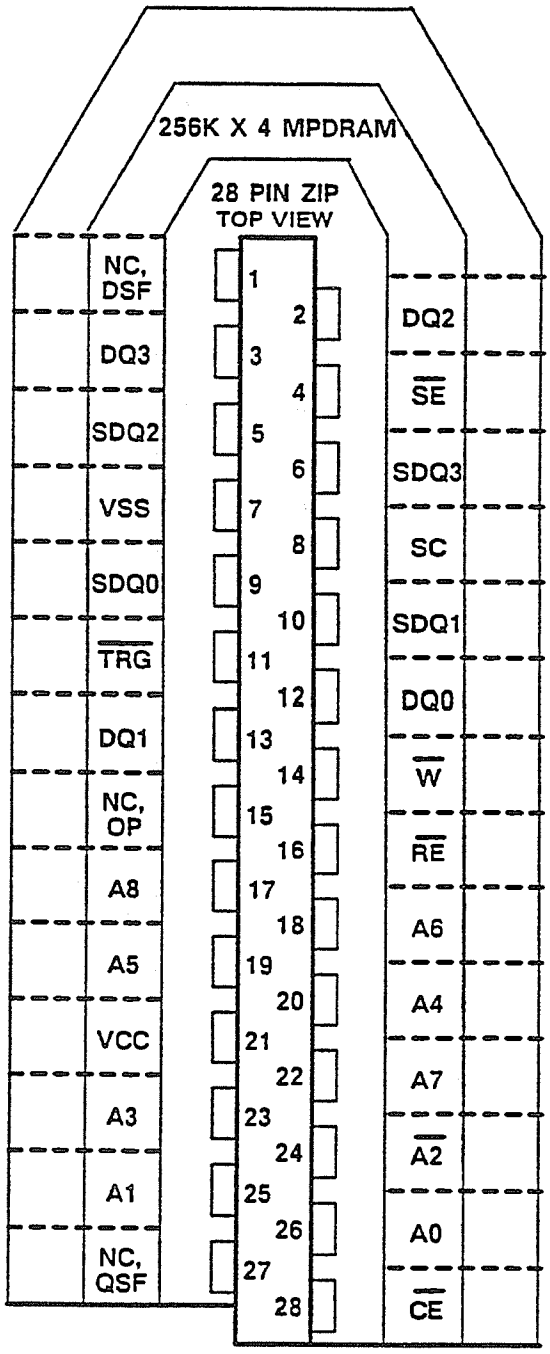


FIGURE 3.10.1-4
256K BY 4 MPDRAM IN ZIP

STS	SAM TRANSFER SELECT
Lo	TRANSFER TO/FROM SAMa
Hi	TRANSFER TO/FROM SAMb

The STS input pin is used to identify which serial access memory will be used during a TRANSFER operation.

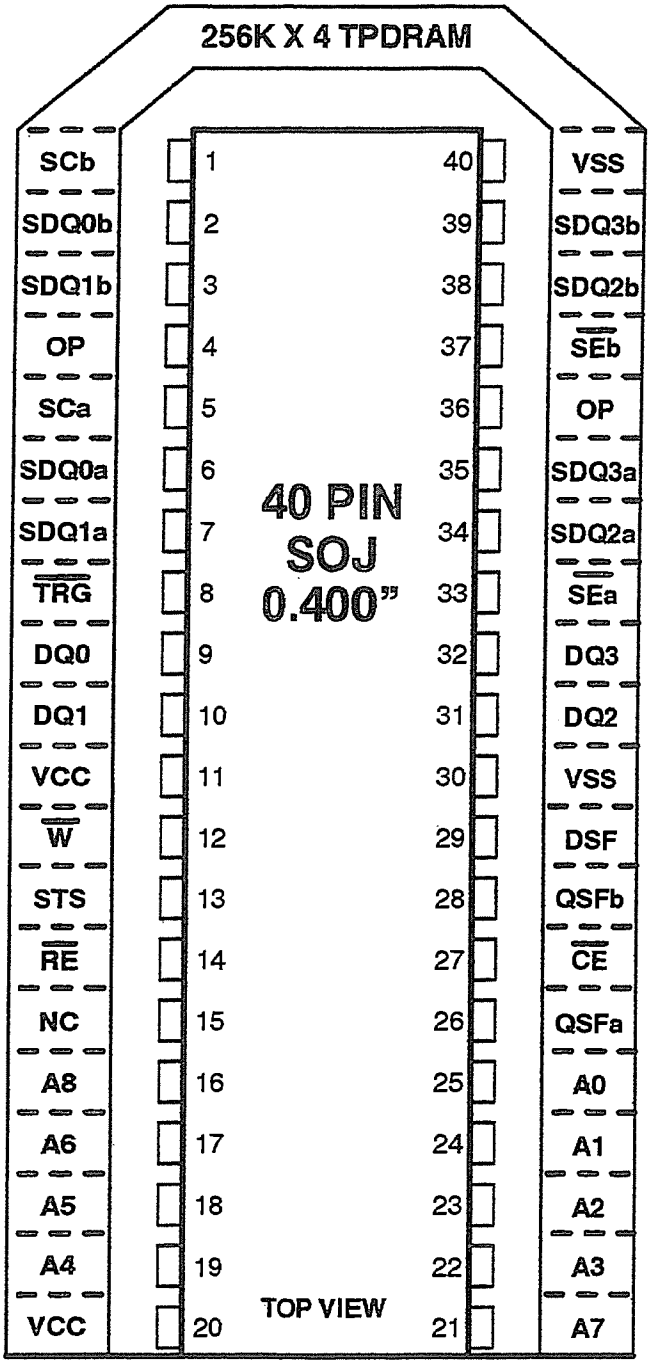


FIGURE 3.10.1–5
256K BY 4 TPDRAM IN SOJ

3.10.2 Byte Wide MPDRAM

3.10.2.1 128K AND 256K BY 8 MPDRAM IN DIP, SOJ, & TSOP2

CAPACITY--128K, & 256K WORDS OF 8 BITS
LOGIC FEATURES--Multiplexed Address
--SERIAL and RAM data ports
The 128K part has two versions: in DIP, and SOJ
PACKAGE--128K PART, 40 PIN DIP, 0.600" WIDE
PIN ASSIGNMENTS--FIG. 3.10.2-1
PACKAGE--128K & 256K PARTS, 40 PIN SOJ, 0.400" WIDE
PIN ASSIGNMENTS--FIG. 3.10.2-1
PACKAGE--128K PART, 44/40 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENTS--FIG. 3.10.2-2

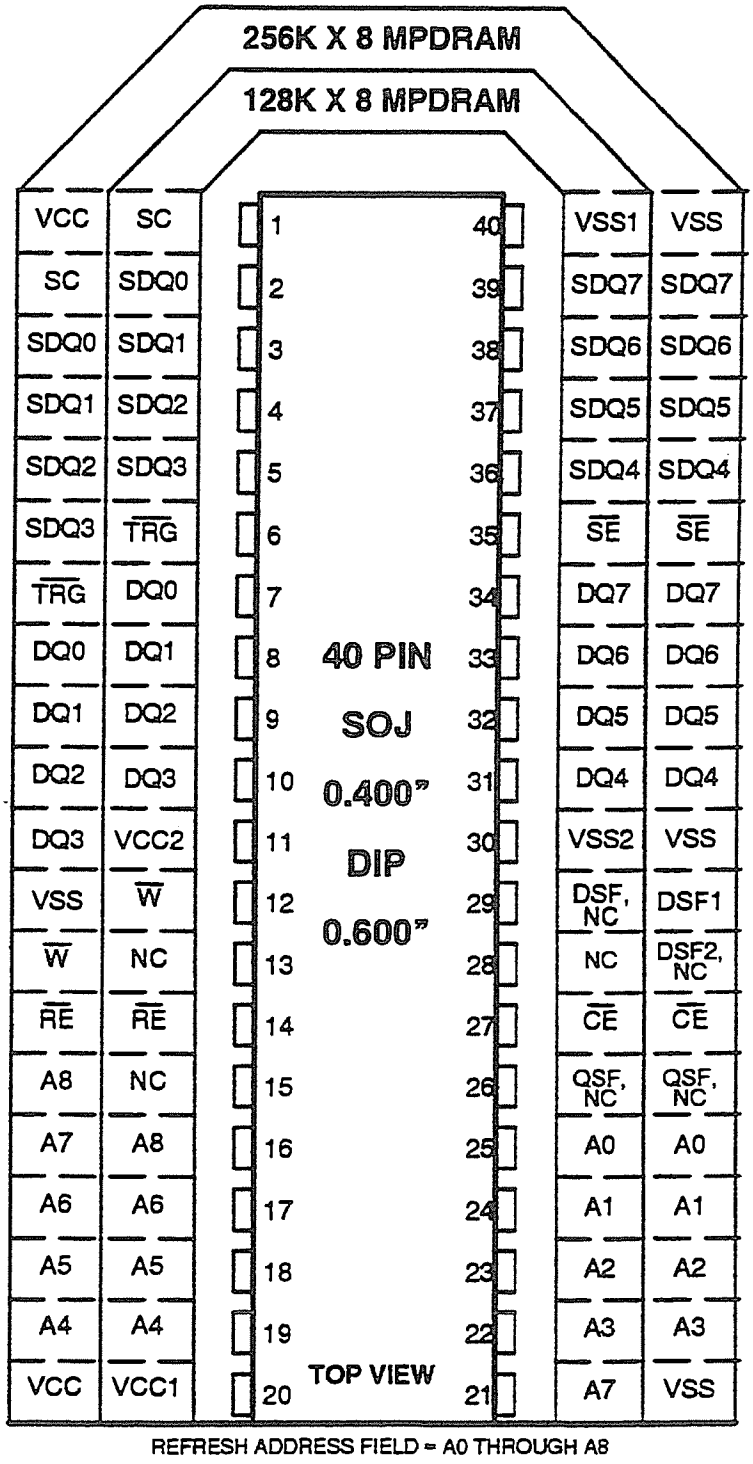
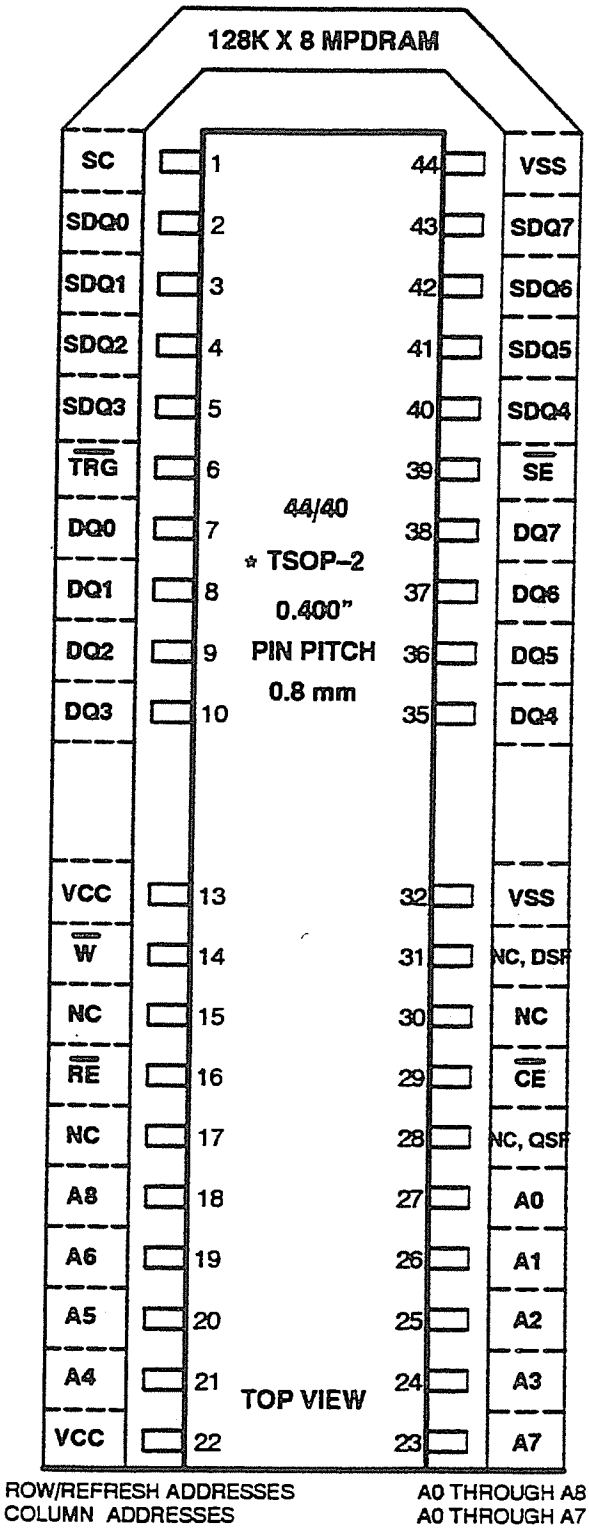


FIGURE 3.10.2–1
128K AND 256K BY 8 MPDRAM IN DIP & SOJ



☆ Note: The JEDEC Standard 30 term for the TSOP–2 package is PDSO–G

FIGURE 3.10.2–2
128K BY 8 MPDRAM IN TSOP–2

3.10.3 Word Wide MPDRAM & GRAM

3.10.3.1 – 128K & 256K BY 16 MPDRAM IN SOG WITH MULTIPLE CLOCKS

CAPACITY—256K WORDS OF 16 BITS
LOGIC FEATURES—Multiplexed Address
—SERIAL and RAM data ports
There are two versions of these parts: One with 2 $\overline{W}$ and the other with 2 $\overline{CE}$, controlling the lower and upper bytes of data.: 128K & 256K with 2 W, 256K with 2 CE. .
PACKAGE—64 PIN SOG, 12 mm wide, 0.8 mm pin pitch
PIN ASSIGNMENTS—FIG. 3.10.3–1

3.10.3.2 – 128K & 256K BY 16 MPDRAM IN TSOP–2 WITH MULTIPLE CLOCKS

CAPACITY—128K AND 256K WORDS OF 16 BITS
LOGIC FEATURES—Multiplexed Address
—SERIAL and RAM data ports
There are two versions of these parts: One with 2 $\overline{W}$ and the other with 2 $\overline{CE}$, controlling the lower and upper bytes of data.: 128K & 256K with 2 $\overline{W}$, 128K & 256K with 2 $\overline{CE}$. .
PACKAGE—70 PIN TSOP–2 10.16 mm wide (0.400"), 23.49 mm long. 0.65 mm pin pitch
NOTE: These parts have essentially the same pin rotation as the parts defined in Par. 3.10.3.1 with the exception of the addition of NC pins in the middle.
PIN ASSIGNMENTS—FIG. 3.10.3–2

3.10.3.3 – 256K BY 16 SGRAM IN TSOP–2

CAPACITY—256K WORDS OF 16 BITS
LOGIC FEATURES—Multiplexed Address
—A single data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—50 PIN TSOP–2, 10.16 mm wide (0.400"), 0.8 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–3
NOTE: This part has the same pinout as the SDRAM part shown in Fig. 3.11.4–1 with the exception of the DSF function on P 33.

3.10.3.4 – 256K BY 32 SGRAM IN QFP or TQFP

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—A single data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–4
NOTE: This part has the same pinout as the SDRAM part shown in Fig. 3.11.4–4 with the exception of the DSF function on P 33.

3.10.3.5 – 256K BY 32 SGRAM IN TSOP2

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—A single data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—80 PIN TSOP2, 10.16 mm wide (0.400"), 0.65 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–5

3.10.3.6 – 256K BY 32 SYNCHRONOUS MPDAM IN TSOP2

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—A multiple data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—120 PIN QFP or TQFP, 20 mm X 14 mm, 0.5 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–5

3.10.3.7 – 256K BY 32 SYNCHRONOUS MPDAM IN TSOP2

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—A multiple data port with Graphics oriented features.
—Synchronous address & control interface.
PACKAGE—100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm PP
PIN ASSIGNMENTS—FIG. 3.10.3–6

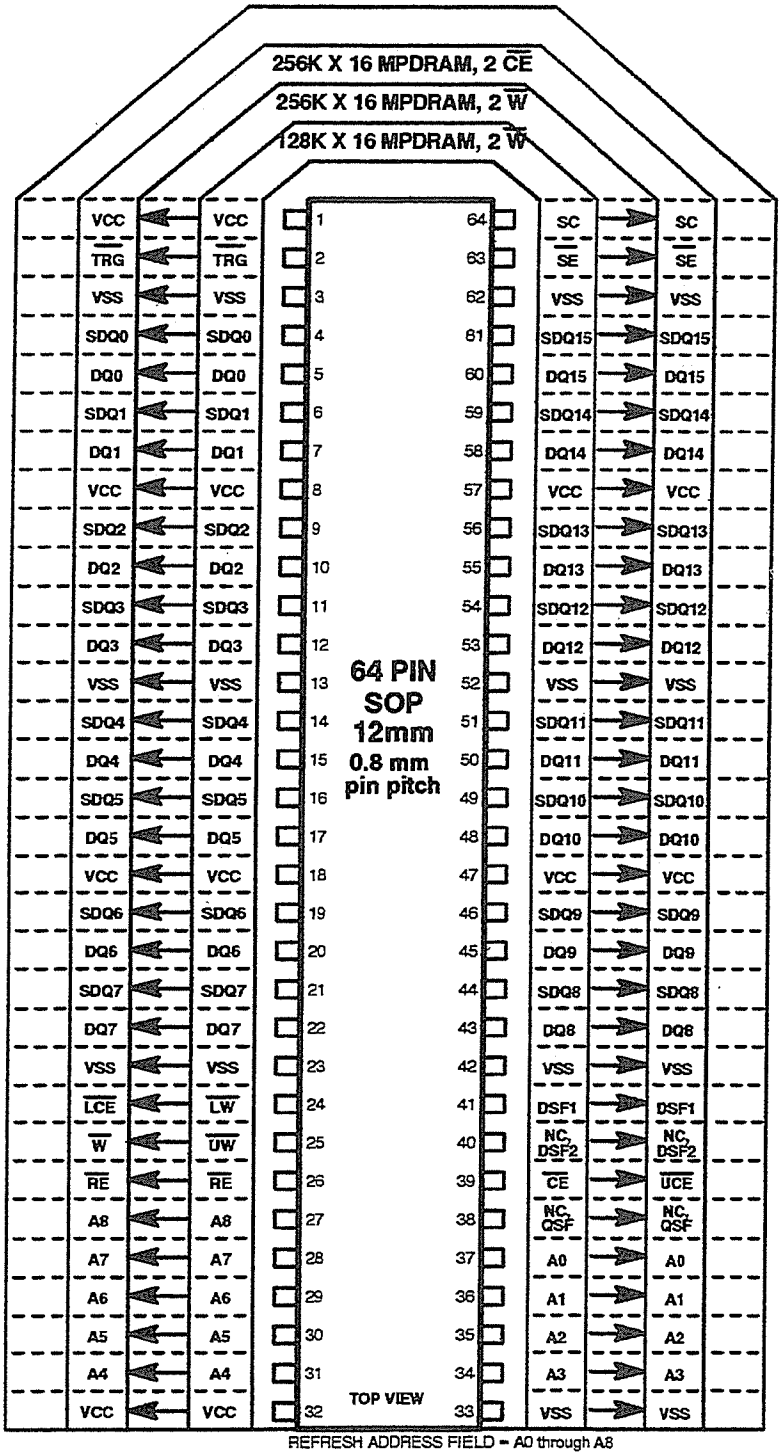
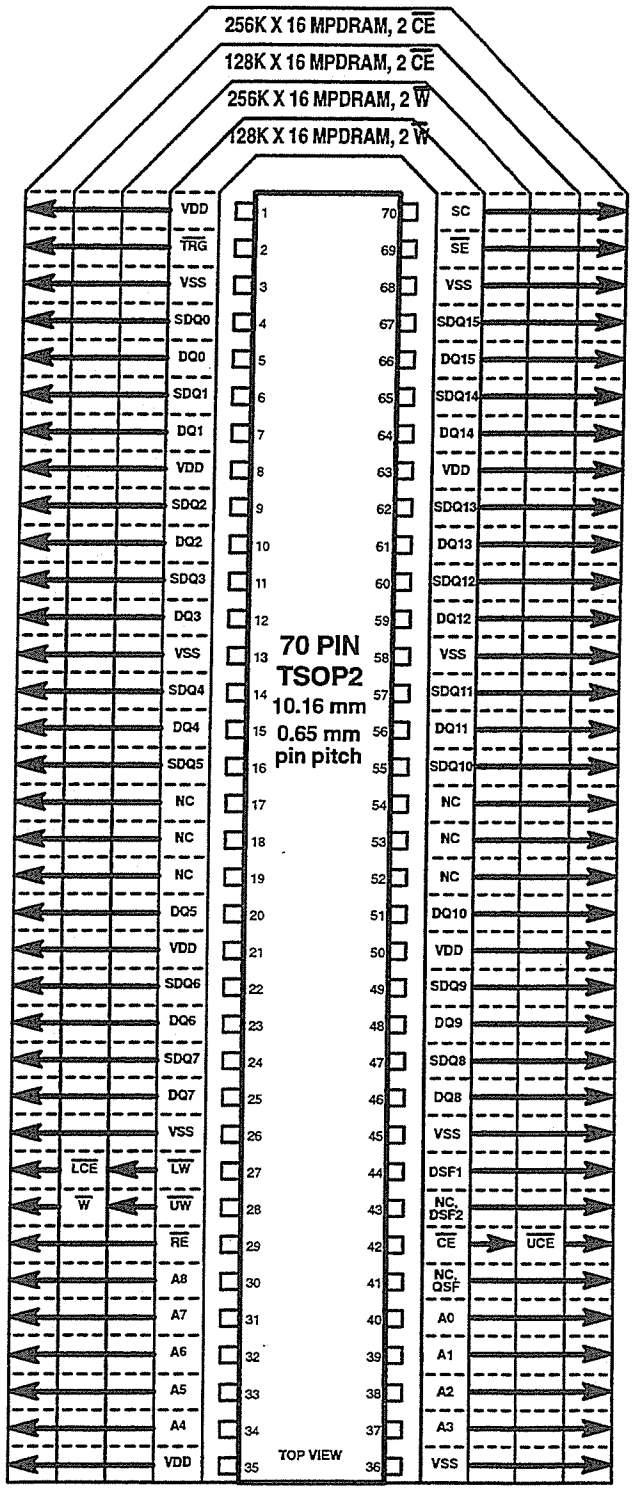


FIGURE 3.10.3–1
128K & 256K BY 16 MPDRAM WITH 2 $\overline{W}$
256K BY 16 WITH 2 $\overline{CE}$ IN SOP

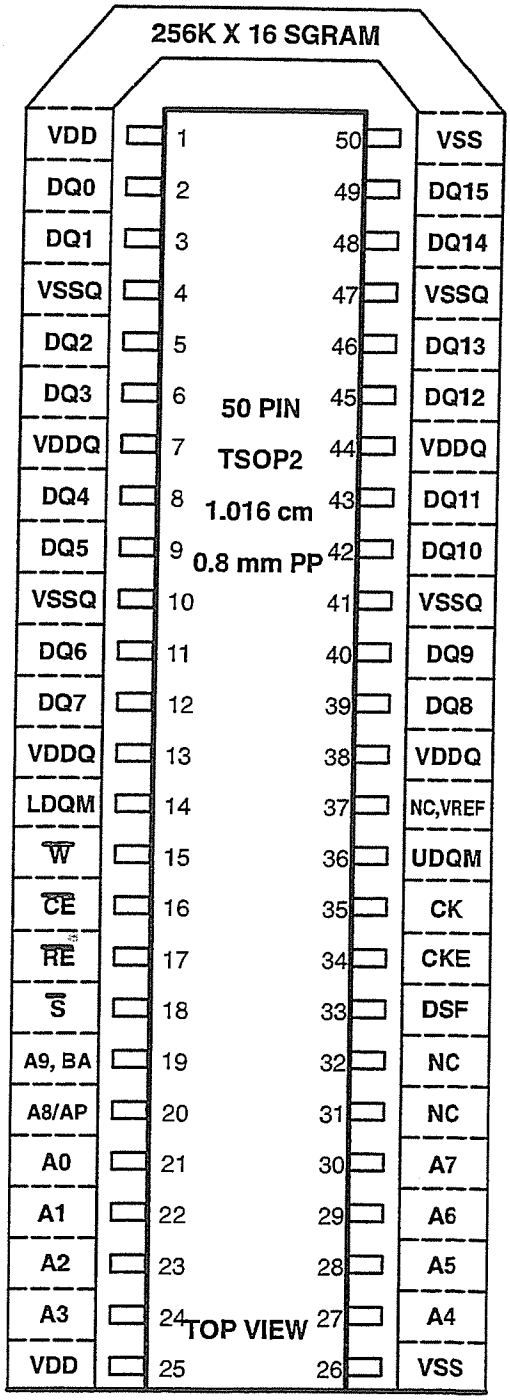


REFRESH ADDRESS FIELD = A0 through A8

* NOTE: The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

FIGURE 3.10.3–2

128K & 256K BY 16 MPDRAM IN TSOP–2 with 2 $\overline{W}$ & 2 $\overline{CE}$



This pinout is the same as the one for the 256K X 16 SDRAM shown in Fig. 3.11.4–1 except for the DSF function on pin 33.

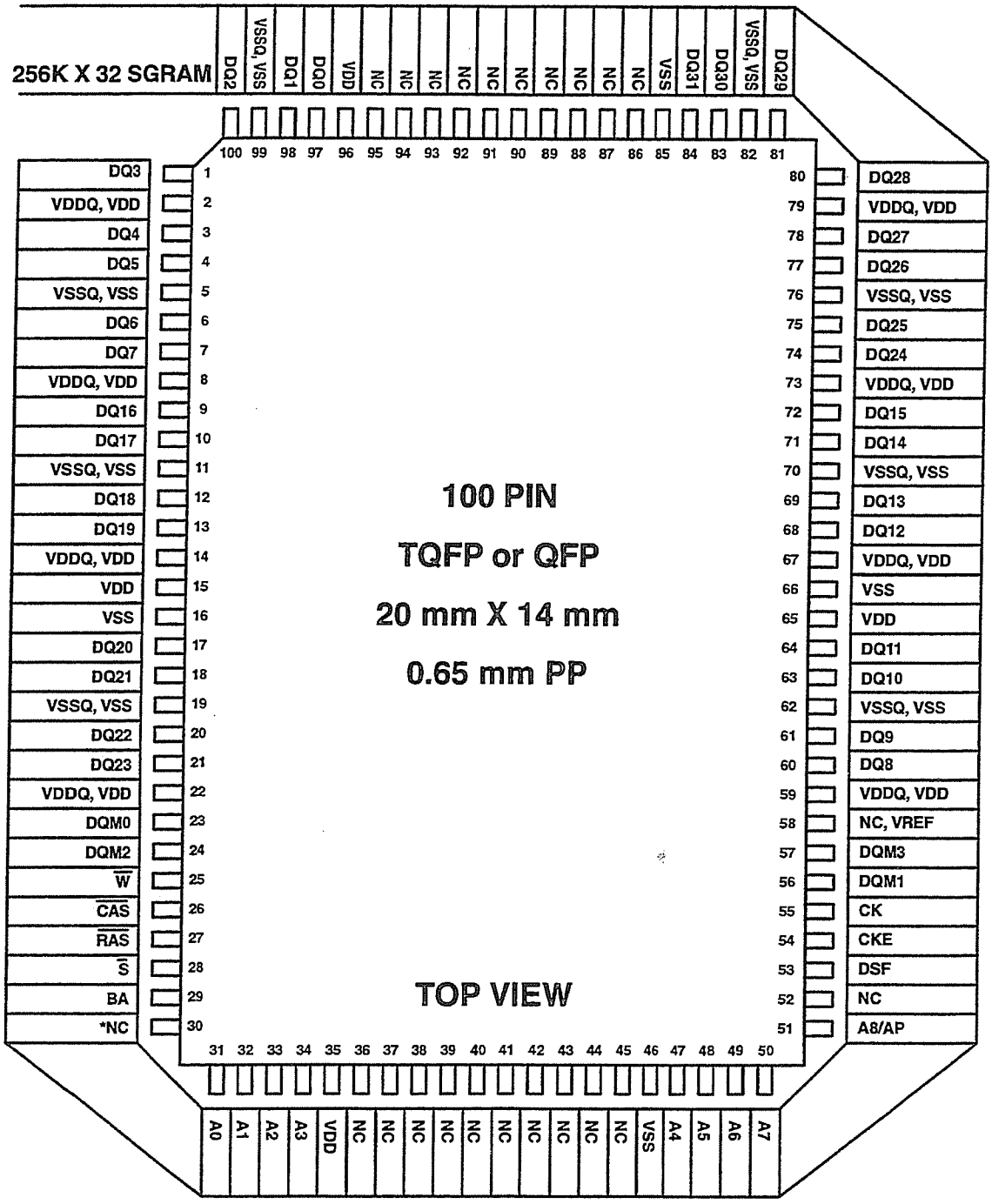
The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO–G

* NOTE—All VDDQ and VSSQ pins may be VDD and VSS at the option of the supplier.

ADDRESS STRUCTURE

RA	A0 ⇒ A8
CA	A0 ⇒ A7

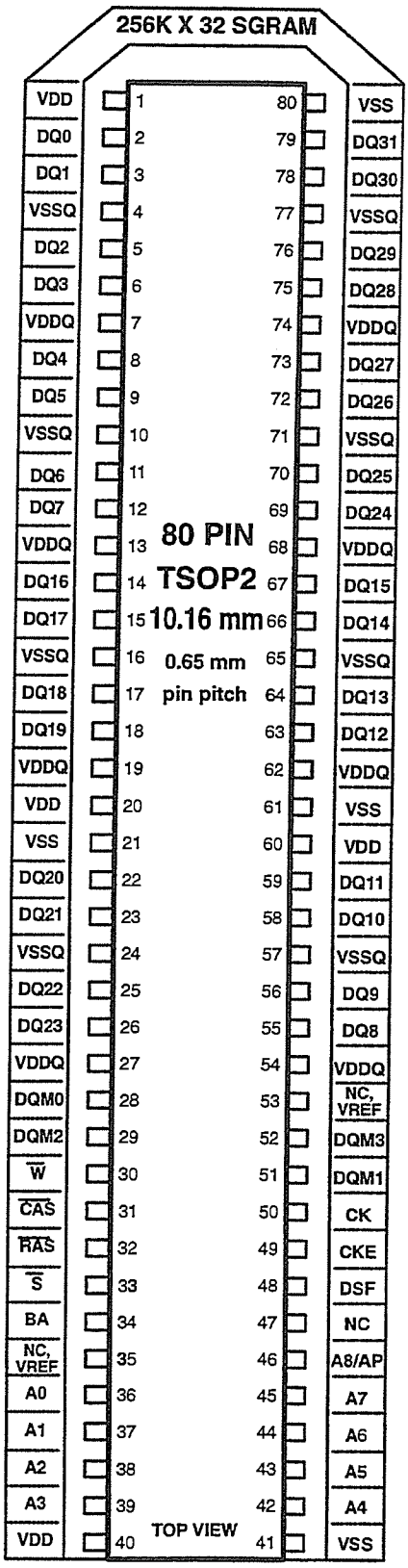
FIGURE 3.10.3–3
256K BY 16 SGRAM IN TSOP2



* In Release 6, Pin 30 had an optional VREF. This was deleted by action of the Committee in Release 7.

FIGURE 3.10.3–4
256K BY 32 SGRAM IN QFP

Release 6c7



The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO–G

FIGURE 3.10.3–5
256K BY 32 SGRAM IN TSOP2

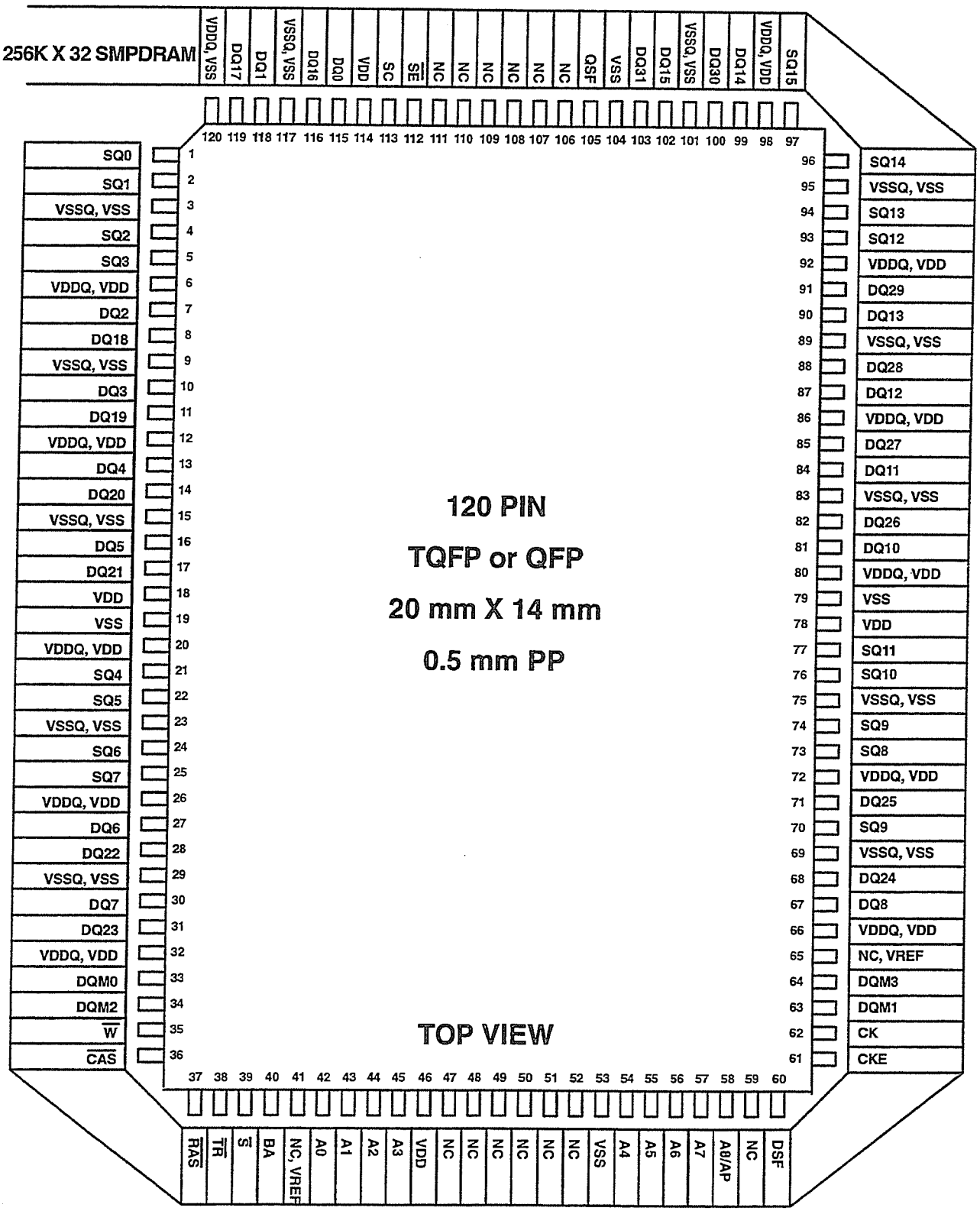
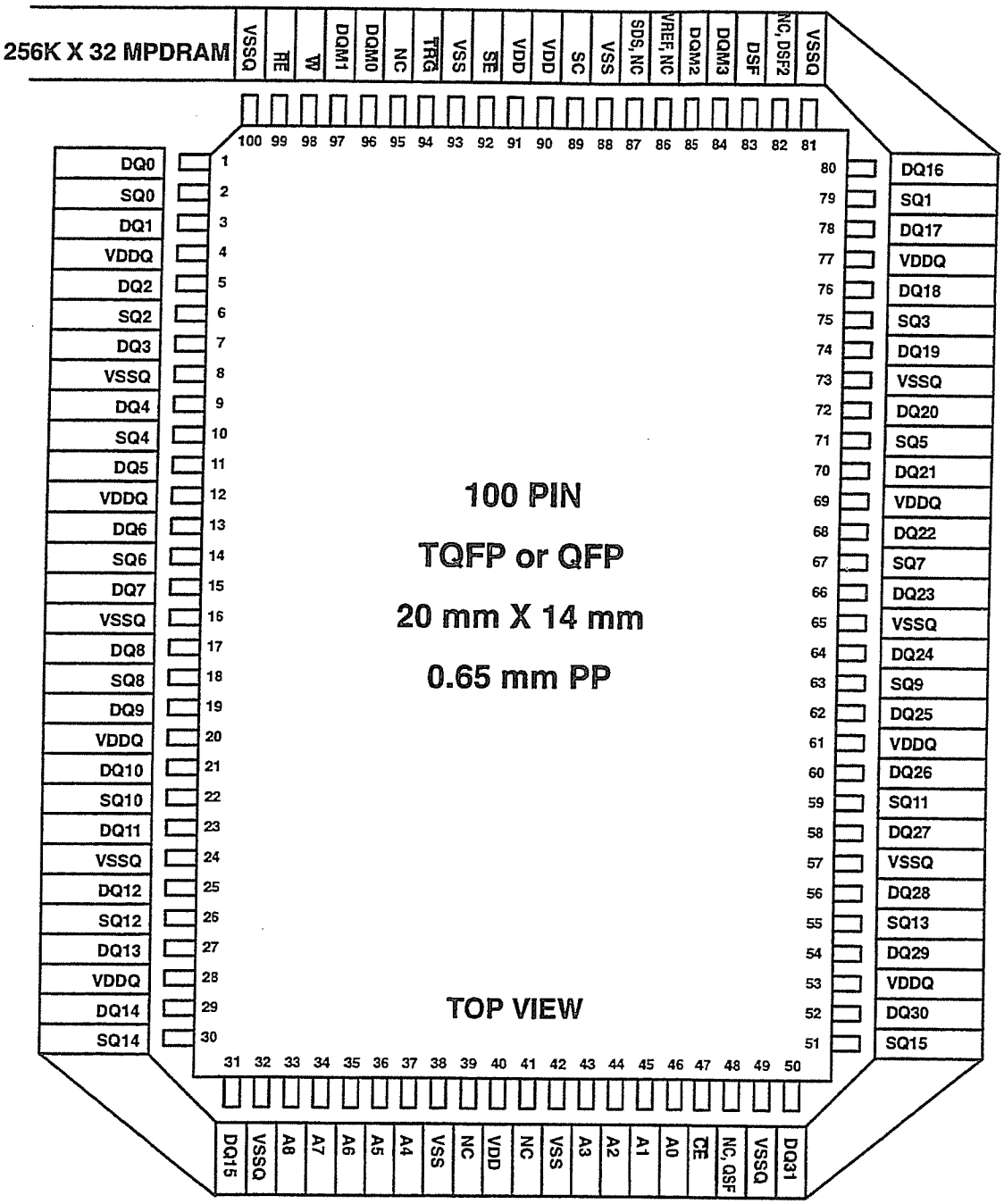


FIGURE 3.10.3–6
256K BY 32 SYNCHRONOUS MPDRAM IN QFP



Configuration
DRAM = 256K X 32
SAM = 512 X 16
ROW ADDRESS A0⇒A8
COLUMN ADDRESS A0⇒A8

FIGURE 3.10.3–7
256K BY 32 MPDRAM IN QFP

3.10.4 MPDRAM Optional Features

3.10.4.1 – 256K X 4 MPDRAM MINIMUM FEATURE SET TRUTH TABLE

The 256K X 4 MPDRAM described in this Standard must contain, as a minimum, the feature set described in Table 3.10.4–1, 256K X 4 MPDRAM FEATURE SET TRUTH TABLE.

3.10.4.2 – 256K X 4 MPDRAM EXTENDED FEATURE SET TRUTH TABLE

The 256K X 4 MPDRAM described in this Standard, in addition to the minimum feature set defined in Table 3.10.4–1, may contain any of the features described in the Table, 256K X 4 MPDRAM FEATURE SET TRUTH TABLE, and still meet the Standard. These logic features must operate exactly as defined in the table to conform to the Standard.

3.10.4.3 – MPDRAM BIT WRITE OPTIONAL FEATURE

This feature allows individual data bits of a memory array with a multi bit data interface to be selectively modified during a write cycle while other bits remain unchanged. The timing sequence used to control the feature is shown in figure 3.10.4–1 and operates as follows:

1–If W\ is low at the time that RE\ goes low, the state of the individual DQ pins determines if that data bit is to be written.

2–If DQ is HIGH write is ENABLED for that bit and the data present on DQ at the time that CE\ goes low is written.

3–If DQ is LOW, write is DISABLED for that bit and no subsequent writing can occur during that RE\ cycle.

4–If W\ is high at the time that RE\ goes low but goes low later in the cycle, a normal write cycle will be performed and all data bits will be written.

3.10.4.4 – 128K X 8 MPDRAM MINIMUM FEATURE SET TRUTH TABLE

The 128K BY 8 MPDRAM described in this standard must contain, as a minimum, the feature set described in Table 3.10.4–2, 128K X 8 MPDRAM FEATURE SET TRUTH TABLE.

3.10.4.5 – 128K X 8 MPDRAM EXTENDED FEATURE SET TRUTH TABLE

The 128K X 8 MPDRAM described in this Standard may, in addition to the minimum feature set defined, contain any of the other features described in Table 3.10.4–2, 128K X 8 MPDRAM FEATURE SET TRUTH TABLE, and still meet the Standard. These logic features must operate exactly as defined in the table to conform to the Standard.

3.10.4.6 – 128K X 16, 256K X 8, & 256K X 16 MPDRAM MINIMUM FEATURE SET TRUTH TABLE

The 2Mb & 4Mb density MPDRAMs described in this Standard must contain, as a minimum, the feature set described in Table 3.10.4–3, 2Mb & 4Mb MPDRAM FEATURE SET TRUTH TABLE. Note: Release 5 contains a new TRUTH TABLE.

3.10.4.7 – 128K X 16, 256K X 8, & 256K X 16 MPDRAM EXTENDED FEATURE SET TRUTH TABLE INCLUDING REQUIRED MINIMUM OPTIONAL FEATURE SET

The 2Mb & 4Mb density MPDRAMs described in this Standard must, in addition to the minimum basic feature set defined in Par. 3.10.4.6, contain all of the minimum defined set of optional features if any of them are included. In addition, any of the other features described may be included. The basic and optional features are shown in Table 3.10.4–3, 2Mb & 4Mb MPDRAM FEATURE SET TRUTH TABLE. These logic features must operate exactly as defined in the table to conform to the Standard. Note: Release 5 contains a new TRUTH TABLE.

3.10.4.8 – SPLIT REGISTER WITH PROGRAMMABLE STOPS FOR MPDRAM

This standard describes an option internal architectural feature which is applicable to the SERIAL PORT in MPSRAMs. The details are shown in Figure 3.10.4–2.

3.10.4.8 – SPLIT REGISTER WITH PROGRAMMABLE STOPS FOR MPDRAM

This standard describes an option internal architectural feature which is applicable to the SERIAL PORT in MPSRAMs. The details are shown in Figure 3.10.4–2.

3.10.4.9 – PIPELINED FAST PAGE MODE FOR MPDRAM

This standard describes the operational characteristics of an optional serial access data mode for the RAM PORT of MPDRAMs. The details and timing diagrams are given in Figures 3.10.4–3A and 3.10.4–3B.

3.10.4.10 – EXTENDED DATA OUT FAST PAGE MODE FOR MPDRAM

The EXTENDED DATA OUT FAST PAGE MODE defined in Sec. 3.9.5, DRAM OPTIONAL Features, on Page 3.9.5–11, Par. 1.4 is also applicable to MPDRAM as is needed. The mode is further defined with timing diagrams in Fig. 3.10.4–4.

3.10.4.11 – SAM OPTIONS FOR 4Mb MPDRAM

For 4 Mb MPDRAMs organized as 256K x 16, there are two options for the length of the SAM (Serial Access Memory). It may be either (1), 256 (Half SAM) or (2), 512 bits (Full SAM) for a 512 Column Page Depth. The details of these two options are described in Figs. 3.10.4–5A and 3.10.4–5B.

3.10.4.12 – Synchronous GRAM Special Mode Set Procedure

This standard defines a procedure for setting SPECIAL OPERATIONAL MODES into a Synchronous Graphics DRAM. A timing diagram and logic truth table are given in Fig. 3.10.4–6 on Page 3.10.4–15.

3.10.4.13 – Synchronous MPDRAM Special Mode Set Procedure

This standard defines a procedure for setting SPECIAL OPERATIONAL MODES into a Synchronous Multiport DRAM. A timing diagram and logic truth table are given in Fig. 3.10.4–7 on Page 3.10.4–16.

3.10.4.14 – Synchronous GRAM OPERATIONAL FUNCTION TABLES

This standard gives a set of functional truth tables for Synchronous Graphics DRAM. Three truth tables are given that define all standard operational functions. They are given in Tables 3.10.4–4A⇒C on Pages 3.10.4–17⇒19.

3.10.4.15 – 8Mb MPDRAM FEATURE SET FUNCTION TABLE

The 8Mb MPDRAM described in this Standard must contain, as a minimum, the feature set described in Table 3.10.4–15 on Page 3.10.4–8. This standard applies to devices with any interface data word length.

3.10.4.16 – Extended Functions for SGRAM and MPDRAM.

These standards define two special write function operations for SGRAM and MPDRAM. The functions defined are:

Write–Per–Bit
Block Write

These logic features must operate exactly as defined in the table to conform to the Standard. Details of the standards are given on Page 3.10.4–6.

CYCLE	$\overline{RE}$				$\overline{CE}$	A(n)		DQ(n)			WRITE	RASTER	REGISTER			FUNCTION
CODE	$\overline{CE}$	TRG	$\overline{W}$	DSF	$\overline{SE}$	DSF	$\overline{RE}$	$\overline{CE}$	$\overline{RE}$	$\overline{CE}$	$\overline{CE}$, $\overline{W}$	MASK	OP'N	WM1	WM2	COLOR	
Mandatory Features																	
RT	1	0	1	0	X	X	ROW	TAP +MSB	X	X	X	X	X	X	X	X	READ TRANSFER CYCLE
RW	1	1	1	0	X	0	ROW	COL	X	-	DATA INPUT	NO	YES	X	USE	X	READ WRITE CYCLE (NON MASK)
RWNM	1	1	0	0	X	0	ROW	COL	WM1	-	DATA INPUT	NEW WM1	X	LOAD USE	X	X	READ WRITE CYCLE (NEW MASK DATA)
CBR	0	X	1	X	X	-	X	-	X	-	X	X	X	X	X	X	$\overline{CE}$ BEFORE $\overline{RE}$ REFRESH
Optional Features																	
SWT	0	0	0	1	X	-	ROW	-	X	-	X	OLD	X	USE	X	X	SELECTIVE SPLIT WRITE XFR CYCLE (OLD MASK)
LS	0	1	0	X	X	-	CODE	-	WM2	-	X	X	SET-UP	X	LOAD	X	LOGIC SET-UP CYCLE (RASTER OPERATION CODE)
MWT	1	0	0	0	0	X	ROW	TAP +MSB	WM1	X	X	NEW WM1	X	LOAD USE	X	X	MASK WRITE TRANSFER (NEW MASK)
PWT	1	0	0	0	1	X	ROW	TAP +MSB	WM1	X	X	NEW WM1	X	LOAD	X	X	PSEUDO WRITE TRANSFER CYCLE
FWT	1	0	0	1	X	X	ROW	X	WM1	X	X	NEW WM1	X	LOAD USE	X	USE	FLASH WRITE WITH MASK (NEW MASK DATA)
SRT	1	0	1	1	X	X	ROW	TAP +MSB	X	X	X	X	X	X	X	X	SPLIT READ TRANSFER
RWOM	1	1	0	1	X	0	ROW	COL	X	-	DATA INPUT	OLD WM1	X	USE	X	X	READ WRITE CYCLE (OLD MASK DATA)
LWR	1	1	1	1	X	0	ROW	COL	X	-	WM1	X	X	LOAD	X	X	LOAD WRITE MASK 1 REGISTER
BWNM	1	1	0	0	X	1	ROW	COL CA2-8	WM1	COL SEL	-	NEW WM1	X	LOAD USE	X	USE	BLOCK WRITE CYCLE (NEW MASK DATA)
BWOM	1	1	0	1	X	1	ROW	COL CA2-8	X	COL SEL	-	OLD WM1	X	USE	X	USE	BLOCK WRITE CYCLE (OLD MASK DATA)
BW	1	1	1	0	X	1	ROW	COL CA2-8	X	COL SEL	-	NO	X	X	X	USE	BLOCK WRITE (NO MASK)
LCR	1	1	1	1	X	1	ROW	COL	X	-	COLOR	X	X	X	X	LOAD	LOAD COLOR REGISTER

TABLE 3.10.4-1
256K BY 4 MPDRAM FEATURE SET TRUTH TABLE

256K BY 4 MPDRAM FEATURE SET TRUTH TABLE

CYCLE	RE				CE	A(n)		DQ(n)			WRITE	RASTER	REGISTER			FUNCTION
CODE	CE	TRG	W	DSF	SE	DSF	RE	CE	RE	CE	CE, W	MASK	OP'N	WM1	WM2	COLOR	
Mandatory Features																	
RT	1	0	1	0	0	ROW	TAP +MSB	0	0	0	0	0	0	0	0	0	READ TRANSFER CYCLE
RW	1	1	1	0	0	ROW	COL	0	-	DATA INPUT	NO	YES	0	USE	0	READ WRITE CYCLE (NON MASK)
RWNM	1	1	0	0	0	ROW	COL	WM1	-	DATA INPUT	NEW WM1	0	LOAD USE	0	0	READ WRITE CYCLE (NEW MASK DATA)
CBR	0	0	1	0	-	0	-	0	-	0	0	0	0	0	0	$\overline{CE}$ BEFORE $\overline{RE}$ REFRESH
Optional Features																	
SWT	0	0	0	1	0	-	ROW	-	0	-	0	OLD	USE	0	0	0	SELECTIVE SPLIT WRITE XFR CYCLE (OLD MASK)
LS	0	1	0	0	0	-	CODE	-	WM2	-	0	0	SET-UP	0	LOAD	0	LOGIC SET-UP CYCLE (FASTER OPERATION CODE)
MWT	1	0	0	0	0	0	ROW	TAP +MSB	WM1	0	0	NEW WM1	0	LOAD USE	0	0	MASK WRITE TRANSFER (NEW MASK)
PWT	1	0	0	0	1	0	ROW	TAP +MSB	WM1	0	0	NEW WM1	0	LOAD	0	0	PSEUDO WRITE TRANSFER CYCLE
FWT	1	0	0	1	0	0	ROW	0	WM1	0	0	NEW WM1	0	LOAD USE	0	USE	FLASH WRITE WITH MASK (NEW MASK DATA)
SRT	1	0	1	1	0	0	ROW	TAP +MSB	0	0	0	0	0	0	0	0	SPLIT READ TRANSFER
RWOM	1	1	0	1	0	0	ROW	COL	0	-	DATA INPUT	OLD WM1	0	USE	0	0	READ WRITE CYCLE (OLD MASK DATA)
LWR	1	1	1	1	0	0	ROW	COL	0	-	WM1	0	0	LOAD	0	0	LOAD WRITE MASK 1 REGISTER
BWNM	1	1	0	0	0	1	ROW	COL CA2-8	WM1	COL SEL	-	NEW WM1	0	LOAD USE	0	USE	BLOCK WRITE CYCLE (NEW MASK DATA)
BWOM	1	1	0	1	0	1	ROW	COL CA2-8	0	COL SEL	-	OLD WM1	0	USE	0	USE	BLOCK WRITE CYCLE (OLD MASK DATA)
BW	1	1	1	0	0	1	ROW	COL CA2-8	0	COL SEL	-	NO	0	0	0	USE	BLOCK WRITE (NO MASK)
LCR	1	1	1	1	0	1	ROW	COL	0	-	COLOR	0	0	0	0	LOAD	LOAD COLOR REGISTER

128K BY 8 MPDRAM FEATURE SET TRUTH TABLE

TABLE 3.10.4-2
128K BY 8 MPDRAM FEATURE SET TRUTH TABLE

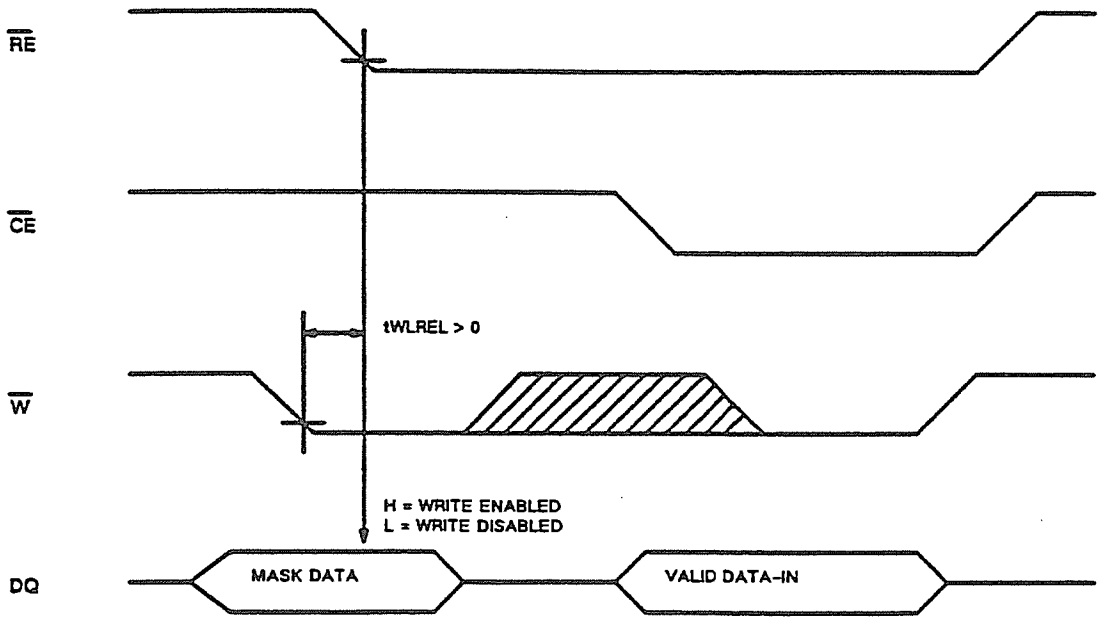


FIGURE 3.10.4-1
BIT WRITE TIMING

CYCLE	RE				CE	A(n)		DQ(n)		WRITE	REGISTER		FUNCTION
CODE	CE	TRG	W	DSF	DSF2	DSF	RE	CE.	RE	CE/W	MASK	WM	COLOR	
Mandatory Non-Optional Features (for 256K X 16, 128K X 16, or 256K X 8 MPDRAM)														
CBR [1]	0	X	1	0	0	—	X	—	X	—	—	—	—	CE BEFORE RE REFRESH (OPTION RESET)
RT	1	0	1	0	0	X	ROW	TAP	X	—	—	—	—	READ TRANSFER CYCLE
SRT	1	0	1	1	0	X	ROW	TAP	X	—	—	—	—	SPLIT READ TRANSFER CYCLE
RWM	1	1	0	0	0	0	ROW	COL	WM [1]	DATA	YES	LOAD/ USE	—	READ WRITE CYCLE (NEW MASK DATA)
RW	1	1	1	0	0	0	ROW	COL	X	DATA	NO	X	X	READ WRITE CYCLE (NO MASK)
Mandatory Optional Features (If any optional featured are used this full set must be included) (for 256K X 16, 128K X 16, or 256K X 8 MPDRAM)														
CBRS [1,4]	0	X	0	1	0	—	STOP5	—	X	—			—	CBR REFRESH/STOP (NO RESET)
CBRN [1]	0	X	1	1	0	—	X	—	X	—			—	CBR REFRESH (NO RESET)
MWT	1	0	0	0	0	X	ROW	TAP	WM [1]	—	YES	LOAD/USE	0	MASK WRITE TRANSFER (NEW MASK)
MSWT	1	0	0	1	0	X	ROW	TAP	WM [1]	—	YES	LOAD/USE	0	MASK SPLIT WRITE TRANSFER (NEW)
BWM	1	1	0	0	0	1	ROW	COL	WM [1]	COL	YES	LOAD/USE	USE	BLOCK WRITE CYCLE (NEW MASK)
FWM	1	1	0	1	0	X	ROW	X	WM [1]	—	YES	LOAD/USE	USE	FLASH WRITE (NEW MASK)
BW	1	1	1	0	0	1	ROW	COL	X	COL	NO	—	USE	BLOCK WRITE (NO MASK)
LCR	1	1	1	1	0	1	ROW	X	X	COLOR	—	—	LOAD	LOAD COLOR REGISTER
Optional Features (After the Mandatory Optional feature set is incorporated these features may be used at the option of the manufacturer)														
OPTION	0	0	0	0	0	—	MODE	—	DATA	—	—	—	—	OPTIONAL (512 POSSIBLE ENTRIES)
LMR [2]	1	1	1	1	0	0	ROW	X	X	WM1	—	LOAD	—	LOAD (OLD) MASK REGISTER
RWM(P)	1	1	0	0	1	0	ROW	COL	WM [17]	DATA	YES	LOAD USE	—	PFP[6] READ WRITE (NEW/OLD MASK)
BWM(P)	1	1	0	0	1	1	ROW	COL	WM [17]	COL	YES	LOAD USE	USE	PFP BLOCK WRITE (NEW/OLD MASK)
RW(P)	1	1	1	0	1	0	ROW	COL	X	DATA	NO	—	—	PFP READ WRITE (N0 MASK)
BW(P)	1	1	1	1	0	1	ROW	COL	X	COL	NO	—	USE	PFP BLOCK WRITE (NO MASK)
LS [3]	0	1	0	0	0	—	OPCODE	X	WM [2]	—	—	—	—	LOGIC FUNCTION SET CYCLE

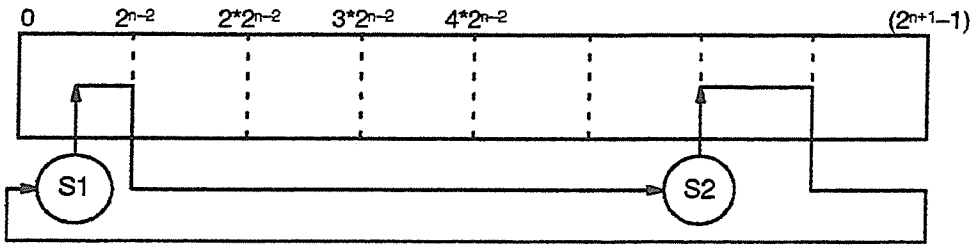
X = Don't care 0 or 1
— = NOT APPLICABLE
RE ONLY Refresh does not Reset STOP, LMR, or LS FUNCTIONS
All Control Signals are X prior to falling edge of RE.
1 CBRS, CBRN, and CBR all perform CAS (CE) before RAS (RE) refresh cycles. CBR is used to reset all options and either CBRS or CBRN are used to continue to refresh the RAM without clearing any of the options.
2 After LMR, RWM, BWM, MWT, MSWT, PWM, RWM(P), AND BWM(P), use old mask (CBR Resets to new mask. Use CBRS or CBRN to perform CAS Before RAS refresh while using old mask).
3 CBR Resets Logic Functions to source. Use CBRS or CBRN to perform CAS before RAS refresh while using Logic Function.
4 With CBRS all SAM operations use stop register.
5 STOP defines the Column on which shift out moves to the other half of the SAM
6 PFP is Pipelined Fast Page Mode Cycle.
7 After LMR, WM1 is only changed by LMR (CBR Resets).

2M & 4M COMBINED MPDRAM FEATURE SET TRUTH TABLE
TABLE 3.10.4-3

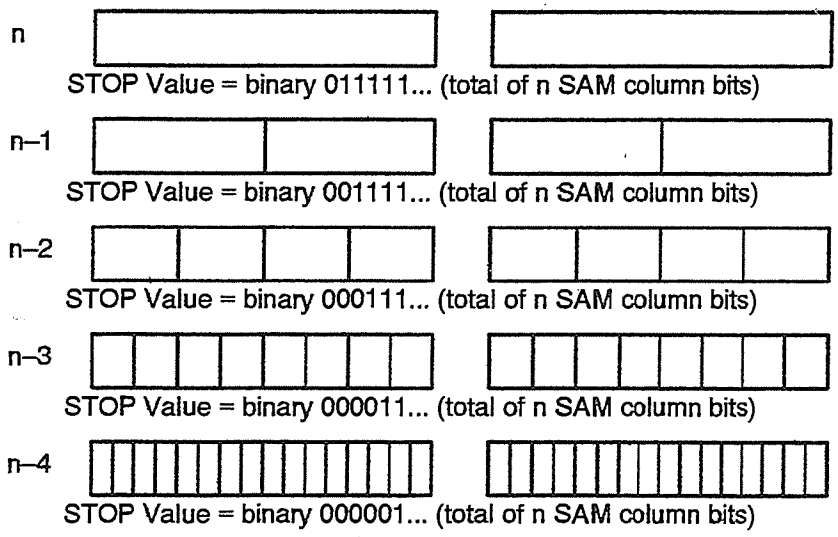
SPLIT REGISTER WITH PROGRAMMABLE STOPS

WHERE THE NUMBER OF COLUMNS IN THE SERIAL SHIFT REGISTER IS 2^{n+1}, n BEING A BINARY NUMBER WITH:
MSB = n
LSB = 0
STOP VALUE IS ASSERTED ON ADDRESS LINES AT RE\ FALLING IN CBRS CYCLE.IN THE FOLLOWING EXAMPLE, PROGRAMMABLE STOP IS COLUMN BIT (n–2).SWITCH TO OTHER HALF OF SAM OCCURS EVERY TIME BIT (n–2) CHANGES.

SINGLE SPLIT REGISTER WITH PROGRAMMABLE STOPS



STOP COLUMN BIT — SHIFT REGISTER ORGANIZATION



The definition of the split reister with programmable stops is intended to be valid for any size of shift register (SAM). The following table is included as additional clarification of the stop register value asserted on the address lines, relative to the actual stop widths for two popular sizes of the SAM.

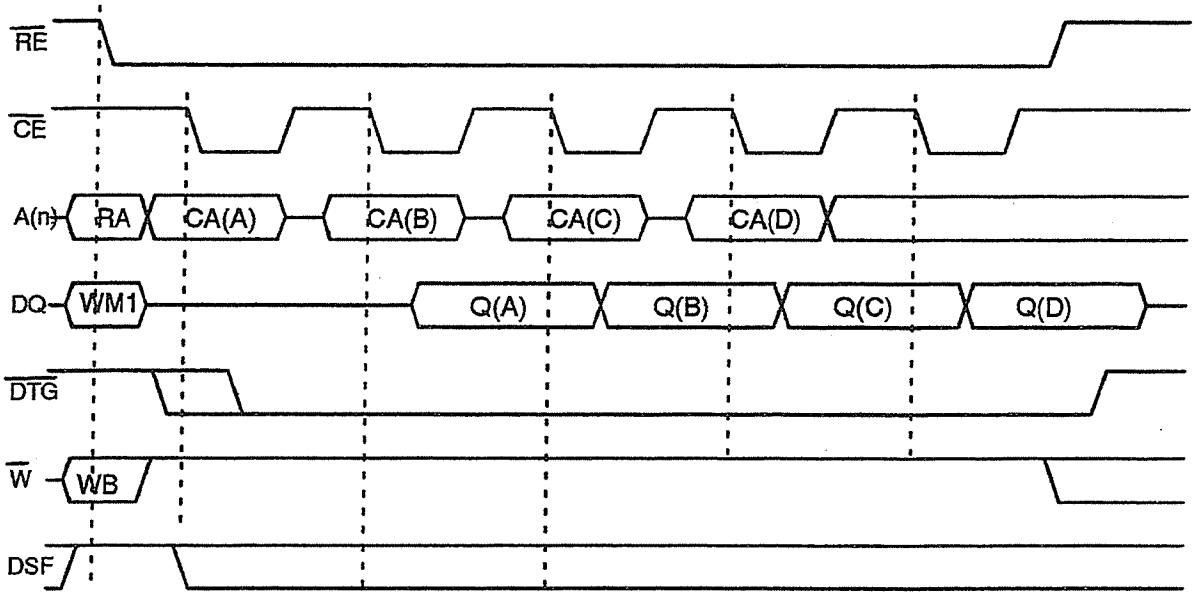
512 Bit SAM			STOP Width	256 Bit SAM		
Bit	A8	A0	Decimal	A8	A0	Bit
n	011111111		256	N/A		
n–1	001111111		128	–01111111		n
n–2	000111111		64	–00111111		n–1
n–3	000011111		32	–00011111		n–2
n–4	000001111		16	–00001111		n–3

FIGURE 3.10.4–2
SPLIT REGISTER WITH PROGRAMMABLE STOPS

PIPELINED FAST PAGE MODE

Pipelined fast page (PFP) mode is a read/write mode similar to page mode defined for RAM that actually "pipelines" data into and out of a RAM. During a write, the concept is to get data onto the die in the first CE state and into the RAM on the second CE state. During a read operation, the concept is to latch the read address on the first assertion of CE and assert the data for that address on the data lines on the next assertion of CE. Shown in the figures are sample timing diagrams illustrating PFP reads, writes, as well as read/write, and write/read.

PIPELINED FAST PAGE MODE READS



PIPELINED FAST PAGE MODE WRITES

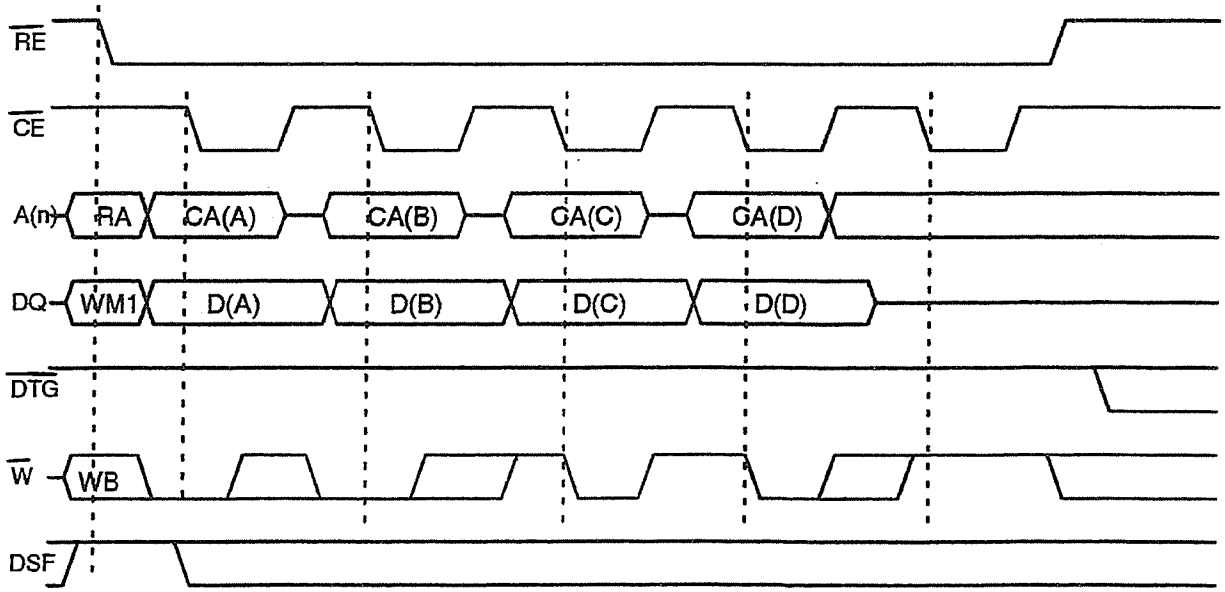
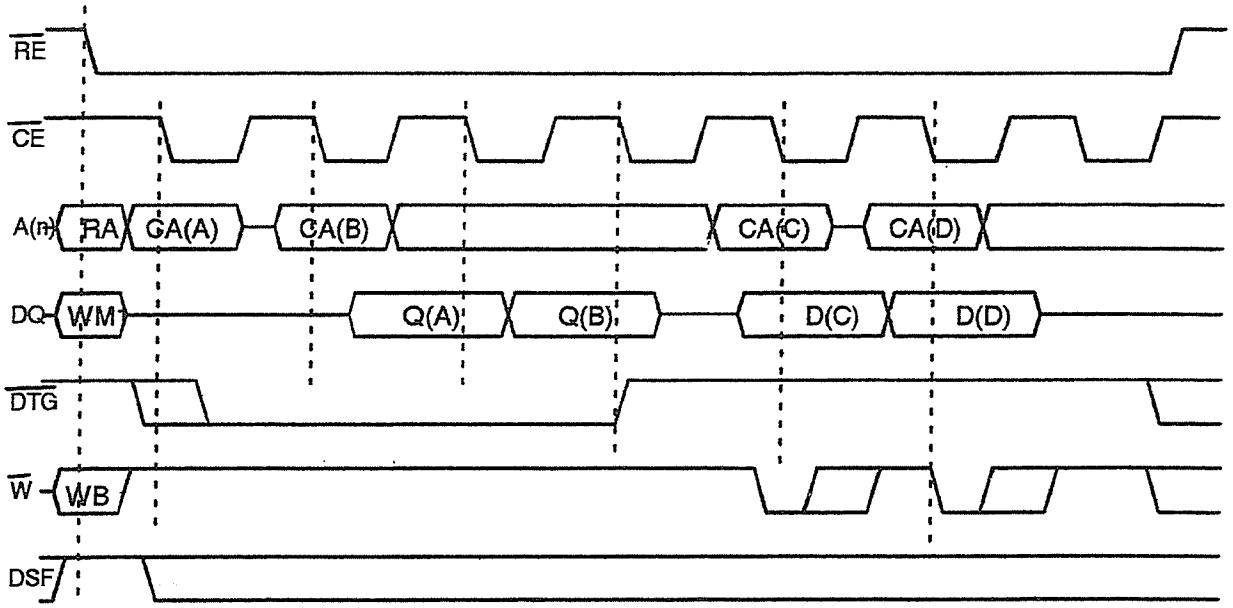


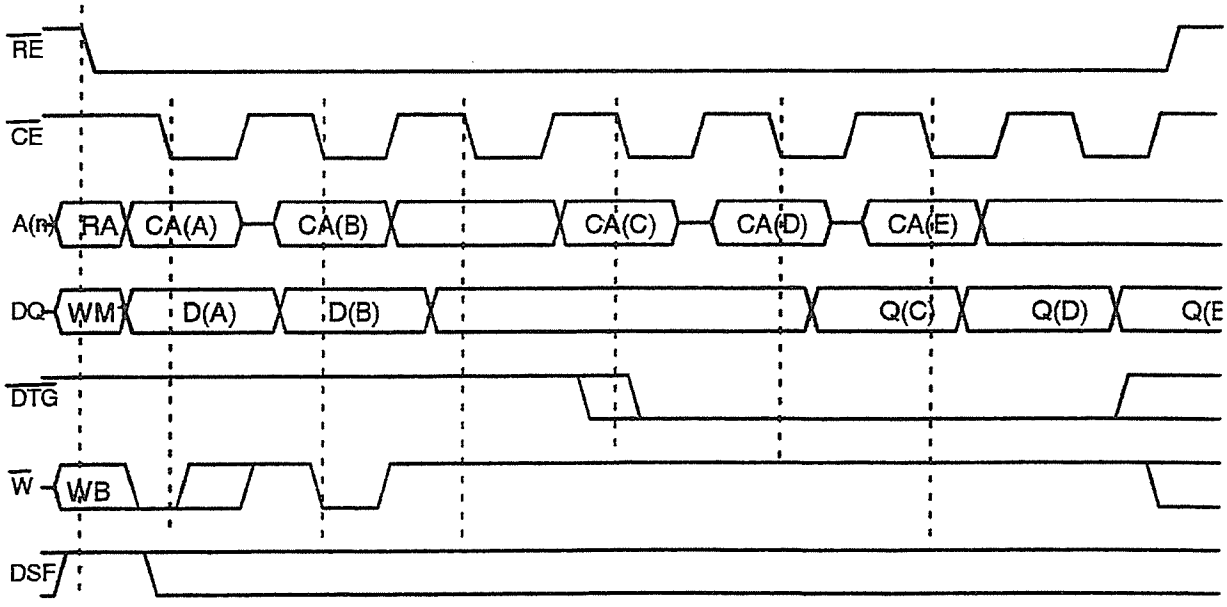
FIGURE 3.10.4–3A

PIPELINED FAST PAGE MODE

PIPELINED FAST PAGE MODE READ – WRITE



PIPELINED FAST PAGE MODE WRITE – READ



NOTE: BOTH EARLY WRITES AND LATE WRITES ARE REPRESENTED

FIGURE 3.10.4–3B

MPDRAM OPTIONAL MODES and CYCLES

This Standard defines an optional READ mode for address multiplexed Multi–Port DRAMs.

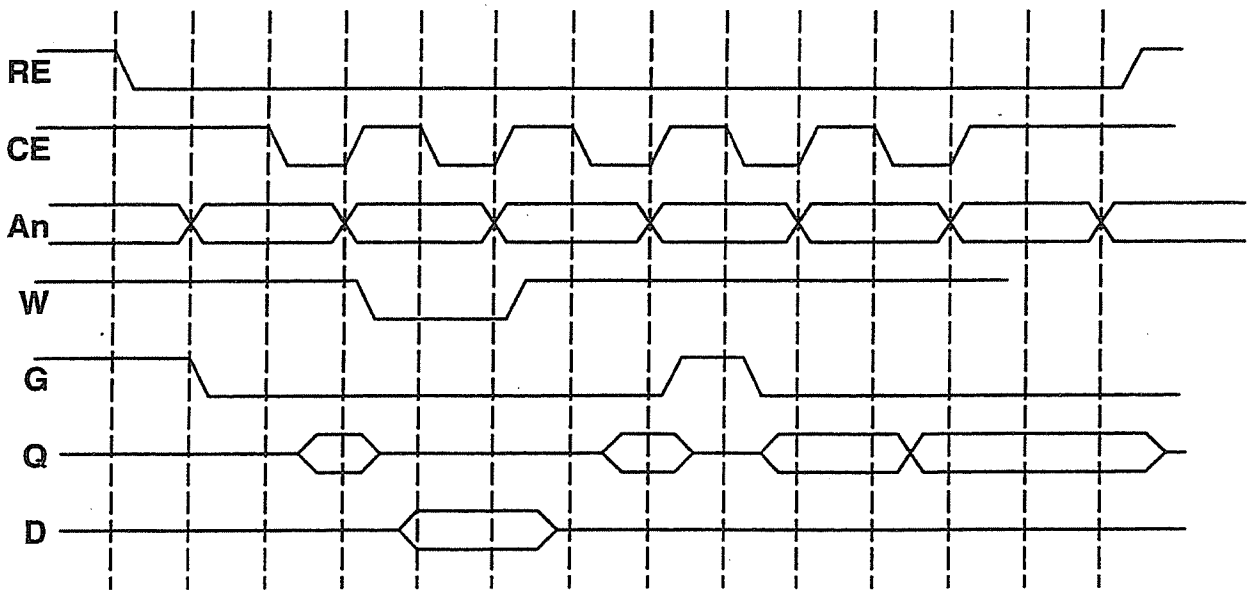
EXTENDED DATA OUT FAST PAGE MODE

This is a variation of the Fast Page Mode defined in Sec. 3.9.5.4, Par. 1.3.. It differs from Fast Page Mode as follows: 1) in a READ operation, the LH transition of CE\ with RE\ active will not cause the data out terminals to go into a high impedence state. Instead, the data out will remain valid with data from the previously read address. During sequential READ operations, the data out terminals will transition from old data to new data at a time defined by the performance specification for the part.
Any of the following conditions will cause the data out terminals to go to the high impedence state:

1) RE\ and CE\ are both inactive.
2) G\ is inactive.
3) W\ in active.

The following timing diagram illustrates this operating mode but is included for reference only.

EXTENDED DATA OUT FAST PAGE MODE



Data Out may be either translate or Active depending on the state of CE\ when the cycle is entered.

FIGURE 3.10.4–4
MPDRAM EXTENDED DATA OUT FAST PAGE MODE

SAM OPTIONS FOR 4Mb MPDRAM

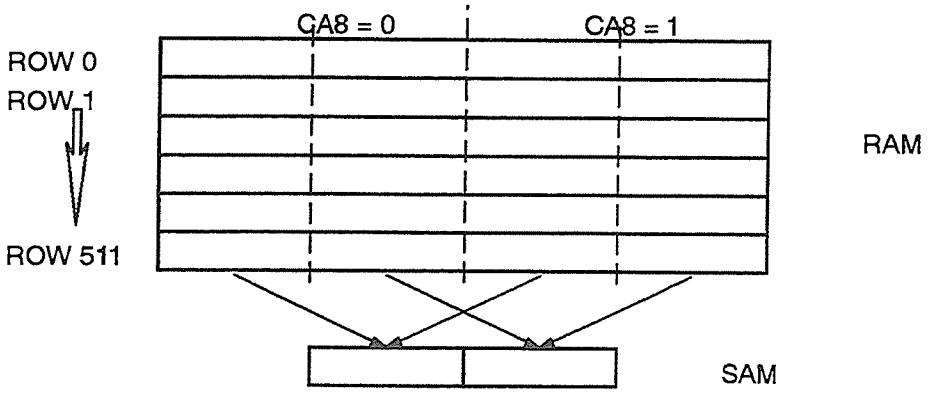
For 4 Mb MPDRAMs organized as 256K x 16, there are two options for the length of the SAM (Serial Access Memory). It may be either (1), 256 (Half SAM) or (2), 512 bits (Full SAM) for a 512 Column Page Depth. The details of these two options are described in the following sections.

OPTION 1: HALF SAM FOR 4Mb MPDRAM

For 4 Mb MPDRAMs organized as 256K x 16, the length of the SAM (Serial Access Memory) may be 256 bits for each 256K array. In the Split Register Mode, the register shall conditionally be divided in half by the most significant Column Address (CA8) or the second most significant column address (CA7) depending on whether the part is in stop register mode or not. The internal swapping of these two address pins is dependent on stop register mode for ALL RAM AND SAM OPERATIONS is necessary to allow for system level compatibility with the 512 bit SAM parts. Both possibilities are detained in the following discussion.

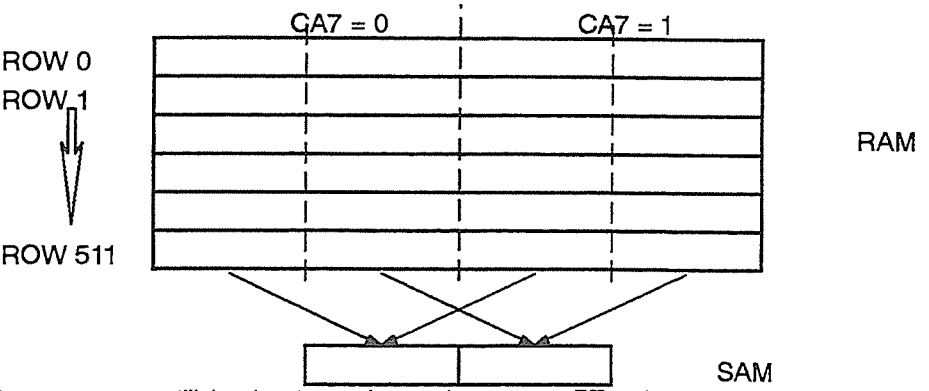
If a CBRS cycle has not occured since the last CBR (reset) cycle, the following conditions are true: The half of the ROW to be transfered into the SAM is determined by the MSB of the Column address (CA8). The internal state of CA7 for SAM operations can only be set by an RT cycle. During SRT cycles, the internal state of CA7 will be determined by an internal counter and the actual value of the CA7 input pin will be ignored to allow for system level compatibility with the 512 bit SAM parts.

ADDRESS MAPPING FOR 256 BIT SAM WITH 512 BIT PAGE



If a CBRS cycle has occured since the last CBR (reset) cycle, the following conditions are true: The half of the ROW to be transfered into the SAM is determined by the second MSB of the Column address (CA7). The internal state of CA8 for SAM operations can only be set by an RT cycle. During SRT cycles, the internal state of CA8 will be determined by an internal counter and the actual value of the CA8 input pin will be ignored to allow for system level compatibility with the 512 bit SAM parts.

ADDRESS MAPPING FOR 256 BIT SAM WITH 512 BIT PAGE



NOTE 1: For systems **not** utilizing the stop register, twice as many RT cycles must be performed if not using SRT, and twice as many SRT cycles must be performed if SRT cycles are used

NOTE 2: for systems utilizing the stop register, only stop values of 128 or less will allow for system compatibility. No additional transfer cycles are necessary.

FIGURE 3.10.4-5A

4Mb MPDRAM 256 COLUMN SAM

OPTION 2: FULL SAM FOR 4Mb MPDRAM

For 4 Mb MPDRAMs organized as 256K x 16, the length of the SAM (Serial Access Memory) shall be 512 bits for each 256K array. In the Split Register Mode, the register shall be divided in half by the most significant Column Address (CA8). The internal state of CA8 for SAM operation can only be set by an RT cycle. During SRT cycles the internal state of CA8 will be determined by an inter counter and the actual value of CA8 input will be ignored to allow for system level compatibility with the 256 bit SAM parts.

ADDRESS MAPPING FOR 512 BIT SAM WITH 512 BIT PAGE

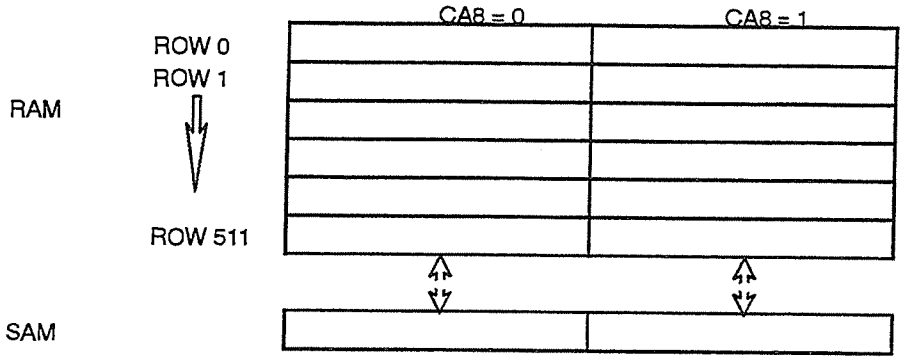
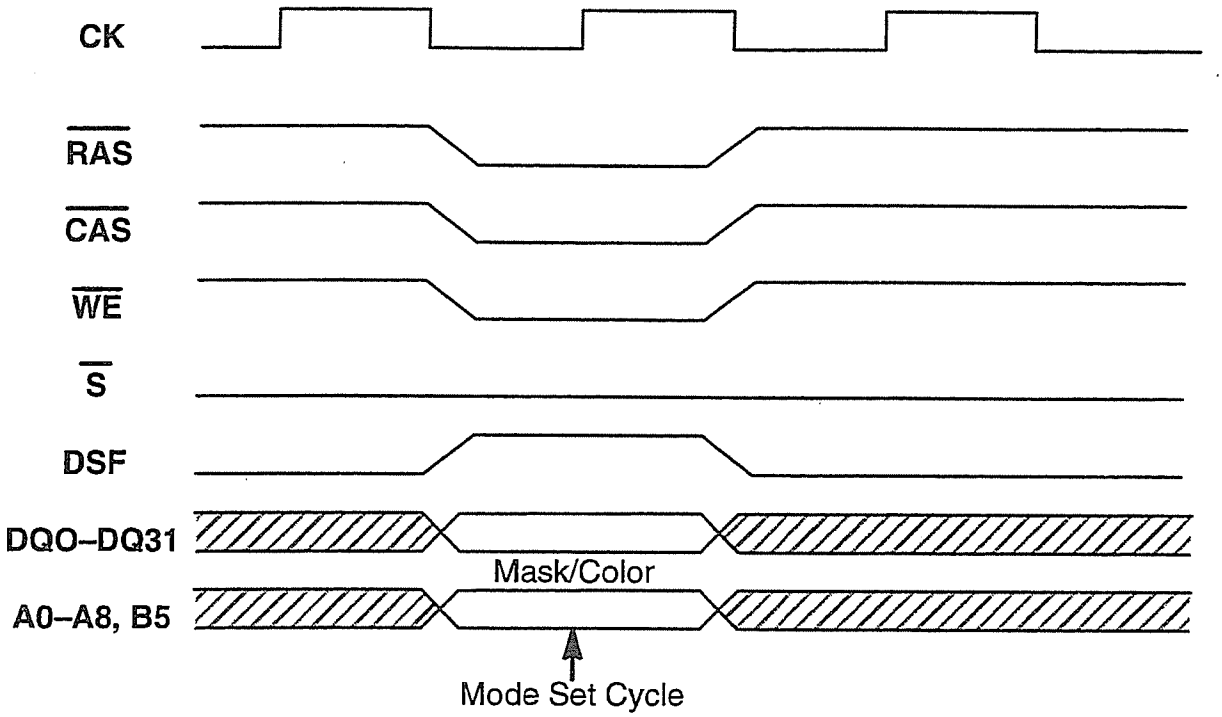


FIGURE 3.10.4-5B
4Mb MPDRAM 512 COLUMN SAM

Synchronous GRAM Special Mode Set Procedure

The following cycle details shall be used to set special modes into a Synchronous Graphics DRAM.

1. Special Mode Register Set Cycle



2. Mode Field

B5	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	LC	LM	0	0	0	0	0

The address field used to establish the Special Mode shall be as follows:

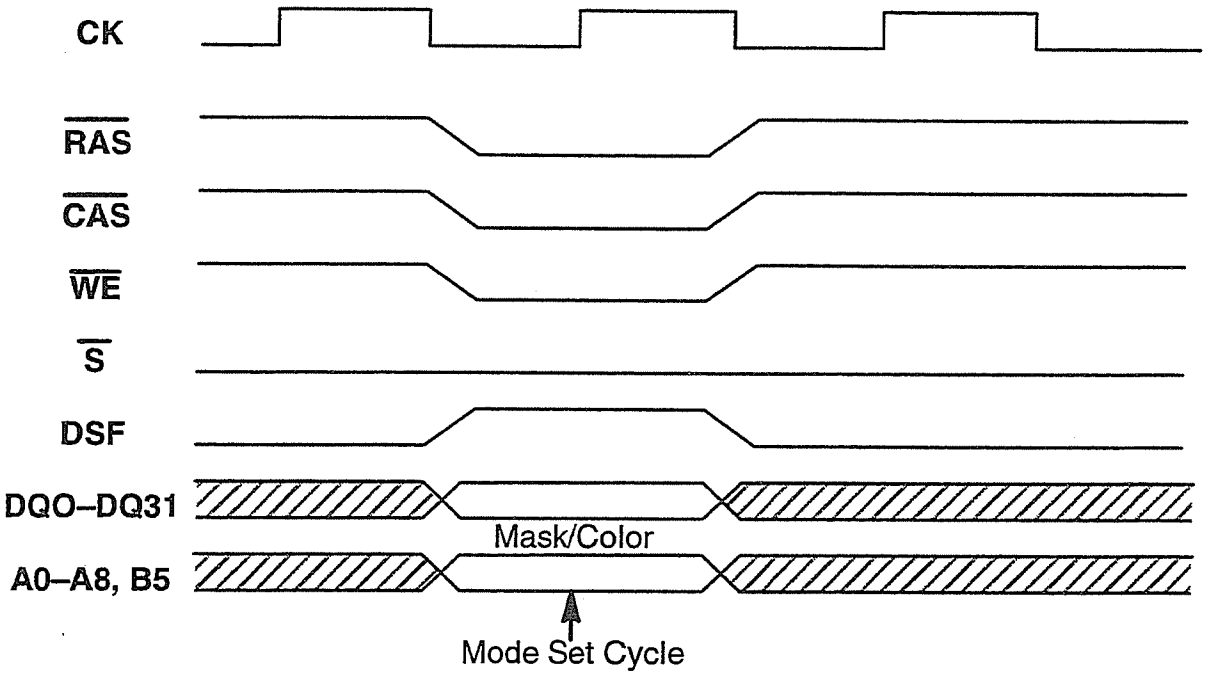
Address	Field	Value	Mode
A4⇒A0	Field for SVRAM	00000	
A5	Load Mask Register Set (LM)	0	Unchanged
		1	Load
A6	Load Color Register Set (LC)	0	Unchanged
		1	Load
A8⇒A7, B5	Mode Set Command	000	

FIGURE 3.10.4–6
SYNCHRONOUS GRAM SPECIAL MODE SET PROCEDURE

Synchronous MPDRAM Special Mode Set Procedure

The following cycle details shall be used to set special modes into a Synchronous MPDRAM. (VRAM)

1. Special Mode Register Set Cycle



2. Mode Field

B5	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	LC	LM	LS	SR	SR	SR	SR

The address field used to establish the Special Mode shall be as follows:

Address	Field	Value	Mode Number Columns/Half
A3⇒A0	Stop Register Set (SR)	1111	256 Columns
		0111	128 Columns
		0011	64 Columns
		0001	32 Columns
		0000	16 Columns
A4	Load Stop Register Set (LS)	0	Unchanged
		1	Load
A5	Load Mask Register Set (LM)	0	Unchanged
		1	Load
A6	Load Color Register Set (LC)	0	Unchanged
		1	Load
A8⇒A7, B5	Mode Set Command	000	

Note: The case where A5=A6=1 is illegal

FIGURE 3.10.4-7

SYNCHRONOUS MPDRAM SPECIAL MODE SET PROCEDURE

SGRAM FUNCTION TABLE

CURRENT STATE	$\overline{S}$	$\overline{TR}$	DSF	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
IDLE	H	X	X	X	X	X	X	NOP
	L	X	X	H	H	H	X	NOP
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	H	X	H	L	X	BA, CA	ILLEGAL[2]
	L	L	X	H	L	H	CA	Latch Tap Address[7]
	L	H	L	L	H	H	BA, RA	Row (&Bank) active; Latch Row Address; No Mask
	L	H	H	L	H	H	BA, RA	Row (&Bank) active; Latch Row Address; Use Mask
	L	L	L	L	H	H	BA, RA	Read Transfer; Latch Row Address ⇒ Precharge
	L	L	H	L	H	H	BA, RA	Split Read Transfer; Latch Row Address ⇒ Precharge
	L	H	L	L	H	L	BA, AP	NOP[4]
	L	H	H	L	H	L	X	ILLEGAL
	L	L	X	L	H	L	X	ILLEGAL
	L	H	L	L	L	H	X	Auto–Refresh[6]
	L	H	H	L	L	H	X	ILLEGAL
	L	L	X	L	L	H	X	ILLEGAL
	L	H	L	L	L	L	Op–code	Mode Register Access[6]
	L	H	H	L	L	L	Op–code	Special Register Access[5]
	L	L	X	L	L	L	X	ILLEGAL
ROW ACTIVE	H	X	X	X	X	X	X	NOP
	L	X	X	H	H	H	X	NOP
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	H	L	H	L	H	BA, CA, AP	Begin Read; Latch CA; Determine AP
	L	H	H	H	L	H	X	ILLEGAL
	L	L	X	H	L	H	CA	ILLEGAL[2]
	L	H	L	H	L	L	BA, CA, AP	Begin Write; Latch CA; Determine AP
	L	H	H	H	L	L	BA, CA, AP	Block Write; Latch CA; Determine AP
	L	L	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	H	L	L	H	L	BA, AP	Precharge
	L	H	H	L	H	L	X	ILLEGAL
	L	L	X	L	H	L	X	ILLEGAL
	L	X	X	L	L	H	X	ILLEGAL
	L	H	L	L	L	L	Op–code	ILLEGAL
	L	H	H	L	L	L	Op–code	Special Register Access[5]
	L	L	X	L	L	L	X	ILLEGAL

TABLE 3.10.4–4 A
SGRAM FUNCTION TABLE

SGRAM FUNCTION TABLE (continued)

CURRENT STATE	$\overline{S}$	$\overline{TR}$	DSF	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
READ	H	X	X	X	X	X	X	NOP (Continue Burst to End;⇒Row Active)
	L	X	X	H	H	H	X	NOP(Continue Burst to End;⇒Row Active)
	L	H	L	H	H	L	X	RESERVED (Term. Burst);⇒Row Active
	L	H	H	H	H	L	X	ILLEGAL
	L	L	X	H	H	L	X	ILLEGAL
	L	H	L	H	L	H	BA, CA, AP	Term Burst, New Read, Determine AP[3]
	L	H	H	H	L	H	X	ILLEGAL
	L	L	X	H	L	H	CA	ILLEGAL[2]
	L	H	L	H	L	L	BA, CA, AP	Term Burst, Start Write, Determine AP[3]
	L	H	H	H	L	L	BA, CA, AP	Term Burst, Start Write, Determine AP[3]
	L	L	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	H	L	L	H	L	BA, AP	Term Burst, Precharge Timing for Reads
	L	H	H	L	H	L	X	ILLEGAL
	L	L	X	L	H	L	X	ILLEGAL
	L	X	X	L	L	X	X	ILLEGAL
WRITE	H	X	X	X	X	X	X	NOP(Continue Burst to End;⇒Row Active)
	L	X	X	H	H	H	X	NOP(Continue Burst to End;⇒Row Active)
	L	H	L	H	H	L	X	RESERVED (Term Burst);⇒Row Active
	L	H	H	H	H	L	X	ILLEGAL
	L	L	X	H	H	L	X	ILLEGAL
	L	H	L	H	L	H	BA, CA, AP	Term Burst, Start Read, Determine AP[3]
	L	H	H	H	L	H	X	ILLEGAL
	L	L	X	H	L	H	CA	ILLEGAL[2]
	L	H	L	H	L	L	BA, CA, AP	Term Burst, New Write, Determine AP[3]
	L	H	H	H	L	L	BA, CA, AP	Term Burst, Block Write, Determine AP[3]
	L	L	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	H	L	L	H	L	BA, AP	Term Burst, Precharge[3]
	L	X	X	L	L	X	X	ILLEGAL
READ with AUTO Precharge	H	X	X	X	X	X	X	NOP (Continue Burst to End;⇒Precharge)
	L	X	X	H	H	H	X	NOP (Continue Burst to End;⇒Precharge)
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	X	X	H	L	H	BA, CA, AP	ILLEGAL[2]
	L	X	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	X	BA, RA, AP	ILLEGAL[2]
	L	X	X	L	L	X	X	ILLEGAL
WRITE with AUTO Precharge	H	X	X	X	X	X	X	NOP (Continue Burst to End;⇒Precharge)
	L	X	X	H	H	H	X	NOP (Continue Burst to End;⇒Precharge)
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	X	X	H	L	H	BA, CA, AP	ILLEGAL[2]
	L	X	X	H	L	L	X	ILLEGAL
	L	X	X	L	H	X	BA, RA, AP	ILLEGAL[2]
	L	X	X	L	L	X	X	ILLEGAL

TABLE 3.10.4–4 B
SGRAM FUNCTION TABLE (Continued)

SGRAM FUNCTION TABLE (continued)

CURRENT STATE	$\overline{S}$	TR	$\overline{DSF}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
Precharging	H	X	X	X	X	X	X	NOP⇒idle after tRP
	L	X	X	H	H	H	X	NOP⇒idle after tRP
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	H	X	H	L	X	BA, CA, AP	ILLEGAL[2]
	L	L	X	H	L	H	CA	Latch Tap Address[7]
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	X	X	L	H	L	BA, AP	NOP[4]
	L	X	X	L	L	X	X	ILLEGAL
ROW Activating	H	X	X	X	X	X	X	NOP⇒Row Active after tRCD
	L	X	X	H	H	H	X	NOP⇒Row Active after tRCD
	L	X	X	H	H	H	X	ILLEGAL[2]
	L	X	X	H	L	X	BA, CA, AP	ILLEGAL[2]
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	X	X	L	H	L	BA, AP	ILLEGAL[2]
	L	X	X	L	L	X	X	ILLEGAL
WRITE Recovering	H	X	X	X	X	X	X	NOP
	L	X	X	H	H	H	X	NOP
	L	X	X	H	H	L	X	ILLEGAL[2]
	L	X	X	H	L	X	BA, CA, AP	ILLEGAL[2]
	L	X	X	L	H	H	BA, RA	ILLEGAL[2]
	L	X	X	L	H	L	BA, AP	ILLEGAL[2]
	L	X	X	L	L	X	X	ILLEGAL
Refreshing	H	X	X	X	X	X	X	NOP⇒idle after tRP
	L	X	X	H	H	X	X	NOP⇒idle after tRP
	L	X	X	H	L	X	X	ILLEGAL
	L	X	X	L	H	X	X	ILLEGAL
	L	X	X	L	L	X	X	ILLEGAL
Mode Register Accessing	H	X	X	X	X	X	X	NOP
	L	X	X	H	H	H	X	NOP
	L	X	X	H	H	L	X	ILLEGAL
	L	X	X	H	L	X	X	ILLEGAL
	L	X	X	L	X	X	X	ILLEGAL

ABBREVIATIONS

RA = Row Address BA = Bank Address Term = Terminate

CA = Column Address AP = Auto Precharge NOP = No Operation

NOTES:

1. All entries assume that CKE was active (HIGH) during the preceeding clock cycle and the current clock cycle.
2. Illegal to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy the "2n–rule", bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank(s) indicated by BA (and AP).
5. Legal only if all banks are in idle or row active state.
6. Illegal if any bank is not idle.
7. Illegal if any bank is not idle or precharging.

ILLEGAL = Device operation and/or data–integrity are not guaranteed

TABLE 3.10.4–4 C
SGRAM FUNCTION TABLE (Continued)

8 Mb BURST MPDRAM FUNCTION TRUTH TABLE

CYCLE	RE Fall					CE		A(n)		DQ(n)			FUNCTION
CODE	CE	TRG	W	DSF1	DSF2	DSF1	DSF2	RE	CE.	RE	CE	DQM	
OPTION	0	0	0	0	0	—	0	MODE	—	X	—	X	OPTIONAL
CBRR	0	X	1	0	0	—	0	X	—	X	—	X	CBR REFRESH (OPTION RESET)
CBRS	0	X	0	1	0	—	0	STOP Addr	—	X	—	X	CBR REFRESH STOP POINT SET
CBRSD	0	X	0	1	1	—	0	X	—	X	—	X	CBR REFRESH SDS MODE SET
CBRN	0	X	1	1	0	—	0	X	—	X	—	X	CBR REFRESH NO RESET
RT	1	0	1	0	0	0	0	ROW	TAP	X	X	X	READ TRANSFER CYCLE
SRT	1	0	1	1	0	0	0	ROW	TAP	X	X	X	SPLIT READ TRANSFER CYCLE
RWM	1	1	0	0	0	0	0	ROW	COL	WPBM	DATA IN	DQM	READ MASKED WRITE CYCLE
BRWM	1	1	0	0	1	0	0	ROW	COL	WPBM	DATA IN	DQM	BURST READ MASKED WRITE CYCLE
BWM	1	1	0	0	0	1	0	ROW	CA3–CA8 CA0=CR	WPBM	COL ADDR MASK	DQM	MASKED BLOCK WRITE CYCLE
RW	1	1	1	0	0	0	0	ROW	COL	X	DATA IN	DQM	READ WRITE CYCLE (NO MASK)
BRW	1	1	1	0	1	0	0	ROW	COL	X	DATA IN	DQM	BURST READ WRITE CYCLE (NO MASK)
BI	—	—	—	—	—	0	1	ROW	COL	X	X	X	BURST INTERRUPT
BW	1	1	1	0	0	1	0	ROW	CA3–CA8 CA0 = CR	X	COL ADDR. MASK	DQM	BLOCK WRITE
LCR	1	1	1	1	0	1	0	ROW	CA0 = CR	X	COLOR	DQM	LOAD COLOR REGISTER
LMR	1	1	1	1	0	0	0	ROW	X	X	WPBM	DQM	LOAD MASK REGISTER

X = Don't care 0 or 1 — = NOT APPLICABLE

NOTES: CR = 0 selects Color Register 0 CR = 1 selects Color Register 1
All states not defined are illegal. If used, device operation and/or data integrity are not guaranteed.

BYTE ENABLE TRUTH TABLE

	CE FALLING	
DQM0–DQM3		
DQM0	0	Byte Write Enable (DQ0–DQ7)
	1	Byte Write Disable (DQ0–DQ7)
DQM1	0	Byte Write Enable (DQ8–DQ15)
	1	Byte Write Disable (DQ8–DQ15)
DQM2	0	Byte Write Enable (DQ16–DQ23)
	1	Byte Write Disable (DQ16–DQ23)
DQM3	0	Byte Write Enable (DQ24–DQ31)
	1	Byte Write Disable (DQ24–DQ31)

8M BURST MPDRAM FUNCTION TABLE

8MB BURST MPDRAM FUNCTION TABLE
TABLE 3.10.4–5

Extended Functions for SGRAM and SVRAM

WRITE–PER–BIT WPB, for Synchronous Video RAMs (SVRAM), and Synchronous Graphics RAMs (SGRAM) is a function that selectively masks bits of data being written to the devices. The mask is stored in an internal register and applied to each bit of data written when enabled.

1) A Bank Active Command with DSF = 1 (high) enables Write–per–bit for the associated bank. A bank active command with DSF = O (low) disables Write–Per–Bit for the associated bank.

2) The mask used for Write per–bit operations is stored in the Mask Register accessed by Special Register Access command. When a mask bit = 1 (high), the associated data bit is written when a Write Command is executed and Write–per–bit has been enabled for the bank being written. When a mask bit = O (low) the associated data bit is unaltered when a Write Command is executed and Write–per–bit has been enabled for the bank being written.

3) No additional, timing conditions are required for Write per–bit operations. Write–per–bit writes can be either single writes, burst writes, or block writes.

4) DQM masking is the same for WPB and non–WPB writes.

BLOCK WRITE for Synchronous Multi–port DRAMs (SMPRAM), and Synchronous Graphics RAMs (SGRAM). A feature allowing the simultaneous writing of consecutive columns of data within RAM device during a single access cycle. During block write the data to be written comes from an internal "color" register and the DQ I/O pins are used for independent column selection. The block of columns to be written is aligned on 8 column boundaries and is defined by the column address with the 3 LSB's ignored.

1) A Write Command with DSF = 1 (high) enables Block Write for the associated bank. A Write Command with DSF = O (low) disables Block Write for the associated bank.

2) The block size is 8 columns. Where column = "n" bits for by "n" part.

3) The Color Register is the same width as the data port of the part. It is written via a special register access where data present on the DQ pins is copied into the internal color register. The color register provides the data to be copied to the 8 column locations during a block write cycle as masked by the DQ column select, WPB mask (if enabled), and DQM byte mask.

4) Column data masking is provided on an individual column basis for each byte of data. The column mask is driven on the DQ pins during a block write command. The DQ column mask function is segmented on a per byte basis (i.e. DQ[0:7] provides the column mask for data byte [0;7], DQ[8.15] provides the column mask for data byte [8:15] and so on). A DQ column mask of 1 (high) enables the particular column to be written while a value of 0 (low) disables writing of the data. The relationship between DQ bits and column within the block is logically equivalent within each byte (i.e. DQ[0] masks column [0] for data bits [0:7] DQ[8] masks column [0] for data bits [8:15], DQ[1] masks column [1] for data bits [0:7], DQ[9] masks column [1] for data bits 18:15], etc.).

5) Block Writes are always non–burst, independent of the burst length that has been programmed into the Mode Register. Back–to–back Block Writes are allowed provided that the specified Block Write cycle time is satisfied.

6) If Write–per–bit was enabled to the bank by executing a Bank Active Command with DSF=1 (high), then write–per–bit masking of the Color Register data is enabled. If Write–per–bit was disabled to the bank by executing a Bank Active Command with DSF=O (Low), then write–per–bit masking of the color Register data is disabled.

7) DQM masking provides independent data byte masking during block write exactly the same as it does during normal write operations, except that the control is extended to the 8 consecutive columns of the block write.

3.11 Synchronous Dynamic Random Access Memory (SDRAM)

The following SDRAM standards were developed by Committee 42.3. The devices described are compatible with TTL and/or one or more of the low voltage interface standards adopted by Committee JC–16 as defined in the individual device standards. The device standards require that the memory devices must operate with signal levels and power supply voltages that are consistent with those used in the logic family(s) specified.

3.11.1 Bit Wide SDRAM

No standards have been developed for devices with this configuration.

3.11.2 NIBBLE WIDE SDRAM

3.11.2.1 – 4M BY 4 SDRAM IN TSOP2

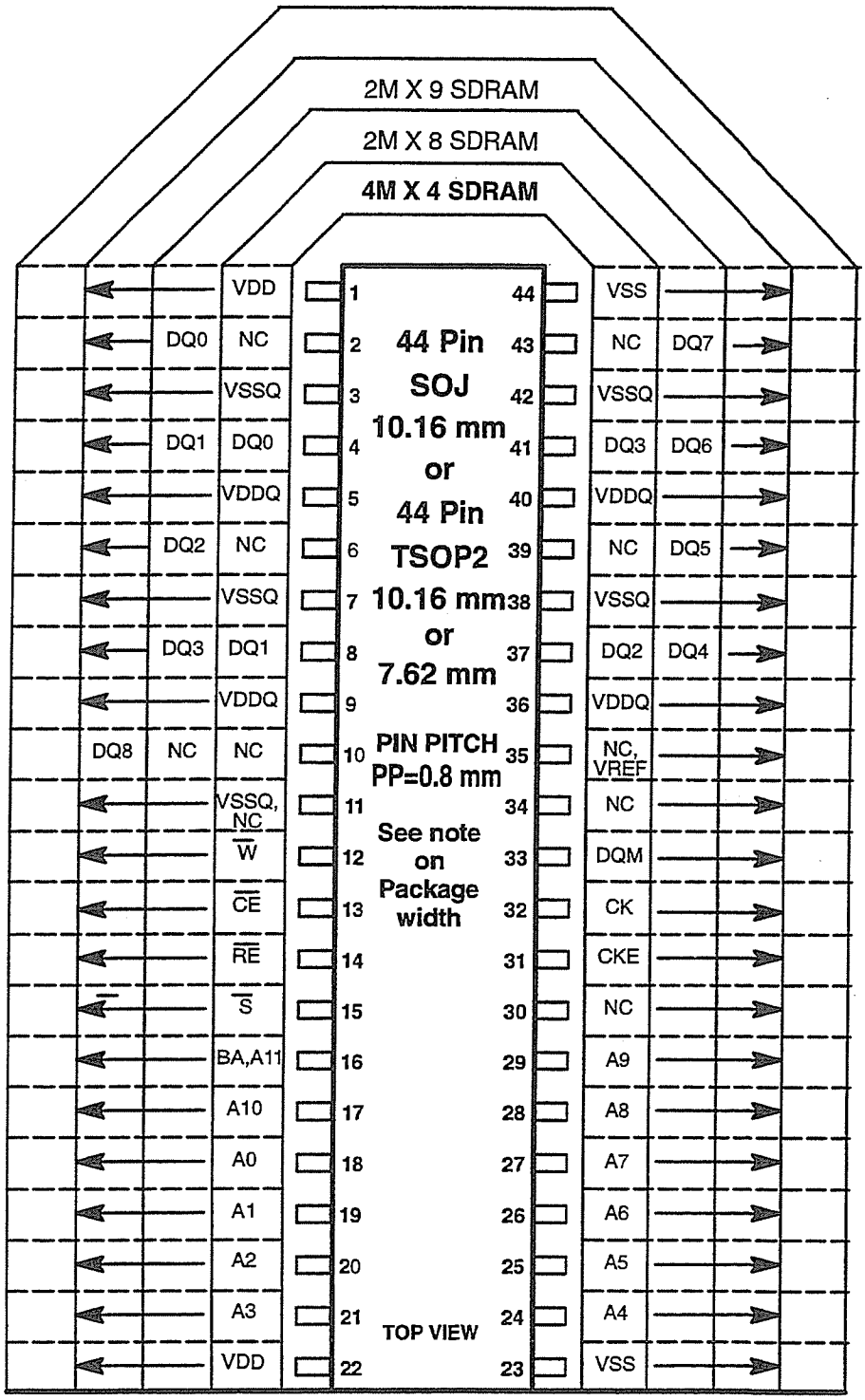
CAPACITY—4M WORDS OF 4 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—44 Pin TSOP2, 7.62 mm or 10.16 mm WIDE, 0.8mm PIN PITCH
—44 Pin SOJ 10.16 mm WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.2–1

3.11.2.2 – 16M BY 4 SDRAM IN TSOP2

CAPACITY—16M WORDS OF 4 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—54 Pin TSOP2, 10.16 mm WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.2–1

3.11.2.3 – 64M BY 4 SDRAM PIN ROTATION

CAPACITY—64M WORDS OF 4 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.11.2–5
NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

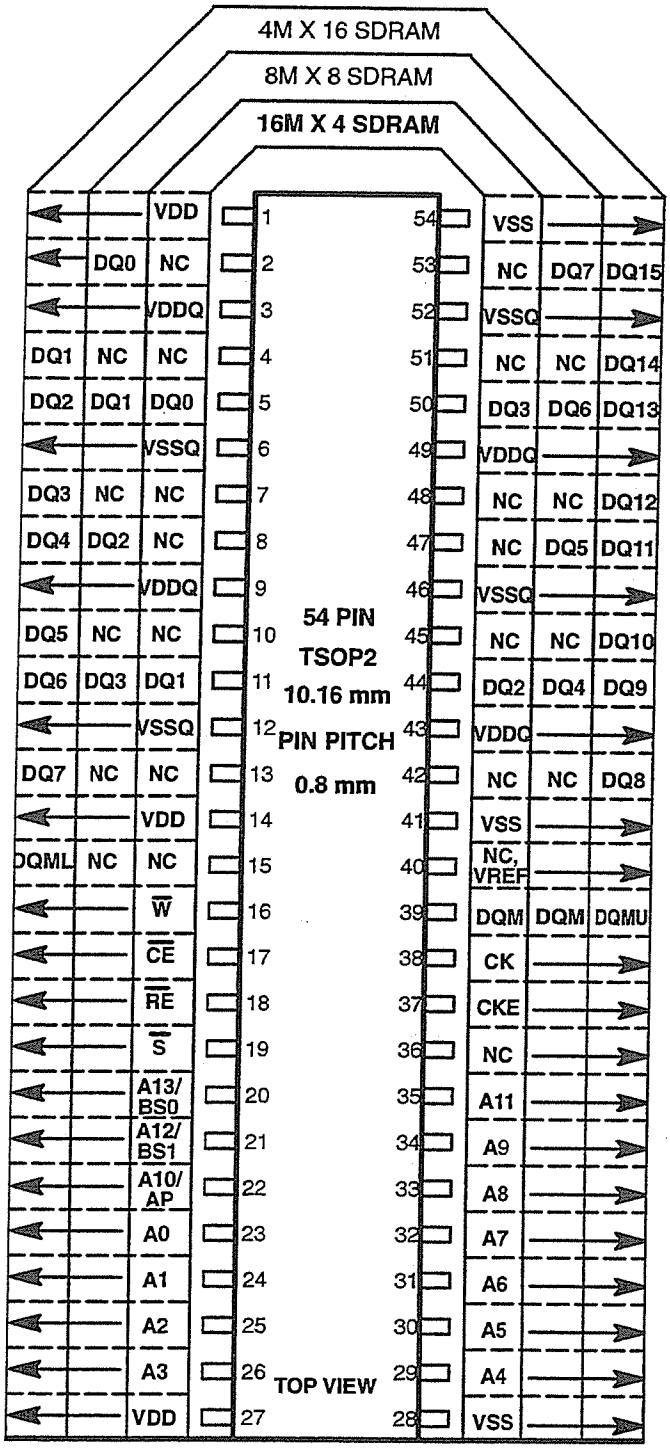


CONFIGURATION	4M X 4	2M X 8/9
ROW ADDRESS	A0 TO A11	A0 TO A11
COLUMN ADDRESS	A0 TO A9 & A11	A0 TO A8 & A11

Notes:
1) The VREF option on P35 was added when the 0.3" package was approved.

2) The JEDEC Std. No 30 designator for the TSOP2 package is PDSO–G
The 4M X 4 and 2M X 8 parts are also approved for delivery in a 7.62 mm package.

FIGURE 3.11.2–1
4M X 4 SDRAM IN TSOP2



	ROW ADDR.	COL ADDR
X4	A0⇒A13	A0⇒A9
X8	A0⇒A13	A0⇒A8
X16	A0⇒A13	A0⇒A7

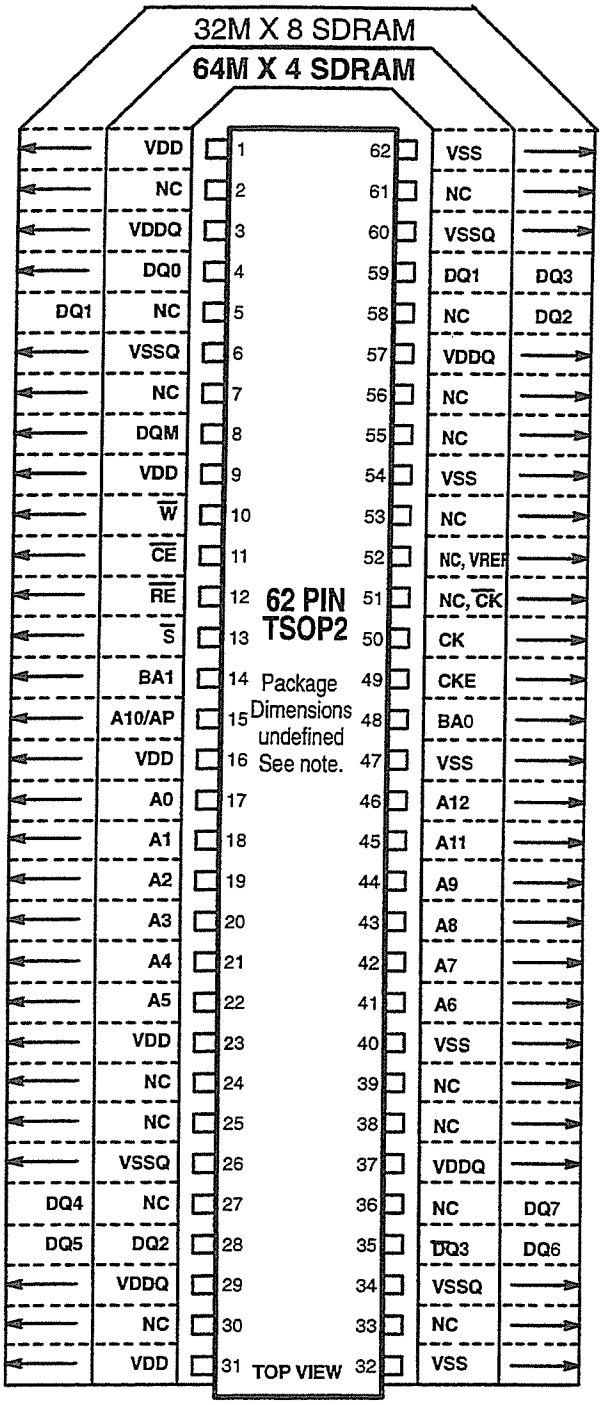
A10	AUTO PRECHARGE

BANKS	BANK SELECT ADDRESS
4	A13/A12
2	A13

* PACKAGE NOTES:

The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

FIGURE 3.11.2–2
16M BY 4 SDRAM IN TSOP2



Configuration	64M X 4	32M X 8
ROW ADDRESS	A0⇒A12	A0⇒A12
COLUMN ADDRESS	A0⇒A9,A11	A0⇒A9

NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. CBR refresh is the only standardized method of refreshing non–synchronous DRAMs with densities of 256Mb and higher.

3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms. (7.8 µs per row with 8K rows, 3.9 µs with 16K rows.

4. (NC, VREF) is VREF on devices that require an external voltage reference.

5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.

6. The VSSQ designator is used when the ground reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS).

7. BA0 is the Least Significant Bank Addr.

8. BA1 is the Most Significant Bank Addr.

9. A10/AP is row addr. A10, autoprecharge and precharge all banks input.

* NOTE: The JEDEC Std. 0 term for the TSOP–2 package is PDSO–G.

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.2–3
64M BY 4 SDRAM PIN ROTATION IN TSOP2

3.11.3 BYTE WIDE SDRAM

3.11.3.1 – 2M BY 8 or 9 SDRAM IN TSOP2

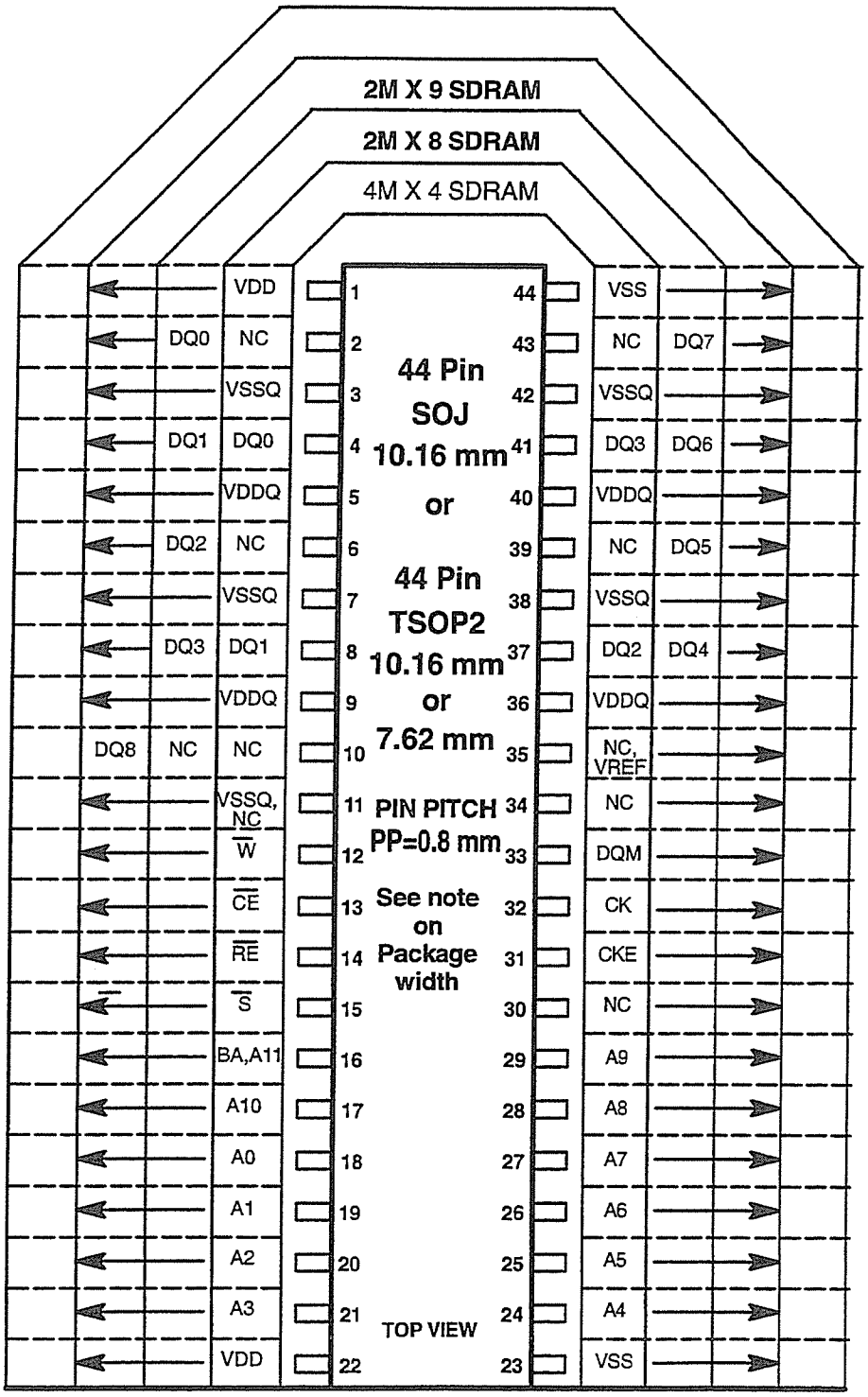
CAPACITY—2M WORDS OF 8 or 9 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
ELECTRICAL INTERFACE—TTL or LVTTL
PACKAGE—44 Pin TSOP2, 7.62 mm WIDE, 0.8mm PIN PITCH (2M X 8 part only)
PACKAGE—44 Pin TSOP2, 10.16 WIDE, 0.8mm PIN PITCH
PACKAGE—44 Pin SOJ, 10.16 WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.3–1

3.11.3.2 – 8M BY 8 SDRAM IN TSOP2

CAPACITY—8M WORDS OF 8 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—54 Pin TSOP2, 10.16 mm WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.3–2

3.11.3.3 – 32M BY 8 SDRAM PIN ROTATION

CAPACITY—32M WORDS OF 8 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.11.3–5
NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

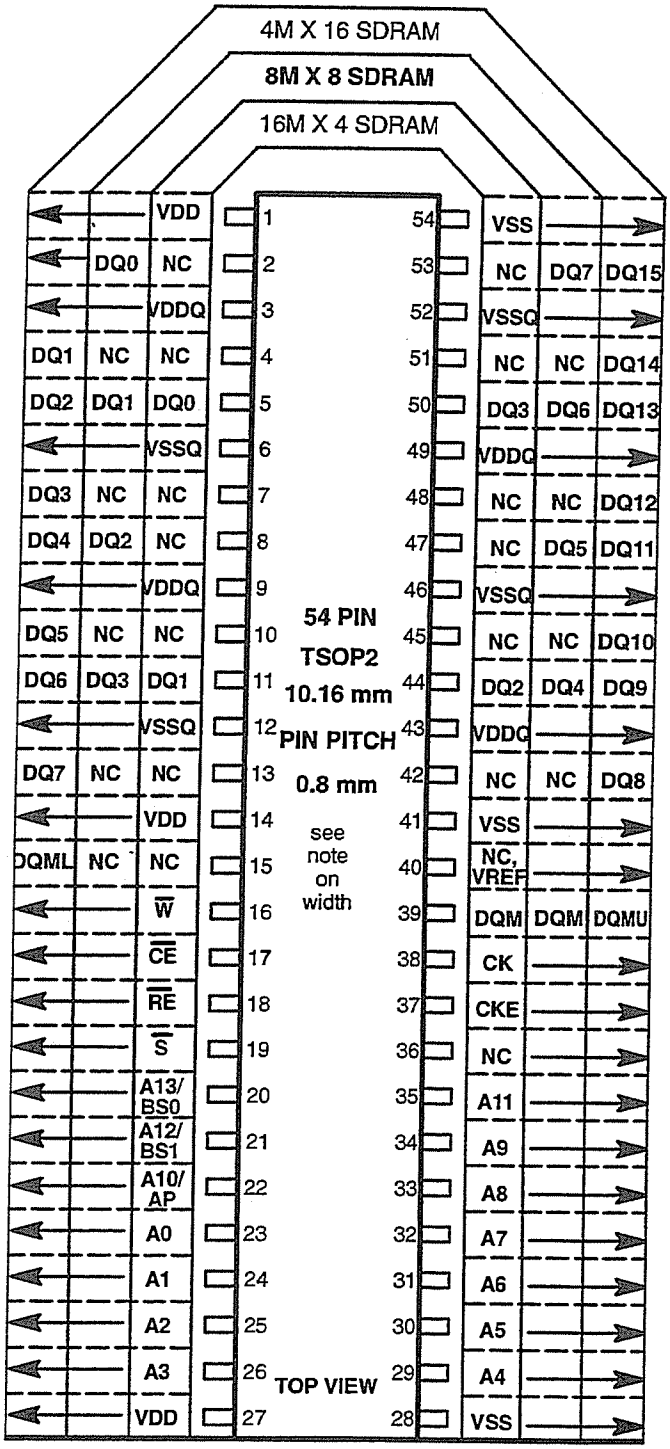


CONFIGURATION	4M X 4	2M X 8/9
ROW ADDRESS	A0 TO A11	A0 TO A11
COLUMN ADDRESS	A0 TO A9 & A11	A0 TO A8 & A11

Notes:
1) The VREF option on P35 was added when the 0.3" package was approved.

2) The JEDEC Std. No 30 designator for the TSOP2 package is PDSO–G
The 4M X 4 and 2M X 8 parts are also approved for delivery in a 7.62 mm package.

FIGURE 3.11.3–1
2M BY 8 OR 9 SDRAM IN TSOP2



	ROW ADDR.	COL ADDR
X4	A0⇒A13	A0⇒A9
X8	A0⇒A13	A0⇒A8
X16	A0⇒A13	A0⇒A7

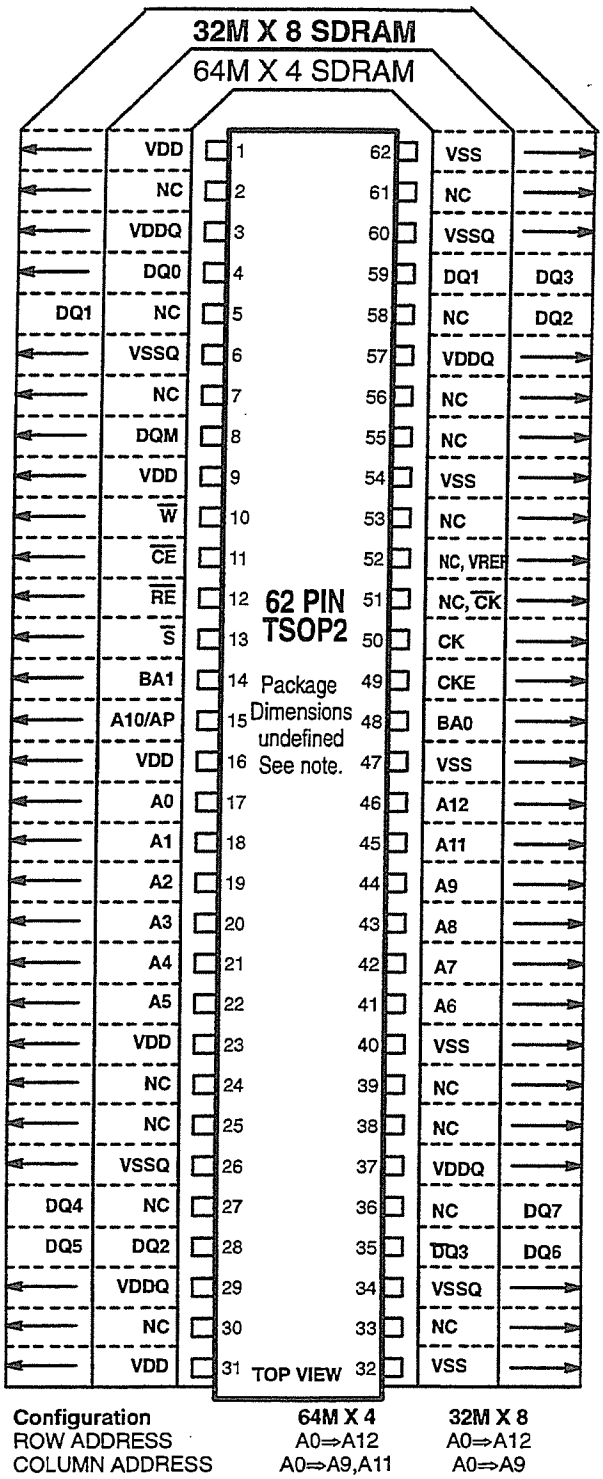
A10	AUTO PRECHARGE

BANKS	BANK SELECT ADDRESS
4	A13/A12
2	A13

* PACKAGE NOTES:

The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

FIGURE 3.11.3–2
8M BY 8 SDRAM IN TSOP2



Configuration	64M X 4	32M X 8
ROW ADDRESS	A0⇒A12	A0⇒A12
COLUMN ADDRESS	A0⇒A9,A11	A0⇒A9

NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. CBR refresh is the only standardized method of refreshing non–synchronous DRAMs with densities of 256Mb and higher.

3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms. (7.8 µs per row with 8K rows, 3.9 µs with 16K rows.

4. (NC, VREF) is VREF on devices that require an external voltage reference.

5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.

6. The VSSQ designator is used when the ground reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS).

7. BA0 is the Least Significant Bank Addr.

8. BA1 is the Most Significant Bank Addr.

9. A10/AP is row addr. A10, autoprecharge and precharge all banks input.

* NOTE: The JEDEC Std. 0 term for the TSOP–2 package is PDSO–G.

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.3–3
32M BY 8 SDRAM PIN ROTATION IN TSOP2

3.11.4 WORD WIDE SDRAM

3.11.4.1 – 256K BY 16 AND 1M BY 16 & 18 SDRAM IN TSOP2

CAPACITY—256K WORDS OF 16 BITS AND 1M WORDS OF 16 OR 18
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
ELECTRICAL INTERFACE—TTL or LOWER LEVEL INTERFACE CONSISTENT WITH THE VALUE OF VDD CHOSEN.
PACKAGE—50 Pin SOJ, 10.16 mm WIDE, 0.8mm PIN PITCH
PACKAGE—50 Pin TSOP2, 0.400" WIDE (10.16 mm), 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.4–1

NOTE: The 256K part has the same pinout as the SGRAM part shown in Fig. 3.10.3–3 with the exception of the DSF function on P 33.

3.11.4.2 – 2M & 4M BY 16 SDRAM IN TSOP2

CAPACITY—2M or 4M WORDS OF 16 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
PACKAGE—54 Pin TSOP2, 10.16 mm WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.4–2

3.11.4.3 – 16M BY 16 SDRAM IN TSOP2 PIN ROTATION

CAPACITY—16M WORDS OF 16 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
—This standard is for a 4 Bank version only.
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.11.4–3

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

3.11.4.4 – 256K BY 32 SDRAM IN QFP or TQFP

CAPACITY—256K WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—Synchronous address & control interface.
PACKAGE—100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm PP
PIN ASSIGNMENTS—FIG. 3.11.4–4

NOTE: This part has the same pinout as the SDRAM part shown in Fig. 3.10.3–4 with the exception of the DSF function on P 33.

3.11.4.5 – 2M BY 32 SDRAM IN TSOP2

CAUTION: See note in Fig. 3.11.4–5 regarding the use of this device.
CAPACITY—2M WORDS OF 32 BITS
LOGIC FEATURES—Multiplexed Address
—Synchronous address & control interface.
PACKAGE—84 PIN TSOP2, 10.16 mm WIDE, 0.5 mm PP
PIN ASSIGNMENTS—FIG. 3.11.4–5

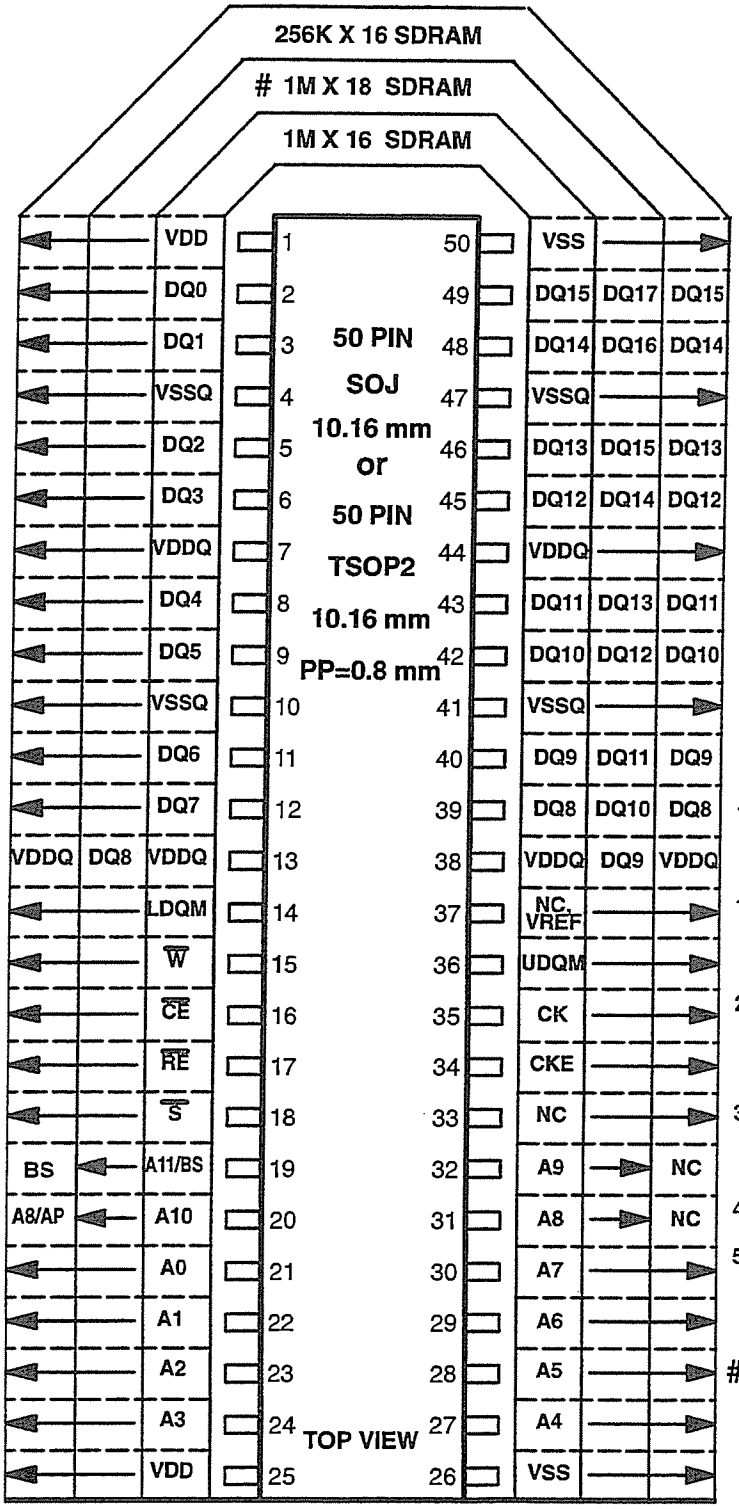
3.11.4.6 – 8M BY 32 SDRAM IN TSOP2 PIN ROTATION

CAPACITY—8M WORDS OF 32 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
—This standard is for a 4 Bank version only.
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.11.4–6

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

3.11.4.7 – 2M BY 32 & 36 SDRAM IN TSOP2

CAPACITY—8M WORDS OF 32 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
—This standard is for a 4 Bank version only.
PACKAGE—86 PIN TSOP2, 10.16 mm Wide, 0.5 mm PP
PIN ASSIGNMENT—Fig. 3.11.4–7



* Note: The JEDEC Standard 30 term for the TSOP–2 package is PDSO–G

1) Pin 20 (A10) id the auto–precharge input during read and write commands.

2) Pin 37 (NC, VREF) is VREF on devices that need an external voltage reference. On other devices, it is a NC.

3) All VDDQ and VSSQ pins may be VDD and VSS at the option of the supplier

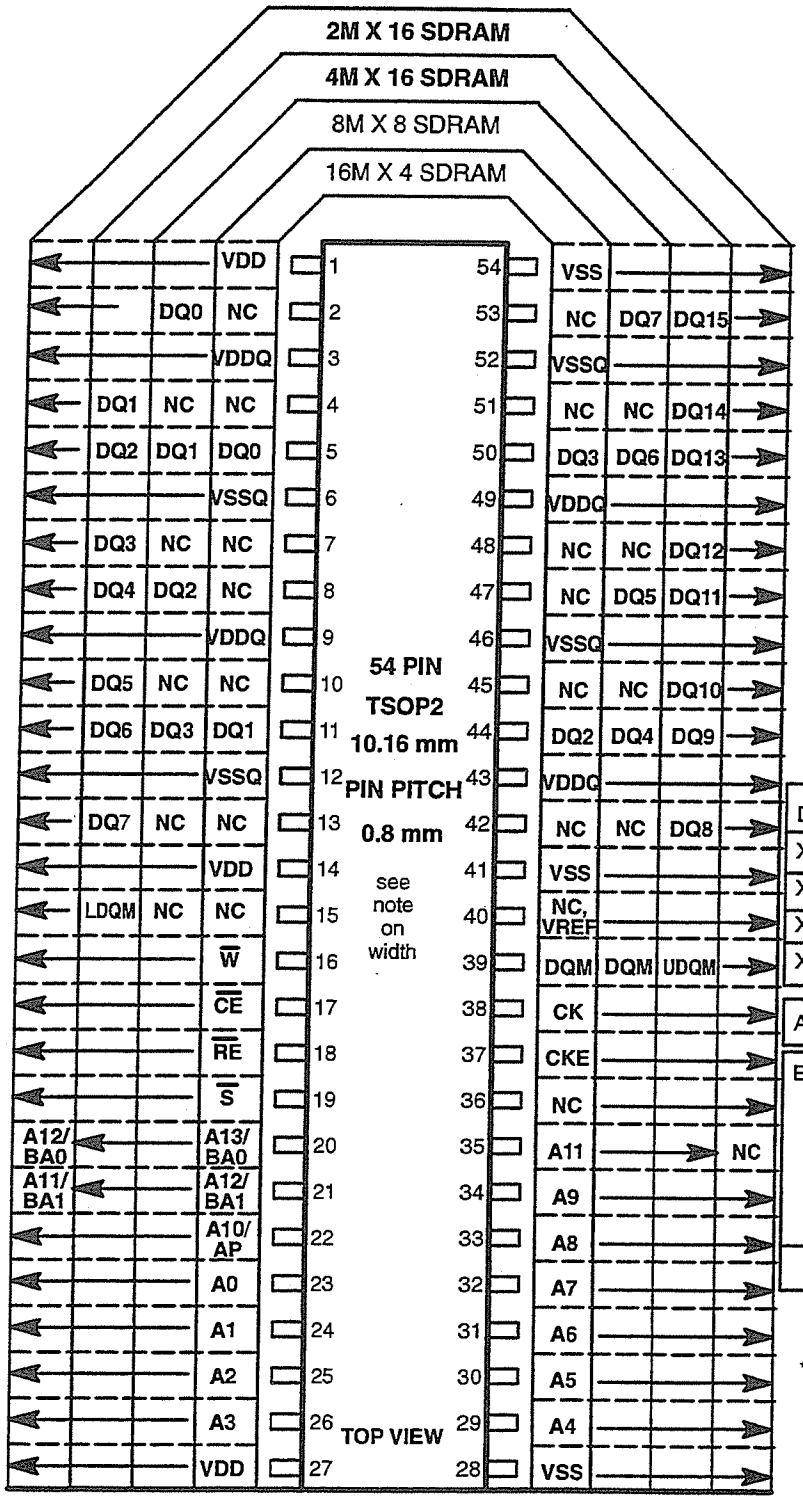
4) BS is the Bank Select Address

5) The 256K device has the same pinout as the 256K X 16 SGRAM shown in Fig 3.10.3–3 except for the lack of a DSF function on pin 33.

\# The 1M X 18 device is approved for use in the TSOP2 package only.

	256K	1M 1K RFSH	1M 4K RFSH
ROW/REFRESH ADDRESSES	A0 ⇒ A8	A0 ⇒ A9	A0 ⇒ A11
COLUMN ADDRESSES	A0 ⇒ A7	A0 ⇒ A9	A0 ⇒ A7

FIGURE 3.11.4–1
256K X 16 & 1M X 16/18 SDRAM IN SOJ & TSOP–2



Device	ROW ADDR.	COL ADDR
X4	A0⇒A13	A0⇒A9
X8	A0⇒A13	A0⇒A8
X16, 4M	A0⇒A13	A0⇒A7
X16, 2M	A0⇒A12	A0⇒A7

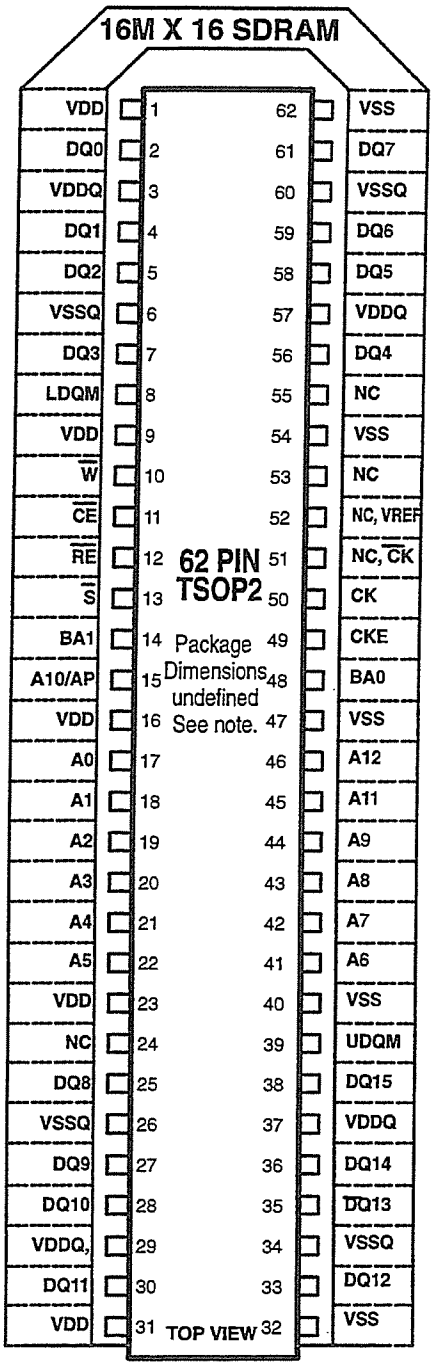
A10	AUTO PRECHARGE

BANKS	BANK SELECT ADDRESS
4	A13/A12
4 #	A12/A11
2	A13
2 #	A12
# 2M X 16	

* PACKAGE NOTES:

The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

FIGURE 3.11.4–2
2M & 4M BY 16 SDRAM IN TSOP2



Configuration	16M X 16
ROW ADDRESS	A0–A12
COLUMN ADDRESS	A0–A8

NOTES

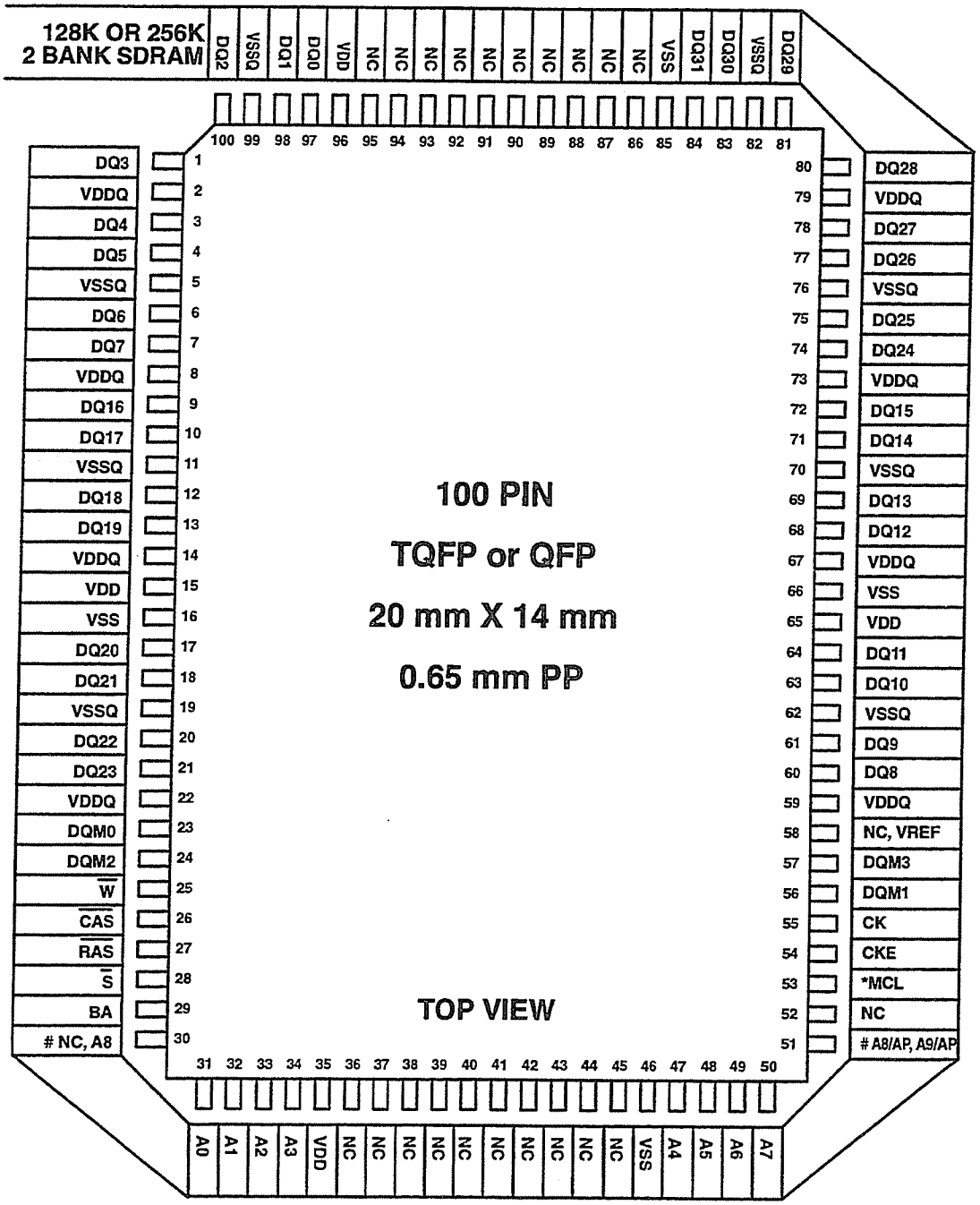
1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. The standard refresh interval (tREF) for 256Mb SDRAMs is 64ms.
3. (NC, VREF) is VREF on devices that require an external voltage reference.
4. BA0 is the least significant bank address
5. BA1 is the most significant bank address
6. A10/AP is row address A10, autoprecharge and precharge all banks.
7. (NC, $\overline{CK}$) is NC for devices using a single ended clock. $\overline{CK}$ is used for devices using a differential clock.
8. (NC, VREF) is VREF on devices that require an external voltage reference.
9. This standard is for a 4 Bank version only.

* NOTE: The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.4–3
16M BY 16 SDRAM PIN ROTATION IN TSOP2



Note: This pinout is for both 128K and 256K parts. The Pin assignments are as follows

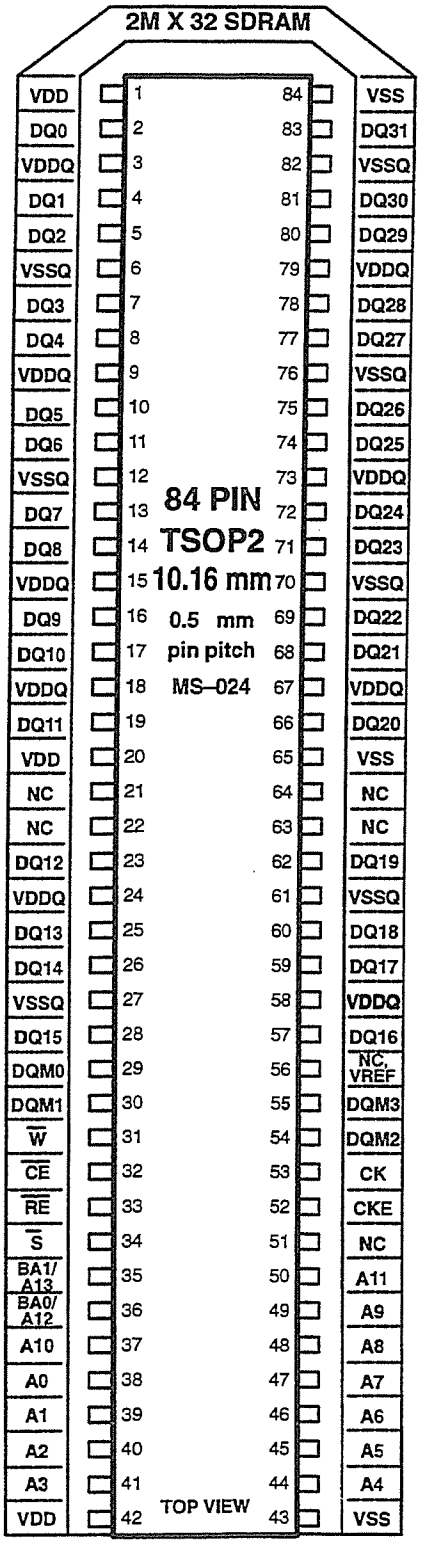
Configuration	P30	P51
128K x 2 Bank	NC	A8/AP;
256K X 2 Bank	A8	A9/AP

* Note: This part is a subset of the SGRAM shown in Fig. 3.10.3–4. P53 is DSF for the SGRAM version and MCL for the SDRAM.
MCL = Must Connect to Logic Low

Configuration	128K X 2	256K X 2
ROW ADDRESS	A0⇒A8,BA	A0⇒A9,BA
COLUMN ADDRESS	A0⇒A7	A0⇒A7
BANK SELECT		A9
REFRESH PERIOD	16 ms	32 ms
# ROWS REFRESH	1024	2048

FIGURE 3.11.4–4
128K & 256K BY 32, 2 BANK SDRAM IN QFP

Release 6r7



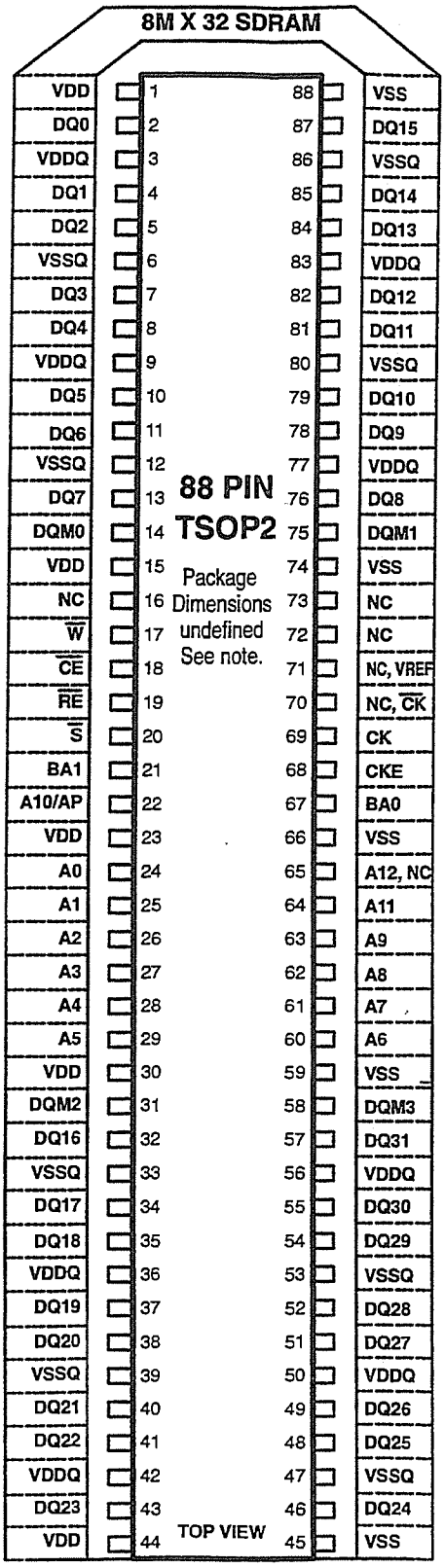
NOTE:
In addition to this pinout for a 2M X 32 SDRAM, there is another one that has the DQ pins at the outer ends of the package and the control pins in the center and superceeds this one. The other device should be used for all new designs. It is found in figure 3.11.4-7.

The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO-G

ADDRESS ORGANIZATION

NUMBER BANKS	2	4
ROW ADDR.	A0⇒A13	A0⇒A13
COL. ADDR.	A0⇒A6	A0⇒A6
AUTO-PRECHARGE	A10	A10
BANK ADDRESS	A13	A12, A13

FIGURE 3.11.4-5
2M BY 32 SDRAM IN TSOP2



NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. The standard refresh interval (tREF) for 256Mb SDRAMs is 64ms.
3. (NC, VREF) is VREF on devices that require an external voltage reference.
4. BA0 is the least significant bank address
5. BA1 is the most significant bank address
6. A10/AP is row address A10, autoprecharge and precharge all banks.
7. (NC, $\overline{CK}$) is NC for devices using a single ended clock. $\overline{CK}$ is used for devices using a differential clock.
8. (NC, VREF) is VREF on devices that require an external voltage reference.
9. This standard is for a 4 Bank version only.

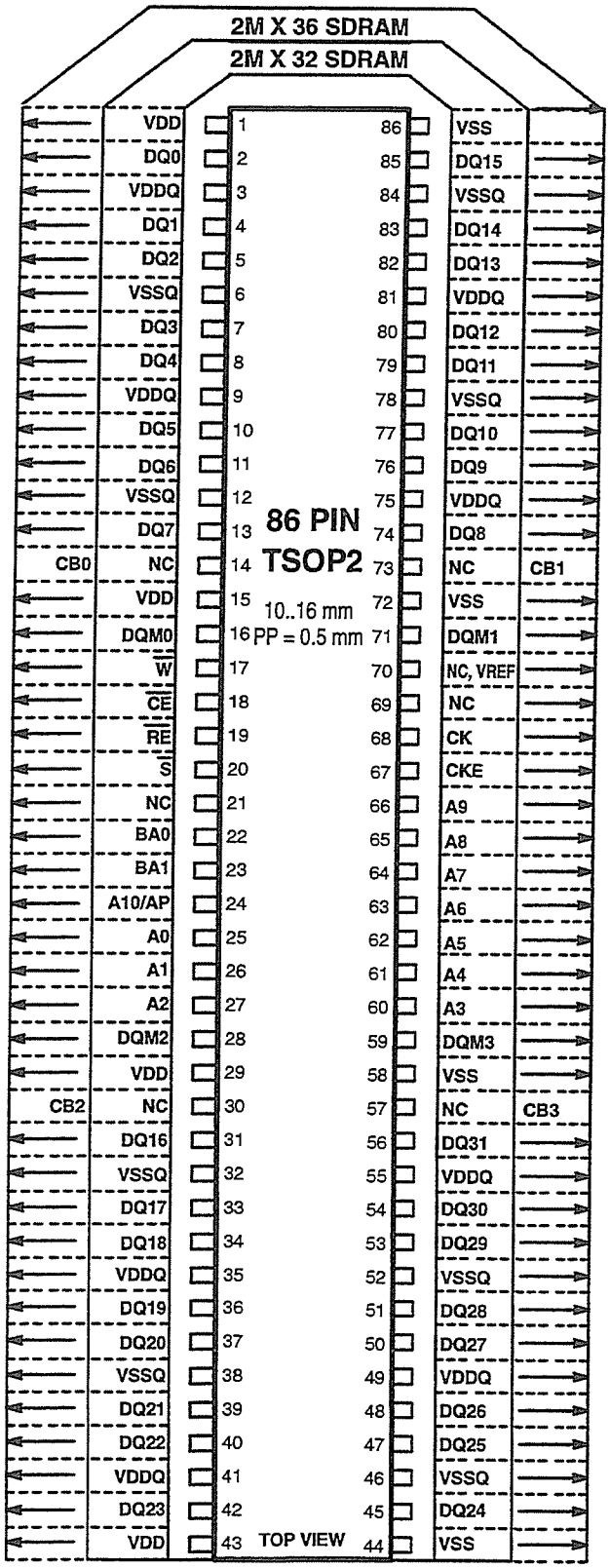
The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO–G

Configuration	8M X 32	8M X 32
Number RA	13	12
ROW ADDRESS	A0⇒A12	A0⇒A11
COLUMN ADDRESS	A0⇒A7	A0⇒A8

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.4–6
8M BY 32 SDRAM PIN ROTATION IN TSOP2

Release 6c7



NOTES

1. A10/AP Is Row Address A10, Autoprecharge And Precharge All Banks Input.

2. (NC,VREF) is VREF on devices that require an external voltage reference.

3. The VDDQ designator is used when th power supply pins for the DQ I/O drivers are internally DC isolated from the VDD power supply pins.

4. The VSSQ designator is used when th ground reference pins for the DQ I/O drivers are internally DC isolated from the primary ground reference (VSS) power supply pins.

The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO–G

Configuration	2M X 32
REFRESH ADDR.	A0 ⇒ A11
ROW ADDRESS	A0 ⇒ A11
COLUMN ADDRESS	A0 ⇒ A8

FIGURE 3.11.4–7
2M BY 32 & 36 SDRAM IN TSOP2

3.11.5 SDRAM Architectural and Operational Features

The following standards describe features or characteristics that are applicable to one or more of the SDRAM devices described in section 3.11 of Std. 21–C.

3.11.5.1 – SDRAM FUNCTION TRUTH TABLE

This table defines the interface states required to execute the standard SDRAM operational functions. The original publication of this standard in Release 4 contained errors that are corrected in Release 5

3.11.5.2 – SDRAM FUNCTION TRUTH TABLE FOR CKE

This table defines the interface states required to execute the standard SDRAM operational functions with respect to the CKE input. The original publication of this standard in Release 4 contained errors that are corrected in Release 5

3.11.5.3 – SDRAM MODE REGISTER ARCHITECTURE

This standard describes the architecture of the SDRAM internal MODE REGISTER and the codes that are allowable for use in it.

3.11.5.4 through 3.11.5.15 — SDRAM OPERATIONAL CYCLES AND MODES

The following standards define and describe a number of operational cycles and modes of SDRAM. They are ordered roughly in the sequence in which they would be used in normal SDRAM operation.

3.11.5.4 – POWER ON SEQUENCE (RECOMMENDED)

This standard gives a recommended power, clock, and logic–level sequence to be used on power–up to prevent data bus contention.

3.11.5.5 – AUTO PRECHARGE

This standard gives the logic function used to active the AUTO–PRECHARGE function.

3.11.5.6 – PRECHARGE ALL BANKS

This standard gives the logic function used to activate the PRECHARGE–ALL–BANKS function.

3.11.5.7 – MODE REGISTER WRITE TIMING

This standard defines the logic sequence and timing required to write into the MODE REGISTER.

3.11.5.8 – AUTO REFRESH

This standard defines the logic state and interface sequence required to perform an AUTO REFRESH

3.11.5.9 – WRITE LATENCY

This standard defines WRITE LATENCY and illustrates it with a timing diagram.

3.11.5.10 – DQM LATENCY FOR READS AND WRITES

In this standard DQM LATENCY is defined and the relationships between the DQM signal and the interface data for READs and WRITEs is defined and shown in timing diagrams.

3.11.5.11 – PRECHARGE TIMING FOR READS

This standard describes the relationship between the assertion of a PRECHARGE command and data out from a READ command.

3.11.5.12 – COLUMN ADDRESS TO COLUMN ADDRESS DELAY

This standard defines constraints imposed on the CA to CA delay and illustrates them with a timing diagram.

3.11.5.13 – CKE TIMING FOR POWER DOWN

This standard describes the interface sequence required to place the SDRAM into the POWER–DOWN state using CKE.

3.11.5.14 – SELF REFRESH ENTRY AND EXIT

This standard defines the logic states and timing sequence used to enter and exit the SELF–REFRESH mode.

3.11.5.15 – CKE TIMING FOR CLOCK SUSPEND

This standard describes the interface timing sequence when CKE is used to suspend the clock.

SDRAM FUNCTION TRUTH TABLE

CURRENT STATE	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
IDLE	H	X	X	X	X	NOP
	L	H	H	H	X	NOP
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	X	BA, CA	ILLEGAL[2]
	L	L	H	H	BA, RA	Row (& Bank) active; Latch Row Address
	L	L	H	L	BA, A10	NOP[4]
	L	L	L	H	X	Auto–Refresh[5]
	L	L	L	L	Op–code	Mode Register Access[5]
ROW ACTIVE	H	X	X	X	X	NOP
	L	H	H	X	X	NOP
	L	H	L	H	BA, CA, A10	Begin Read; Latch CA; Determine AP
	L	H	L	L	BA, CA, A10	Begin Write; Latch CA; Determine AP
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	Precharge
	L	L	L	X	X	ILLEGAL
READ	H	X	X	X	X	NOP (Continue Burst to End;⇒Row Active)
	L	H	H	H	X	NOP(Continue Burst to End;⇒Row Active)
	L	H	H	L	BA	RESERVED (Term. Burst);⇒Row Active
	L	H	L	H	BA, CA, A10	Term Burst, New Read, Determine AP[3]
	L	H	L	L	BA, CA, A10	Term Burst, Start Write, Determine AP[3]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	Term Burst, Precharge Timing for Reads
	L	L	L	X	X	ILLEGAL
WRITE	H	X	X	X	X	NOP(Continue Burst to End;⇒Row Active)
	L	H	H	H	X	NOP(Continue Burst to End;⇒Row Active)
	L	H	H	L	BA	RESERVED (Term Burst);⇒Row Active
	L	H	L	H	BA, CA, A10	Term Burst, Start Read, Determine AP[3]
	L	H	L	L	BA, CA, A10	Term Burst, New Write, Determine AP[3]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	Term Burst, Precharge[3]
	L	L	L	X	X	ILLEGAL
READ with AUTO Precharge	H	X	X	X	X	NOP (Continue Burst to End;⇒Precharge)
	L	H	H	H	X	NOP (Continue Burst to End;⇒Precharge)
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	H	BA, CA, A10	ILLEGAL[2]
	L	H*	L	L	X	ILLEGAL
	L	L	H	X	BA, RA, A10	ILLEGAL[2]
	L	L	L	X	X	ILLEGAL
WRITE with AUTO Precharge	H	X	X	X	X	NOP (Continue Burst to End;⇒Precharge)
	L	H	H	H	X	NOP (Continue Burst to End;⇒Precharge)
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	H	BA, CA, A10	ILLEGAL[2]
	L	H	L	L	X	ILLEGAL
	L	L	H	X	BA, RA, A10	ILLEGAL[2]
	L	L	L	X	X	ILLEGAL

TABLE 3.11.5–1

SDRAM FUNCTION TRUTH TABLE

SDRAM FUNCTION TRUTH TABLE (continued)

CURRENT STATE	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
Precharging	H	X	X	X	X	NOP⇒idle after tRP
	L	H	H	H	X	NOP⇒idle after tRP
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	X	BA, CA	ILLEGAL[2]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	NOP[4]
	L	L	L	X	X	ILLEGAL
ROW Activating	H	X	X	X	X	NOP⇒Row Active after tRCD
	L	H	H	H	X	NOP⇒Row Active after tRCD
	L	H	H	L*	BA *	ILLEGAL[2]
	L	H	L	X	BA, CA	ILLEGAL[2]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	ILLEGAL[2]
	L	L	L	X	X	ILLEGAL
WRITE Recovering	H	X	X	X	X	NOP
	L	H	H	H	X	NOP
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	X	BA, CA	ILLEGAL[2]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	ILLEGAL[2]
	L	L	L	X	X	ILLEGAL
Refreshing	H	X	X	X	X	NOP⇒idle after tRC*
	L	H	H	X	X	NOP⇒idle after tRC *
	L	H	L	X	X	ILLEGAL
	L	L	H	X	X	ILLEGAL
	L	L	L	X	X	ILLEGAL
Mode Register Accessing	H	X	X	X	X	NOP
	L	H	H	H	X	NOP
	L	H	H	L	X	ILLEGAL
	L	H	L	X	X	ILLEGAL
	L	L	X	X	X	ILLEGAL

ABBREVIATIONS

RA = Row Address BA = Bank Address Term = Terminate
CA = Column Address AP = Auto Precharge NOP = No Operation

NOTES:

1. All entries assume that CKE was active (HIGH) during the preceeding clock cycle and the current clock cycle.
2. Illegal to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy the "2n–rule", bus contention, but turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank(s) indicated by BA (and A10).
5. Illegal if any bank is not idle.

ILLEGAL = Device operation and/or data–integrity are not guaranteed

* Elements of the table that were in error in the first printing of Release 4

TABLE 3.11.5–1

SDRAM FUNCTION TRUTH TABLE (Continued)

SDRAM FUNCTION TRUTH TABLE for CKE

CURRENT STATE	CKE_{n-1}	CKE_n	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
Self–refresh[6]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Self–Refresh⇒ ABI
	L	H	L	H	H	H	X	EXIT Self–Refresh⇒ ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self–Refresh)
Power–Down	H	X *	X	X	X	X	X	INVALID
	L	H *	H	X*	X*	X*	X	EXIT Power Down⇒ABI
	L	H *	L	H	H	H	X	EXIT Power Down⇒ABI
	L	H *	L	H	H*	L*	X	ILLEGAL
	L	H *	L	H*	L*	X*	X	ILLEGAL
	L	H*	L	L	X*	X*	X	ILLEGAL
	L	L	X	X*	X*	X	X	NOP(Maintain Low–Power Mode)
All Banks Idle[7]	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power–Down
	H	L	L	H	H	H	X	Enter Power–Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self–Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State other than listed above	H	H	X	X	X	X	X	Refer to operations Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle[8]
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle[8]
	L	L	X	X	X	X	X	Maintain Clock Suspend.

ABBREVIATIONS
ABI = All Banks Idle
NOTES:

6. CKE Low–to–High transition will re–enable CK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
7. Power–Down and Self–Refresh can be entered only from the All Banks Idle State.
8. Must be legal command.
* Elements of the table that were in error in the first printing of Release 4

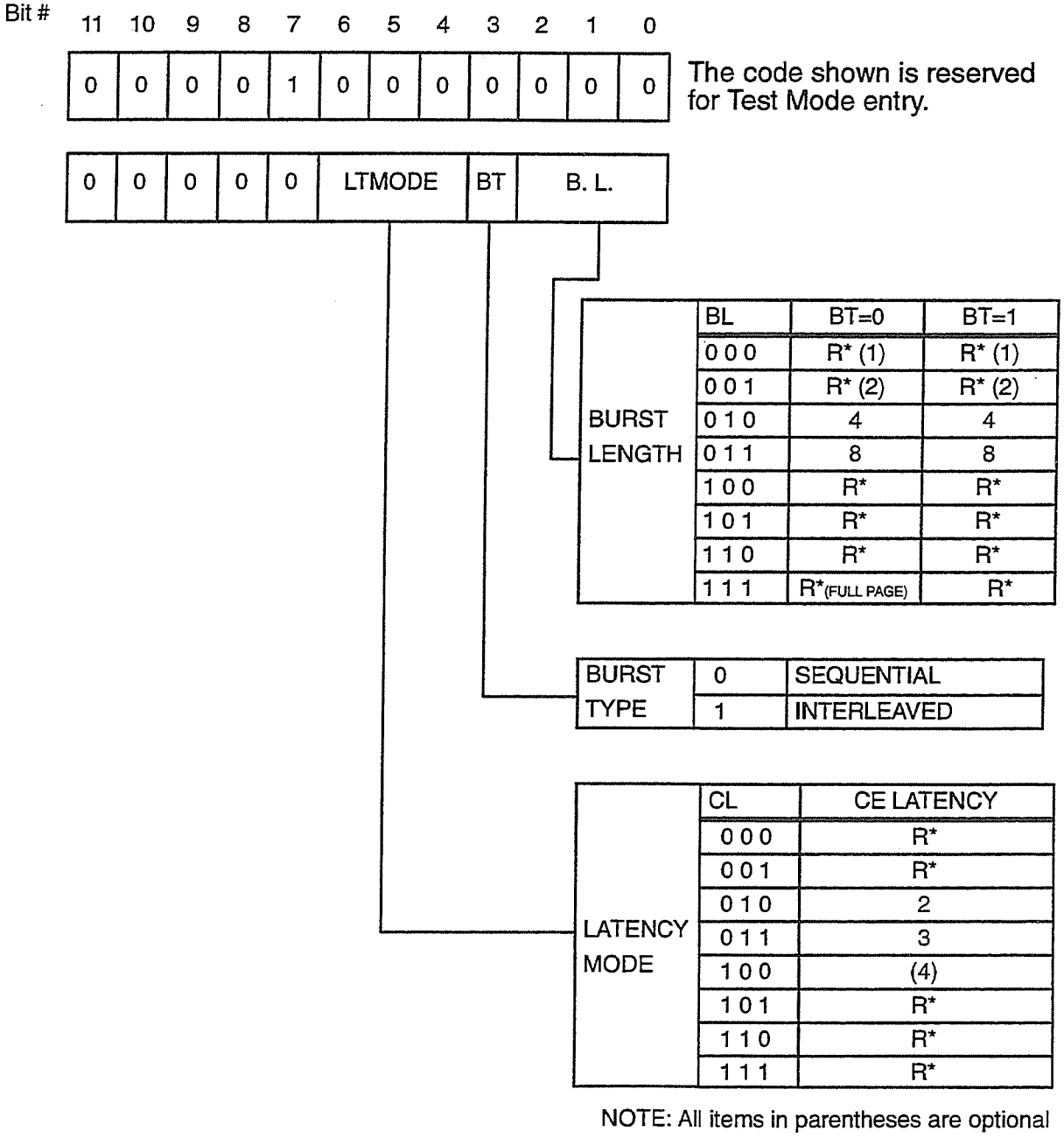
TABLE1 3.11.5–2

SDRAM FUNCTION TRUTH TABLE for CKE

SDRAM Mode Register

This Mode Register is located on the Synchronous DRAM (SDRAM) chip. Its purpose is to store the mode–of–operation data. This data is written after power–on and before normal operation. The data contains the Burst Length, the Burst Type, the $\overline{CE}$ Latency, and whether it is to be operating in Test Mode, or Normal operating mode. During operation, this register (and therefore operation of the chip) may be changed, according to the requirements of the Mode–Register–Write Timing diagram. So, while operating in one mode, for example Burst of 4 in sequential addresses; it can change to Burst of 8 in Interleaved address mode.

SDRAM Mode Register architecture:



NOTE: All items in parentheses are optional

FIGURE 3.11.5–1
SDRAM MODE REGISTER ARCHITECTURE

3.11.5.4–Power On Sequence (Recommended)

The synchronous nature of the inputs and outputs of the SDRAM device create the possibility that a SDRAM device could power up in a state with data being driven out of the part, and in a multipart system, such a condition may cause data contention and possibly device damage in the long term. In an attempt to reduce the possibility of data contention, both system and device designers should strive toward ensuring a High–Z output state during the initial power up sequence. The following recommended power on sequence is offered for both system and device designers as a means to help the device power up with the outputs in a High–Z state.

The default power on value for the mode register is supplier specific and may be undefined.

The default power on value for the device is supplier specific and may be undefined.

The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 μS.
3. Issue precharge commands for all banks of the device.
4. Issue 8 or more autorefresh commands.
5. Issue a mode register set command to initialize the mode register.

The device is now in the IDLE state and is ready for normal operation.

3.11.5.5–Auto Precharge

The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using address bit AP during the column address cycle. The following table defines the options available from AP during the column address portion of any cycle.

AP	Option
0	Do not auto precharge, leave bank active at end of burst.
1	Auto precharge bank specified by BA at end of burst.

The user must wait until the precharge is completed before issuing another command to the device. Timing for auto precharge is required to be the same as or less than the minimum requirement of external precharge.

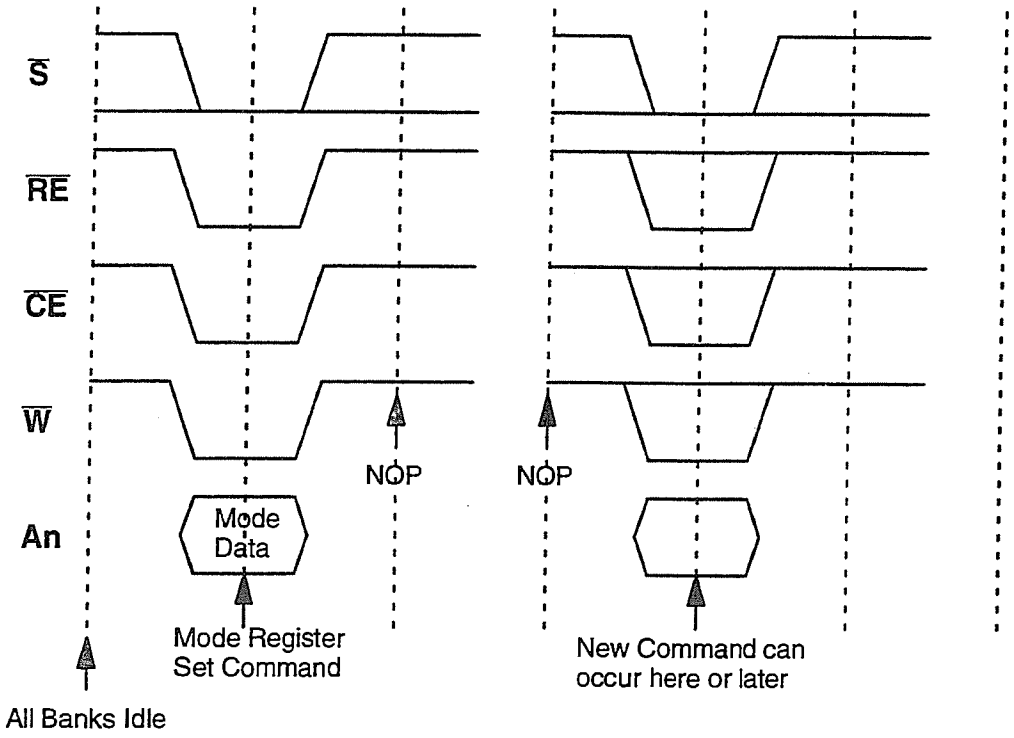
3.11.5.6–Precharge All Banks

The user may specify, during a precharge command, whether to precharge only the specified bank or to precharge all banks. BA is used to specify the bank to be precharge, and AP is used to indicate the precharge option. The following table defines the options available from AP during the precharge cycle.

PA	Option
0	Precharge bank specified by BA
1	Precharge All banks

3.11.5.7–Mode Register Write Timing

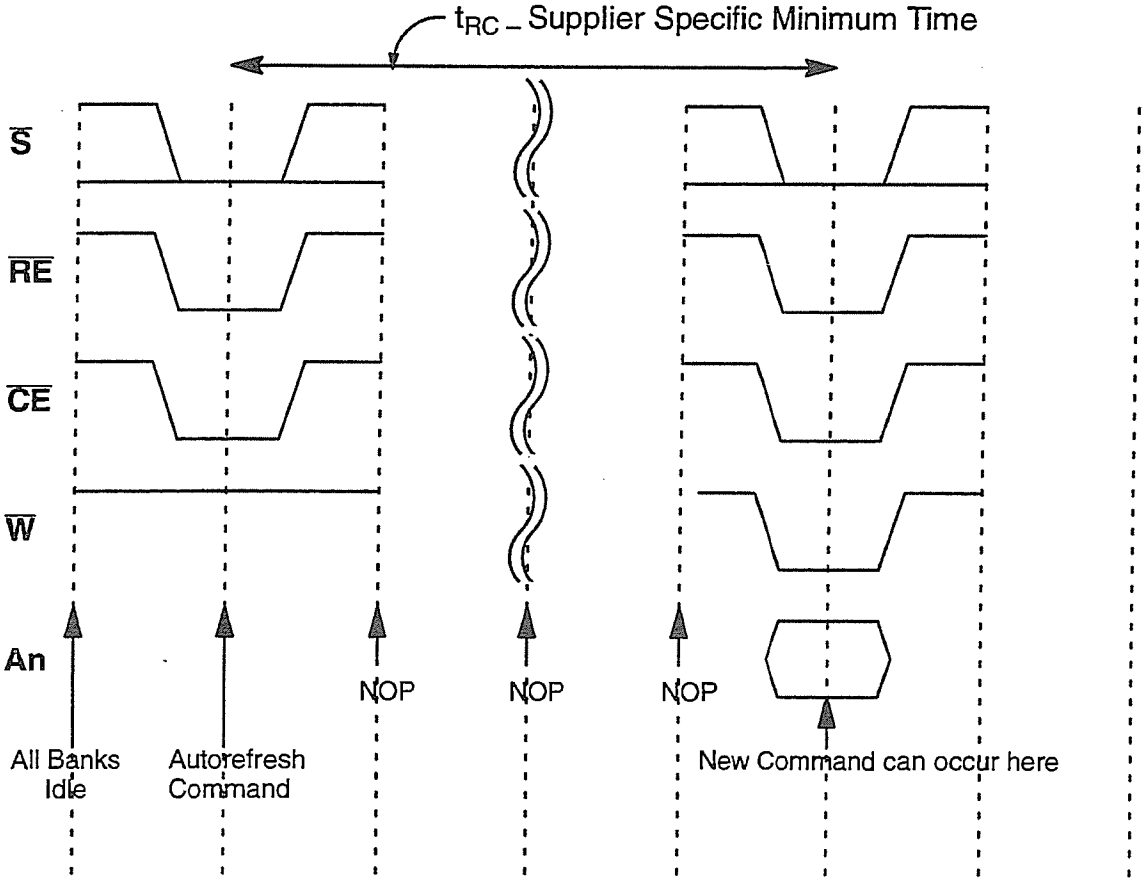
The Mode Register Set Cycle is initiated by holding the $\overline{S}$, $\overline{RE}$, $\overline{CE}$, and $\overline{W}$ signals low at the clock rising edge. The address lines at the same clock edge contain the mode register set opcode and the valid mode information to be written into the mode register. A mode register set cycle can be followed by a new command in no less than 3 clock cycles as illustrated in the diagram below.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.8–Auto Refresh

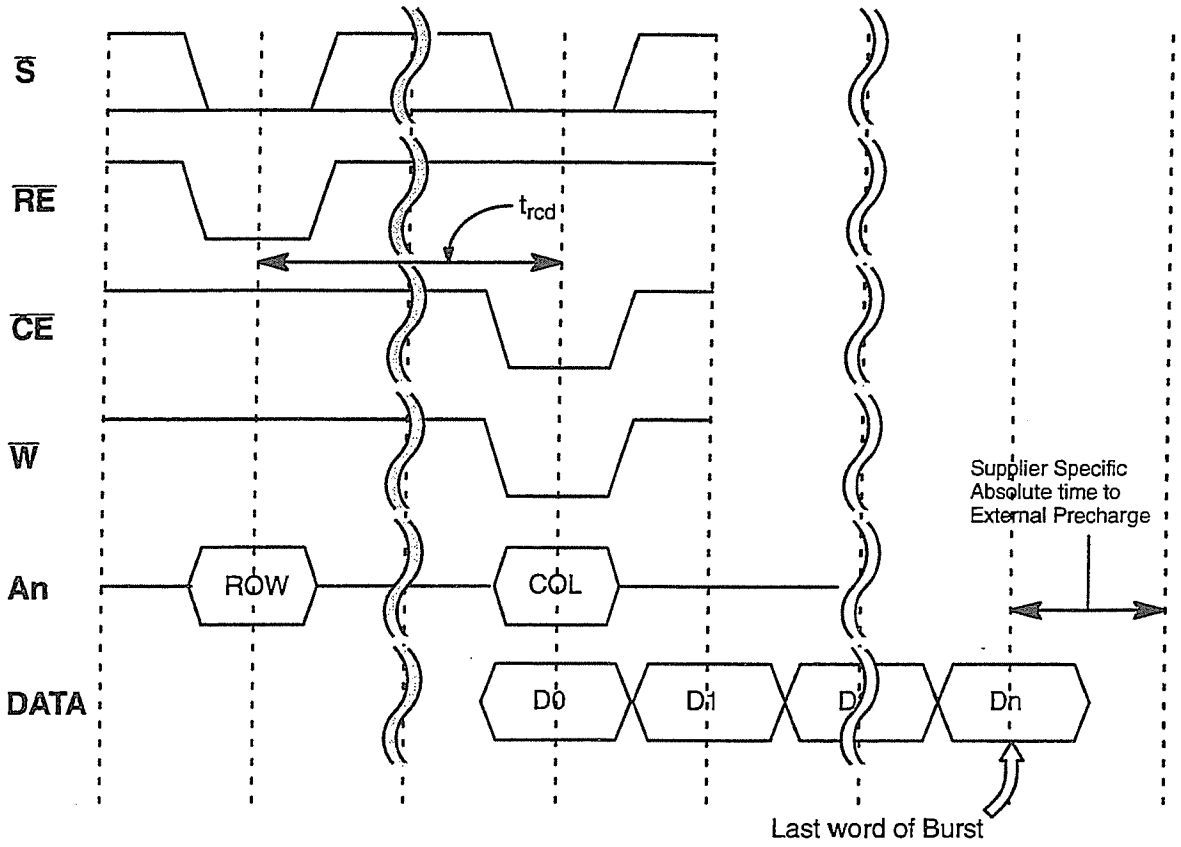
AutoRefresh is an operation that initiates a single refresh cycle for an SDRAM, but that once initiated, is completed by internal control in the device with the refresh address being supplied by an internal register in the device. Before performing an Autorefresh, all banks of the device must be precharged (IDLE). Autorefresh is entered by asserting RE and CE on the same clock cycle. All banks will automatically precharge at the end of the refresh cycle. Additional commands must not be supplied to the device during the minimum refresh time specified. The following timing diagram illustrates the refresh cycle requirements.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.9–Write Latency
(Write Latency = 0)

Write Latency for Synchronous DRAM shall be as defined as the clock cycle difference between the clock where write command and collumn address are asserted and the clock where first data to be written is asserted.

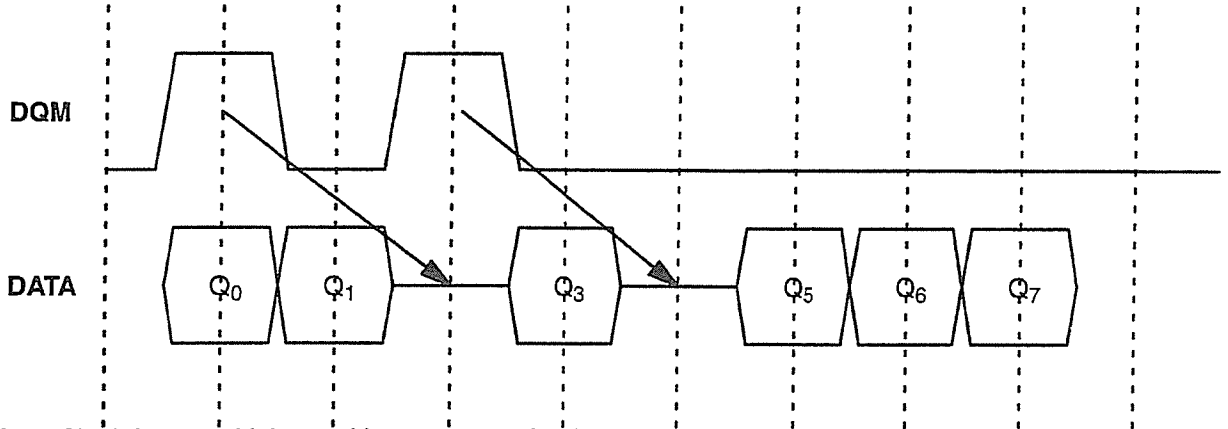


Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.10–DQM Latency for Reads and Writes (DQM Write Latency = 0)

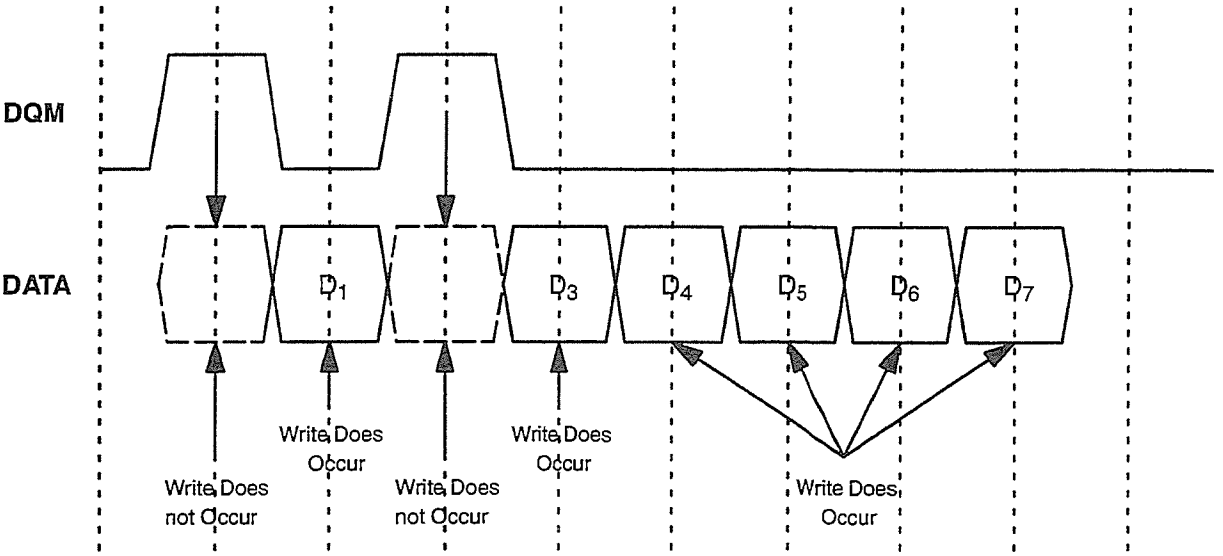
DQM is a multiple–function signal defined as the data mask for both reads and writes. During reads, DQM performs synchronous output enable. During writes, DQM performs write data masking. The requirement for high–speed operation, and the synchronous nature of SDRAM devices requires that DQM latency be different for reads than it is for writes.

For Reads, DQM latency is defined as the difference between the clock when DQM is asserted and the clock when the output bus has been forced to High–Z. The following timing diagram illustrates the standard of 2 clocks.



Note: Clock Low–to–high transitions occur at the dotted lines.

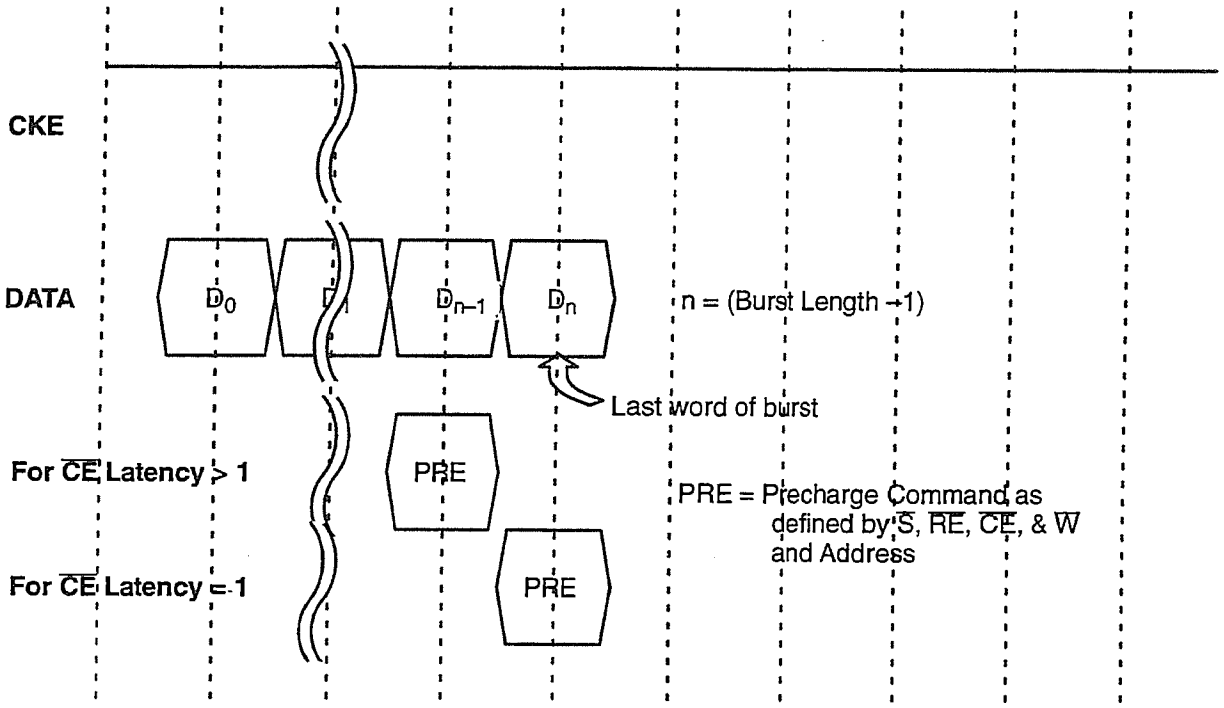
For Writes, DQM latency is defined as the difference between the clock when DQM is asserted and the clock when the write input data is inhibited. The following timing diagram illustrates the standard of 0 clocks.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.11–Precharge Timing for Reads

The assertion of the precharge command has a direct relationship to the timing of data out for a read cycle. For a CE latency of 1, the minimum requirements is that the precharge command will be allowed to coincide with output of the last data from a bu;rst regardless of burst length. For a CE latency greater than 1, the minimum requirement is that the precharge command will be allowed to coincide with output of the next–to–last data from a burst, regardless of burst length, without interrupting burst data. The following timing diagrams illustrate the requirements.



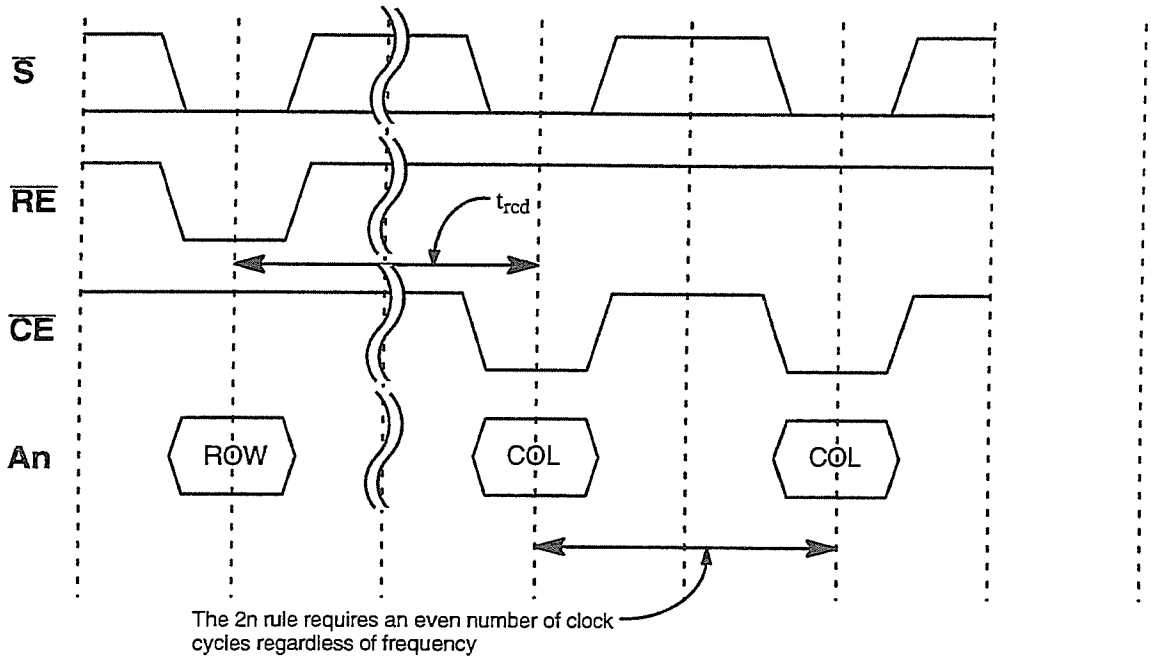
Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.12–Column Address to Column Address Delay

The minimum column–address–to–column–address delay time, for page mode accesses, is two clock cycles, independent of operating frequency.

For interrupted bursts, column addresses must, at a minimum, follow the "2n rule" while a read or write burst is in progress. 2n rule: after the initial read or write command, a new column address can be presented to the device every other clock cycle. That is, if the initial read–or–write command occured on an odd clock cycle, the new column addresses must presented on an odd clock cycle while the burst is in progress.

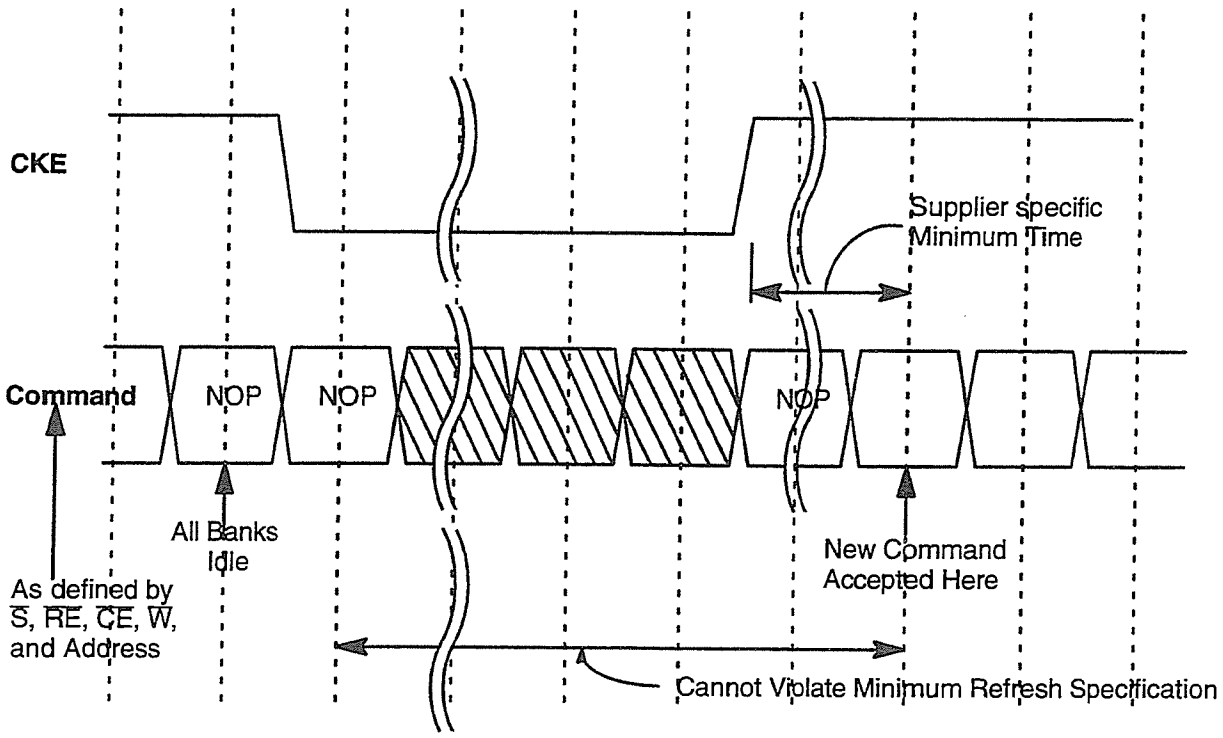
After the burst is completed, the 2n rule no longer applies, and a new column address may be presented to the device on any clock cycle. Essentially the 2n rule remains in effect for (CE Latency + burst length) clock cycles for reads and (write recovery + burst length) clock cycles for writes.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.13–CKE Timing for Power Down

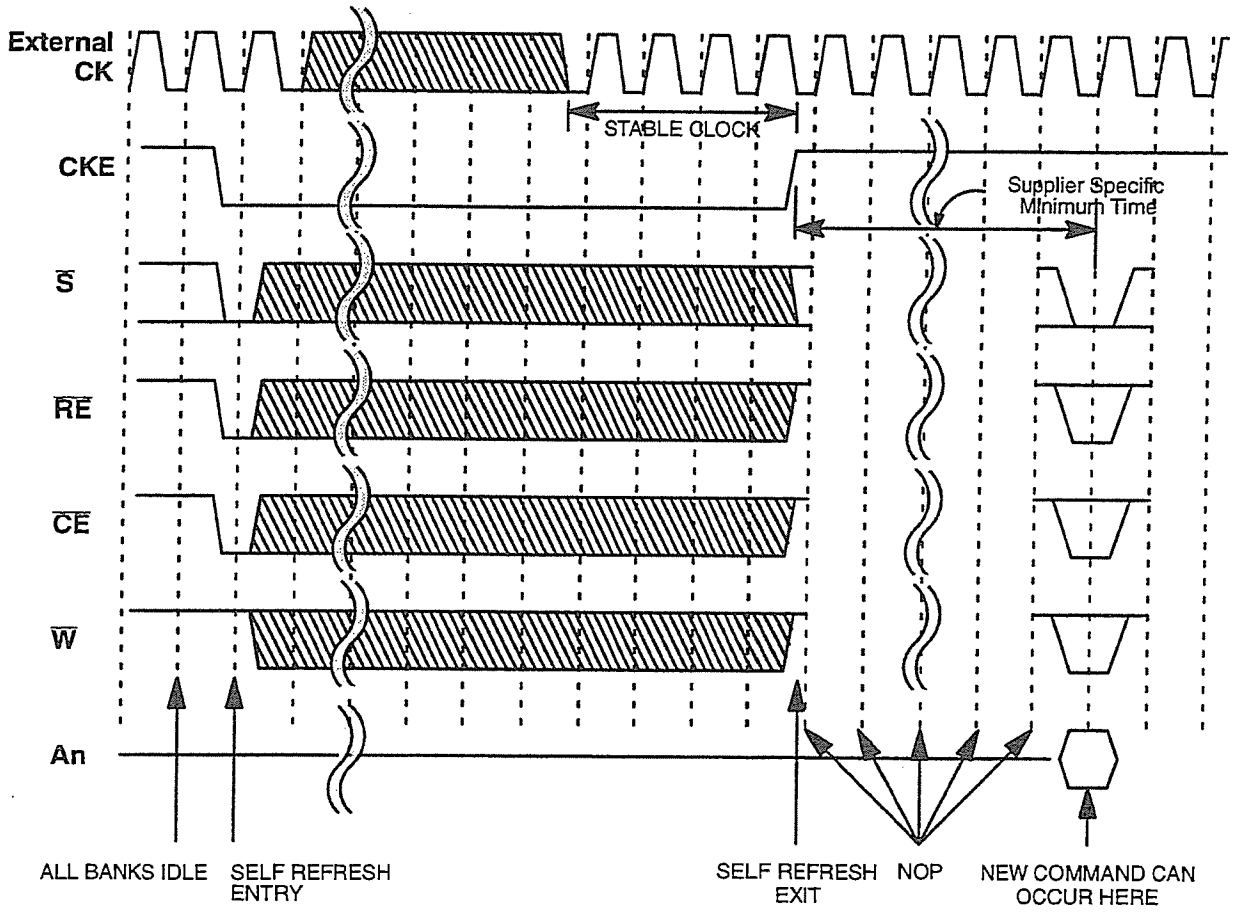
CKE is defined as the clock–enable signal and actually has the dual purpose of also being the signal that puts an SDRAM into a low power state. Using CKE to enter the low power state can only be performed while all internal banks of the device are precharged (IDLE). If all internal banks have been precharged, then CKE is used to gate the input buffers of the device. During power down the device is not refreshed. Therefore the minimum refresh specification still applies during power down. The following timing diagram illustrates power down mode.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.14–Self–Refresh Entry and Exit

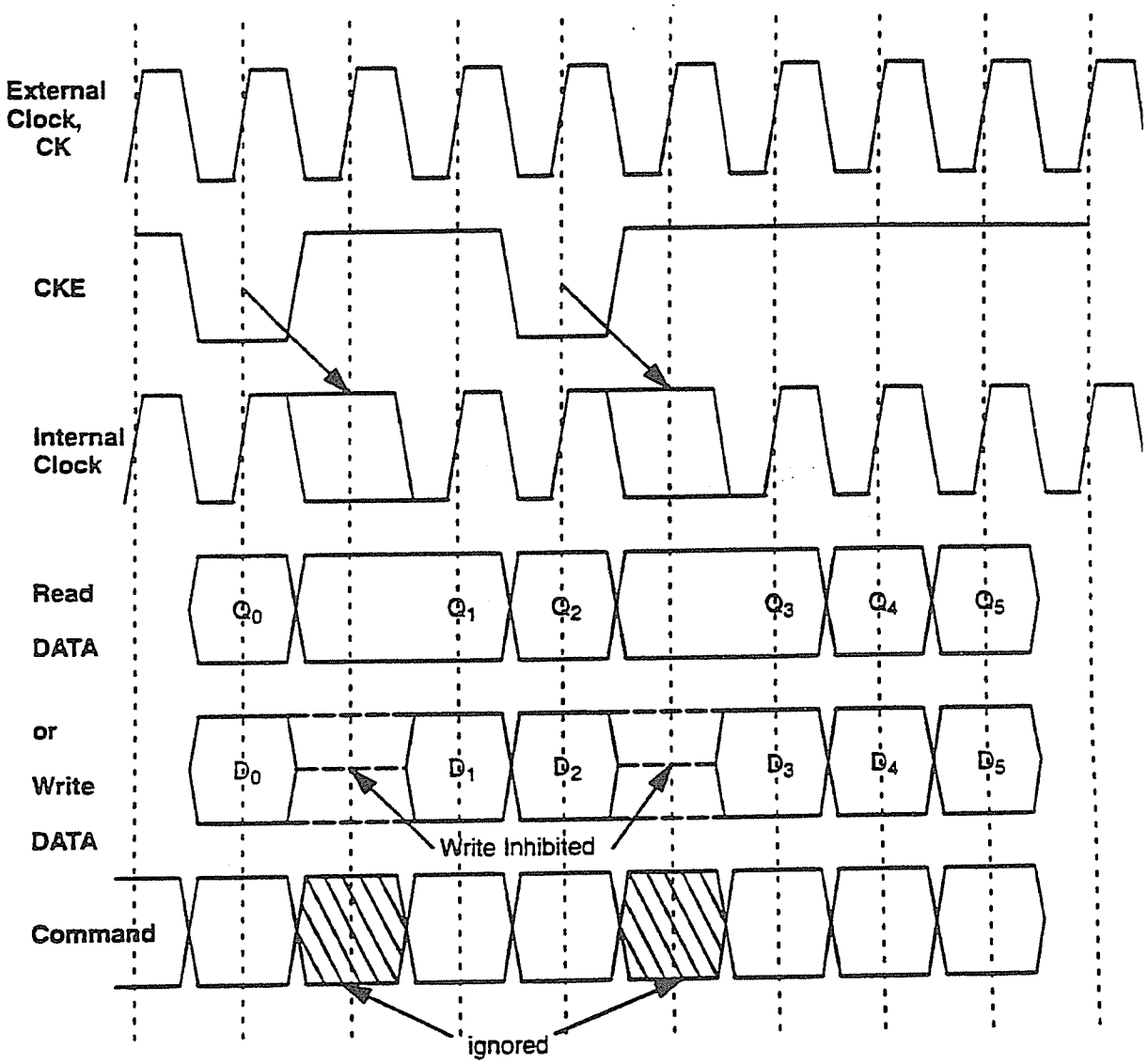
In self refresh mode, the device refreshes itself without outside intervention. While the device is in self–refresh mode, CKE is the only enabled input to the device. All other inputs including the clock are disabled and any input is ignored. Self–refresh mode is entered by precharging all banks and then inserting an auto–refresh command with CKE low. Exit from self–refresh mode is accomplished by starting the clock and then asserting CKE. NOP commands must be asserted for a supplier–specified minimum period, which must include 3 clocks, to allow the device to return to the IDLE state.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.15–CKE Timing for Clock Suspend

The following timing diagram is shown for CKE when 1 or more banks of the device are active. The effect on read data, write data, and command are all shown on the same diagram for reference only. The clock may be suspended for one or more clock cycles.



Note: Clock Low–to–high transitions occur at the dotted lines.

4 MEMORY MODULES AND CARDS

The following standards for MODULES and CARDS were developed by Committee JC–42.5. In earlier releases of JESD 21–C, the individual standards were intermixed and appeared in one section, 4, in the order in which they were approved with no regard for the module structure or organization. In Release 7, the section has been reorganized and the individual standards grouped in sub–sections by the data word length. A separate section is included (4.1) for those standards that describe features that are generic in nature and independent of the module organization.

The standards establish pin assignments for a series of multi–chip modules. The package configurations and dimensions are as defined in JEDEC Publication 95. The modules will normally be made using surface mount devices described in section 3 of this standard. The initial standards were for DRAM modules, but the since the publication of Std. 21–B, a standard for a families of SRAM and non–volatile modules have been approved. In addition to the device standards, there is a standard that addresses special nomenclature related to the modules.

The sub–sections are as follows:

4.1 Module Features & Properties

The following standards are applicable to modules and cards without regard to the data word length except as where specifically indicated.

4.1.1 Memory Module Nomenclature

4.1.2 Memory Module Serial Presence Detect (SPD) General Standard

4.1.2.1 SPD Appendix A

4.1.2.2 SPD Appendix B

4.1.2.3 SPD Appendix C

4.1.2.4 SPD Appendix D

4.1.2.5 SPD Appendix E

4.1.2.6 SPD Appendix F

4.1.1 Memory Module Nomenclature

4.1.1.1 – Purpose

The purpose of this standard is to establish a format for a number system which defines the format of a number which is an architectural description of multi–chip memory modules. It is intended to be used with but not restricted to modules made with DRAM devices.

4.1.1.2 – Number Format

The description number designation shall consist of 8 fields with the form nnSccbbDttlpp where :
nn = the number of longitudinal positions on the module: 4, 5, 8, 9.
S = the number of sides on the module stated as "single or double" : S, D
cc = the capacity of the memory chip stated in terms of the log(2) of the capacity (i.e.–the number of address bits needed for the chip): 16, 18, 20, 22
bb = the number of data bits in the interface: 1, 2, 4, 5, 8, 9, 10, 17
D = the data interface configuration, common, separate, or mixed: C, S, M
tt = total number of words stated as log(2) of the capacity: 16—26
l = mechanical interface: P = pins, E = edge card connector
pp = number of pins or pads

4.1.1.3 – Number Example

A module with the following attributes:
9 chips long
Double sided
18 bit data interface
Separate I/O for parity bits, common I/O for other bits
1M X 1 memory chips
Pin interface
Architectural number: 9D2018M20P40

4.1.2 – SERIAL PRESENCE DETECT STANDARD, General Standard

Introduction: New memory technologies are continually being introduced to the industry. As these new technologies are considered, the need for expansion modules becomes evident; consequently, new memory technologies are being incorporated onto existing module form factors. Unfortunately, upon a module's first implementation, the module designer is often unable to predict all of the (as yet unreleased) memory technologies which would eventually be used on the module form factor; hence the parallel Presence Detect method did not allow for these newer technologies. Given that memory modules do not regularly change form factor when a new memory technology is implemented, a Serial Presence Detect (SPD) method should be available and predefined so that it can be considered for new memory modules when needed.

1 **Scope:** This standard defines the means to implement a Presence Detect (PD) scheme serially. This Serial Presence Detect (SPD) standard is intended for use on any memory module independent of memory technology or module form factor. At the point of standardization of any given memory module, SPD being defined within this standard, may be easily implemented if so chosen. The body of this standard will depict generally how SPD is implemented; this will be independent of the module's memory technology.

When a specific memory technology is being depicted (e.g. Fast Page Mode DRAM), an appendix to this standard will be added describing the characteristics, features, and attributes of that memory technology needed for Presence Detection. The entire address map of the SPD scheme must be presented in each appendix.

When a new module form factor implementing SPD is standardized, the (proposed) standard for that module must also include the following information pertinent to the SPD:

- SPD Interface protocol (see section 2 herein)
- Acceptable module configurations,
- Legitimate architectures: depth, width, #banks, addressing
- Acceptable error checking schemes (ECC, Parity...)
- SPD Wiring diagram and pinout to module.

2 **Interface Protocol.** Upon the development/standardization of a new module form factor incorporating SPD, the SPD interface protocol will be defined. As long as that module form factor is used, this protocol must remain constant. Examples of SPD interface protocol include IIC, Microwire, etc. The physical implementation (pinouts etc.) must also be defined in the standard for the module form factor if it implements SPD.

3 **Data Order and PD Size:** This document will present the order in which the PD bytes should follow. It also defines how many bytes must be used to define a given PD; in most cases it will be one byte per PD. The SPD address map is fixed upon selection of any given fundamental technology, this includes all required and optional data; when a fundamental memory technologies' PD bits are defined, then the entire address map for those SPDs must also be defined.

4 **SPD Data Types:** SPD data is stored in a non–volatile serial memory device. The different types of data include, but are not limited to:

- Look Up Table entries
- Binary data
- Optional data (Binary, ASCII, etc. data)
- Checksums

4.1 **Look Up Table (LUT) Entries:** Much of the SPD data is organized as a series of table entries. Each table entry contains one or more bytes of information. Each table entry represents one particular characteristic pertinent to the memory module; e.g. fast page mode DRAM will have specific tables for tRAC, tCAC, # of banks, number of row addresses, number of column addresses, error detection/correction, refresh rates, data width, and interface standard. Each table entry corresponds to a position on a look–up– table specified within an appendix within this standard. The number of bytes (one or more) needed to express a particular aspect of the module is fixed and defined in this standard or in one of its appendices.

4.2 **Optional Data:** The current Jedec Standard allows for manufacturers to insert some of their own specific data into the SPD ROM. This data includes manufacturer ID, manufacturers' module serial numbers, and other ASCII, Binary Coded Decimal, or binary data.

4.3 **Checksums:** In various cases, checksums are required. Checksum calculation method is currently being proposed at time of publication of this standard.

5 **SPD Content:** The Serial Presence Detect standard calls for various features and items to be defined. Specifically, the following must be addressed in any SPD implementation:

Description	Data Type	Address Map Byte #
SPD size	LUT Entry	0
Total SPD memory size	LUT Entry	1
Fundamental memory type	LUT Entry, Appendix A	2
Definition of features specific to the fundamental memory	See pertinent appendix	3–31
(Optional) Superset memory type	See appendix B	32
(Optional) definition of features specific to the superset memory	See pertinent appendix	33–61
SPD Revision designator	LUT	62
Checksum for bytes 0–62	Checksum	63
Manufacturers Jedec ID code per JEP–106	LUT	64–71
Manufacturing location	Supplier Unique	72
Manufacturer's Part Number	Supplier Unique	73–90
Revision Code	Supplier Unique	91–92
Manufacturing date	BCD	93–94
Assembly Serial Number	Supplier Unique	95–98
Manufacturer Specific Data	Supplier Unique	99–125
Reserved	N/A	126–127
Open free–form area	Application Specific	128–255

Detailed descriptions follow in paragraphs 5.x

5.1 **Byte 0,** Number of Bytes used by Module Manufacturer: This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data:

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

5.2 **Byte 1, Total SPD Memory Size:** This field describes the total size of the serial memory (often an EEPROM) used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

5.3 **Byte 2,** Fundamental Memory Type: This field will identify the fundamental type of memory. The fundamental type of memory may include Fast Page Mode DRAM, EDO DRAM, Masked ROM, EEPROM, Synchronous DRAM, etc. The table listing all the types of Fundamental memory is contained in **appendix A** herein. New fundamental types can be added to this table anytime after standardization of a fundamental memory type. Note that if a given new technology is completely backward compatible with pre–existing technology, then it should be considered a Superset technology and so described as detailed (in paragraph 5.5) within this standard.

5.4 **Bytes 3–31:** Descriptions of Module Specific Features: Appendices to this standard detail the tables for the features specific to each of the fundamental memory types as described above. For example, see appendix C for details of SPD features for Fast Page Mode and Extended Data Out DRAM Modules.

5.5 **Byte 32:** Superset Memory Type: When a new technology is developed which is completely backward compatible to an already specified (fundamental) technology, then it may be considered a $Superset' technology. The benefits of specifying a technology as a superset are obvious; if a system is capable of operating in a $fundamental' mode only and a superset module is inserted, then the system can still use the module. The memory superset type or technology is specified in appendix B to this standard. Appendix B provides the decode of specific superset technologies. It references other appendices where the specific superset PDs are further detailed. As new supersets are created, appendices must also be added. Presence Detects for a superset technology are specified just as for any given fundamental technology except that any and all backward compatible fundamental technologies must be referenced.

5.6 **Bytes 33–63:** Superset Features: Appendices to this standard detail the tables for the features specific to each of the superset memory types as described above. A new appendix must be added to this standard detailing the PDs for that superset technology detailed in appendix B and represented in byte 32. Appendix B would identify the superset technology type and would also reference the appropriate appendix where the superset is detailed.

5.9.0 **Bytes 64–127:** Module manufacturers may include information which is pertinent to their particular modules. This information is detailed below in paragraph 5.9.X:

5.9.1 **Bytes 64–71**: Manufacturers Jedec ID code per JEP106. Manufacturers of a given module may include their identifier per Jedec spec JEP106. 00h is not allowed and FF indicated continuation. The first byte is utilized, the second byte filling. Unused locations/bytes would be FFh.

5.9.2 **Byte 72:** Manufacturing Location. Manufacturers may include an identifier which uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

5.9.3 **Bytes 73–90:** Manufacturer's Part Number: Manufacturers may include their part number in 6–bit ASCII format within these bytes.

5.9.4 **Bytes 91–92:** Revision Code: This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

5.9.5 **Bytes 93–94:** Date of Module Manufacture: The module manufacturer may include a date code for the module. If this is done, then specifically, byte 93 must contain the year in Binary and byte 94 must contain the week in Binary.

5.9.6 **Bytes 95–98:** Module Serial Number: The supplier may include a serial number for module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

5.9.7 **Bytes 99–125:** Manufacturers specific data, open area. The module manufacturer may add any additional information desired into the module within these locations.

5.9.8 **Bytes 126–127:** Reserved. These bytes are reserved and cannot be later allocated.

5.10 **Bytes 128–255:** System Integrators specific information: The system integrator may choose to use the SPD ROM for various items. If so, then bytes 128–255 may be used.

4.1.2.1 – Appendix A: Table of Fundamental Memory Types:

This table is modified/appended whenever a new fundamental memory technology is to be added to the Serial Presence Detect (SPD) standard. When a new memory type is added to this standard, a new appendix must also be added which details the specific features pertinent to the new fundamental type. The following table details the fundamental memory types.

Byte 2, Fundamental Memory Type: This field identifies the fundamental type of memory. The fundamental type of memory may include Fast Page Mode DRAM, EDO DRAM, Masked ROM, EEPROM, Synchronous DRAM, etc. The table listing all the types of Fundamental memory is contained in this Appendix herein. New fundamental types can be added to this table anytime after standardization of a fundamental memory type. Note that if a given new technology is completely backward compatible with pre–existing technology, then it should be considered a Superset technology and so described as detailed (in paragraph 5.5 of the General Standard) within this standard.

The fundamental memory types are identified as follows:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	See Appndx
Reserved	0	0	0	0	0	0	0	0	N/A
Standard FPM DRAM	0	0	0	0	0	0	0	1	C
EDO	0	0	0	0	0	0	1	0	C
PNEDO									
	0	0	0	0	0	0	1	1	TBD
Sync Dram	0	0	0	0	0	1	0	0	E
Multiplexed ROM	0	0	0	0	0	1	0	1	F
TBD	0	0	0	0	0	1	1	0	TBD
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	0	1	TBD
TBD	1	1	1	1	1	1	1	0	TBD
TBD									
	1	1	1	1	1	1	1	1	TBD

4.1.2.2 – Appendix B: Table(s) of Superset Memory Types:

This table is modified/appended whenever a new Superset memory technology is to be added to the Serial Presence Detect (SPD) standard. When a new superset memory type is added to this standard, a new appendix must also be added which details the specific features pertinent to the new superset type. The following table identifies the Superset memory types and their pertinent fundamental technologies.

The Superset memory types are identified as follows:

Superset Mem. Type Appndx	Fundamental memory type. (note 1)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	See
Reserved		0	0	0	0	0	0	0	0	N/A
TBD		0	0	0	0	0	0	0	1	TBD
TBD		0	0	0	0	0	0	1	0	TBD
TBD		0	0	0	0	0	0	1	1	TBD
TBD		0	0	0	0	0	1	0	0	TBD
TBD		0	0	0	0	0	1	0	1	TBD
TBD		0	0	0	0	0	1	1	0	TBD
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
TBD		1	1	1	1	1	1	0	1	TBD
TBD		1	1	1	1	1	1	1	0	TBD
TBD		1	1	1	1	1	1	1	1	TBD

Note 1: The fully backward compatible Fundamental memory type must be referenced when a superset is specified.

4.1.2.3 – Appendix C: Specific PD's for Fast Page Mode or Extended Data Out DRAM.

1 **Introduction:** This appendix describes the Presence Detects for Fast Page Mode DRAM and Extended Data Out (EDO) DRAM Modules. These PD's are those referenced in the SPD standard as "Specific Features". The following PD fields will occur, in the order presented, at the point in the standard where the Specific Features are referenced; that is after the identification of the Fundamental Memory Type and before identification of whether there is any Superset Features presented. For convenience sake however, the complete address map is presented herein.

1.1 **Address map:** The following is the SPD address map for FPM and EDO. It describes where the individual LUT–Entries/bytes will be held in the serial EEPROM:

Byte Number	Function described	Notes
0	Defines # bytes written into serial memory at module mfgr	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Addresses on this assembly	3
4	# Column Addresses on this assembly	
5	# DRAM Banks on this Assembly	
6	Data Width of this assembly...	
7	...Data Width continuation	
8	Voltage interface standard of this assembly	
9	RAS# access time of this assembly	4
10	CAS# access time of this assembly	4
11	DIMM Configuration type (Non–parity, Parity, ECC)	
12	Refresh Rate/Type	4,5
13	DRAM width, Primary DRAM	
14	Error Checking DRAM data width	
15–31	Reserved for future offerings	
32	Superset Memory Type (may be used in future)	
33–62	Superset Memory Specific Features (may be used in future)	
63	Checksum for bytes 0–62	
64–71	Manufacturers JEDEC ID code per JEP–106	6
72	Manufacturing location	6
73–90	Manufacturer's Part Number	6
91–92	Revision Code	6
93–94	Manufacturing date	6
95–98	Assembly Serial Number	6
99–125	Manufacturer Specific Data	6
126–127	Reserved	
128–255	Open User Free–Form area$not defined	

notes:

1) This will be 128 bytes for FPM and EDO DRAM

2) This will be 256 bytes, represented as 08h. See below.

3) High order bit defines is assembly has "redundant" addressing (if set to "1", highest order RAS# address must be re–sent as highest order CAS# address.)

4) From data sheet.

5) High order bit (MSB) is Self Refresh $flag'. If bit seven is "1", assembly supports self refresh.

6) Per the JEDEC spec, these are optional.

2 **Bytes 0–2,** For Reference: Descriptions of bytes 0–1 can be found in the main body of the SPD standard, and byte 2 is detailed in **appendix A** to this standard. For reference and convenience, applicable portions of their descriptions are presented again:

2.1 **BYTE 0,** From General SPD Standard, Number of Bytes used by Module Manufacturer: This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

2.2 **Byte 1,** From General SPD Standard, Total SPD Memory Size: This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

2.3 **Byte 2,** From Appendix A, Memory Type: This byte describes the fundamental memory type (or technology) implemented on the module:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
Standard FPM DRAM	0	0	0	0	0	0	0	1
EDO	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

3 **Data Type(s):** Even though many of the PD's seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries.

4 The following PD bytes are those specific to modules implementing Fast Page Mode and EDO DRAM technology. Note that full descriptions start at byte 3 and are not covered in the main body of the SPD standard since they are specific to a given fundamental memory type/technology.

4.1 **Byte #3, Number of ROW Addresses:** This first field describes the number of Row Addresses in the DRAM array:

No. of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
Undefined	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
12(redundant)	1	0	0	0	1	1	0	0
13(redundant)	1	0	0	0	1	1	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
126(redundant)	1	1	1	1	1	1	1	0
127(redundant)	1	1	1	1	1	1	1	1

Bit7: "0" indicates normal addressing; "1" indicates redundant addressing

4.2 **Byte #4, Number of COLUMNs Addresses:** This field describes the number of COLUMN addresses in the module's DRAM array:

Number of COLUMN Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.3 **Byte #5, Number of Banks:** This field describes the number of banks on the DRAM Module:

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4 **Bytes 6 & 7,** Module Data Width: Bytes 6 and 7 are used to designate the modules data width. The data width is presented as a 16 bit word; bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and bit7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 bits wide, byte 7 will be 00h. If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width. For example, if the module's

data width is:	then byte 7 is	and byte 6 is:
64	0000 0000	0100 0000
72	0000 0000	0100 1000
576	0000 0010	0100 0000

Byte 6:

Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
64	0	1	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
72	0	1	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
144	1	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4.1 **Byte 7, Module Data Width Continued:** This byte will be left at 00h if the original module data width is less than 256 bits wide. If the width is more than 255, then this byte will be used in conjunction with byte 6.

Module Data Width Cont.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	0
1024(+)	0	0	0	0	0	0	1	1
2048(+)	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

4.5 **Byte 8, Module Interface Levels:** This field describes the module's voltage interface:

Voltage Interface	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5	0	0	0	0	0	0	1	0
SSTL 3.3	0	0	0	0	0	0	1	1
SSTL 2.5	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
New Table	1	1	1	1	1	1	1	1

4.6 **Byte 9, RAS Access Time (tRAC):** This field describes the module's RAS access time:

RAS Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1ns	0	0	0	0	0	0	0	1
2ns	0	0	0	0	0	0	1	0
3ns	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
50ns	0	0	1	1	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
60ns	0	0	1	1	1	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
70ns	0	1	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
80ns	0	1	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
254ns	1	1	1	1	1	1	1	0
255ns	1	1	1	1	1	1	1	1

4.7 **Byte 10, CAS Access Time (tCAC):** This field describes the module's CAS access time:

CAS Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1ns	0	0	0	0	0	0	0	1
2ns	0	0	0	0	0	0	1	0
3ns	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
10ns	0	0	0	0	1	0	1	0
11ns	0	0	0	0	1	0	1	1
12ns	0	0	0	0	1	1	0	0
13ns	0	0	0	0	1	1	0	1
14ns	0	0	0	0	1	1	1	0
15ns	0	0	0	0	1	1	1	1
16ns	0	0	0	1	0	0	0	0
17ns	0	0	0	1	0	0	0	1
18ns	0	0	0	1	0	0	1	0
19ns	0	0	0	1	0	0	1	1
20ns	0	0	0	1	0	1	0	0
21ns	0	0	0	1	0	1	0	1
22ns	0	0	0	1	0	1	1	0
23ns	0	0	0	1	0	1	1	1
24ns	0	0	0	1	1	0	0	0
25ns	0	0	0	1	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254ns	1	1	1	1	1	1	1	0
255ns	1	1	1	1	1	1	1	1

4.8 Byte 11, Module Configuration type: This field describes the module's error detection and or correction schemes:

Error Det/Cor	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	1

4.9 Byte 12, Refresh Rate/Type: This field describes the module's refresh rate and type:

Refresh Period	Bit 7, Self Refresh Flag	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal (15.625 us)	0	0	0	0	0	0	0	0
Reduced (.25x)...3.9us	0	0	0	0	0	0	0	1
Reduced (.5x)...7.8us	0	0	0	0	0	0	1	0
Extended (2x)...31.3us	0	0	0	0	0	0	1	1
Extended (4x)...62.5us	0	0	0	0	0	1	0	0
Extended (8x)...125us	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
TBD	0	0	0	0	0	1	1	1
TBD	0	0	0	0	1	0	0	0
TBD	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
Self Refresh Entries								
Normal (15.625us)	1	0	0	0	0	0	0	0
Reduced (0.25x)...3.9us	1	0	0	0	0	0	0	1
Reduced (0.5x)...7.8us	1	0	0	0	0	0	1	0
Extended (2x)...31.3us	1	0	0	0	0	0	1	1
Extended (4x)...62.5us	1	0	0	0	0	1	0	0
Extended (8x)...125us	1	0	0	0	0	1	0	1
TBD	1	0	0	0	0	1	1	0
TBD	.	.	.	.	.	.	.	.
TBD	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	0
TBD	1	1	1	1	1	1	1	1

4.10 **Byte 13, DRAM width, Primary DRAM:** This field describes the width of the primary DRAMs used on the module. The primary DRAM is that which is used for data; examples of primary (data) DRAM widths are x4, x8, x16, x32. Note that if the module is made with DRAMs which provide extra bits for data and error checking e.g. x9, x18, x36, then it is also designated in this field. Examples using x72 modules include:

Module width	Primary Data DRAM Width	Error Checking DRAM Width	Qty Primary Data DRAMs	Byte 13 (Binary)
x72	x9	—	8	0000 1001
x72	x8	x8	9	0000 1000
x72	x16	x1	4	0001 0000

DRAM Width, Primary DRAM	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
15	0	0	0	0	1	1	1	1
16	0	0	0	1	0	0	0	0
17	0	0	0	1	0	0	0	1
18	0	0	0	1	0	0	1	0
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

4.11 **Byte 14, Error Checking DRAM data width:** If the module incorporates error checking and if the primary data DRAM does not include these bits; i.e. there are separate error checking DRAMs, then the error checking DRAM's width is expressed in this byte. Examples of error checking DRAM widths include x1, x4, x8. For Example:

Module width	Primary DRAM Width	Error Checking DRAM Width	Qty of Error Checking DRAMs	Byte 14 (Binary)
x72	x9	—	—	0000 0000
x72	x8	x8	1	0000 1000
x72	x16	x1	8	0000 0001

DRAM Width Error Checking DRAM	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

4.12 **Bytes 15–31:** Open. There are no defined PD settings for these bytes.

4.13 **Bytes 32 through 62, Superset information:** If a superset technology is developed and is completely backward compatible, it may be specified and its SPD may be defined in bytes 32 through 62.

4.14 **Byte 63, Checksum for bytes 0–62:** At time of the publish of this standard, the checksum method is currently in ballot and is not yet incorporated, suggested method is modulo 256.

5 **From the general SPD standard:** The descriptions of bytes 64–127 are repeated here For Reference ONLY. Manufacturers MAY include information which is pertinent to their particular modules, place and date of manufacture, etc. If a module manufacturer decides to write data into bytes 64–127, they must follow the format and order presented below. If a module manufacturer chooses not to include the data outlined below, they must leave bytes 64–127 unprogrammed; blank state of these bytes may be 00h or FFh. Detailed implementation of bytes 64–127 is detailed below in paragraphs 5.X:

5.1 **Bytes 64–71:** Manufacturers ID code per EIA/JEP106. Manufacturers of a given module may include their identifier per Jedec spec JEP106. 00h is not allowed and FFh indicated continuation. The first byte is utilized, the second byte filling. Unused locations/bytes should be FFh.

5.2 **Byte 72:** Manufacturing Location. Manufacturers may include an identifier which uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

5.3 **Bytes 73–90:** Manufacturer's Part Number: Manufacturers may include their part number in 6–bit ASCII format within these bytes.

5.4: **Bytes 91–92:** Revision Code: This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

5.5 **Bytes 93–94:** Date of Module Manufacture: The module manufacturer may include a date code for the module. Specifically, byte 93 may contain the year in Binary and byte 94 may contain the week in Binary.

5.6 **Bytes 95–98:** Module Serial Number: The supplier may include a serial number for module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

5.7 **Bytes 99–125:** Manufacturers specific data, open area. The module manufacturer may add any additional information desired into the module within these locations.

5.8 **Bytes 126–127:** Reserved. These bytes are reserved and cannot be later allocated.

4.1.2.4 – Appendix D: Table not yet defined

Table D is not yet defined. It will be placed in this location when it is published.

4.1.2.5 – Appendix E: Specific PD's for Synchronous DRAM (SDRAM).

Date of last update: 11/25/96

1. **Introduction:** This appendix describes the Presence Detects for Synchronous DRAM Modules. These PD's are those referenced in the SPD standard document for "Specific Features". The following PD fields will occur, in the order presented, in table 1.1. Further descriptions of bytes 0 and 1 are found in the SPD standard. Further description of byte 2 is found in appendix A of the SPD standard.

1.1 **Address map:** The following is the SPD address map for SDRAM. It describes where the individual LUT–Entries/bytes will be held in the serial EEPROM:

Byte Number	Function described	Notes
0	Defines # bytes written into serial memory at module mfgr	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Addresses on this assembly	3
4	# Column Addresses on this assembly	
5	# Module Banks on this Assembly	
6	Data Width of this assembly...	
7	...Data Width continuation	
8	Voltage interface standard of this assembly	
9	SDRAM Cycle time at Max. Supported CAS Latency (CL), CL=X	4
10	SDRAM Access from Clock	4
11	DIMM Configuration type (Non–parity, Parity, ECC)	
12	Refresh Rate/Type	4,5
13	SDRAM width, Primary DRAM	
14	Error Checking SDRAM data width	
15	Minimum Clock Delay, Back to Back Random Column Addresses	
16	Burst Lengths Supported	
17	# Banks on Each SDRAM device	4
18	CAS# Latencies Supported	4
19	CS# Latency	4
20	Write Latency	4
21	SDRAM Module Attributes	
22	SDRAM Device Attributes: General	
23–31	TBD	
32–62	Superset information	
63	Checksum for bytes 0–62	
64–71	Manufacturers JEDEC ID code per JEP–106E	6
72	Manufacturing location	6
73–90	Manufacturer's Part Number	6
91–92	Revision Code	6
93–94	Manufacturing date	6
95–98	Assembly Serial Number	6
99–125	Manufacturer Specific Data	
126–127	Reserved	
128–255	Open for Customer use.	7

notes:

1) This will be programmed as 128 bytes for the 168 pin DIMM Module.
2) This must be programmed as 256 bytes, 256 byte EEPROM's will be used for SPD on 168 pin SDRAM DIMMs.
3) High order bit defines if assembly has "redundant" addressing (if set to "1", highest order RAS# address must be re–sent as highest order CAS# address.)
4) From data sheet.
5) High order bit (MSB) is Self Refresh $flag'. If bit seven is "1", assembly supports self refresh.
6) The JEDEC spec specifies that these bytes are optional.
7) Module suppliers will need to assure that these bytes are open for reads/writes by Customer.

2 **For Reference, Bytes 1–3:** Descriptions of bytes 1 and 2 can be found in the main body of the SPD standard, and byte 3 is detailed in appendix A to this standard. For reference and convenience, applicable portions of their descriptions are presented again:

2.1 **BYTE 0:** From General SPD Standard, Number of Bytes used by Module Manufacturer: This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

2.2 **Byte 1:** From General SPD Standard, Total SPD Memory Size: This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

2.3 Byte 2, From Appendix A, Memory Type: This byte describes the fundamental memory type (or technology) implemented on the module:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
SDRAM	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

3. **Data Type(s):** Even though many of the PD's seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries.

4. The following PD bytes are those specific to modules implementing Synchronous DRAM technology. Note that these full descriptions start at byte 3 below and are not covered in the main body of the SPD standard since they are specific to a given fundamental memory type/technology

4.1 **Byte 3: Number of ROW Addresses:** This first field describes the number of row Addresses in the SDRAM array. This does not include the Bank Select pin. For example, the number of Row Addresses used on a 2MX64 SDRAM DIMM is

Decimal 11 Binary 0000 1011 Addresses (for RA0 through RA10):

No. of Row Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
Undefined	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
12(redundant)	1	0	0	0	1	1	0	0
13(redundant)	1	0	0	0	1	1	0	1
14(redundant)	1	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
126(redundant)	1	1	1	1	1	1	1	0
127(redundant)	1	1	1	1	1	1	1	1

Bit7: "0" indicates normal addressing; "1" indicates redundant addressing

4.2 **Byte 4: Number of COLUMN Addresses:** This field describes the number of COLUMN Addresses in the module's SDRAM array:

Number of Columns	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.3 **Byte 5: Number of Banks on module:** This field describes the number of physical banks on the SDRAM Module. This is not to be confused with the number of logical banks on a given SDRAM device :

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4 **Bytes 6 & 7, Module Data Width:** Bytes 6 and 7 are used to designate the modules data width. The data width is presented as a 16 bit word; bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and bit7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 bits wide, byte 7 will be 00h. If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width. For example, if the module's

data width is:	then byte 7 is	and byte 6 is:
64	0000 0000	0100 0000
72	0000 0000	0100 1000
80	0000 0000	0101 0000
576	0000 0010	0100 0000

4.4.1 Byte 6:

Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
64	0	1	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
72	0	1	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
80	0	1	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
144	1	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4.2 Byte 7. Module Data Width Continued: This byte will be left at 00h if the original module data width is less than 256 bits wide. If the width is more than 255, then this byte will be used in conjunction with byte 6.

Module Data Width Cont.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	0
1024(+)	0	0	0	0	0	0	1	1
2048(+)	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

4.5 **Byte 8, Module Interface Levels:** This field describes the module's voltage interface:

Voltage Interface	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5	0	0	0	0	0	0	1	0
SSTL 3.3	0	0	0	0	0	0	1	1
SSTL 2.5	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	1

4.6 Byte 9, SDRAM Cycle time (tCYC): This byte defines the minimum cycle time for the SDRAM Module at the highest CAS Latency, CAS Latency=X, defined in byte 18. If other CAS latencies are supported, then the associated minimum cycle times are not related in this version of the SPD standard. At this time of publication, proposals are being made to widen the standard to relate cycletimes at lower CAS Latencies. Byte 9, Cycle time for CAS Latency = X, is split into two nibbles: the higher order nibble (bits 4 through 7) designate the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0 through 3) has a granularity of 1/10ns and is added to the value designated by the higher nibble. For example, if

Bits 7:4 are		and bits 3:0 are		then the cycle time is
1010		0101		
(10ns)	+	(0.5ns)	=	10.5ns

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDRAM Cycle Time Subfield A:								
Units of nanoseconds (bits 4 through 7)					SEE Subfield Table B			
Undefined	0	0	0	0				
1ns/16ns	0	0	0	1				
2ns	0	0	1	0				
3ns	0	0	1	1				
4ns	0	1	0	0				
5ns	0	1	0	1				
6ns	0	1	1	0				
7ns	0	1	1	1				
8ns	1	0	0	0				
9ns	1	0	0	1				
10ns	1	0	1	0				
11ns	1	0	1	1				
12ns	1	1	0	0				
13ns	1	1	0	1				
14ns	1	1	1	0				
15ns	1	1	1	1				
SDRAM Cycle Time Subfield B:								
Tenths of ns (bits 0 through 3)	SEE Subfield table A							
+0ns					0	0	0	0
+0.1ns					0	0	0	1
+0.2ns					0	0	1	0
+0.3ns					0	0	1	1
+0.4ns					0	1	0	0
+0.5ns 1						0	1	0
+0.6ns					0	1	1	0
+0.7ns					0	1	1	1
+0.8ns					1	0	0	0
+0.9ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	.
Undefined	1	1	1	1	1	1	1	1

4.7 **Byte 10, SDRAM Access time from Clock (tAC):** This byte defines the maximum clock to data out for the module. This is the Clock to data out specification at the highest given CAS Latency specified/depicted in byte 18 of this SPD specification/ standard. If other CAS latencies are supported, then the associated Maximum Clock Access times are not related in this version of the SPD standard. At this time of publication, proposals are being made to widen the standard to relate tAC's at lower CAS Latencies. The byte is split into two nibbles: the higher order nibble (bits 4 through 7) designate the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0 through 3) has a granularity of 1/10ns and is added to the value designated by the higher nibble. For example, if

Bits 7:4 are	and bits 3:0 are	then the cycle time is
1001	0000	
(9ns) +	(0.0ns)	= 9.0ns

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDRAM Access time from Clock:								
Subfield A: Units of nanoseconds (bits 4 through 7)								
Undefined	0	0	0	0	SEE Subfield Table B			
1ns	0	0	0	1				
2ns	0	0	1	0				
3ns	0	0	1	1				
4ns	0	1	0	0				
5ns	0	1	0	1				
6ns	0	1	1	0				
7ns	0	1	1	1				
8ns	1	0	0	0				
9ns	1	0	0	1				
10ns	1	0	1	0				
11ns	1	0	1	1				
12ns	1	1	0	0				
13ns	1	1	0	1				
14ns	1	1	1	0				
15ns	1	1	1	1				
SDRAM Access time from CLK								
Subfield B: Tenths of ns (bits 0 through 3)								
+0ns	SEE Subfield Table A				0	0	0	0
+0.1ns					0	0	0	1
+0.2ns					0	0	1	0
+0.3ns					0	0	1	1
+0.4ns					0	1	0	0
+0.5ns					0	1	0	1
+0.6ns					0	1	1	0
+0.7ns					0	1	1	1
+0.8ns					1	0	0	0
+0.9ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	.
Undefined	1	1	1	1	1	1	1	1

4.8 **Byte 11, Module Configuration type:** This field describes the module's error detection and or correction schemes:

Error Det/Cor	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	1

4.9 Byte 12, Refresh Rate/Type: This field describes the module's refresh rate and type:

Refresh Period Bit 0	Bit 7, Self Refresh Flag	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal (15.625 us)	0	0	0	0	0	0	0	0
Reduced (.25x)...3.9us	0	0	0	0	0	0	0	1
Reduced (.5x)...7.8us	0	0	0	0	0	0	1	0
Extended (2x)...31.3us	0	0	0	0	0	0	1	1
Extended (4x)...62.5us	0	0	0	0	0	1	0	0
Extended (8x)...125us	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
TBD	0	0	0	0	0	1	1	1
TBD	0	0	0	0	1	0	0	0
TBD	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
Self Refresh Entries								
Normal (15.625us)	1	0	0	0	0	0	0	0
Reduced (0.25x)...3.9us	1	0	0	0	0	0	0	1
Reduced (0.5x)...7.8us	1	0	0	0	0	0	1	0
Extended (2x)...31.3us	1	0	0	0	0	0	1	1
Extended (4x)...62.5us	1	0	0	0	0	1	0	0
Extended (8x)...125us	1	0	0	0	0	1	0	1
TBD	1	0	0	0	0	1	1	0
TBD	.	.	.	.	.	.	.	.
TBD	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	0
TBD	1	1	1	1	1	1	1	1

4.10 Byte 13, SDRAM width, Primary SDRAM: This field describes the width of the primary SDRAMs used on the module. The primary SDRAM is that which is used for data; examples of primary (data) SDRAM widths are x4, x8, x16, x32. Note that if the module is made with SDRAMs which provide for data and error checking e.g. x9, x18, x36, then it is also designated in this field. Examples using (1 bank) x72 modules include:

Module width	Primary Data SDRAM Width	Error Checking SDRAM Width	Qty Primary Data SDRAMs	Byte 13 (Binary)
x72	x9	—	8	0000 1001
x72	x8	x8	9	0000 1000
x72	x16	x4	4	0001 0000

SDRAM Width, Primary SDRAM Bit 0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
15	0	0	0	0	1	1	1	1
16	0	0	0	1	0	0	0	0
17	0	0	0	1	0	0	0	1
18	0	0	0	1	0	0	1	0
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

4.11 **Byte 14, Error Checking SDRAM data width:** If the module incorporates error checking and if the primary data SDRAM does not include these bits; i.e. there are separate error checking SDRAMs, then the error checking SDRAM's width is expressed in this byte. Examples of error checking SDRAM widths include x4, x8, x16. For Example:

Module width	Primary SDRAM Width	Error Checking SDRAM Width	Qty of Error Checking SDRAMs	Byte 14 (Binary)
x72	x9	—	—	0000 0000
x72	x8	x8	1	0000 1000
x72	x16	x4	8	0000 0100

SDRAM Width Error Checking DRAM	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

4.12 **Byte 15, as determined by the limiting part on the assembly, SDRAM Device Attributes:** Minimum Clock Delay, Back to Back Random Column Accesses. Note that SDRAM architecture can be gained with this parameter. A latency of 1 for random writes denotes Pipelined SDRAM and a latency of 2 for random writes denotes Prefetch SDRAMs:

Number of Clocks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
.	.					.		
.	.					.		
255	1	1	1	1	1	1	1	1

4.13 **Byte 16, SDRAM Device Attributes, Burst Lengths Supported:** This byte describes which various programmable burst lengths are supported by the devices on the module. If the bit is "1", then that Burst Length is supported on the module; If the bit is "0", then that burst length is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Burst Length = Page	TBD	TBD	TBD	Burst Length = 8	Burst Length = 4	Burst Length = 2	Burst Length = 1
1 or 0	0	0	0	1 or 0	1 or 0	1 or 0	1 or 0

4.14 **Byte 17, SDRAM Device Attributes, Number of Banks on the discrete SDRAM Device:** This byte details how many banks are on each discrete SDRAM installed onto the module:

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
.	.					.		
.	.					.		
255	1	1	1	1	1	1	1	1

4.15 **Byte 18, SDRAM Device Attributes, CAS# Latency:** This byte describes which of the programmable CAS# Latencies are supported by the Module. If the bit is "1", then that CAS# Latency is supported on the module; If the bit is "0", then that CAS# Latency is not supported by the module. Bytes 9,10,23–26 all relate CAS Latency dependent timings.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	CAS# Latency = 7	CAS# Latency = 6	CAS# Latency = 5	CAS# Latency = 4	CAS# Latency = 3	CAS# Latency = 2	CAS# Latency = 1
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.16 **Byte 19, SDRAM Device Attributes, CS# Latency:** This byte describes which of the programmable CS# Latencies are acceptable for the Module. If the bit is "1", then that CS# Latency is supported on the module; If the bit is "0", then that CS# Latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	CS# Latency = 6	CS# Latency = 5	CS# Latency = 4	CS# Latency = 3	CS# Latency = 2	CS# Latency = 1	CS# Latency = 0
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.17 **Byte 20, SDRAM Device Attributes, WE# Latency:** This byte describes which of the programmable WE# Latencies are acceptable for the Module. If the bit is "1", then that WE# Latency is supported on the module; If the bit is "0", then that WE# Latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	WE# Latency = 6	WE# Latency = 5	WE# Latency = 4	WE# Latency = 3	WE# Latency = 2	WE# Latency = 1	WE# Latency = 0
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.18 **Byte 21, SDRAM Module Attributes:** This byte depicts various aspects of the module. It details various unrelated but critical elements pertinent to the module. A given module characteristic is detailed in the designated bit; if the aspect is TRUE, then the bit is "1". Conversely, if the aspect is FALSE, then the designated bit is "0".

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	Differential Clock Input	Registered DQMB Inputs	Buffered DQMB Inputs	On–Card PLL (Clock)	*Registered Address/Control Inputs	*Buffered Address/Control Inputs
0	0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

* Address, RAS, CAS, WE, CKE, CS

4.19 **Byte 22, SDRAM Device Attributes, General:** This byte depicts various aspects of the SDRAMs on the module. It details various unrelated but critical elements pertinent to the SDRAMs. A given SDRAM characteristic is detailed in the designated bit; if the aspect is TRUE, then the bit is "1". Conversely, if the aspect is FALSE, then the designated bit is "0".

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	TBD	TBD	Supports Write1/Read Burst	Supports Precharge All	Supports Auto–Precharge	Supports Early RAS# Precharge
0	0	0	0	1 or 0	1 or 0	1 or 0	1 or 0

4.1.2.6 – Appendix F: Specific PD's for Address Multiplexed ROMs (MXROM).

1.0 Introduction: This appendix describes the Presence Detects for Multiplexed ROM modules. These PD's are those referenced in the SPD standard as "Specific Features". The following PD fields will occur, in the order presented, at the point in the standard where the Specific Features are referenced; that is after the identification of the Fundamental Memory Type and before identification of whether there is any Superset Features presented. For convenience sake however, the complete address map is presented herein.

1.1 Address map: The following is the SPD address map for Multiplexed ROM. It describes where the individual LUT–Entries/ bytes will be held in the serial EEPROM:

Byte Number	Function described	Notes
0	Defines # bytes written into serial memory at module mfgr	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Addresses on this assembly	
4	# Column Addresses on this assembly	
5	# ROM Banks on this Assembly	
6	Data Width of this assembly...	
7	...Data Width continuation	
8	Voltage interface standard of this assembly	
9	Address Access Time of this assembly$	3
10	$Address Access Time continuation	3
11	DIMM Configuration type (Non–parity, Parity, ECC)	
12	Reserved	
13	Page Mode Access Time of this assembly	3
14	Output Enable Access Time of this assembly	3
15	Chip Enable Access Time of this assembly$	3
16	$Chip Enable Access Time continuation	3
17	Burst Length of this assembly	
18–31	Reserved for future offerings	
32	Superset Memory Type (may be used in future)	
33–62	Superset Memory Specific Features (may be used in future)	
63	Checksum for bytes 0–62	
64–71	Manufacturers JEDEC ID code per JEP–106	4
72	Manufacturing location	4
73–90	Manufacturer's Part Number	4
91–92	Revision Code	4
93–94	Manufacturing date	4
95–98	Assembly Serial Number	4
99–125	Manufacturer Specific Data	4
126–127	Reserved	
128–255	Open User Free–Form area$not defined	

notes:

1) This will be 128 bytes for Multiplexed ROM assemblies.
2) This will be 256 bytes, represented as 08h. See below.
3) From data sheet.
4) Per the JEDEC spec, these are optional.

2 **Bytes #0–2, For Reference:** Descriptions of bytes 0–1 can be found in the main body of the SPD standard, and byte 2 is detailed in appendix A to this standard. For reference and convenience, applicable portions of their descriptions are presented again:

2.1 **BYTE #0, From General SPD Standard, Number of Bytes used by Module Manufacturer:** This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

2.2 **Byte #1, From General SPD Standard, Total SPD Memory Size:** This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

2.3 **Byte #2, From Appendix A, Memory Type:** This byte describes the fundamental memory type (or technology) implemented on the module:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
Standard FPM DRAM	0	0	0	0	0	0	0	1
EDO	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
Multiplexed ROM	0	0	0	0	0	1	0	1

3 **Data Type(s):** Even though many of the PD's seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries.

4 The following PD bytes are those specific to modules implementing ROM devices with a multiplexed address interface. Note that full descriptions start at byte 3 and are not covered in the main body of the SPD standard since they are specific to a given fundamental memory type/technology.

4.1 **Byte #3, Number of ROW Addresses:** This first field describes the number of Row Addresses in the ROM array:

No. of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.2 **Byte #4, Number of COLUMN Addresses:** This field describes the number of COLUMN addresses in the module's ROM array:

Number of COLUMN Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.3 **Byte #5, Number of Banks:** This field describes the number of banks on the ROM Module.

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4 **Bytes 6 & 7, Module Data Width:** Bytes 6 and 7 are used to designate the modules data width. The data width is presented as a 16 bit word; bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and bit7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 bits wide, byte 7 will be 00h. If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width. For example, if the module's

data width is:	then byte 7 is	and byte 6 is:
64	0000 0000	0100 0000
72	0000 0000	0100 1000
80	0000 0000	0101 0000
576	0000 0010	0100 0000

4.4.1 Byte 6:

Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
64	0	1	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
72	0	1	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
144	1	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4.2 Byte #7, Module Data Width Continued: This byte will be left at 00h if the original module data width is less than 256 bits wide. If the width is more than 255, then this byte will be used in conjunction with byte 6.

Module Data Width Cont.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	0
1024(+)	0	0	0	0	0	0	1	1
2048(+)	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

4.5 **Byte #8, Module Interface Levels:** This field describes the module's voltage interface:

Voltage Interface	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5	0	0	0	0	0	0	1	0
SSTL 3.3	0	0	0	0	0	0	1	1
SSTL 2.5	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
New Table	1	1	1	1	1	1	1	1

4.6 **Bytes #9 & #10, Address Access Time (t_{AA}):** Bytes 9 and 10 are used to designate the address access time of the module. This access time is presented as a 16 bit word; bit 0 of byte 9 becomes the LSB of the 16 bit access time identifier and bit 7 of byte 10 becomes the MSB. Consequently, if the module has an address access time of less than 256ns, byte 10 will have a value of 00h. If the address access time is 256ns or greater, byte 10 is used in conjunction with byte 9 to designate the total access time.

4.6.1 **Byte 9:**

Address Access Time (LSB)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit	Bit 0
Reserved	0	0	0	0	0	0	0	0
1 (+x0A) ns	0	0	0	0	0	0	0	1
2 (+x0A) ns	0	0	0	0	0	0	1	0
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
254 (+x0A) ns	1	1	1	1	1	1	0	1
255 (+x0A) ns	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
New Table	1	1	1	1	1	1	1	1

4.6.2 **Byte #10, Address Access Time Continued:** This byte will be left at 00h if the address access time of the module is less than 256 nanoseconds. If the address access time of the module is 256 nanoseconds or greater, byte 10 is used in conjunction with byte 9 to determine the access time of the assembly.

Address Access Time (MSB)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (+x09) ns	0	0	0	0	0	0	0	0
256 (+x09) ns	0	0	0	0	0	0	0	1
512 (+x09) ns	0	0	0	0	0	0	1	0
1024 (+x09) ns	0	0	0	0	0	0	1	1
2048 (+x09) ns	0	0	0	0	0	1	0	0
4096 (+x09) ns	0	0	0	0	0	1	0	1
8192 (+x09) ns	0	0	0	0	0	1	1	0
16384 (+x09) ns	0	0	0	0	0	1	1	1
–	–	–	–	–	–	–	–	–

4.7 **Byte #11, Module Configuration type:** This field describes the module's error detection and or correction schemes:

Error Det/Cor	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	1

4.8 **Byte #12, Reserved:** This byte is reserved for future offerings.

4.9 **Byte #13, Page Mode Access Time (t_{PA}):** Byte 13 represents the page mode access time from chip enable of the device (t_{PA}) in nanoseconds.

Page Mode Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
1 ns	0	0	0	0	0	0	0	1
2 ns	0	0	0	0	0	0	1	0
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
253 ns	1	1	1	1	1	1	0	1
254 ns	1	1	1	1	1	1	1	0
New Table	1	1	1	1	1	1	1	1

4.10 **Byte #14, Output Enable Access Time (t_{OE}):** Byte x14 represents the access time from output enable of the device (t_{OE}) in nanoseconds.

Output Enable Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
1 ns	0	0	0	0	0	0	0	1
2 ns	0	0	0	0	0	0	1	0
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
253 ns	1	1	1	1	1	1	0	1
254 ns	1	1	1	1	1	1	1	0
New Table	1	1	1	1	1	1	1	1

4.11 **Bytes #15 & #16, Chip Enable Access Time (t_{OE}):** Bytes 15 and 16 are used to designate the access time from chip enable of the module. This access time is presented as a 16 bit word; bit 0 of byte 15 becomes the LSB of the 16 bit access time identifier and bit 7 of byte 16 becomes the MSB. Consequently, if the module has a chip enable access time of less than 256ns, byte 16 will have a value of 00h. If the chip enable access time is 256ns or greater, byte 16 is used in conjunction with byte 15 to designate the total chip enable access time.

4.11.1 **Byte #15:**

Chip Enable Access Time (LSB)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
1 (+x0F) ns	0	0	0	0	0	0	0	1
2 (+x0F) ns	0	0	0	0	0	0	1	0
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
254 (+x0F) ns	1	1	1	1	1	1	0	1
255 (+x0F) ns	1	1	1	1	1	1	1	1

4.11.2 **Byte #16, Chip Enable Access Time Continued:** This byte will be left at 00h if the chip enable access time of the module is less than 256 nanoseconds. If the chip enable access time of the module is 256 nanoseconds or greater, byte 16 is used in conjunction with byte 15 to determine the chip enable access time of the assembly.

Chip Enable Access Time (MSB)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (+x0F) ns	0	0	0	0	0	0	0	0
256 (+x0F) ns	0	0	0	0	0	0	0	1
512 (+x0F) ns	0	0	0	0	0	0	1	0
1024 (+x0F) ns	0	0	0	0	0	0	1	1
2048 (+x0F) ns	0	0	0	0	0	1	0	0
4096 (+x0F) ns	0	0	0	0	0	1	0	1
8192 (+x0F) ns	0	0	0	0	0	1	1	0
16384 (+x0F) ns	0	0	0	0	0	1	1	1
–	–	–	–	–	–	–	–	–

4.12 **Byte #17, Burst Length:** Byte 17 is an 8 bit mask which indicates all burst lengths supported by the device. If a bit in byte 17 is "1" then the associated burst length is supported by the module. If the bit is "0", then that burst length is not supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Burst Length = Page	TBD	TBD	TBD	Burst Length 8	Burst Length 4	Burst Length 2	Burst Length 1
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.13 **Bytes 18–31:** Open. There are no defined PD settings for these bytes.

4.14 **Bytes 32 through 62, Superset information:** If a superset technology is developed and is completely backward compatible, it may be specified and its SPD may be defined in bytes 32 through 62.

4.15 **Byte 63, Checksum for bytes 0–62:** At time of the publish of this standard, the checksum method is currently in ballot and is not yet incorporated, suggested method is modulo 256.

5 **From the general SPD standard:** The descriptions of bytes 64–127 are repeated here For Reference ONLY. Manufacturers MAY include information which is pertinent to their particular modules, place and date of manufacture, etc. If a module manufacturer decides to write data into bytes 64–127, they must follow the format and order presented below. If a module manufacturer chooses not to include the data outlined below, they must leave bytes 64–127 unprogrammed; blank state of these bytes may be 00h or FFh. Detailed implementation of bytes 64–127 is detailed below in paragraphs 5.X:

5.1 **Bytes 64–71, Manufacturers ID code per EIA/JEP106.** Manufacturers of a given module may include their identifier per Jedec spec JEP106. 00h is not allowed and FFh indicated continuation. The first byte is utilized, the second byte filling. Unused locations/bytes should be FFh.

5.2 **Byte 72, Manufacturing Location.** Manufacturers may include an identifier which uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

5.3 **Bytes 73–90, Manufacturer's Part Number:** Manufacturers may include their part number in 6–bit ASCII format within these bytes.

5.4 **Bytes 91–92, Revision Code:** This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

5.5 **Bytes 93–94, Date of Module Manufacture:** The module manufacturer may include a date code for the module. Specifically, byte 93 may contain the year in Binary and byte 94 may contain the week in Binary.

5.6 **Bytes 95–98, Module Serial Number:** The supplier may include a serial number for module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

5.7 **Bytes 99–125, Manufacturers specific data, open area:** The module manufacturer may add any additional information desired into the module within these locations.

5.8 **Bytes 126–127, Reserved:** These bytes are reserved and cannot be later allocated.

4.2 One Byte Memory Modules

4.2.1 – 22 PIN SIP/SIMM DRAM MODULE

CAPACITY—64K, 256K WORDS OF 4 BITS
CONFIGURATION—SINGLE SIDED MODULE USING 64K OR 256K DEVICES
PACKAGE—22 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–1

– 24 PIN SIP/SIMM DRAM MODULE

CAPACITY—128K, 512K WORDS OF 4 BITS
CONFIGURATION—DOUBLE SIDED MODULE USING 64K OR 256K DEVICES
PACKAGE—24 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–1

– 30 PIN SIP/SIMM DRAM MODULE

CAPACITY—64K, 256K, 1M, 4M WORDS OF 8 OR 9 BITS, & 16M WORDS OF 8 BITS
CONFIGURATION—SINGLE SIDED MODULE
—USING 64K, 256K, 1M, 4M, OR 16M MEMORY DEVICES
LOGIC FEATURES—Some of the modules contain a "presence detect" feature which conists of outputs that supply an encoded value which defines the storage capacity of the module.
PACKAGE—30 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–1

4.2.2 – 30 PIN SIP/SIMM DRAM MODULE FAMILY

CAPACITY —64K TO 8M WORDS OF 4 OR 5 BITS
—128K TO 16M WORDS OF 2 BITS
—256K TO 32M WORDS OF 1 BIT
CONFIGURATION—ONE OR TWO SIDED,
—USING 64K, 256K, 1M, OR 4M DEVICES
CAPACITY—32K, 64K, 128K, 256K WORDS OF 8 BITS
PACKAGE—30 PIN SIP MODULE
PIN ASSIGNMENT Fig. 4.2–2

4.2.3 – 23/25/26/28 PIN ZIP/SIMM DRAM MODULE FAMILY

CAPACITY —256K TO 16M WORDS OF 4 BIT
—1M TO 64M WORDS OF 1 BIT
CONFIGURATION—DOUBLE SIDED, USING 1M, 4M, 16M, OR 64M DEVICES
PACKAGE—THE X4 MODULES, 26 PIN ZIP/SIP MODULE
THE X1 MODULES, 23 PIN ZIP/SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–3
NOTE: At the highest density using 64M memory devices, the modules must be expanded to 25 or 28 pins to provide the needed addresses. These modules will be defined in more detail when the packages for the 64M memory devices have been defined.

4.2.4 – 60 PIN ZIP/SIMM SRAM MODULE

CAPACITY—2 X 64K, 2 X 256K, 2 X 1M WORDS OF 4 BITS
CONFIGURATION—DUAL BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 8, 128K, 512K, OR 2M BY 4
PACKAGE—60 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.2–4

– 70 PIN ZIP/SIMM SRAM MODULE

CAPACITY—64K, 256K, 1M WORDS OF 9 BITS
CONFIGURATION—SINGLE BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 9
LOGIC FEATURE—SEPARATELY CONTROLLABLE BIT FOR USE AS PARITY BIT
PACKAGE—70 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.2–5

PHYSICAL CONFIGURATION	4 DEVICES LONG				8 OR 9 DEVICES LONG			
	SINGLE BANK		DOUBLE BANK		SINGLE BANK			DOUBLE BANK
VERSION	N X 4	@ 4N X 1	2N X 4	N X 8	* N X 8(9)	* N X 8(9)	16M X 8	* 2N X 8(9)
[1] 1	$ A8	VSS	** NC	% NC	VDD	VDD	VDD	VDD
[2] 2	VDD	VDD	A8	A8	CE	CE	CE	CE
[3] 3	D0	RE0	VDD	VDD	DQ0	DQ0	DQ0	DQ0
[4] 4	Q0	Q	D0	DQ0	A0	A0	A0	A0
[5] 5	CE	A3	Q0	DQ1	A1	A1	A1	A1
[6] 6	A7	A6	CE	CE	DQ1	DQ1	DQ1	DQ1
[7] 7	A5	D	A7	A7	A2	A2	A2	A2
[8] 8	A4	W	A5	A5	A3	A3	A3	A3
[9] 9	D1	RE1	A4	A4	VSS	VSS	VSS	VSS
[10] 10	Q1	A0	D1	DQ2	DQ2	DQ2	DQ2	DQ2
[11] 11	W	A7	Q1	DQ3	A4	A4	A4	A4
[12] 12	A1	A8	W	W	A5	A5	A5	A5
[13] 13	A3	CE	A1	A1	DQ3	DQ3	DQ3	DQ3
[14] 14	A6	RE2	A3	A3	A6	A6	A6	A6
[15] 15	Q2	A2	A6	A6	A7	A7	A7	A7
[16] 16	D3	A1	Q2	DQ4	DQ4	DQ4	DQ4	DQ4
[17] 17	A2	@ A9	D2	DQ5	A8	A8	A8	A8
[18] 18	A0	A4	A2	A2	* A9	* A9	A9	* A9
[19] 19	RE	RE3	A0	A0	* A10	NC	A10	RE2
[20] 20	D3	A5	RE1	RE	DQ5	DQ5	DQ5	DQ5
[21] 21	Q0	VDD	D3	DQ6	W	W	W	W
[22] 22	VSS	VSS	Q3	DQ7	VSS	VSS	VSS	VSS
[23] 23			VSS	VSS	DQ6	DQ6	DQ6	DQ6
[24] 24			*** RE2	NC	# NC	PD1	A11	PD1
[25] 25					DQ7	DQ7	DQ7	DQ7
[26] 26					Q8	PD2	NC	PD2
[27] 27					RE	RE	RE	RE1
[28] 28					CE8	NC	NC	NC
[29] 29					D8	DQ8	NC	DQ8
[30] 30					VDD	VDD	VDD	VDD

TOP VIEW

* ON THE 30 PIN MODULE, 1M & 4M DEVICES MAY BE USED. PINS 18 & 19 ARE USED TO PROVIDE ADDRESS EXPANSION. THE OTHER MODULES WILL ACCOMIDATE 64K & 256K DEVICES ONLY.

** OPTIONAL VSS

*** NC FOR SINGLE BANK VERSION

$ OPTIONAL VSS WHEN A8 NOT NEEDED

OPTIONAL REFRESH (F) FUNCTION

@ ON THE 22 PIN 4N X 1 MODULE, 1 MB & 4 MB DEVICES MAY BE USED. PIN 17 IS USED FOR ADDRESS EXPANSION

% POTENTIAL VSS

PRESENCE DETECT TRUTH TABLE			
SIZE	256K	512K	1M
PIN			
PD1	L	H	L
PD2	H	L	L

CONFIGURATION DEFINES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEVICES ON THE MODULE, GIVING LENGTH AND NUMBER OF SIDES POPULATED.

VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE "N" IS THE CAPACITY OF THE MEMORY DEVICE USED.

FIGURE 4.2-1

22, 24,& 30 PIN DRAM MODULES

PHYSICAL CONFIGURATION		4 OR 5 DEVICES LONG SINGLE SIDED			4 OR 5 DEVICES LONG DOUBLE SIDED		
VERSION		N X 4(5)	2N X 2	4N X 1	2N X 4(5)	4N X 2	8N X 1
[1]	1	VDD					
[2]	2	D4	NC	NC	D4	NC	NC
[3]	3	Q4	NC	NC	Q4	NC	NC
[4]	4	A8					
[5]	5	A9					
[6]	6	*A10					
[7]	7	D3	D1	NC	D3	D1	NC
[8]	8	Q3	Q1	NC	Q3	Q1	NC
[9]	9	VSS					
[10]	10	A6					
[11]	11	A7					
[12]	12	A2					
[13]	13	A1					
[14]	14	D2	NC	D	D2	NC	D
[15]	15	Q2	NC	Q	Q2	NC	Q
[16]	16	A4					
[17]	17	A5					
[18]	18	A3					
[19]	19	A0					
[20]	20	D1	D0	NC	D1	D0	NC
[21]	21	Q1	Q0	NC	Q1	Q0	NC
[22]	22	VSS					
[23]	23	$\overline{W}$					
[24]	24	$\overline{CE}$	$\overline{CE1}$				
[25]	25	NC	$\overline{CE2}$				
[26]	26	$\overline{RE}$			$\overline{RE1}$		
[27]	27	NC	NC	NC	$\overline{RE2}$		
[28]	28	D0	NC	$\overline{CE3}$	D0	NC	$\overline{CE3}$
[29]	29	Q0	NC	$\overline{CE4}$	Q0	NC	$\overline{CE4}$
[30]	30	VDD					

30 PIN SIP MODULE TOP VIEW

* PIN 6 RESERVED FOR OPTIONAL REFRESH (F) WHEN NOT NEEDED FOR A10

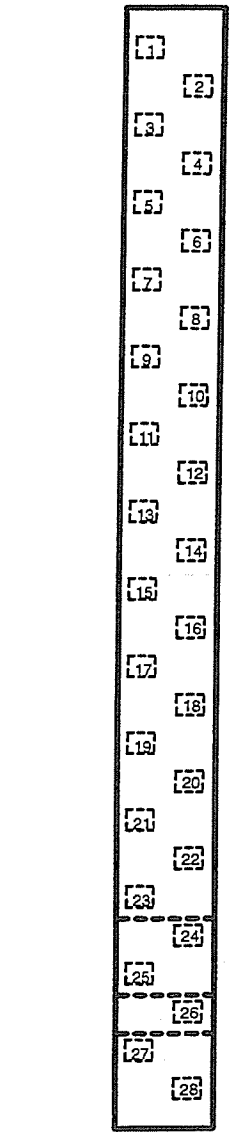
CONFIGURATION DEFINES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEFICES ON THE MODULE, GIVING LENGTH AND NUMBER OF SIDES POPULATED

VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE "N" IS THE CAPACITY OF THE MEMORY DEVICE USED

MEMORY DEVICES WITH A CAPACITY OF UP TO 4Mb BY 1 CAN BE ACCOMIDATED ON THE MODULES DEFINED IN THIS STANDARD

FIGURE 4.2–2

30 PIN DRAM MODULE FAMILY



VERSION	@ N X 1	# N X 1	& N X 4	% N X 4
1	VSS	VSS	VSS	VSS
2	$\overline{RE0}$	$\overline{RE0}$	Q0	Q0
3	$\overline{RE1}$	$\overline{RE1}$	D0	D0
4	*A10	A10	Q0	Q0
5	*A9	A9	D1	D1
6	A0	A0	*A10	A10
7	A1	A1	*A9	A9
8	A2	A2	A0	A0
9	A3	A3	A1	A1
10	VCC	VCC	A2	A2
11	D	D	A3	A3
12	Q	Q	VCC	VCC
13	$\overline{W}$	$\overline{W}$	$\overline{RE}$	$\overline{RE}$
14	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
15	VCC	VCC	$\overline{W}$	$\overline{W}$
16	A4	A4	VCC	VCC
17	A5	A5	A4	A4
18	A6	A6	A4	A4
19	A7	A7	A6	A6
20	A8	A8	A7	A7
21	$\overline{RE2}$	A11	A8	A8
22	$\overline{RE3}$	NC	D2	A11
23	VSS	$\overline{RE2}$	Q2	NC
24		$\overline{RE3}$	D3	D2
25		VSS	Q3	Q2
26			VSS	D3
27				Q3
28				VSS

23, 25, 26, OR 28 PIN ZIP SIMM TOP VIEW

N = THE ADDRESS CAPACITY OF THE MEMORY DEVICE USED

@ THIS CONFIGURATION IS APPLICABLE TO 1M, 4M, & 16M X 1 DEVICES.

THIS CONFIGURATION IS APPLICABLE TO A 64M X 1 DEVICE

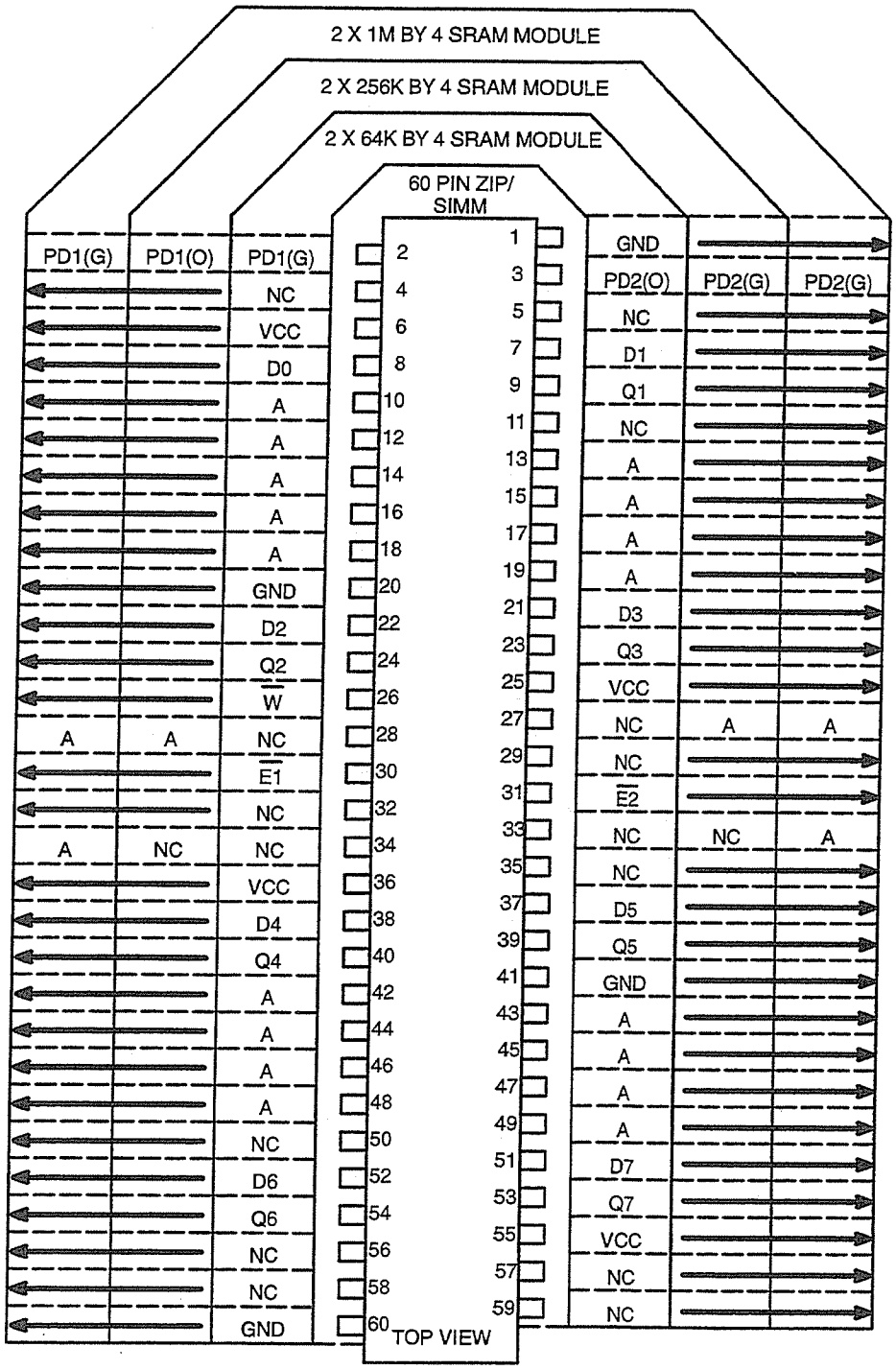
& THIS CONFIGURATION IS APPLICABLE TO 256K, 1M, & 4M X 4 DEVICES.

% THIS CONFIGURATION IS APPLICABLE TO A 16M X 4 DEVICE

* THESE ADDRESS PINS ARE NC WHEN NOT NEEDED FOR THE MEMORY DEVICE USED.

FIGURE 4.2–3

23/25/26/28 PIN DRAM MODULE FAMILY

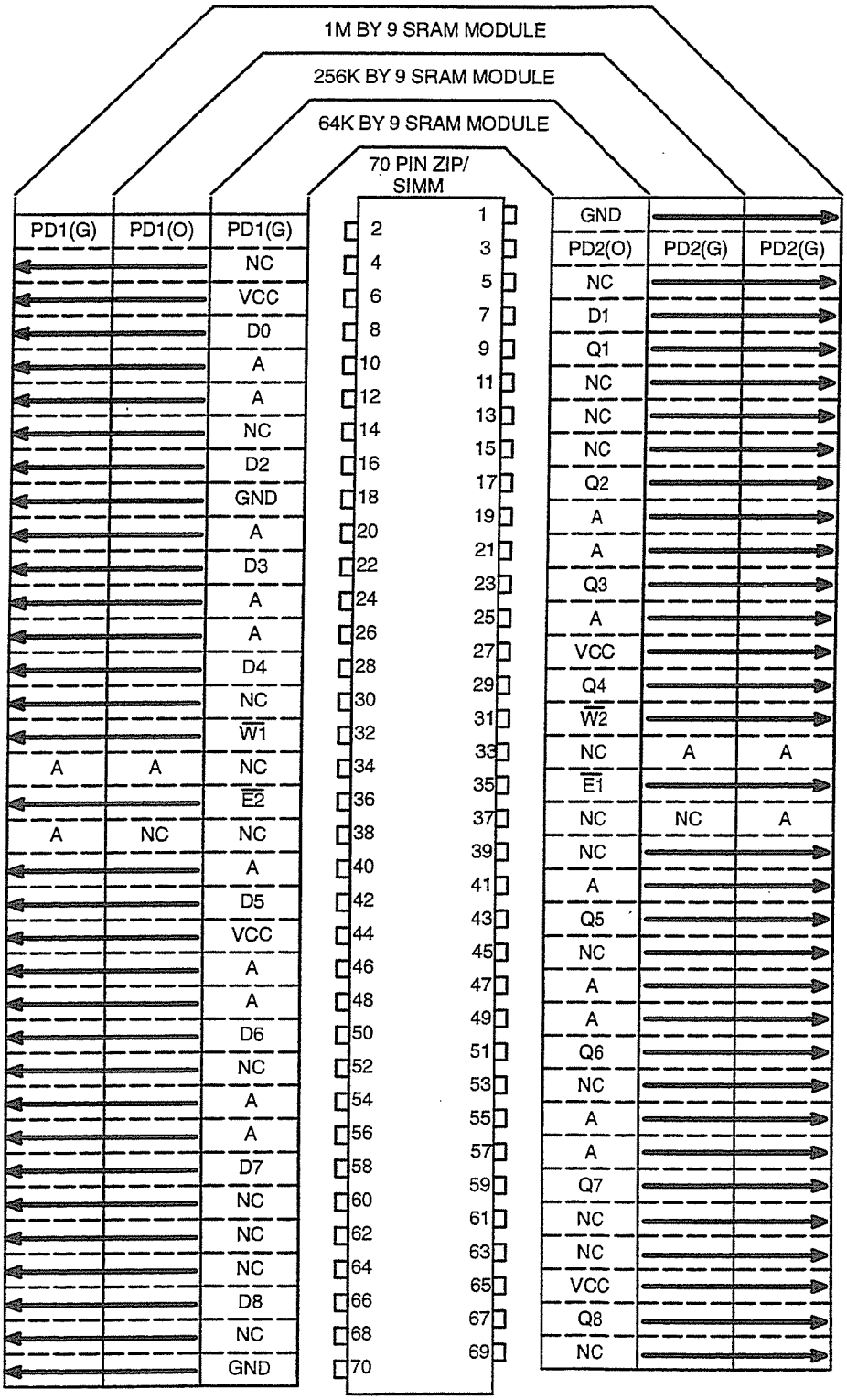


The PD(n) pins are connected to GND (G) or left optn (O).

E1 ENABLES Q0, Q2, Q4, & Q6
E2 ENABLES Q1, Q3, Q5, & Q7

FIGURE 4.2-4

2 X 64K TO 1M BY 4, 60 PIN SRAM MODULE FAMILY



The PD(n) pins are connected to GND (G) or left optn (O).

E1 & W1 CONTROL Q0, Q1, Q2, Q3, Q5, Q6, Q7, Q8
E2 & W2 CONTROL Q4

FIGURE 4.2–5

64K TO 1M BY 9, 70 PIN SRAM MODULE FAMILY

4.3 Two Byte Modules & Cards

4.3.1 – 76 PIN ZIP/SIMM SRAM MODULE

CAPACITY—2 X 64K, 2 X 256K, 2 X 1M WORDS OF 9 BITS
CONFIGURATION—DUAL BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—
SELECTABLE AS 64K, 256K, OR 1M BY 18
128K, 512K, OR 2M BY 9
LOGIC FEATURE—2 SEPARATELY CONTROLLABLE BITS FOR USE AS PARITY BITS
PACKAGE—76 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.3–1

4.3.2 – 40 PIN SIP/SIMM DRAM MODULE FAMILY

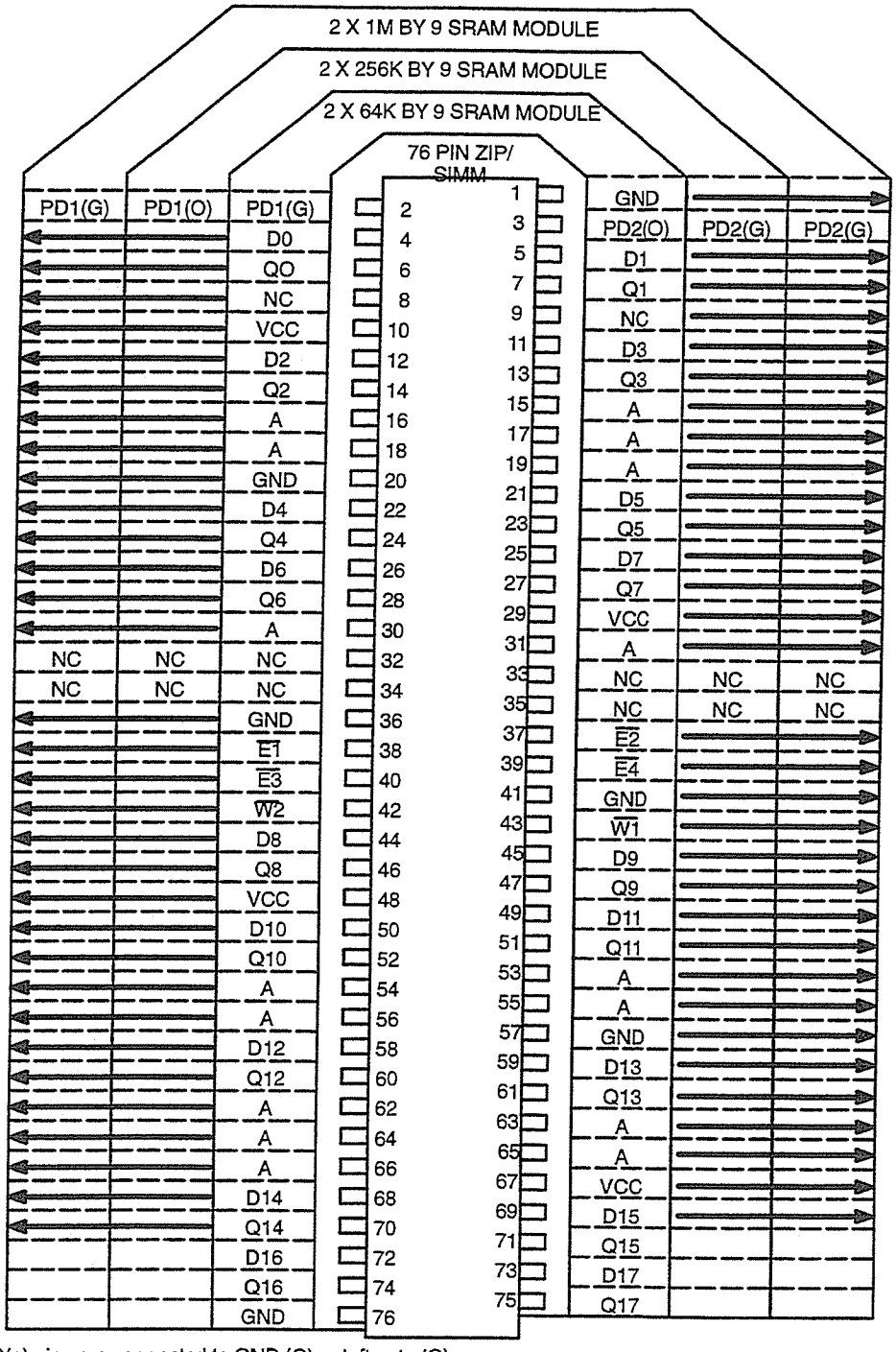
CAPACITY —64K TO 4M WORDS OF 16 OR 18 BITS
—64K TO 8M WORDS OF 8 OR 9 BITS
—128K TO 16M WORDS OF 4 BITS
—256K TO 32M WORDS OF 2 BITS
—512K TO 64M WORDS OF 1 BIT
CONFIGURATION—ONE OR TWO SIDED,
—USING 64K, 256K, 1M, OR 4M DEVICES
PACKAGE—40 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.3–2

4.3.3 – 60 PIN DRAM CARD FAMILY

CAPACITY—512K, 1M, 2M, 4M, & 8M WORDS OF 16 OR 18 BITS
CONFIGURATION—SEVEN DIFFERENT CONFIGURATIONS
—USING 1Mb & 4Mb DEVICES AND WITH 1, 2, OR 4 RE CLOCKS.
LOGIC FEATURES, The cards contain a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.
PACKAGE—60 PIN JEDEC MEMORY CARD
PIN ASSIGNMENTS—Fig. 4.3–3A
CONFIGURATION BLOCK DIAGRAMS—Fig. 4.3–3B

4.3.4 – 68 PIN MULTIPLE TECHNOLOGY MEMORY CARD FAMILY

CAPACITY—UP TO 32M WORDS OF 16 BITS
CONFIGURATION—ONE BASIC CONFIGURATION that allows the use of SRAM, EEPROM, EPROM, or ROM memory devices with software or firmware control to accomidate the device characteristic differences.
LOGIC FEATURES,
—The card contains an internal MEMORY called the "ATTRIBUTE MEMORY"; the contents describe the hardware and software characteristics, and use of the card.
— The card contains a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.
PACKAGE—68 PIN JEDEC MEMORY CARD
PIN ASSIGNMENTS—Fig. 4.3–4A
MEMORY CARD OPERATION TRUTH TABLE— Page 4.3–4B
MEMORY CARD SPECIFIC TERMINOLOGY— Sec. 2.8, Page 2–13



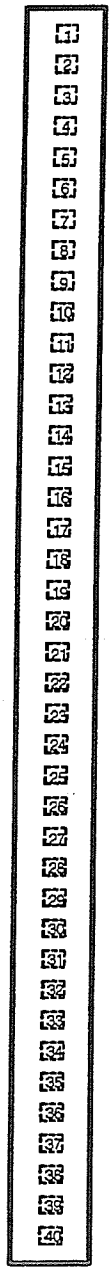
The PD(n) pins are connected to GND (G) or left optn (O).

E1 & W1 CONTROL Q0, Q2, Q4, Q6, Q10, Q12, Q14, Q16
E2 & W1 CONTROL Q1, Q3, Q5, Q7, Q11, Q13, Q15, Q17
E3 & W2 CONTROL Q8
E4 & W2 CONTROL Q9

FIGURE 4.3–1

2 X 64K TO 1M BY 9, 76 PIN SRAM MODULE FAMILY

PHYSICAL CONFIGURATION	8 OR 9 DEVICES LONG, SINGLE SIDED				8 OR 9 DEVICES LONG, DOUBLE SIDED			
VERSION	N X 8(9)	2N X 4	4N X 2	8N X 1	4N X 4	8N X 2	16N X 1	@ N X 18
1	VDD							
2	NC							Q0
3	NC							D0
4	D0	NC						D17
5	Q0	NC						Q17
6	*A10							
7	D1	NC			DQ0'	NC		DQ1
8	Q1	DQ0	NC		DQ0	NC		DQ16
9	A9							
10	VSS							
11	W							
12	D2	NC		CE1	CE1	NC	CE1	DQ2
13	Q2	CE1		CE2	CE2	CE1	CE2	DQ15
14	A8							
15	A7							
16	D3	NC			DQ1'	DQ0'	DQ'	DQ3
17	Q3	DQ1	DQ0		DQ1	DQ0	DQ	DQ14
18	A6							
19	A5							
20	A4							
21	D4	NC		CE3	NC		CE3	DQ4
22	Q4	NC	CE2	CE4	NC	CE2	CE4	DQ13
23	A3							
24	A2							
25	D5	NC			DQ2'	NC		DQ5
26	Q5	DQ2	NC		DQ2	NC		DQ12
27	A1							
28	A0							
29	D6	NC		CE5	NC		CE5	DQ6
30	Q6	NC	CE2	Q6	NC	CE3	CE6	DQ11
31	VSS							
32	D7	NC			DQ3'	DQ1'	NC	DQ7
33	Q7	DQ3	DQ1	NC	DQ3	DQ1	NC	DQ10
34	CE	CE2	CE4	CE7	CE3	CE4	CE7	CE1
35	NC			CE8	CE4	NC	CE8	CE2
36	RE				RE1			
37	NC				RE2			
38	D8	NC						DQ8
39	Q8	NC						DQ9
40	VDD							



40 PIN SIP MODULE TOP VIEW

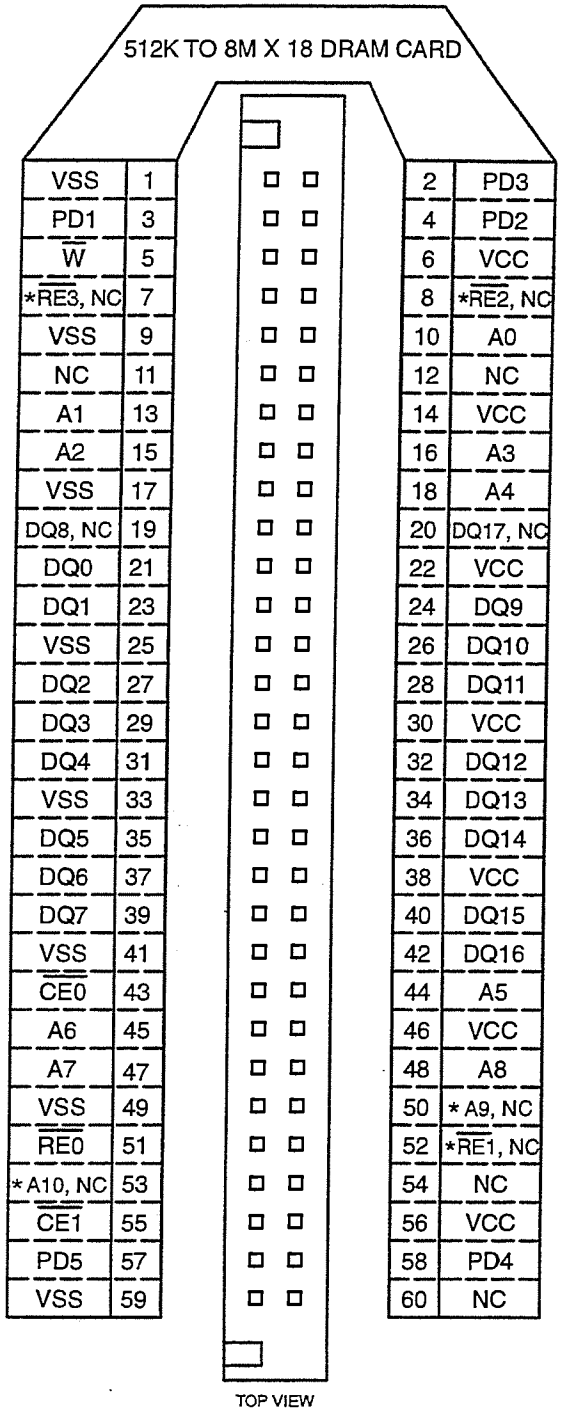
* PIN 5 RESERVED FOR OPTIONAL REFRESH (F) WHEN NOT NEEDED FOR A10

@ N X 18 MODULE CAN BE USED AS A 2N X 9 BY CONNECTING ADJACENT D, Q, & DQ PINS TOGETHER

CONFIGURATION GIVES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEVICES ON THE MODULE GIVING LENGTH AND NUMBER OF SIDED POPULATED. VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE "N" IS THE CAPACITY OF THE MEMORY DEVICE USED.

THOSE PIN NAMES LABELED "'" (PRIME) ARE CONNECTED TO THE BACK SIDE OF THE MODULE ON THE DOUBLE SIDED CONFIGURATIONS.

FIGURE 4.3–2
40 PIN DRAM MODULE FAMILY



* SEE TABLE FOR FUNCTION ASSIGNMENTS FOR THESE PINS AS A FUNCTION OF CARD CAPACITY AND CONFIGURATION

	PD4	PD5
SPEED (tRAC)	58	57
80 NS	VSS	VSS
70 NS	VSS	NC
60 NS	NC	VSS
50 NS	NC	NC

PD SPEED TABLE

	PD1	PD2	PD3
CONFIGURATION	3	4	2
512K X 16/18 2 $\overline{RE}$	VSS	NC	VSS
1M X 16/18 4 $\overline{RE}$	VSS	NC	NC
2M X 16/18 2 $\overline{RE}$	NC	VSS	VSS
4M X 16/18 4 $\overline{RE}$	NC	VSS	NC
1M X 16/18 1 $\overline{RE}$	VSS	VSS	VSS
4M X 16/18 1 $\overline{RE}$	NC	NC	VSS
8M X 16/18 2 $\overline{RE}$	VSS	VSS	NC
NO CARD	NC	NC	NC

PD CONFIGURATION TABLE

	PIN NUMBER				
CONFIGURATION	50	53	52	8	7
512K X 16/18 2 $\overline{RE}$	NC	NC	RE1	NC	NC
1M X 16/18 4 $\overline{RE}$	NC	NC	RE1	RE2	RE3
2M X 16/18 2 $\overline{RE}$	A9	NC	RE1	NC	NC
4M X 16/18 4 $\overline{RE}$	A9	NC	RE1	RE2	RE3
1M X 16/18 1 $\overline{RE}$	A9	NC	NC	NC	NC
4M X 16/18 1 $\overline{RE}$	A9	A10	NC	NC	NC
8M X 16/18 2 $\overline{RE}$	A9	A10	RE1	NC	NC

CONFIGURATION PIN ASSIGNMENT TABLE

Pins 19 & 20 (DQ8 & DQ 17) are NC for X16 Versions

FIGURE 4.3–3A
60 PIN x16 or 18 DRAM CARD FAMILY PIN CONNECTIONS

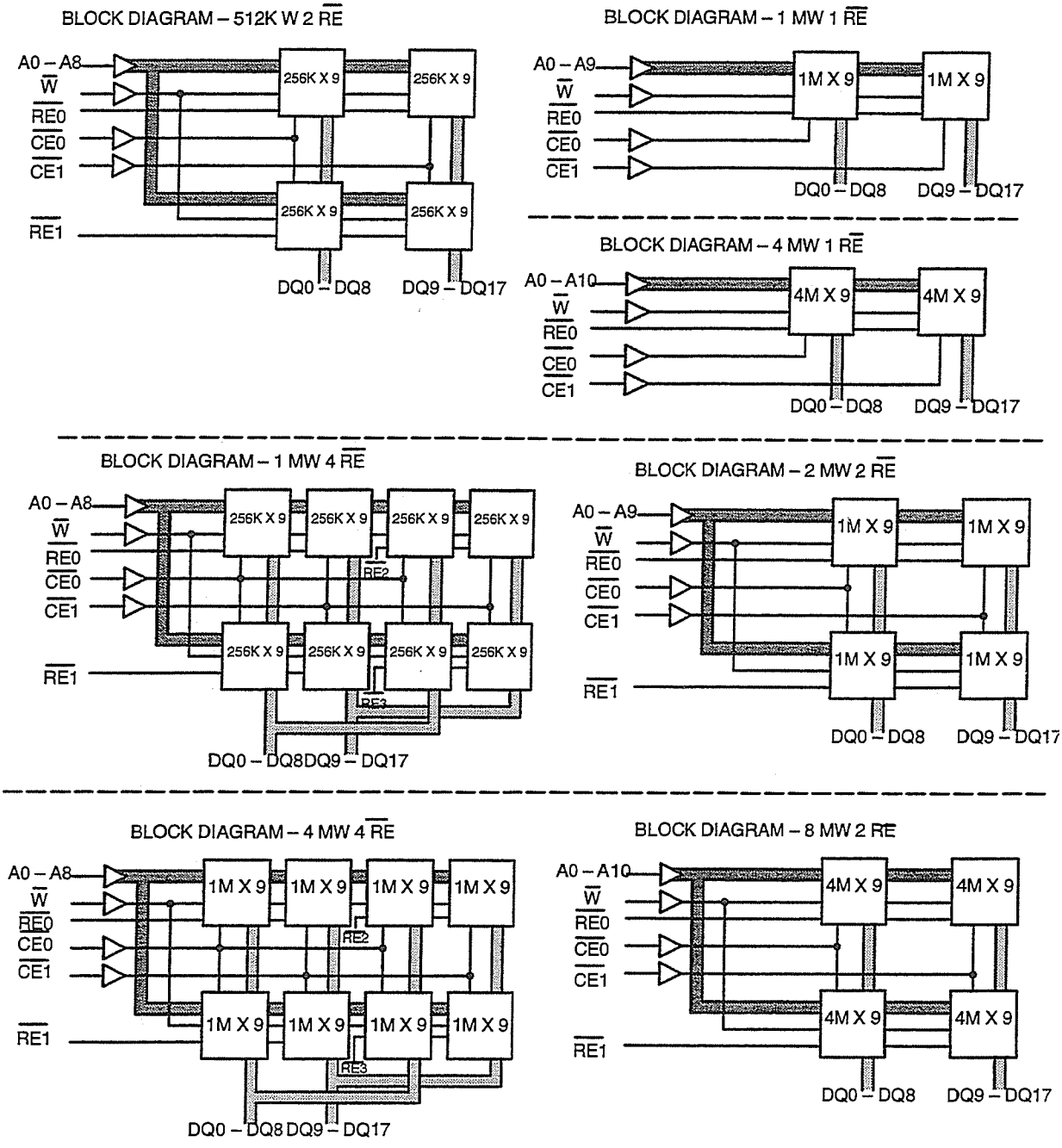
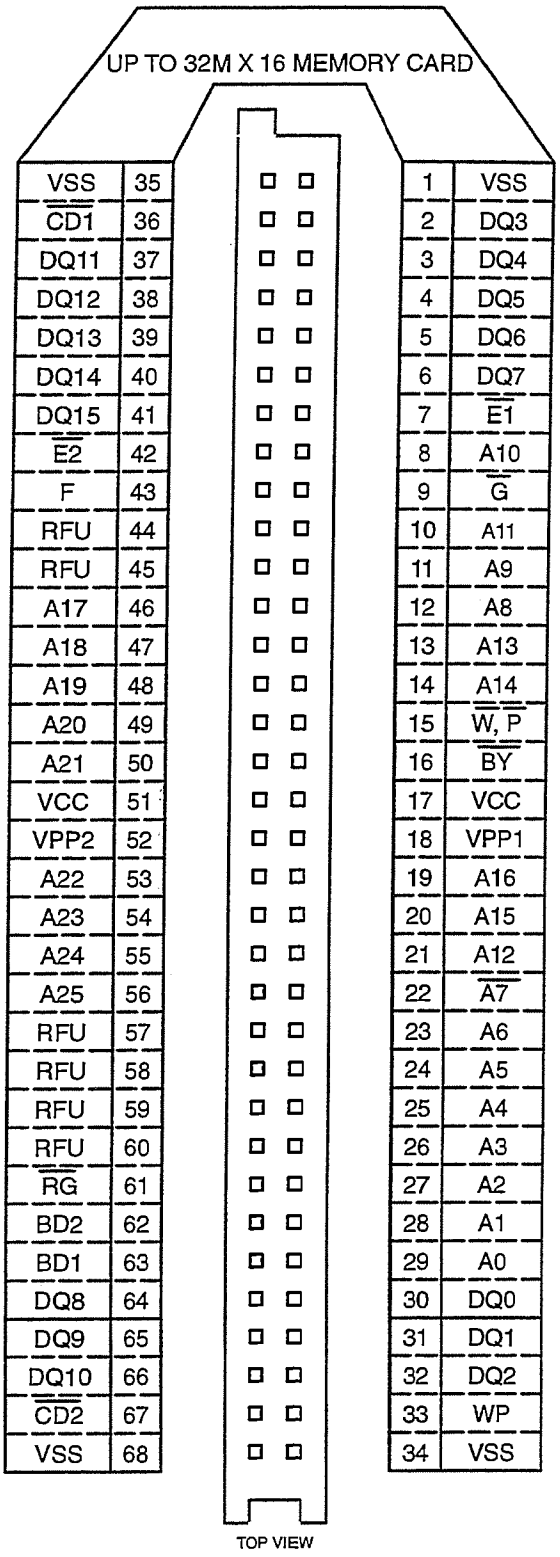


FIGURE 4.3–3B

60 PIN x16 or 18 DRAM CARD FAMILY BLOCK DIAGRAMS



* NOTE: This Standard is applicable to SRAM, EPROM, OTPROM, EEPROM, and FLASH Memory. It is not applicable to DRAM.

FIGURE 4.3–4A

68 PIN MULTIPLE TECHNOLOGY CARD FAMILY

Main Memory Read Function for all types of Memory Card except DRAM										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	High–Z	High–Z
Byte Access (8 bits)	H	H	L	L	L	H	VCC	VCC	High–Z	Even–Byte
	H	H	L	H	L	H	VCC	VCC	High–Z	Odd–Byte
Word Access (16 bits)	H	L	L	X	L	H	VCC	VCC	Odd–Byte	Even–Byte
Odd–Byte Only Access	H	L	H	X	L	H	VCC	VCC	Odd–Byte	High–Z
Main Memory Write Function for SRAM and EEPROM										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	XXX	XXX
Byte Access (8 bits)	H	H	L	L	H	L	VCC	VCC	XXX	Even–Byte
	H	H	L	H	H	L	VCC	VCC	XXX	Odd–Byte
Word Access (16 bits)	H	L	L	X	H	L	VCC	VCC	Odd–Byte	Even–Byte
Odd–Byte Only Access	H	L	H	X	H	L	VCC	VCC	Odd–Byte	High–Z
Main Memory Write Function for OTPROM, EPROM, and FLASH Memory										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC, VPP	VCC, VPP	XXX	XXX
Byte Access (8 bits)	H	H	L	L	H	L	VCC	VPP	XXX	Even–Byte
	H	H	L	H	H	L	VPP	VCC	XXX	Odd–Byte
Word Access (16 bits)	H	L	L	X	H	L	VPP	VPP	Odd–Byte	Even–Byte
Odd–Byte Only Access	H	L	H	X	H	L	VPP	VCC	Odd–Byte	XXX
Attribute Memory Read Function										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	High–Z	High–Z
Byte Access (8 bits)	L	H	L	L	L	H	VCC	VCC	High–Z	Even–Byte
	L	H	L	H	L	H	VCC	VCC	High–Z	Not Valid
Word Access (16 bits)	L	L	L	X	L	H	VCC	VCC	Not Valid	Even–Byte
Odd–Byte Only Access	L	L	H	X	L	H	VCC	VCC	Not Valid	High–Z
Attribute Memory Write Function for SRAM and EEPROM										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	XXX	XXX
Byte Access (8 bits)	L	H	L	L	H	L	VCC	VCC	XXX	Even–Byte
	L	H	L	H	H	L	VCC	VCC	XXX	XXX
Word Access (16 bits)	L	L	L	X	H	L	VCC	VCC	XXX	Even–Byte
Odd–Byte Only Access	L	L	H	X	H	L	VCC	VCC	XXX	XXX
Attribute Memory Write Function for OTPROM, EPROM, and FLASH Memory										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	XXX	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC, VPP	VCC, VPP	XXX	XXX
Byte Access (8 bits)	L	H	L	L	H	L	VCC	VPP	XXX	Even–Byte
	L	H	L	H	H	L	VCC	VCC	XXX	XXX
Word Access (16 bits)	L	L	L	X	H	L	VPP	VPP	XXX	Even–Byte
Odd–Byte Only Access	L	L	H	X	H	L	VPP	VCC	XXX	XXX

NOTE: For those pins in the above tables where "VCC, VPP" is specified, either supply may be used for programming at the option of the manufacturer. However those cards which use VCC must be able to withstand VPP without damage.

FIGURE 4.3–4B

68 PIN MULTIPLE TECHNOLOGY CARD FAMILY FUNCTION TABLES

4.4 Four Byte Modules & Cards

4.4.1 – 64 & 72 PIN ZIP/SIMM SRAM MODULE

4.4.2 – 72 PIN SIMM DRAM MODULE FAMILY

– 72 PIN SIMM DRAM ECC MODULE FAMILY

4.4.3 – 88 PIN DRAM CARD FAMILY

4.4.4 – 72 PIN DRAM SO–DIMM FAMILY

4.4.5 – 88 PIN DRAM SO–DIMM FAMILY

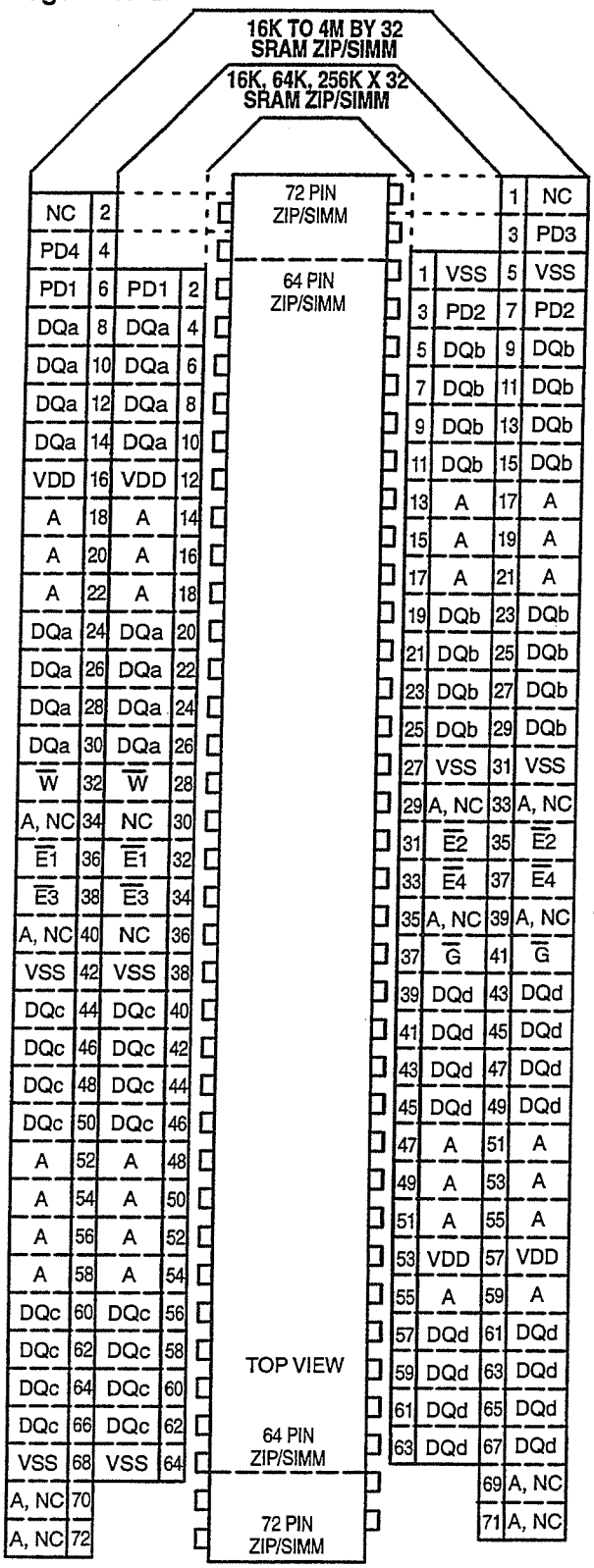
4.4.6 – 112 PIN MPDRAM DIMM FAMILY

4.4.7 – 80 PIN EEPROM SIMM FAMILY

4.4.8 – 100 PIN DRAM, SDRAM & ROM DIMM FAMILY

4.4.1 – 64 & 72 PIN ZIP/SIMM SRAM MODULE

CAPACITY—16K, 32K, 64K, 128K, 256K, 512K, 1M, 2M, or 4M WORDS OF 32 BITS
CONFIGURATION—FOUR BANK MODULE
—SELECTABLE BY BYTE GROUPS
LOGIC FEATURE—The 72 pin modules are supersets of the 64 pin family with added capacity.
PACKAGE—64 and 72 PIN SIP MODULEWITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.4.1–1



NOTES for 72–pin ZIP/SIMM module pinout:
1. $\overline{E1}$ enables DQa pins 8, 10, 12, 14, and 24, 26, 28, 30; $\overline{E2}$ enables DQb pins 9, 11, 13, 15, and 23, 25, 27, 29; $\overline{E3}$ enables DQc pins 44, 46, 48, 50, and 60, 62, 64, 66; $\overline{E4}$ enables DQd pins 43, 45, 47, 49, and 61, 63, 65, 67.
2. $\overline{W}$ enables writing into all enabled devices.
3. $\overline{G}$ enables outputs from any and all enabled devices.
4. This footprint is a superset of the 64–pin JEDEC standard. Any 64 pin JEDEC standard module may be used in the 72–pin footprint. PD3 and PD4 become NC (OPEN) in this case.
5. Two pins (1 & 2) are available for future definition.

PRESENCE DETECT TRUTH TABLE

MOD CONFIG	PD4	PD3	PD2	PD1
72P MOD	PIN 68	PIN 67	PIN 66	PIN 11
# 16K X 32	O	O	O	S
32K X 32	S	S	O	O
# 64K X 32	O	O	S	O
128K X 32	S	O	O	O
# 256K X 32	O	O	S	S
512K X 32	O	S	O	O
1M X 32	O	S	O	S
2M X 32	O	S	S	O
4M X 32	O	S	S	S

O = OPEN CIRCUIT (NO CONNECTION)
S = CONNECTED TO VSS

# Indicates configurations duplicated in 64P package. Use PD1 & PD2 only.

PRESENCE DETECT NOTES
1. Compatibility has been maintained with existing 64–pin standard
2. PD signature has been added for 32K X 32 & 128K X 32 configurations that were not implemented in the 64–pin standard.
3. Six PD signatures are left undefined for future definition.

ADDRESS PIN ASSIGNMENTS

CONFIGURATION	ADDRESS PIN NUMBER							
72 P MODULES	33	34	40	39	69	70	71	72
16K X 32	NC	NC	NC	NC	NC	NC	NC	NC
32K X 32	A	NC	NC	NC	NC	NC	NC	NC
64K X 32	A	A	NC	NC	NC	NC	NC	NC
128K X 32	A	A	A	NC	NC	NC	NC	NC
256K X 32	A	A	A	A	NC	NC	NC	NC
512K X 32	A	A	A	A	A	NC	NC	NC
1M X 32	A	A	A	A	A	A	NC	NC
2M X 32	A	A	A	A	A	A	A	NC
4M X 32	A	A	A	A	A	A	A	A
64 P MODULES	29	30	35	36				
16K X 32	NC	NC	NC	NC				
64K X 32	A	A	NC	NC				
256K X 32	A	A	A	A				

FIGURE 4.4.1–1
16K TO 4M BY 32 SRAM ZIP/SIMM MODULE

NOTE: The 72 pin module standards that follow describe two separate devices. Both have a 4 byte data interface. One is intended to be used with or without parity bits while the other contains error correction bits ECC). The one with ECC is similar to the parity module but is not completely pin compatible

4.4.2 – 72 PIN SIMM DRAM MODULE FAMILY

CAPACITY—256K TO 512M WORDS OF 32 or 36 BITS
CONFIGURATION—SINGLE OR DOUBLE SIDED MODULES
—USING 1M, 4M, 16M. 64M, or 256M MEMORY DEVICES
LOGIC FEATURES, These modules contain a "presence detect" feature which conists of output pins which supply an encoded value which defines the storage capacity and speed of the module.
PACKAGE—72 PIN SIMM MODULE
PIN ASSIGNMENTS—Fig. 4.4.2–2A
BLOCK DIAGRAMS—Fig. 4.4.2–2 A⇒K. A series of block diagrams for recommended configurations is summarized in Fig 4.4.2–1 and detailed in Figs. 4.4.2–2 B⇒K
POWER & INTERFACE VOLTAGE LEVELS: A pinout is provided for 5.0 V and for 3.3 V power and interface levels as defined by a voltage key in the socket.

– 72 PIN SIMM DRAM ECC MODULE FAMILY

CAPACITY—256K TO 512M WORDS OF 36 or 39 BITS
CONFIGURATION—SINGLE OR DOUBLE SIDED MODULES
—USING 1M, 4M, 16M. 64M, or 256M MEMORY DEVICES
LOGIC FEATURES, These modules are optimized for ECC applications. They are similar to but not the same as the modules described in Fig. 4–6. The Standard defines a "presence detect" feature which consists of output pins which supply an encoded value which defines the storage capacity and speed of the module. The PD code identifies the presence of an ECC module as well as the speed and organization of the module. The Standard also defines the logic organization of the modules in Figs. 4.4.2–3B & 4.4.2–3C.
PACKAGE—72 PIN SIMM MODULE
PIN ASSIGNMENTS—Fig. 4.4.2–3A
BLOCK DIAGRAMS—Figs. 4.4.2–3 B & C. A series of block diagrams for recommended configurations is summarized in Fig 4.4.2–1 and detailed in Figs. 4.4.2–3 B & C
POWER & INTERFACE VOLTAGE LEVELS: A pinout is provided for 5.0 V and for 3.3 V power and interface levels as defined by a voltage key in the socket.

72 Pin SIMM Block Diagrams

The block diagrams given in the 12 pages, Figs 4.4.2–2 B ⇒ K and Figs 4.4.2–3 B & C), are applicable to the 72 Pin SIMM pinouts shown in Figures 4.4.2–2 A and 4.4.2–3 A. These block diagrams are provided for guidance only. **Other implementations with different block configurations are also acceptable.**

The following table shows the applicability of the block configurations given to the 5 V and 3.3 V Non–ECC and ECC modules.

Configuration	# Banks	Applies to: 5 V SIMM	Applies to: 3.3 V SIMM
Parity, Non–Parity			
X32/36 W/X4, X1 (X36)	1 or 2	X	X
X32/36 W/X16, X18	1 or 2	X	X
X36 W/X4, X4/4CE	1 or 2	X	X
X36 W/X4, X2/2CE	1 or 2	X	X
X36 W/X16, X4/4CE	1 or 2	X	X
X36 W/X16, X2/2CE	1 or 2	X	X
X32 W/X8	1 or 2		X
X36 W/X8, X2/2CE	1 or 2		X
X32 W/X32	1 or 2		X
X36 W/X32, X2/2CE	1 or 2		X
ECC			
X36/40 W/X4	1 or 2	X	X (X36 only)

Note: To reduce the number of diagrams, only 2 bank versions are shown. In addition, in cases where one SIMM I/O width can be described as a depopulation of another SIMM (i.e. X36⇒X32), the depopulated devices are shown by a "dashed" outline.

$\overline{RE}$ AND $\overline{G}$ WIRING FOR BYTE WRITE SIMMS.		
SIGNAL NAME	5 V SIMMs	3.3 V SIMMs
$\overline{G}$	Tied to GND	Wired to Pin 46
$\overline{RE0}$	Connected as shown. Tied to pin 44 ($\overline{RE0}$)	$\overline{RE0}$, $\overline{RE2}$ nets connected together and tied to pin 44 ($\overline{RE0}$)
$\overline{RE1}$	Connected as shown. Tied to pin 45 ($\overline{RE1}$)	$\overline{RE1}$, $\overline{RE3}$ nets connected together and tied to pin 45 ($\overline{RE1}$)
$\overline{RE2}$	Connected as shown. Tied to pin 34 ($\overline{RE2}$)	$\overline{RE0}$, $\overline{RE2}$ nets connected together and tied to pin 44 ($\overline{RE0}$)
$\overline{RE3}$	Connected as shown. Tied to pin 33 ($\overline{RE3}$)	$\overline{RE1}$, $\overline{RE3}$ nets connected together and tied to pin 45 ($\overline{RE1}$)

FIGURE 4.4.2–1
72 PIN DRAM SIMM APPLICABILITY TABLE

	5 V Byte Write	3.3 V Byte Write
PIN #	PIN NAME	PIN NAME
1	VSS	VSS
2	DQ0	DQ0
3	DQ18	DQ18
4	DQ1	DQ1
5	DQ19	DQ19
6	DQ2	DQ2
7	DQ20	DQ20
8	DQ3	DQ3
9	DQ21	DQ21
10	VDD	VDD
11	NU	PD5
12	A0	A0
13	A1	A1
14	A2	A2
15	A3	A3
16	A4	A4
17	A5	A5
18	A6	A6
19	NC, A10	NC, A10
20	DQ4	DQ4
21	DQ22	DQ22
22	DQ5	DQ5
23	DQ23	DQ23
24	DQ6	DQ6
25	DQ24	DQ24
26	DQ7	DQ7
27	DQ25	DQ25
28	A7	A7
29	NC, A11	NC, A11
30	VDD	VDD
31	A8	A8
32	NC, A9	NC, A9
33	NC, $\overline{RE3}$	NC, A12
34	$\overline{RE2}$	NC, A13
35	PDQ26, NC	PDQ26, NC
36	PDQ8, NC	PDQ8, NC

	5 V Byte Write	3.3 V Byte Write
PIN #	PIN NAME	PIN NAME
37	PDQ17, NC	PDQ17, NC
38	PDQ35,, NC	PDQ35,, NC
39	VSS	VSS
40	$\overline{CE0}$	$\overline{CE0}$
41	$\overline{CE2}$	$\overline{CE2}$
42	$\overline{CE3}$	$\overline{CE3}$
43	$\overline{CE1}$	$\overline{CE1}$
44	$\overline{RE0}$	$\overline{RE0}$
45	NC, $\overline{RE1}$	NC, $\overline{RE1}$
46	NC	$\overline{G}$
47	$\overline{W}$	$\overline{W}$
48	PD(ECC)	PD(ECC)
49	DQ9	DQ9
50	DQ27	DQ27
51	DQ10	DQ10
52	DQ28	DQ28
53	DQ11	DQ11
54	DQ29	DQ29
55	DQ12	DQ12
56	DQ30	DQ30
57	DQ13	DQ13
58	DQ31	DQ31
59	VDD	VDD
60	DQ32	DQ32
61	DQ14	DQ14
62	DQ33	DQ33
63	DQ15	DQ15
64	DQ34	DQ34
65	DQ16	DQ16
66	NC	$\overline{EDO}$
67	PD1	PD1
68	PD2	PD2
69	PD3	PD3
70	PD4	PD4
71	NC	PD(REF)
72	VSS	VSS

PRESENCE DETECT TRUTH TABLE

CONFIGURATION	tRAC	$\overline{ECC}$	PD1	PD2	PD3	PD4
1MB (256K X 36)	100 nS	O	S	O	S	S
64MB (16M X 32/36)	80 nS	O	S	O	O	S
	70 nS	O	S	O	S	O
	60 nS	O	S	O	O	O
2MB (512K X 36)	100 nS	O	O	S	S	S
128MB (32M X 32/36)	80 nS	O	O	S	O	S
	70 nS	O	O	S	S	O
	60 nS	O	O	S	O	O
4MB (1M X 36)	100 nS	O	S	S	S	S
256MB (64M X 32/36)	80 nS	O	S	S	O	S
	70 nS	O	S	S	S	O
	60 nS	O	S	S	O	O
8MB (2M X 36)	100 nS	O	O	O	S	S
0.5GB (128M X 32/36)	80 nS	O	O	O	O	S
	70 nS	O	O	O	S	O
	60 nS	O	O	O	O	O
16MB (4M X 36)	50 nS	O	S	O	S	S
1GB (256M X 32/36)	80 nS	O	S	O	O	S
	70 nS	O	S	O	S	O
	60 nS	O	S	O	O	O
32MB (8M X 36)	50 nS	O	O	S	S	S
2GB (512M X 36)	80 nS	O	O	S	O	S
	70 nS	O	O	S	S	O
	60 nS	O	O	S	O	O

O = NO CONNECTION S = CONNECTED TO VSS

$\overline{EDO}$ Pin: VSS for EDO, NC for Fast Page.

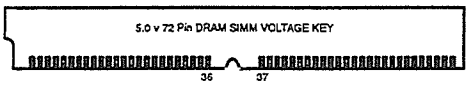
Note: The $\overline{ECC}$ Function (Pin 48) is not a defined function for the devices in this standard, however, it is used in a companion Standard for 72 pin ECC modules shown in Fig. 4–10. The presence of a VSS connection on this pin signifies that an ECC module has been inserted.

CONFIGURATION PIN ASSIGNMENT TABLE

	MODULE SIZE, 36 BIT WORDS											
PIN #	256K	512K	1M	2M	4M	8M	16M	32M	64M	128M	256M	512M
19	NC	NC	NC	NC	A10	A10	A10	A10	A10	A10	A10	A10
*29	NC	NC	NC	NC	A11	A11	A11	A11	A11	A11	A11	A11
32	NC	NC	A9	A9	A9	A9	A9	A9	A9	A9	A9	A9
*33	NC	$\overline{RE3}$	NC	$\overline{RE3}$	NC	$\overline{RE3}$	A12	A12	A12	A12	A12	A12
*34	NC	$\overline{RE2}$	NC	$\overline{RE2}$	NC	$\overline{RE2}$	NC	NC	A13	A13	A13	A13
45	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	RE1

* A11, A12, or A13 on Pins 29, 33, or 34 are used on modules containing devices that require asymetric ROW/ COLUMN addresses.
NOTE – This family of pinouts is approved for use in SIMM modules which are nominally 4.25" long and with a height which varies depencing on the configuration and the memory devices used. See JEDEC Publication 95.

See Figure 4–18 for applicable block diagrams



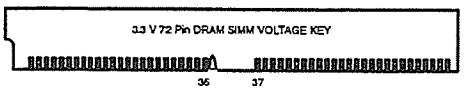


FIGURE 4.4.2–2 A
256K TO 256M BY 36, 72 PIN DRAM MODULE PINOUT

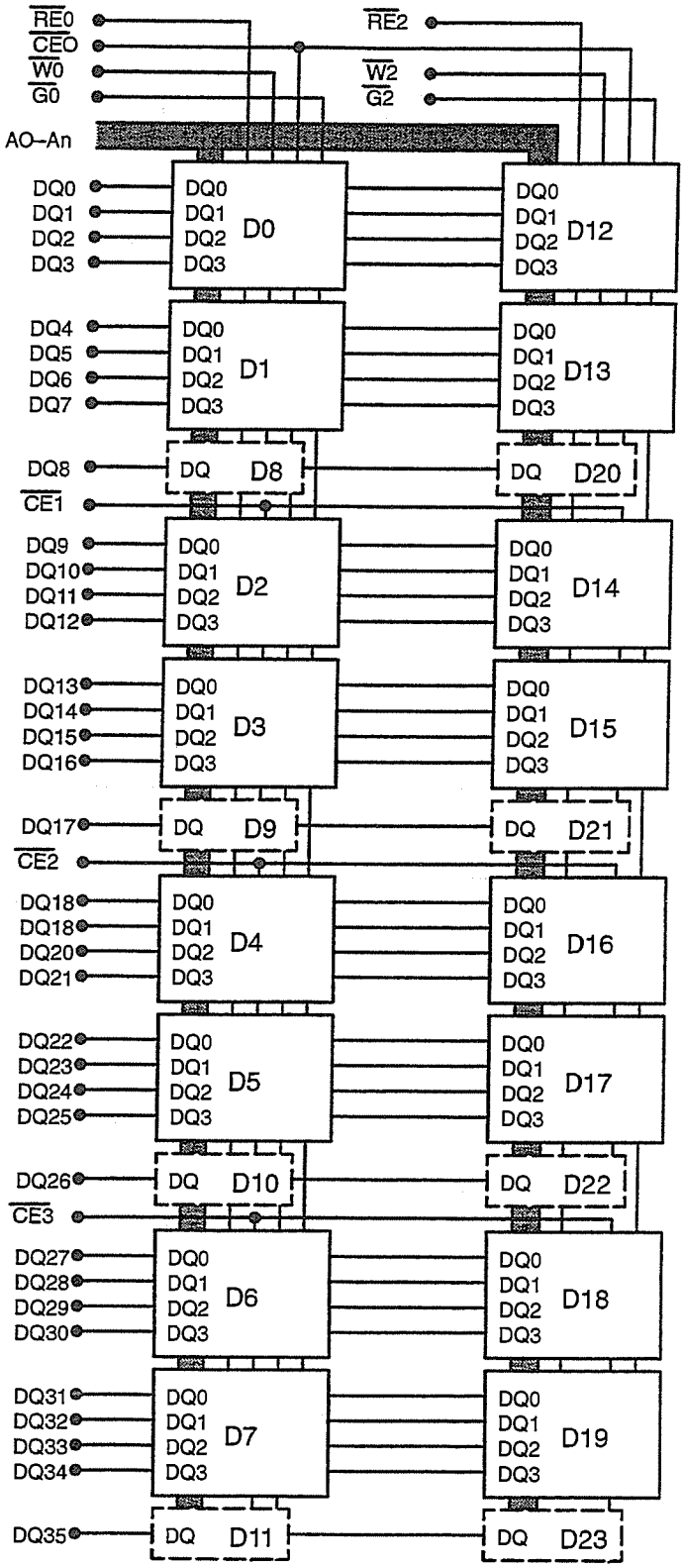
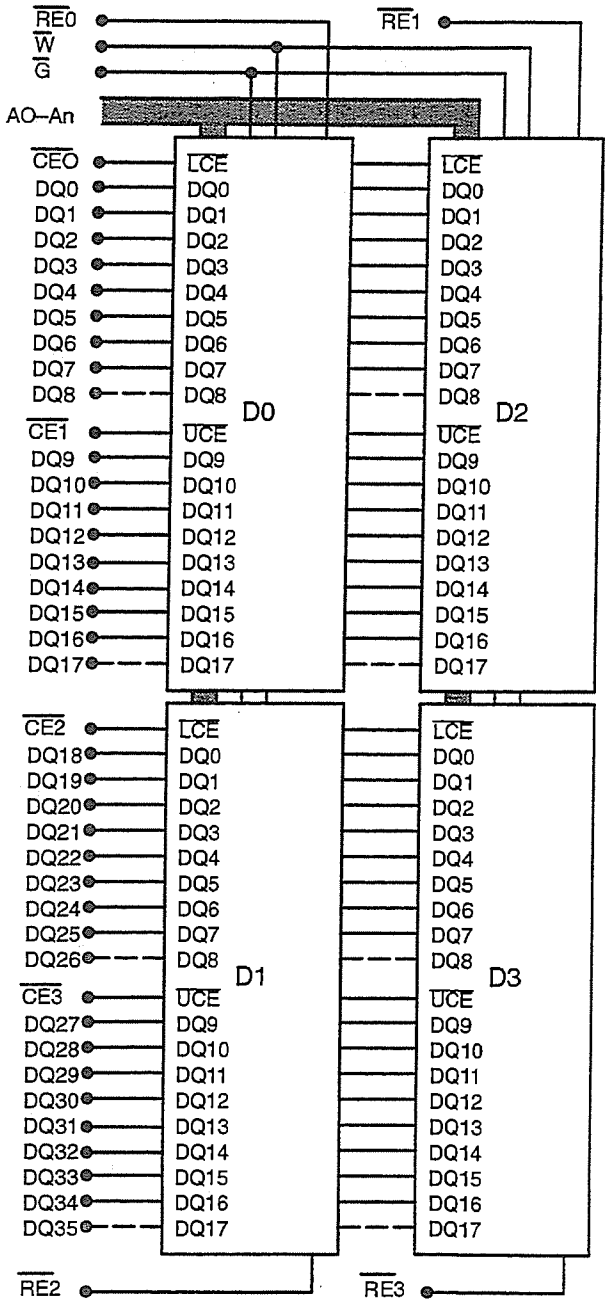


FIGURE 4.4.2–2 B
X32/36 DRAM SIMM, 2 Banks with X4 & X1 DRAMs



DQ8, DQ17, DQ26, & DQ35 ARE NOT USED
ON THE X32 MODULE USING X16 DRAM

FIGURE 4.4.2–2 C
X32/36 DRAM SIMM, 2 Banks with X16/18 DRAMs

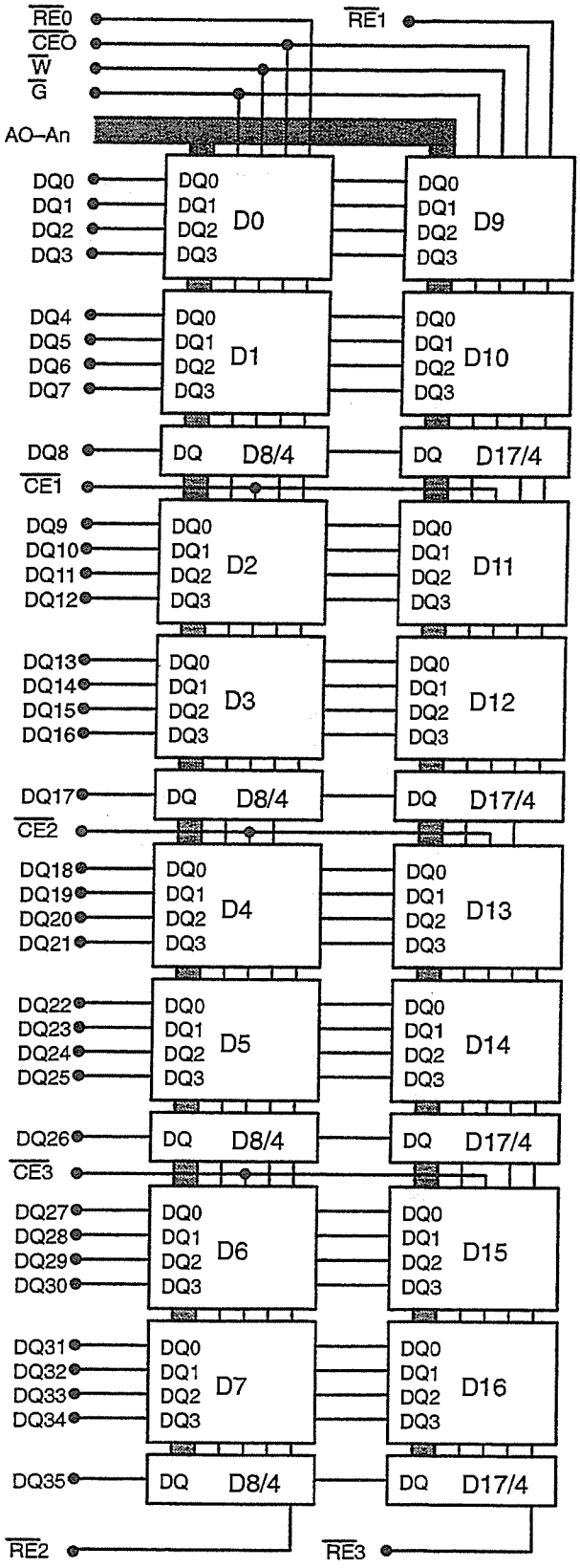


FIGURE 4.4.2–2 D

X36 DRAM SIMM, 2 Banks with X4 & X4 W/4 $\overline{CE}$ DRAMs

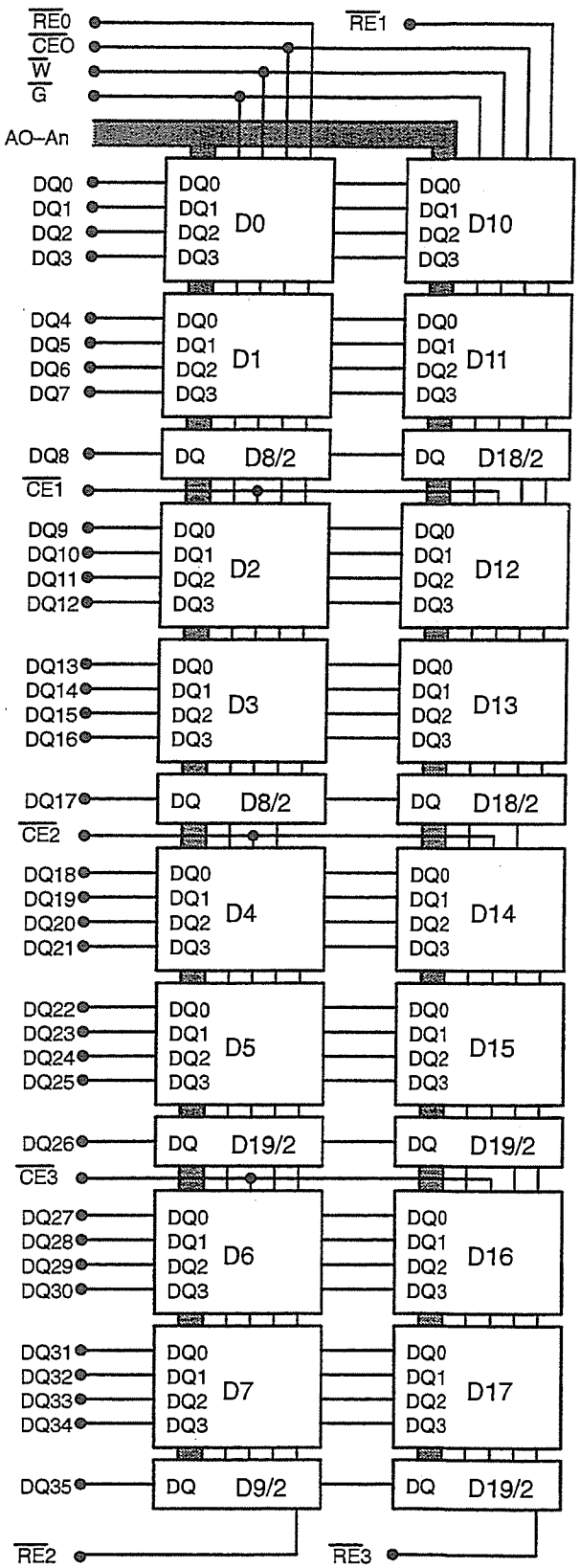


FIGURE 4.4.2–2 E

X36 DRAM SIMM, 2 Banks with X4 & X2 W/2 $\overline{CE}$ DRAMs

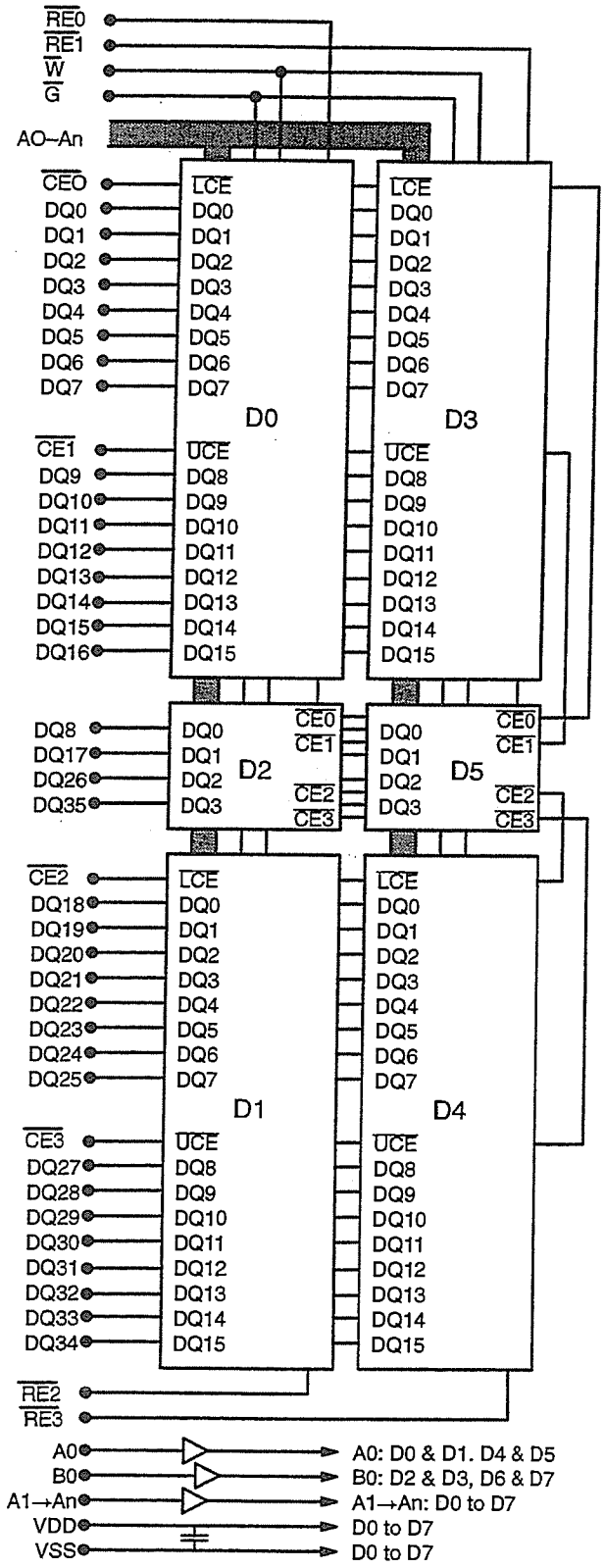


FIGURE 4.4.2–2 F

X36 DRAM SIMM, 2 Banks with X16 & X4 W/4 $\overline{CE}$ DRAMs

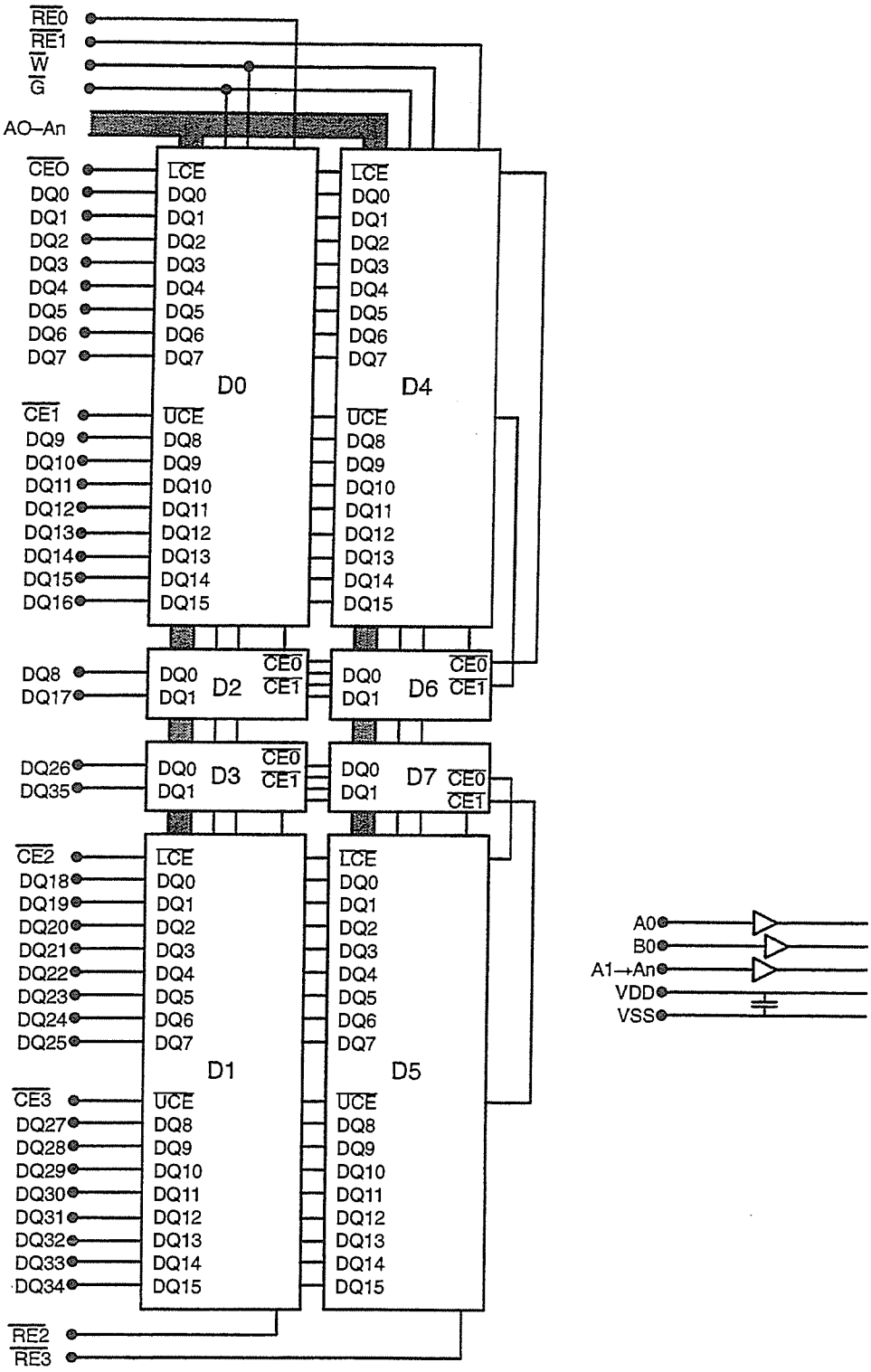


FIGURE 4.4.2–2 G

X36 DRAM SIMM, 2 bank with X16 & X2 W/2 $\overline{CE}$ DRAMs

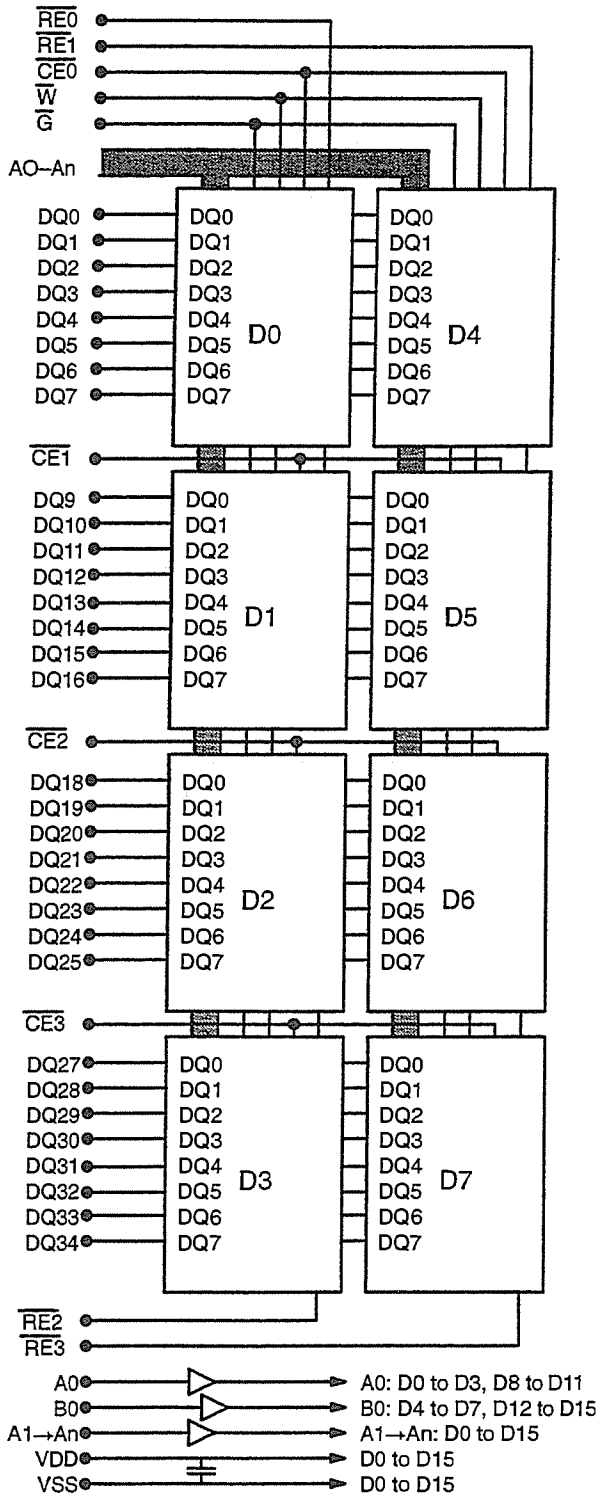


FIGURE 4.4.2–2 H
X32 DRAM SIMM, 2 Banks with X8 DRAMs

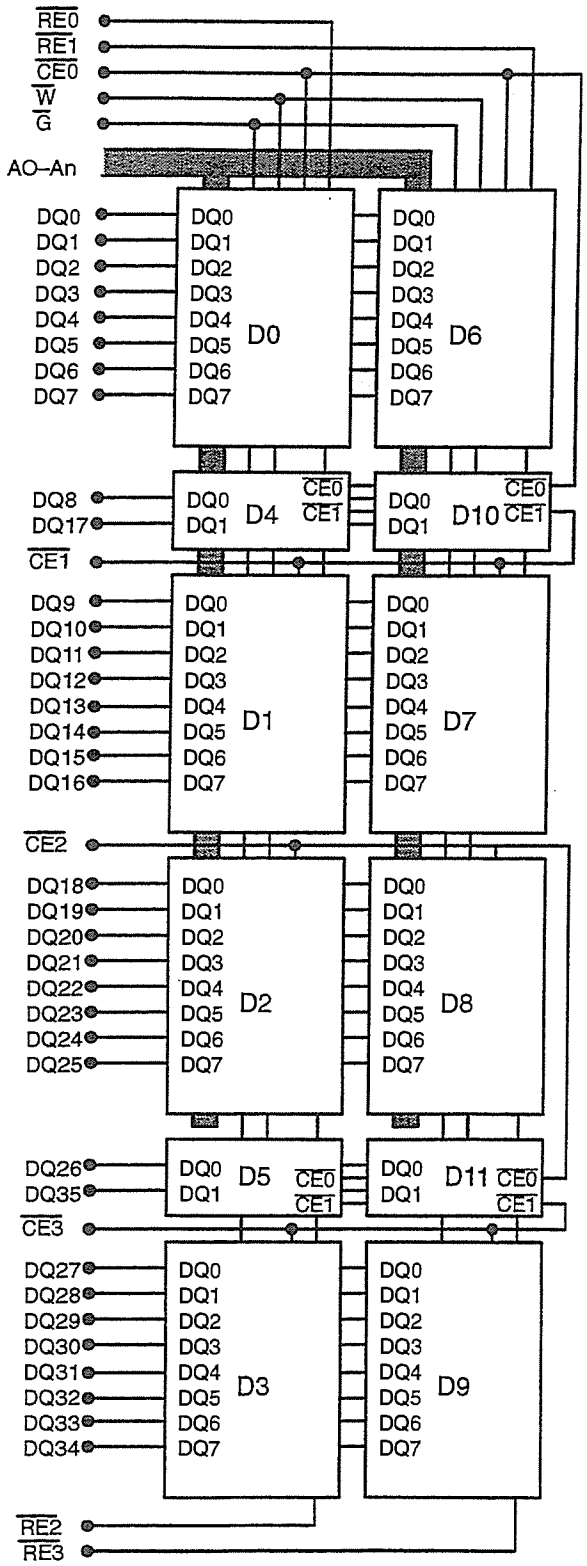


FIGURE 4.4.2–2 I

X36 DRAM SIMM, 2 Banks with X8 & X2 W/2 $\overline{CE}$ DRAMs

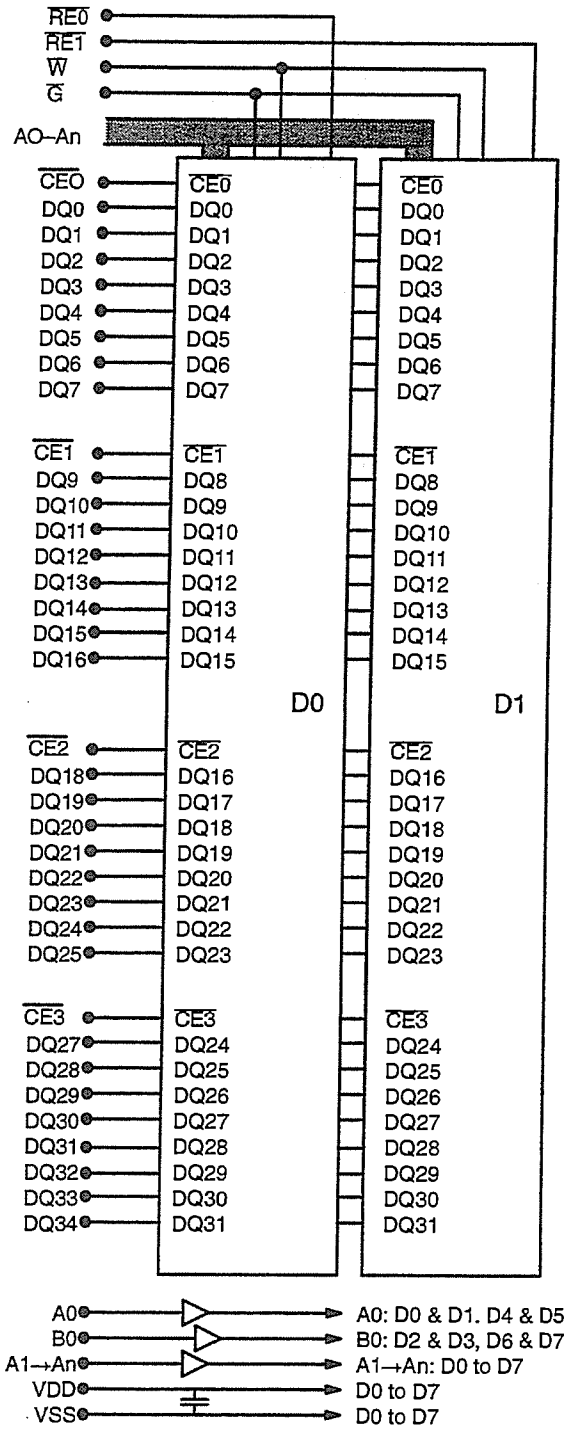


FIGURE 4.4.2–2 J
X32 DRAM SIMM, 2 bank with X32 DRAMs

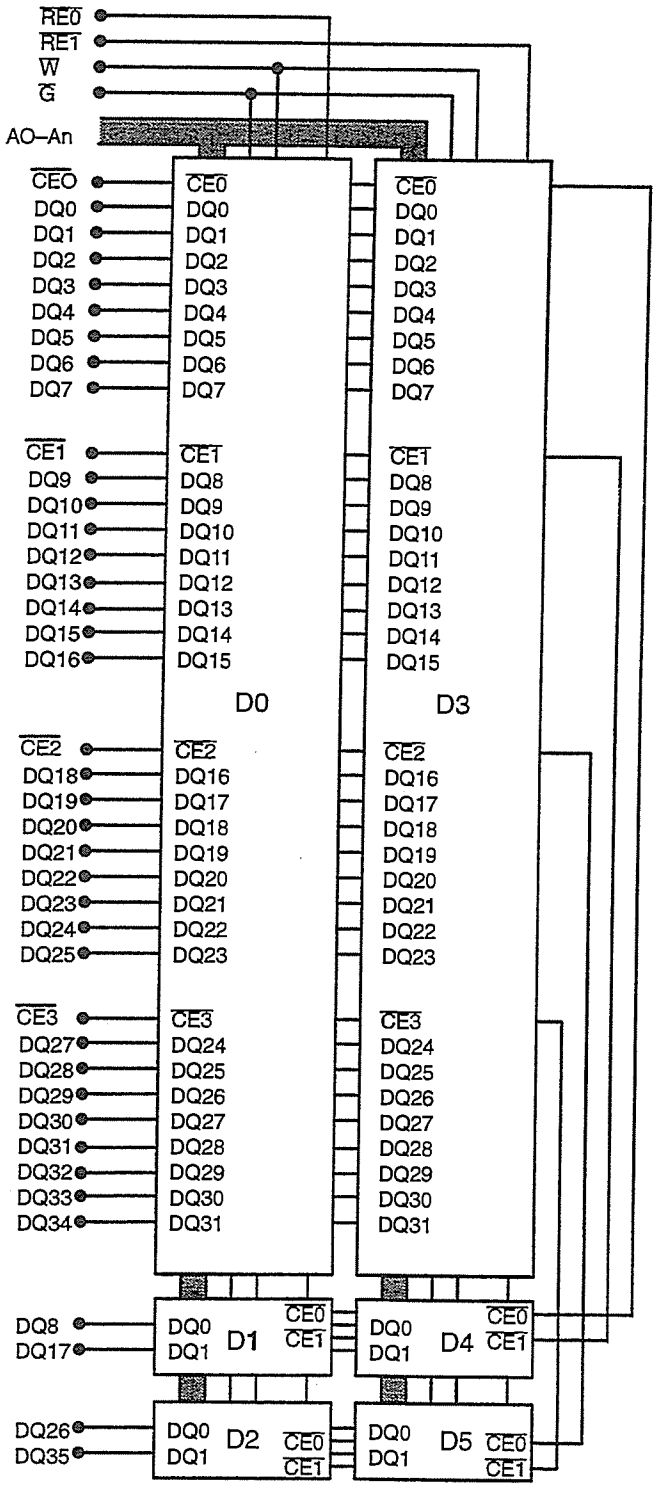


FIGURE 4.4.2–2 K

X36 DRAM SIMM, 2 bank with X32 & X2 W/2 $\overline{CE}$ DRAMs

	5 V ECC	3.3 V ECC
PIN #	PIN NAME	PIN NAME
1	VSS	VSS
2	DQ0	DQ0
3	DQ1	DQ1
4	DQ2	DQ2
5	DQ3	DQ3
6	DQ4	DQ4
7	DQ5	DQ5
8	DQ6	DQ6
9	DQ7	DQ7
10	VDD	VDD
11	PD5	PD5
12	A0	A0
13	A1	A1
14	A2	A2
15	A3	A3
16	A4	A4
17	A5	A5
18	A6	A6
19	$\overline{G}$	$\overline{G}$
20	DQ8	DQ8
21	DQ9	DQ9
22	DQ10	DQ10
23	DQ11	DQ11
24	DQ12	DQ12
25	DQ13	DQ13
26	DQ14	DQ14
27	DQ15	DQ15
28	A7	A7
29	DQ16	DQ16
30	VDD	VDD
31	A8	A8
32	A9	A9
33	NC	NC, A12
34	NC	NC, A13
35	DQ17	DQ17
36	DQ18	DQ18

	5 V ECC	3.3 V ECC
PIN #	PIN NAME	PIN NAME
37	DQ19	DQ19
38	DQ20	DQ20
39	VSS	VSS
40	$\overline{CE0}$	$\overline{CE0}$
41	NC, A10	A10
42	NC, A11	A11
43	NC, $\overline{CE1}$	$\overline{CE1}$
44	$\overline{RE0}$	$\overline{RE0}$
45	NC, $\overline{RE1}$	$\overline{RE1}$
46	DQ21	DQ21
47	$\overline{W}$	$\overline{W}$
48	$\overline{ECC}$	$\overline{ECC}$
49	DQ22	DQ22
50	DQ23	DQ23
51	DQ24	DQ24
52	DQ25	DQ25
53	DQ26	DQ26
54	DQ27	DQ27
55	DQ28	DQ28
56	DQ29	DQ29
57	DQ30	DQ30
58	DQ31	DQ31
59	VDD	VDD
60	DQ32	DQ32
61	DQ33	DQ33
62	DQ34	DQ34
63	DQ35	DQ35
64	DQ36,NC	NC
65	DQ37,NC	NC
66	DQ38,NC	$\overline{EDO}$
67	PD1	PD1
68	PD2	PD2
69	PD3	PD3
70	PD4	PD4
71	DQ39,NC	PD(REF)
72	VSS	VSS

PRESENCE DETECT TRUTH TABLE

TYPE	tRAC	$\overline{ECC}$	PD1	PD2	PD3	PD4	#PD5
256K X 36 or 40	100 nS	S	S	O	S	S	O
16M X 36/39	80 nS	S	S	O	O	S	O
	70 nS	S	S	O	S	O	O
	60 nS	S	S	O	O	O	O
512K X 36 or 40	100 nS	S	O	S	S	S	O
32M X 36/39	80 nS	S	O	S	O	S	O
	70 nS	S	O	S	S	O	O
	60 nS	S	O	S	O	O	O
1M X 36 or 40	100 nS	S	S	S	S	S	O
64M X 36/39	80 nS	S	S	S	O	S	O
	70 nS	S	S	S	S	O	O
	60 nS	S	S	S	O	O	O
2M X 36 or 40	100 nS	S	O	O	S	S	O
128M X 36/39	80 nS	S	O	O	O	S	O
	70 nS	S	O	O	S	O	O
	60 nS	S	O	O	O	O	O
4M X 36 or 40	80 nS	S	S	O	O	S	S
256M X 36/39	70 nS	S	S	O	S	O	S
	60 nS	S	S	O	O	O	S
	50 nS	S	S	O	S	S	S
8M X 36 or 40	80 nS	S	O	S	O	S	S
512M X 36/39	70 nS	S	O	S	S	O	S
	60 nS	S	O	S	O	O	S
	50 nS	S	O	S	S	S	S

O = NC CONNECTION) S = CONNECTED TO VSS
$\overline{EDO}$ Pin: VSS FOR EDO, NC for Fast Page.
$\overline{ECC}$ Pin: VSS for ECC Module, OPEN for NON ECC Module
The connection of PD5 to VSS must be made through a 2..6 KΩ resistor

CONFIGURATION PIN ASSIGNMENT TABLE

	MODULE SIZE, 36 or 39/40 BITS											
PIN #	256K	512K	1M	2M	4M	8M	16M	32M	64M	128M	256M	512M
19	NC	NC	NC	NC	A10	A10	A10	A10	A10	A10	A10	A10
*29	NC	NC	NC	NC	A11	A11	A11	A11	A11	A11	A11	A11
32	NC	NC	A9	A9	A9	A9	A9	A9	A9	A9	A9	A9
*33	NC	$\overline{RE3}$	NC	$\overline{RE3}$	NC	$\overline{RE3}$	A12	A12	A12	A12	A12	A12
*34	NC	$\overline{RE2}$	NC	$\overline{RE2}$	NC	$\overline{RE2}$	NC	NC	A13	A13	A13	A13
45	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	RE1

*A11, A12, or A13 on Pins 29, 33, or 34 are used on modules containing devices that require asymetric ROW/ COLUMN addresses.

NOTE – This family of pinouts is approved for use in SIMM modules which are nominally 4.25" long and with a height which varies depencing on the configuration and the memory devices used. See JEDEC Publication 95.

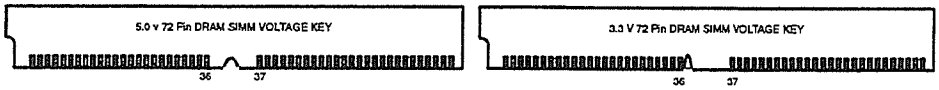
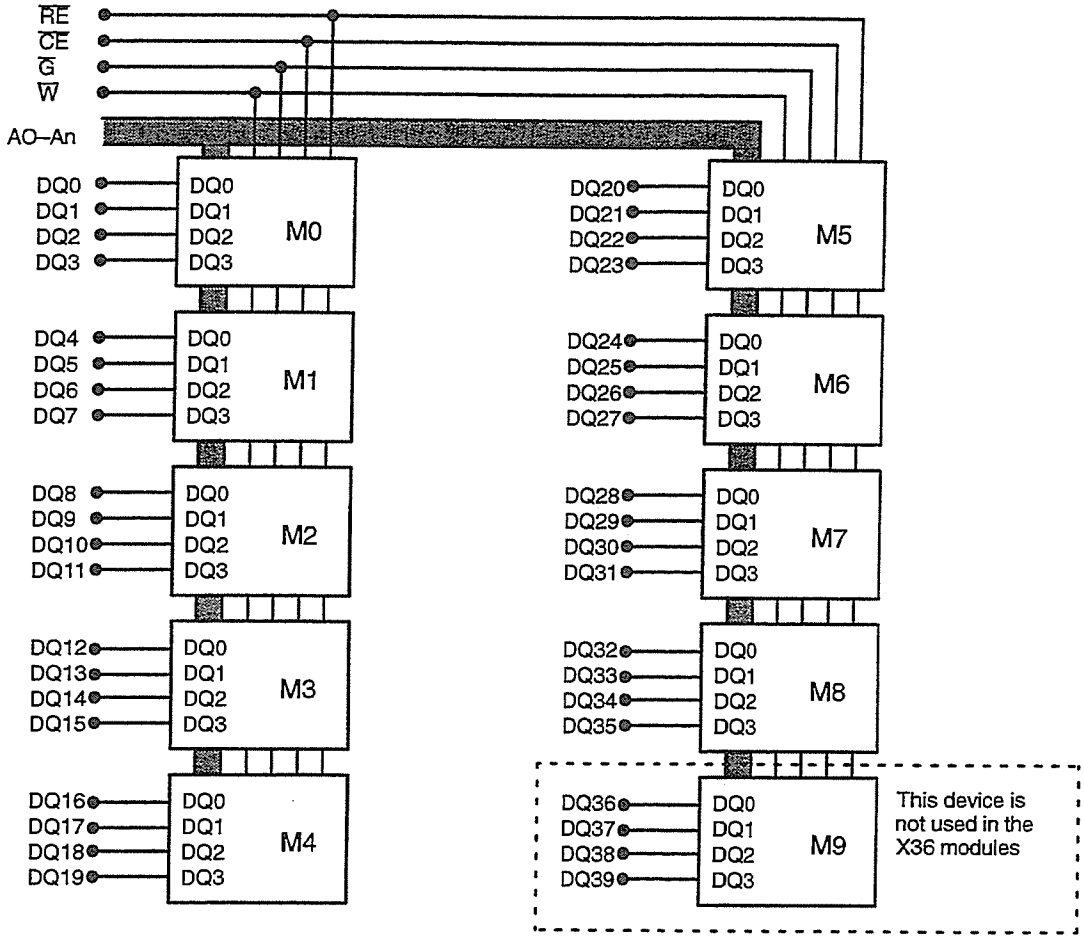


FIGURE 4.4.2–3 A
256K TO 8M BY 36 or 40, 72 PIN ECC DRAM MODULE PINOUT



BLOCK DIAGRAM for 256K/1M/4M X 36 or 40 USING X4 DRAM

FIGURE 4.4.2–3 B
36/40 BIT 72 PIN ECC DRAM SIMM, 1 Bank with X4 DRAMs

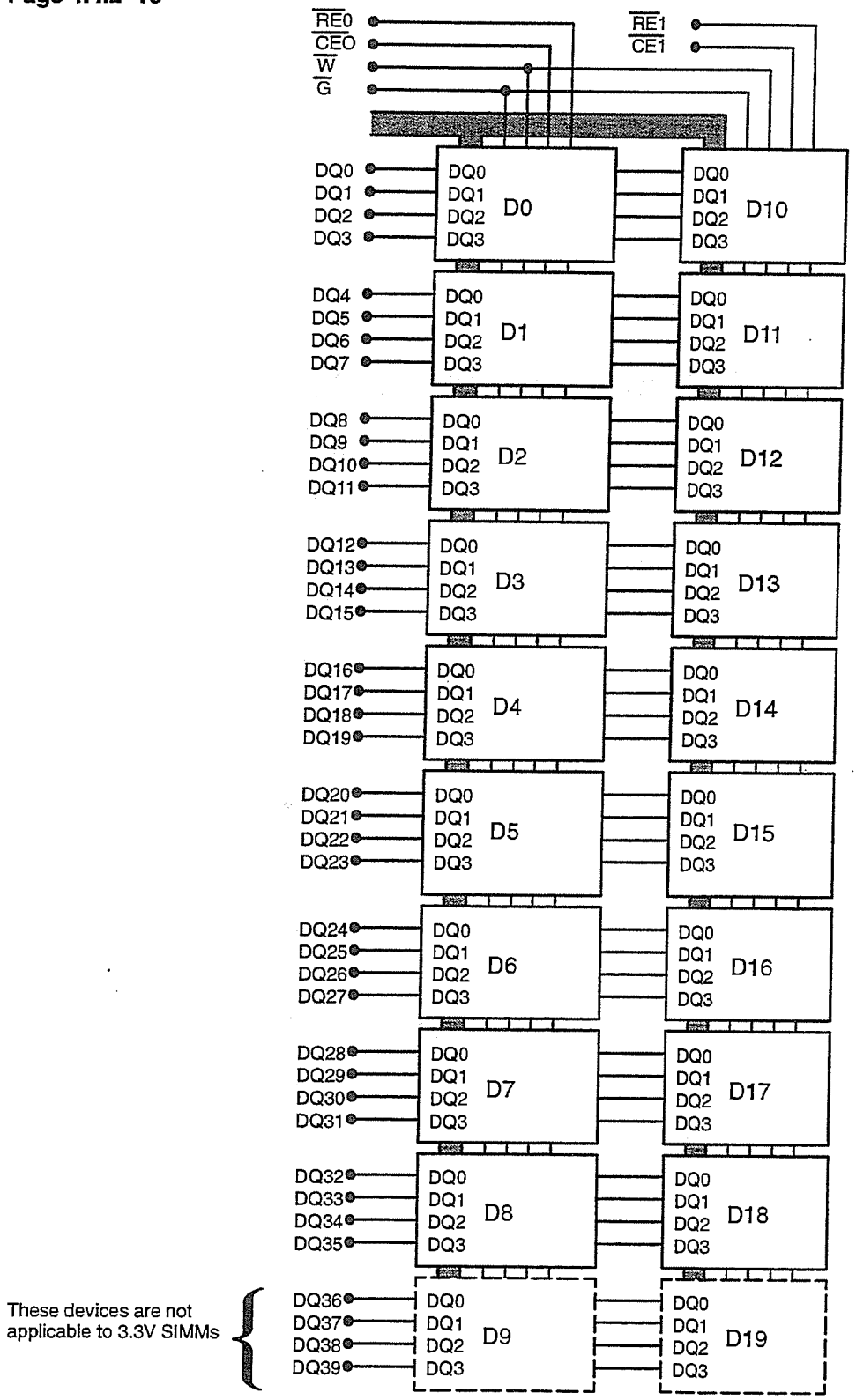
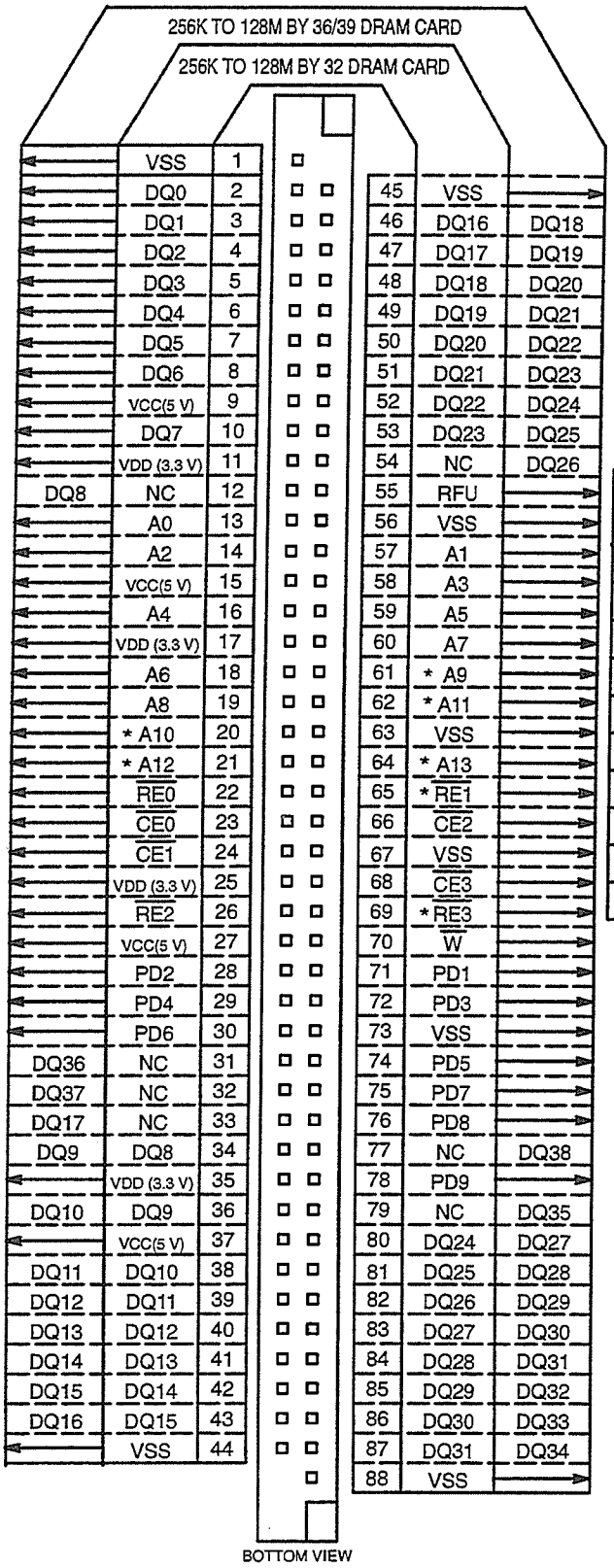


FIGURE 4.4.2–3 C
36/40 BIT 72 PIN ECC DRAM SIMM, 2 Banks with X4 DRAMs

4.4.3 – 88 PIN DRAM CARD FAMILIES

NOTE: There are two versions of this Card, shown in Figure 4.4.3–1 describing X 32 & 36/39 configurations, & 4.4.3–2 describing a X 40 configuration. They are similar but not fully compatible. Caution should be exercised in using these standards.

CAPACITY—256K TO 128M WORDS OF 32, 36, 39 OR 40 BITS
CONFIGURATION—16 Different Configurations Using 1mb, 4mb, 16mb, 64mb, & 256mb Devices And With 2, Or 4 $\overline{Re}$ Clocks.
LOGIC FEATURES—The cards may be used with DATA BUS widths of X16/18 or X32/36 or X39— The cards contain a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.
PIN ASSIGNMENTS, 32, 36, & 39 bit—Fig. 4.4.3–1 A
PRESENCE DETECT TABLE 32, 36, & 39 bit—Fig. 4.4.3–1 B
CONFIGURATION BLOCK DIAGRAMS 32, 36, & 39 bit—Figs. 4.4.3–1 C, 4.4.3–1 D, 4.4.3–1 E, & 4.4.3–1 F
PIN ASSIGNMENTS, 40 bit—Fig. 4.4.3–2 A
PRESENCE DETECT TABLE 40 bit—Fig. 4.4.3–2 B
CONFIGURATION BLOCK DIAGRAMS 40 bit—Figs. 4.4.3–2 C, 4.4.3–2 D, 4.4.3–2 E, & 4.4.3–2 F
PACKAGE—88 PIN JEDEC MEMORY CARD



	PD7	PD6
SPEED (tRAC)	75	30
100 nS	VSS	VSS
80 nS	VSS	NC
70 nS	NC	VSS
60 nS	NC	NC
50 nS	VSS	VSS

PD SPEED TABLE

	PIN NUMBER						
CONFIGURATION	20	21	61	62	64	65	69
256K X 36, 2 $\overline{RE}$	NC	NC	NC	NC	NC	NC	NC
512K X 36, 4 $\overline{RE}$	NC	NC	NC	NC	NC	RE1	RE3
1M X 36, 2 $\overline{RE}$	NC	NC	A9	NC	NC	NC	NC
2M X 36, 4 $\overline{RE}$	NC	NC	A9	NC	NC	RE1	RE3
4M X 36, 2 $\overline{RE}$	A10	NC	A9	A11	NC	NC	NC
8M X 36, 4 $\overline{RE}$	A10	NC	A9	A11	NC	RE1	RE3
16M X 36, 2 $\overline{RE}$	A10	A12	A9	A11	NC	NC	NC
32M X 36, 4 $\overline{RE}$	A10	A12	A9	A11	NC	RE1	RE3
64M X 36, 2 $\overline{RE}$	A10	A12	A9	A11	A13	NC	NC
128M X 36, 4 $\overline{RE}$	A10	A12	A9	A11	A13	RE1	RE3

ADDRESS AND CLOCK PIN ASSIGNMENTS

Data Access Mode	PD9
FAST PAGE	NC
EDO	VSS

* SEE TABLE FOR FUNCTION ASSIGNMENTS FOR THESE PINS AS A FUNCTION OF CARD CAPACITY AND CONFIGURATION

FIGURE 4.4.3–1 A
88 PIN, BY 32 and 36/39 DRAM CARD PINOUT

PD BITS 5 4 3 2 1	CARD DENSITY	DRAM ORGANIZATION	CARD ADDR. REQ'D	RE ADDR.	CE ADDR.	AVAIL. PAGE DEPTH	AVERAGE REFRESH INTERVAL	NOTES
1 1 1 1 1	NO CARD							NO CARD INSTALLED
1 0 0 0 0	1 MB	256K X 1, 4, 16, 18	18	9	9	512	125 mS	
0 0 0 0 0	2 MB	256K X 1, 4, 16, 18	18	9	9	512	125 mS	
1 0 0 0 1	2 MB	512K X 8, 9	19	10	9	512	125 mS	
0 0 0 0 1	4 MB	512K X 8, 9	19	10	9	512	125 mS	
1 0 0 1 0	4 MB	1M X 1, 4, 16, 18	20	10	10	1024	125 mS	
0 0 0 1 0	8 MB	1M X 1, 4, 16, 18	20	10	10	1024	125 mS	
1 1 0 1 0	4 MB	1M X 16, 18	20	12	8	256	62 mS	
0 1 0 1 0	8 MB	1M X 16, 18	20	12	8	256	62 mS	
1 0 0 1 1	8 MB	2M X 8, 9	21	11	10	1024	125 mS	
0 0 0 1 1	16 MB	2M X 8, 9	21	11	10	1024	125 mS	
1 0 1 0 0	16 MB	4M X 1, 4, 16, 18	22	12	*11	**1024	62 mS	SUPPORT 12/10 AND 11/11 ADDRESS
0 0 1 0 0	32 MB	4M X 1, 4, 16, 18	22	12	*11	**1024	62 mS	SUPPORT 12/10 AND 11/11 ADDRESS
1 0 1 0 1	32 MB	8M X 8, 9	23	13	*11	**1024	62 mS	SUPPORT 13/10 AND 12/11 ADDRESS
0 0 1 0 1	64 MB	8M X 8, 9	23	13	*11	**1024	62 mS	SUPPORT 13/10 AND 12/11 ADDRESS
1 0 1 1 0	64 MB	16M X 1, 4, 16, 18	24	14	*11	**1024	31 mS	SUPPORT 13/11 AND 14/10 ADDRESS
0 0 1 1 0	128MB	16M X 1, 4, 16, 18	24	14	*11	**1024	31 mS	SUPPORT 13/11 AND 14/10 ADDRESS

* INDICATES REDUNDANT ADDRESS THAT MUST BE PROVIDED AT CE\ TIME (TO ALLOW USE OF MIXED DRAM ADDRESSING)
** PAGE DEPTH DETERMINED BY THE SMALLEST CE\ ADDRESS DRAM
*** ALL DENSITIES ASSUME 4 BYTE CARD DATA WIDTH (32 OR 36 BITS)
FOR THE PDn PINS, 1 = NC, 0 = VSS

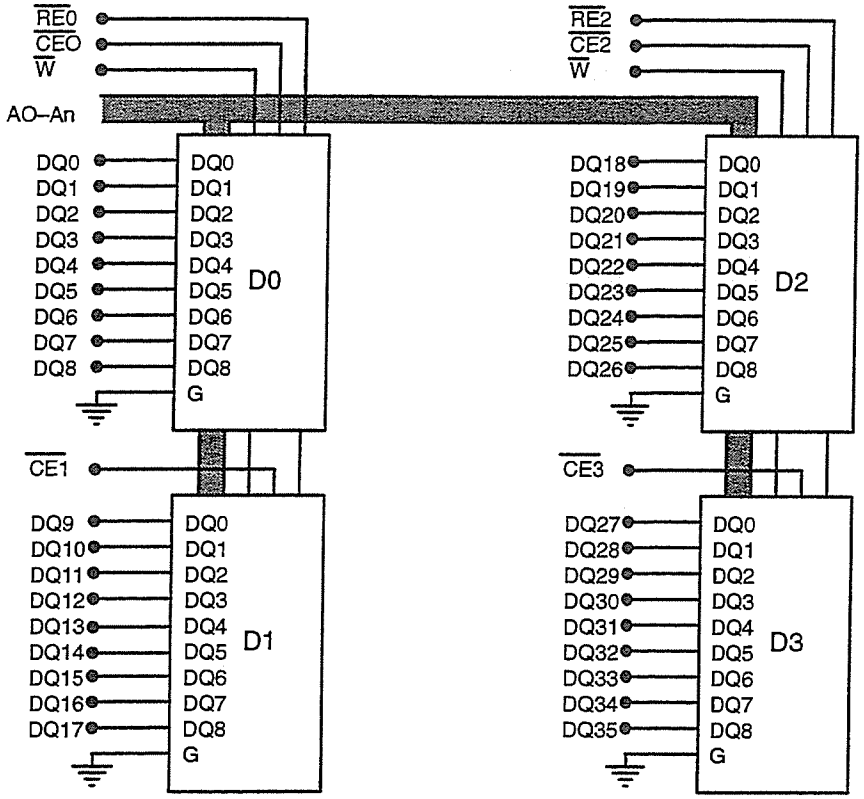
MEMORY CARD ORGANIZATION AND ADDRESS STRUCTURE

BASE DEVICE	CONFIG'N	PIN NUMBER 9	11	15	17	25	27	35	37
1M	256K X 36, 2 $\overline{RE}$	5 V	NC	5 V	NC	NC	5 V	NC	5 V
1M	512K X 36, 4 $\overline{RE}$	5 V	NC	5 V	NC	NC	5 V	NC	5 V
4M	1M X 36, 2 $\overline{RE}$	5 V,NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
4M	2M X 36, 4 $\overline{RE}$	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
16M	4M X 36, 2 $\overline{RE}$	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
16M	8M X 36, 4 $\overline{RE}$	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
64M	16M X 36, 2 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
64M	32M X 36, 4 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
256M	64M X 36, 2 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
256M	128M X 36, 4 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC

VDD POWER PIN ASSIGNMENT TABLE

FIGURE 4.4.3–1 B
88 PIN, BY 32 AND 36/39 DRAM CARD CONFIGURATION TABLES

BLOCK DIAGRAM for 512K /2M/8M/32M X 36 or 1M/4M/16M/64M X 18 USING X8 or X9 DRAM



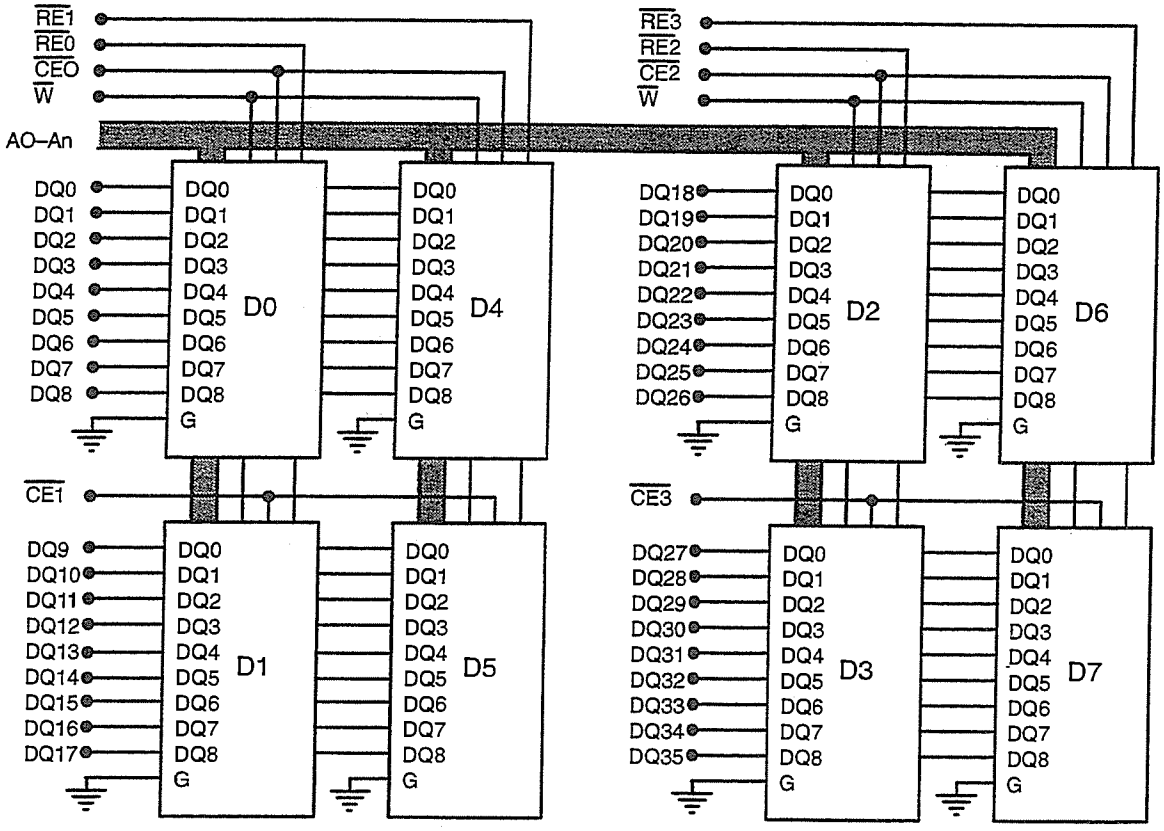
WORD ORGANIZATION	* BASE MEMORY DEVICE	
	D0 – D3	ADDRESS
512K X 36 or 1M X 18	4M (X9)	A0 – A9
2M X 36 or 4M X 18	16M (X9)	A0 – A10
8M X 36 or 16M X 18	64M (X9)	A0 – A12

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

note 1: In an 18 bus system, $\overline{RE0}$ and $\overline{RE2}$ will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card
In a 36 bit system, $\overline{RE0}$ and $\overline{RE2}$ will be actuated simultaneously
note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4.4.3–1 C
88 PIN, BY 36, DRAM CARD 1 BANK USING BY 9 DEVICES

BLOCK DIAGRAM for 1M /4M/16M/64M X 36 or 2M/8M/32M/128M X 18 USING X8 or X9 DRAM



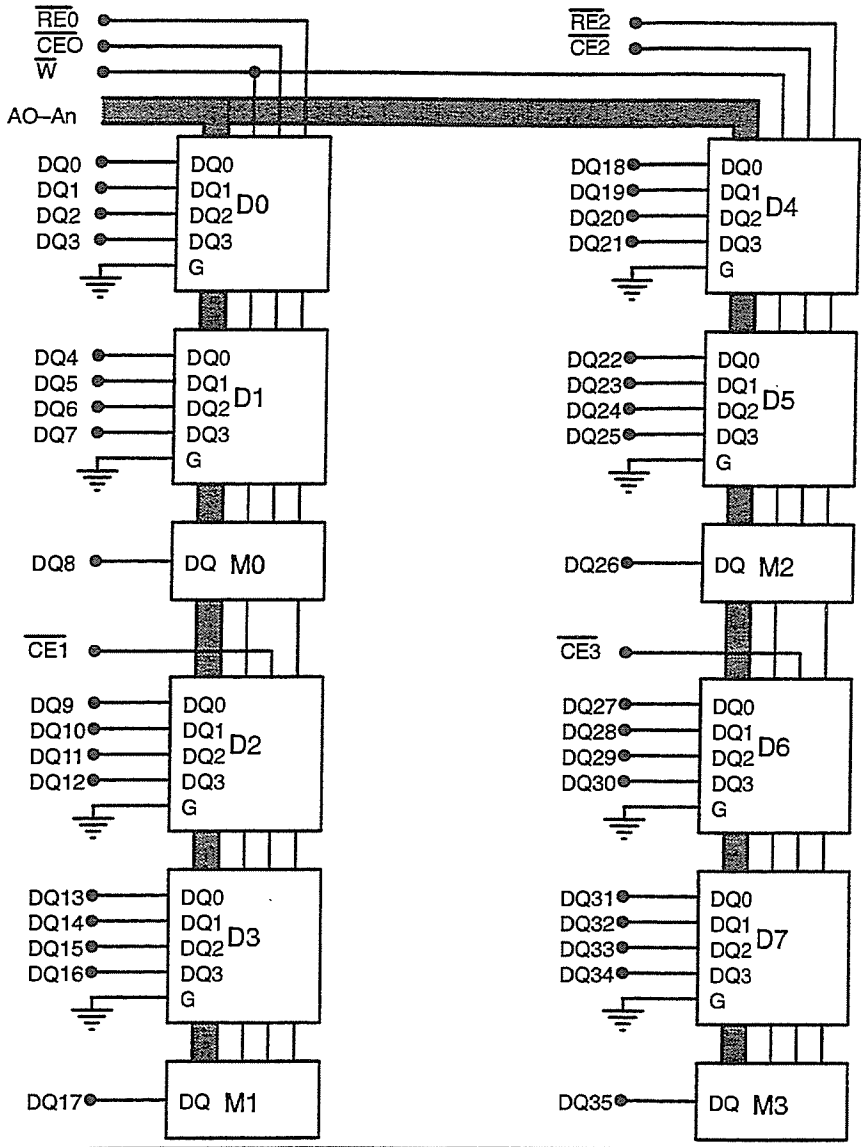
WORD ORGANIZATION	* BASE MEMORY DEVICE	
	D0 – D7	ADDRESS
1M X 36 or 2M X 18	4M (X9)	A0 – A9
4M X 36 or 8M X 18	16M (X9)	A0 – A10
16M X 36 or 32M X 18	64M (X9)	A0 – A12

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

note 1: In an 18 bus system, $\overline{RE0}$ and $\overline{RE2}$ (also $\overline{RE1}$ and $\overline{RE3}$) will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card
In a 36 bit system, $\overline{RE0}$ and $\overline{RE2}$ (also $\overline{RE1}$ and $\overline{RE3}$) will be actuated simultaneously
note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4.4.3–1 D
88 PIN, BY 36, DRAM CARD 2 BANK USING BY 9 DEVICES

BLOCK DIAGRAM for 256K /1M/4M/16M/64M X 36 or 512K/2M/8M/32M/128M X 18 USING X4 and X1 DRAM



WORD ORGANIZATION	* BASE MEMORY DEVICE		
	D0 – D7	M0 – M3	ADDRESS
256K X 36 or 512K X 18	1M (X4)	256K (X1)	A0 – A8
1M X 36 or 2M X 18	4M (X4)	1M (X1)	A0 – A9
4M X 36 or 8M X 18	16M (X4)	4M (X1)	A0 – A11
16M X 36 or 32M X 18	64M (X4)	16M (X1)	A0 – A13

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

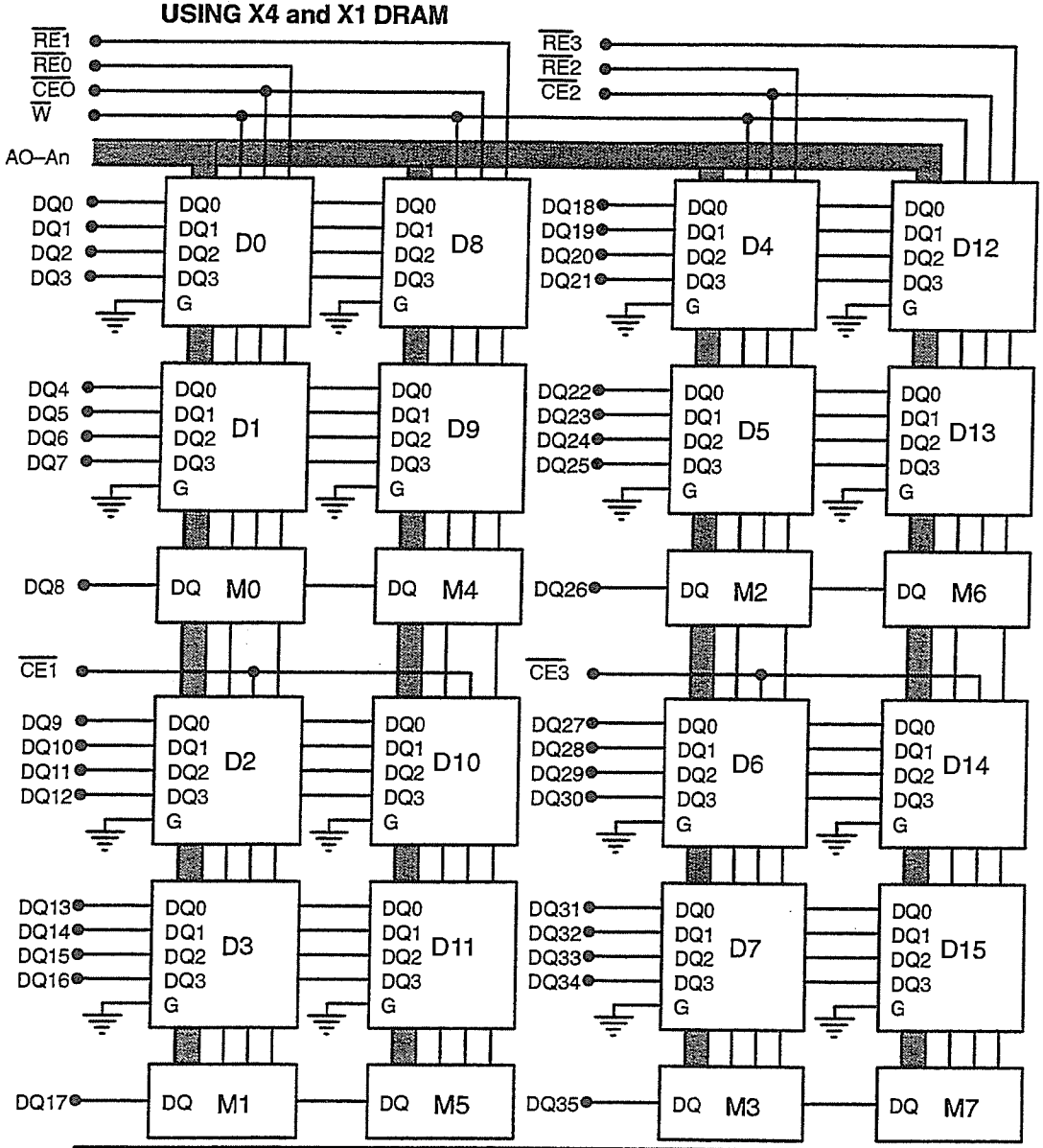
note 1: In an 18 bus system, $\overline{RE0}$ and $\overline{RE2}$ will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card
In a 36 bit system, $\overline{RE0}$ and $\overline{RE2}$ will be actuated simultaneously

note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4.4.3–1 E

88 PIN, 36, DRAM CARD 1 BANK USING BY 4 & BY 1 DEVICES

BLOCK DIAGRAM for 512K/2M/8M/32M/32M/128M X 36 or 1M/4M/16M/256M X 18 USING X4 and X1 DRAM



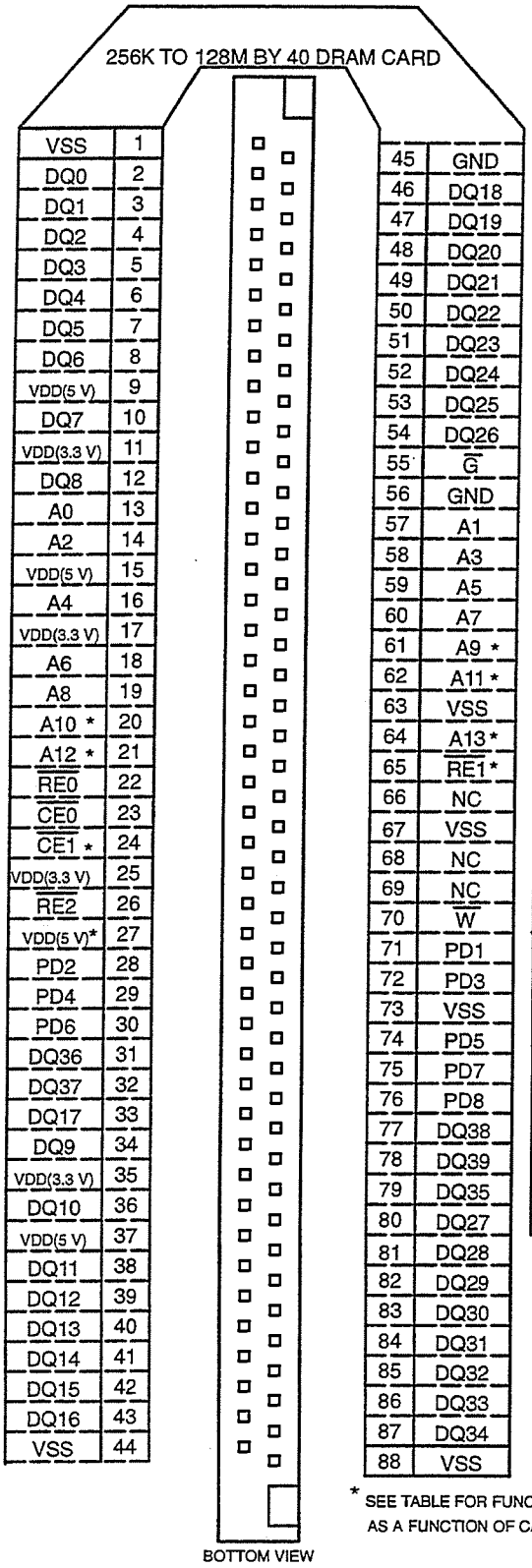
WORD ORGANIZATION	* BASE MEMORY DEVICE		
	D0 – D15	M0 – M7	ADDRESS
512K X 36 or 1M X 18	1M (X4)	256K(X1)	A0 – A8
2M X 36 or 4M X 18	4M (X4)	1M (X1)	A0 – A9
8M X 36 or 16M X 18	16M (X4)	4M (X1)	A0 – A11
32M X 36 or 64M X 18	64M (X4)	16M (X1)	A0 – A13

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

note 1: In an 18 bus system, $\overline{RE0}$ and $\overline{RE2}$ (also $\overline{RE1}$ AND $\overline{RE3}$) will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card,
In a 36 bit system, $\overline{RE0}$ and $\overline{RE2}$ (also $\overline{RE1}$ and $\overline{RE3}$) will be actuated simultaneously
note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4.4.3–1 F

88 PIN, BY 36 DRAM CARD 2 BANK USING BY 4 & BY 1 DEVICES



* SEE TABLE FOR FUNCTIONAL ASSIGNMENTS FOR THESE PINS AS A FUNCTION OF CARD CAPACITY AND CONFIGURATION

Pin Assignment, Cards based on X4 DRAM

	Card Pin Number							
CONFIGURATION	20	21	24	27	61	62	64	65
256K X 40 (1M)	NC	NC	NC	5 V, NC	NC	NC	NC	NC
512K X 40 (1M)	NC	NC	$\overline{CE1}$	5 V, NC	NC	NC	NC	$\overline{RE1}$
1M X 40 (4M)	NC	NC	NC	5 V, NC	A9	NC	NC	NC
2M X 40 (4M)	NC	NC	$\overline{CE1}$	5 V, NC	A9	NC	NC	$\overline{RE1}$
4M X 40 (16M)	A10	NC	NC	5 V, NC	A9	A11	NC	NC
8M X 40 (16M)	A10	NC	$\overline{CE1}$	5 V, NC	A9	A11	NC	$\overline{RE1}$
16M X 40 (64M)	A10	A12	NC	NC	A9	A11	NC	NC
32M X 40 (64M)	A10	A12	$\overline{CE1}$	NC	A9	A11	NC	$\overline{RE1}$
64M X 40 (256M)	A10	A12	NC	NC	A9	A11	A13	NC
128M X 40 (256M)	A10	A12	$\overline{CE1}$	NC	A9	A11	A13	$\overline{RE1}$

Pin Assignment, Cards based on X8 DRAM

	Card Pin Number							
CONFIGURATION	20	21	24	27	61	62	64	65
512K X 40 (4M)	NC	NC	NC	5 V, NC	A9	NC	NC	NC
1M X 40 (4M)	NC	NC	$\overline{CE1}$	5 V, NC	A9	NC	NC	$\overline{RE1}$
2M X 40 (16M)	A10	NC	NC	5 V, NC	A9	A11	NC	NC
4M X 40 (16M)	A10	NC	$\overline{CE1}$	5 V, NC	A9	A11	NC	$\overline{RE1}$
8M X 40 (64M)	A10	A12	NC	NC	A9	A11	NC	NC
16M X 40 (64M)	A10	A12	$\overline{CE1}$	NC	A9	A11	NC	$\overline{RE1}$
32M X 40 (256M)	A10	A12	NC	NC	A9	A11	A13	NC
64M X 40 (256M)	A10	A12	$\overline{CE1}$	NC	A9	A11	A13	$\overline{RE1}$

ADDRESS AND CLOCK PIN ASSIGNMENTS

FIGURE 4.4.3–2 A
88 PIN, BY 40 DRAM CARD

	PD7	PD6
SPEED (tRAC)	P 75	P 30
80 nS	VSS	NC
70 nS	NC	VSS
60 nS	NC	NC
50 nS	VSS	VSS

PD SPEED TABLE

	PD8
REFRESH MODE	P 76
80 nS	VSS
70 nS	NC

PD REFRESH MODE TABLE

PD BITS 5 4 3 2 1	CARD DENSITY	DRAM ORGANIZATION	RE ADDR.	CE ADDR.	REFRESH PERIOD (mS) NORMAL	SLOW
1 1 1 1 1	NO CARD					
1 0 0 0 0	1 MB	256K X 4	9	9	8	64
0 0 0 0 0	2 MB	256K X 4	9	9	8	64
1 0 0 0 1	2 MB	512K X 8	10	9	16	128
0 0 0 0 1	4 MB	512K X 8	10	9	16	128
1 0 0 1 0	4 MB	1M X 4	10	10	16	128
0 0 0 1 0	8 MB	1M X 4	10	10	16	128
1 0 0 1 1	8 MB	2M X 8	11	10	32	256
0 0 0 1 1	16 MB	2M X 8	11	10	32	256
1 0 1 0 0	16 MB	4M X 4	11/12	11/10	64	256
0 0 1 0 0	32 MB	4M X 4	11/12	11/10	64	256
1 0 1 0 1	32 MB	8M X 8	12/13	11/10	TBD	TBD
0 0 1 0 1	64 MB	8M X 8	12/13	11/10	TBD	TBD
1 0 1 1 0	64 MB	16M X 4	13	11	TBD	TBD
0 0 1 1 0	128 MB	16M X 4	13	11	TBD	TBD
1 0 1 0 1	128 MB	32M X 8	TBD	TBD	TBD	TBD
0 0 1 0 1	256 MB	32M X 8	TBD	TBD	TBD	TBD
1 0 1 1 0	256 MB	64M X 4	TBD	TBD	TBD	TBD
0 0 1 1 0	512 MB	64M X 4	TBD	TBD	TBD	TBD

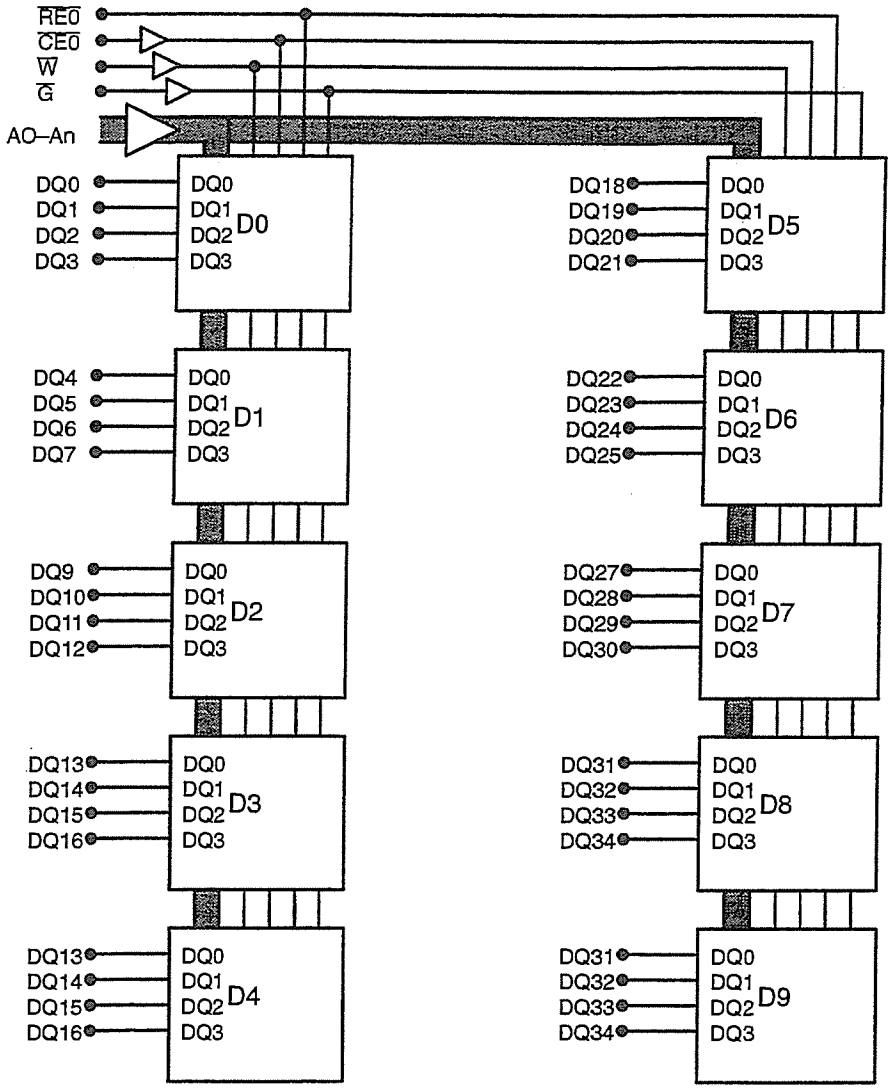
FOR THE PDn PINS, 1 = NC, 0 = VSS
NOTE: In the above address table, optional address configurations are given for some devices to allow for different approved refresh counts.

MEMORY CARD ORGANIZATION AND ADDRESS STRUCTURE

NOTE: The DRAM densities are shown in parentheses (xxxM)

FIGURE 4.4.3–2 B
88 PIN, BY 40 DRAM CARD PD TRUTH TABLE

BLOCK DIAGRAM for 256K/1M/4M/16M/64M X 40 USING X4 DRAM



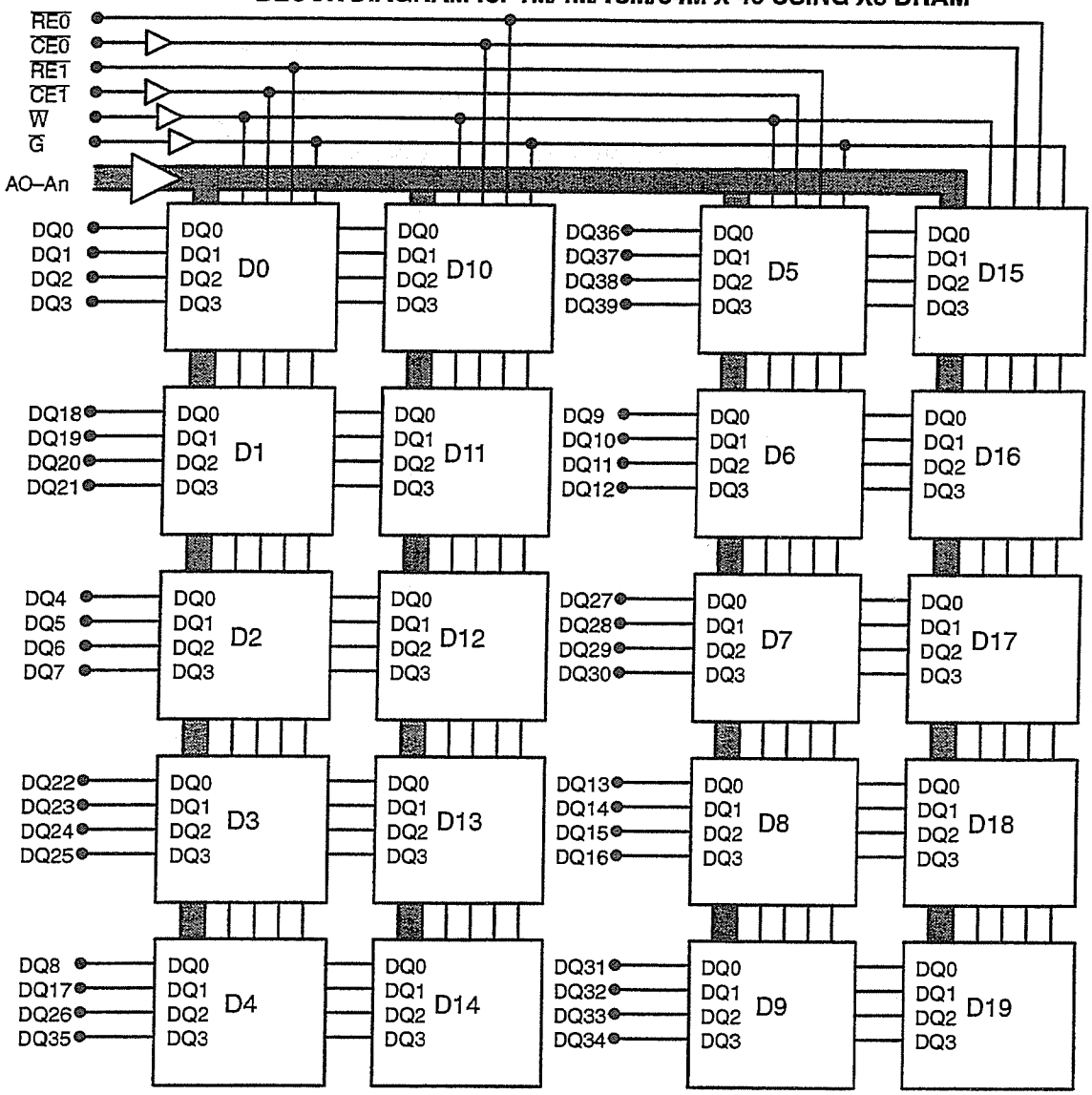
WORD ORGANIZATION	*Base Memory Device D0 to D9	ADDRESS FIELD	OPTIONAL ADDRESS
256K X 40	1M (X4)	A0 – A8	NA
1M X 40	4M (X8)	A0 – A9	NA
4M X 40	16M (X8)	A0 – A10	A0–A11
16M X 40	64M (X8)	A0 – A11	A0–A12
64M X 40	256M (X8)	TBD	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each memory device on the card.

FIGURE 4.4.3–2 C
88 PIN, BY 40 DRAM CARD 1 BANK USING BY 4 DEVICES

BLOCK DIAGRAM for 1M/4M/16M/64M X 40 USING X8 DRAM



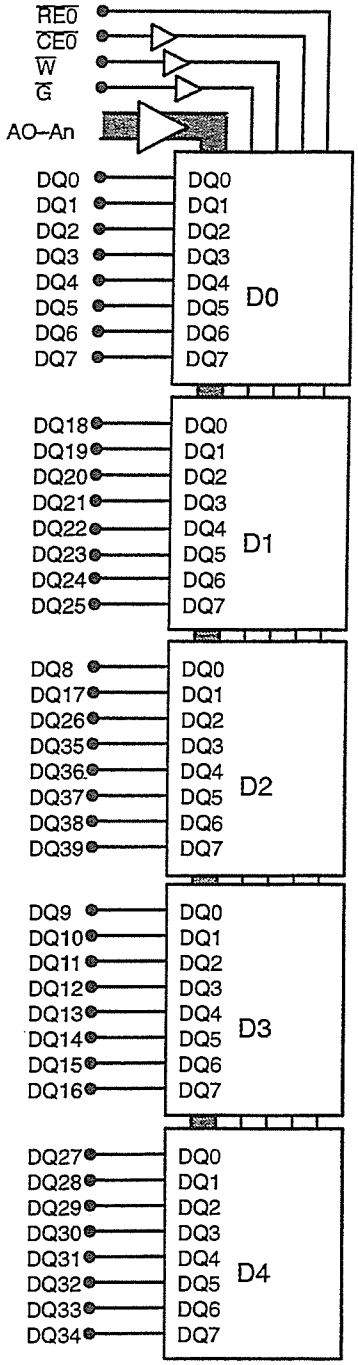
WORD ORGANIZATION	*Base Memory Device D0 to D19	ADDRESS FIELD	OPTIONAL ADDRESS
512K X 40	1M (X4)	A0 – A8	NA
2M X 40	4M (X8)	A0 – A9	NA
8M X 40	16M (X8)	A0 – A10	A0–A11
32M X 40	64M (X8)	A0 – A11	A0–A12
128M X 40	256M (X8)	TBD	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each pair of memory devices on the card. The value of the capacitors will be determined by the memory devices used.

FIGURE 4.4.3–2 D
88 PIN, BY 40 DRAM CARD 2 BANK USING BY 4 DEVICES

BLOCK DIAGRAM for 512K/2M/8M/32M X 40 USING X8 DRAM



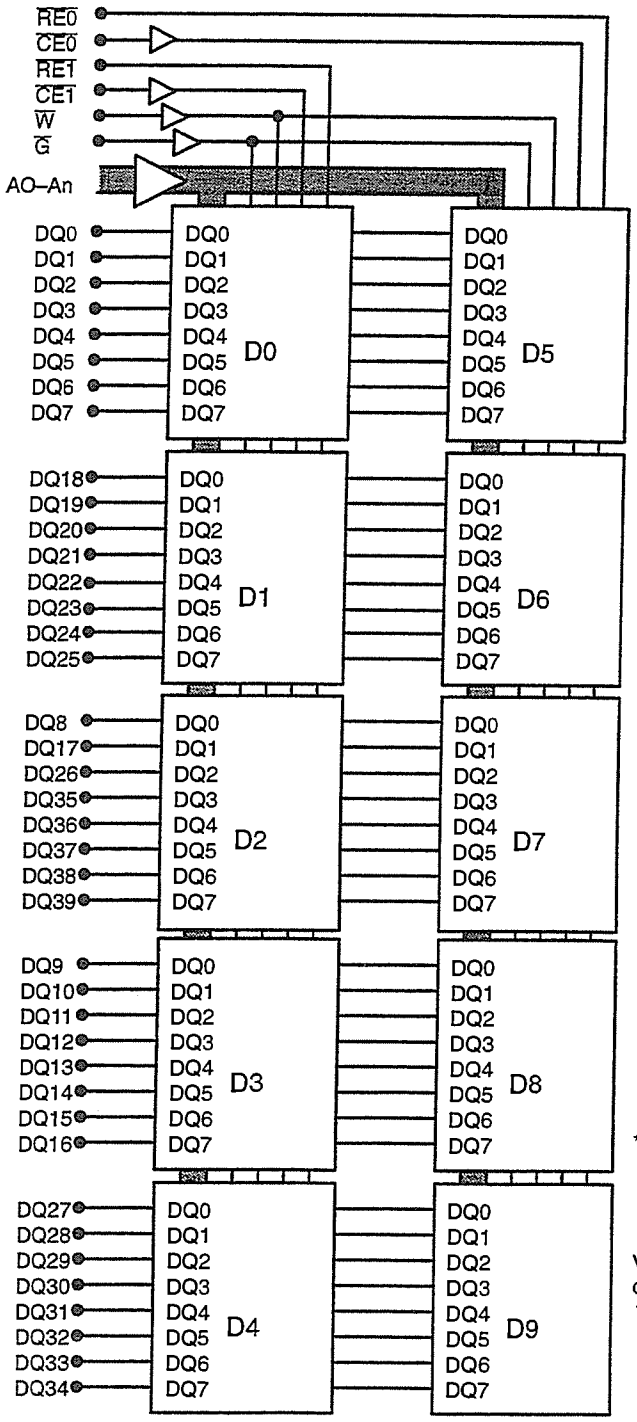
WORD ORGANIZATION	*Base Memory Device D0 to D4	ADDRESS FIELD
512K X 40	4M (X8)	A0 – A9
2M X 40	16M (X8)	A0 – A10
8M X 40	8M (X8)	A0 – A11
32M X 40	32M (X8)	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each memory device on the card. The value of the capacitors will be determined by the memory devices used.

FIGURE 4.4.3–2 E
88 PIN, BY 40 DRAM CARD 1 BANK USING BY 8 DEVICES

BLOCK DIAGRAM for 1M/4M/16M/64M X 40 USING X8 DRAM



WORD ORGANIZATION	*Base Memory Device D0 to D9	ADDRESS FIELD
1M X 40	4M (X8)	A0 – A9
4M X 40	16M (X8)	A0 – A10
16M X 40	64M (X8)	A0 – A11
64M X 40	256M (X8)	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each pair of memory devices on the card. The value of the capacitors will be determined by the memory devices used.

FIGURE 4.4.3–2 F
88 PIN, BY 40 DRAM CARD 2 BANK USING BY 8 DEVICES

4.4.4 – 72 PIN DRAM SO–DIMM FAMILY

CAPACITY—512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 32, OR 36 BITS
DATA CONFIGURATIONS—Two DATA Word configurations are defined:
—32 BIT
—36 BIT
CONFIGURATION—3 Different Configurations are defined using various combinationa of X4, X8, X9 memory devices.
LOGIC FEATURES—The modules contain "PRESENCE DETECT" features that consist of output pins in the PDn field that supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
VDD CHOICE—The choice of VDD value will be determined by the memory device used and defined by a mechanical interlock KEY
ENHANCEMENTS: In Release 6 Refresh was defined and new configurations were added.
PACKAGE—72 PIN JEDEC SO–DIMM MEMORY MODULE
PIN ASSIGNMENTS AND PD TABLES—Figs. 4.4.4–A
CAPACITY / DEVICE CONFIGURATION TABLE—Fig. 4.4.4–A
CONFIGURATION BLOCK DIAGRAM—Figs. 4.4.4–B through 4.4.4–D

PIN NAME	PIN #	PIN #	PIN NAME
VSS	1	2	DQ0
DQ1	3	4	DQ2
DQ3	5	6	DQ4
DQ5	7	8	DQ6
DQ7	9	10	&VDD
PD1	11	12	A0
A1	13	14	A2
A3	15	16	A4
A5	17	18	A6
A10	19	20	@ DQ8, NC
DQ9	21	22	DQ10
DQ11	23	24	DQ12
DQ13	25	26	DQ14
DQ15	27	28	A7
A11	29	30	&VDD
A8	31	32	A9
$\overline{RE3}$	33	34	$\overline{RE2}$
DQ16	35	36	@ DQ17, NC
DQ18	37	38	DQ19
VSS	39	40	$\overline{CE0}$
$\overline{CE2}$	41	42	$\overline{CE3}$
$\overline{CE1}$	43	44	$\overline{RE0}$
$\overline{RE1}$	45	46	A12
$\overline{W}$	47	48	A13
DQ20	49	50	DQ21
DQ22	51	52	DQ23
DQ24	53	54	DQ25
@ DQ26, NC	55	56	DQ27
DQ28	57	58	DQ29
DQ31	59	60	DQ30
&VDD	61	62	DQ32
DQ33	63	64	DQ34
@ DQ35, NC	65	66	PD2
PD3	67	68	PD4
PD5	69	70	PD6
PD7	71	72	VSS

TOP VIEW

PRESENCE DETECT TRUTH TABLE								Ave Refresh Interval (µs)	
MOD CONFIG	DEVICE	ADDR		PD4	PD3	PD2	PD1		
		ROW	COL	Pin 68	Pin 67	Pin 66	Pin 11	Normal	Long
NO MODULE				O	O	O	O		
512K X 32/36	512K X 8/9	10	9	O	S	S	S	15.6	125
1M X 32/36	512K X 8/9	10	9	S	S	S	S	15.6	125
1M X 32/36	1M X 2/4/16/18	10	10	O	S	S	O	15.6	125
1M X 32/36	1M X 16/18	12	8	O	O	S	O	15.6	31.2
2M X 32/36	1M X 2/4/16/18	10	10	S	S	S	O	15.6	125
2M X 32/36	1M X 16/18	12	8	S	O	S	O	15.6	31.2
2M X 32/36	2M X 8/9	11	10	O	S	O	S	15.6	62.4
4M X 32/36	2M X 8/9	11	10	S	S	O	S	15.6	62.4
4M X 32/36	4M X 2/416/18	12*	10*	O	S	O	O	15.6	31.2
	or	11*	11*						62.4
8M X 32/36	4M X 2/4/16/18	12*	10*	S	S	O	O	15.6	31.2
	or	11*	11*						62.4
8M X 32/36	8M X 8/9	12	11	O	O	S	S	15.6	31.2
16M X 32/36	8M X 8/9	12	11	S	O	S	S	15.6	31.2
16M X 32/36	16M X 2/4/16/18	13	11	O	O	O	S	15.6	TBD
32M X 32/36	16M X 2/4/16/18	13	11	S	O	O	S	15.6	TBD
32M X 32/36	32M X 8/9	TBD	TBD	O	S	S	S	TBD	TBD
64M X 32/36	32M X 8/9	TBD	TBD	S	S	S	S	TBD	TBD
64M X 32/36	64M X 2/4	TBD	TBD	O	S	S	O	TBD	TBD

* Indicates that 12/10 or 11/11 may be used on this assembly. The application must determine the appropriate addressing version or provide redundant (12/11) addressing to allow the use of either.

** The DRAM organization is provided for reference and clarification only. X2 implies X2 DRAM with 2 $\overline{CE}$s. X4 can be either X4 or X4 with 4 CEs. X1 options are allowed if approved dimensions are met.

O = OPEN CIRCUIT (NO CONNECTION)

S = CONNECTED TO VSS

	PD6	PD5
SPEED (tRAC)	Pin 70	Pin 69
80 ns	S	O
70 ns	O	S
60 ns	O	O
50 ns	S	S
PD SPEED TABLE		

	PD7
REFRESH MODE	Pin 71
NORMAL	O
* SELF-REFRESH	S
REFRESH MODE	

*SELF-REFRESH/LONG INTERVA

&Note: This standard allows for the use of different values of VDD depending on the memory device requirements. A mechanical key is used to define the voltage as described in the package registration document, MO–160.

@ These Pins are NC for X32, and DQn for X36 modules

FIGURE 4.4.4–A
32 OR 36 BIT DRAM SO–DIMM PINOUT

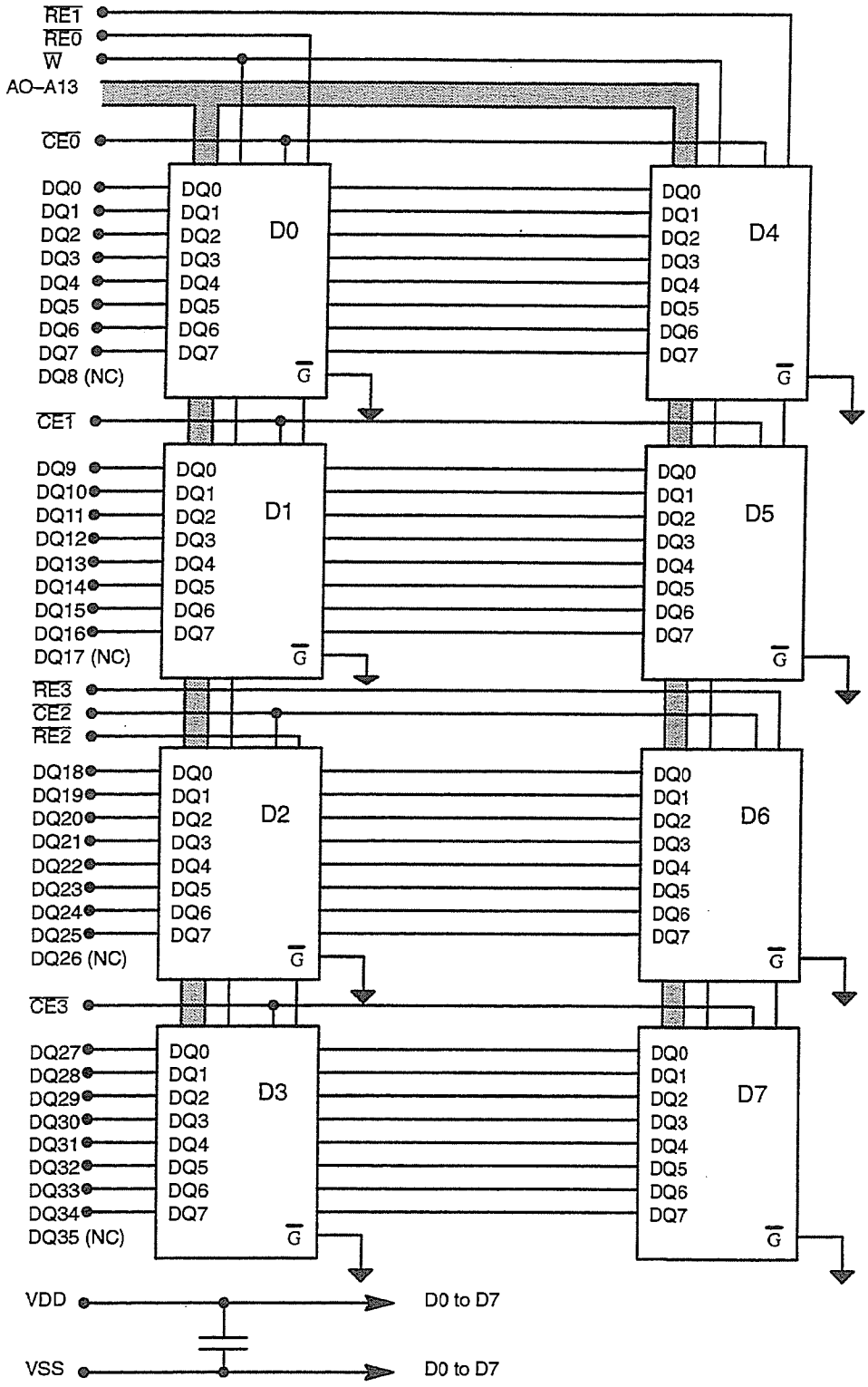


FIGURE 4.4.4–B
BLOCK DIAGRAM for X 32 DRAM SO–DIMM USING X8 DRAM
Release 5c7

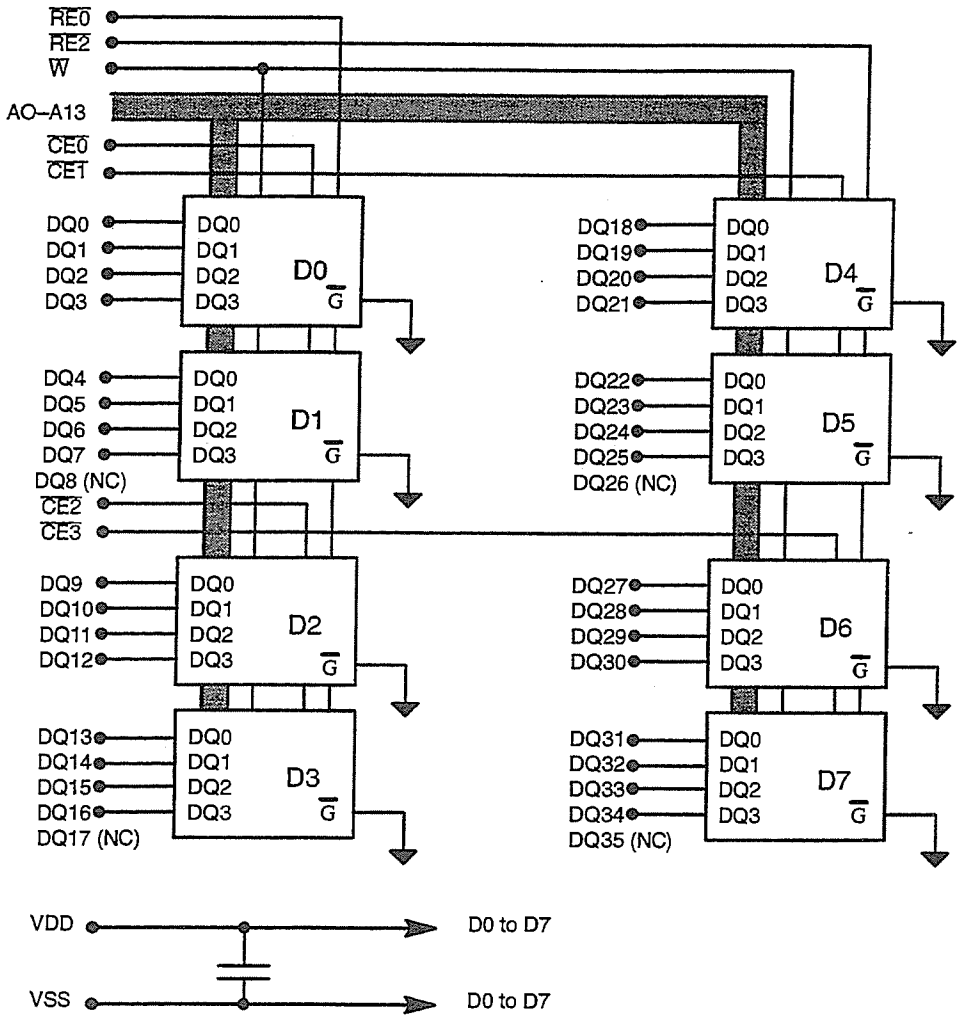


FIGURE 4.4.4–C
BLOCK DIAGRAM for X 32 DRAM SO–DIMM USING X4 DRAM

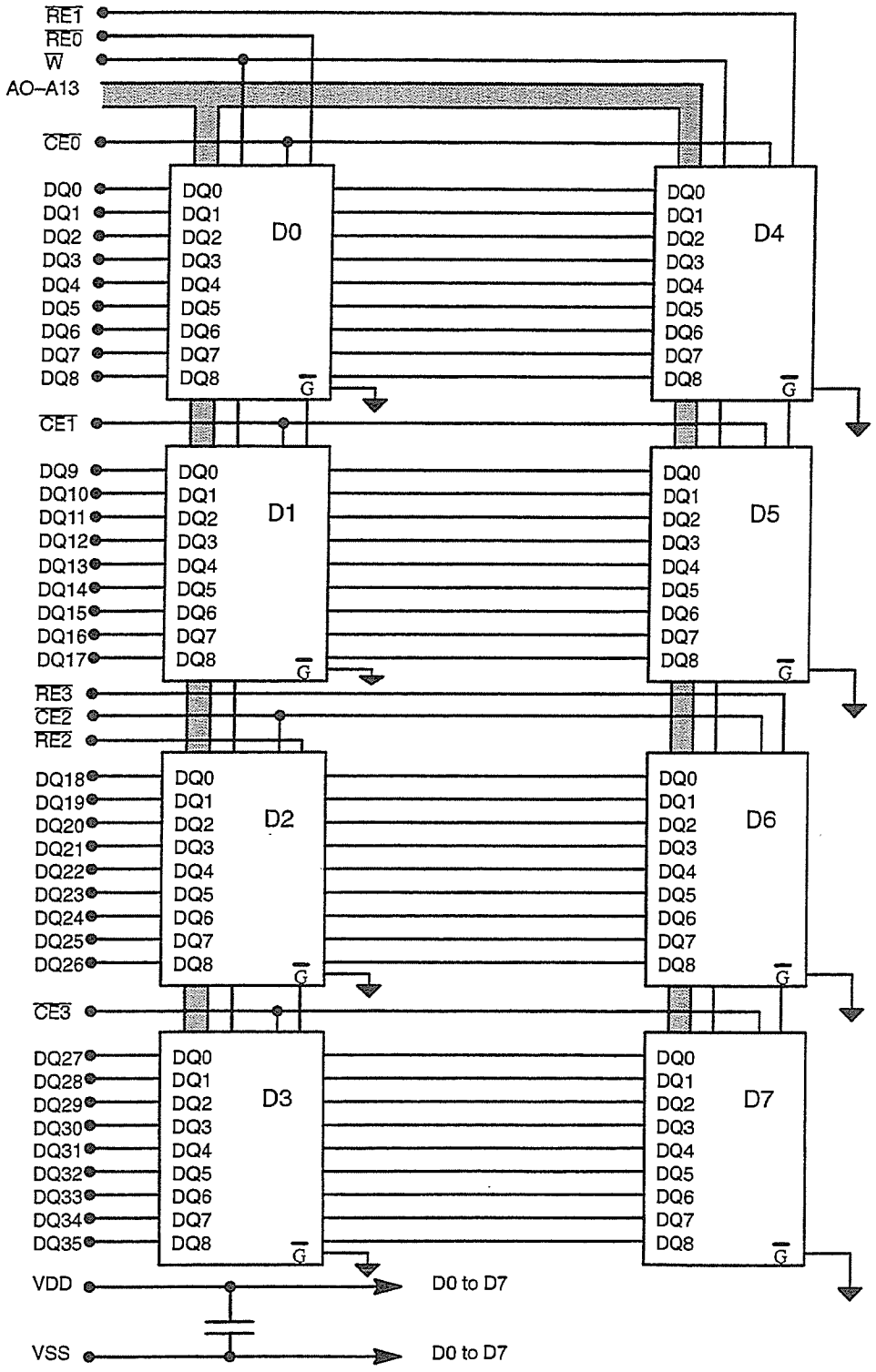


FIGURE 4.4.4–D
BLOCK DIAGRAM for X 36 DRAM SO–DIMM USING X9 DRAM
Release 5c7

4.4.5 – 88 PIN DRAM SO–DIMM FAMILY

CAPACITY—512K TO 128M WORDS OF 32, OR 36 BITS
DATA CONFIGURATIONS—Two DATA Word configurations are defined: X32 & X36
CONFIGURATION—4 Different Configurations are defined using various combinationa of X1, X4, X8, memory devices.
LOGIC FEATURES—The modules contain "PRESENCE DETECT" features that consist of output pins in the PDn field that supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
VDD CHOICE—The choice of VDD value will be determined by the memory device used and defined by a mechanical interlock KEY
PACKAGE—88 PIN JEDEC SO–DIMM MEMORY MODULE
PIN ASSIGNMENTS —Figs. 4.4.5–A
PD, CAPACITY / DEVICE CONFIGURATION TABLES—Fig. 4.4.5–B
CONFIGURATION BLOCK DIAGRAM—Figs. 4.4.5–C through 4.4.5–F

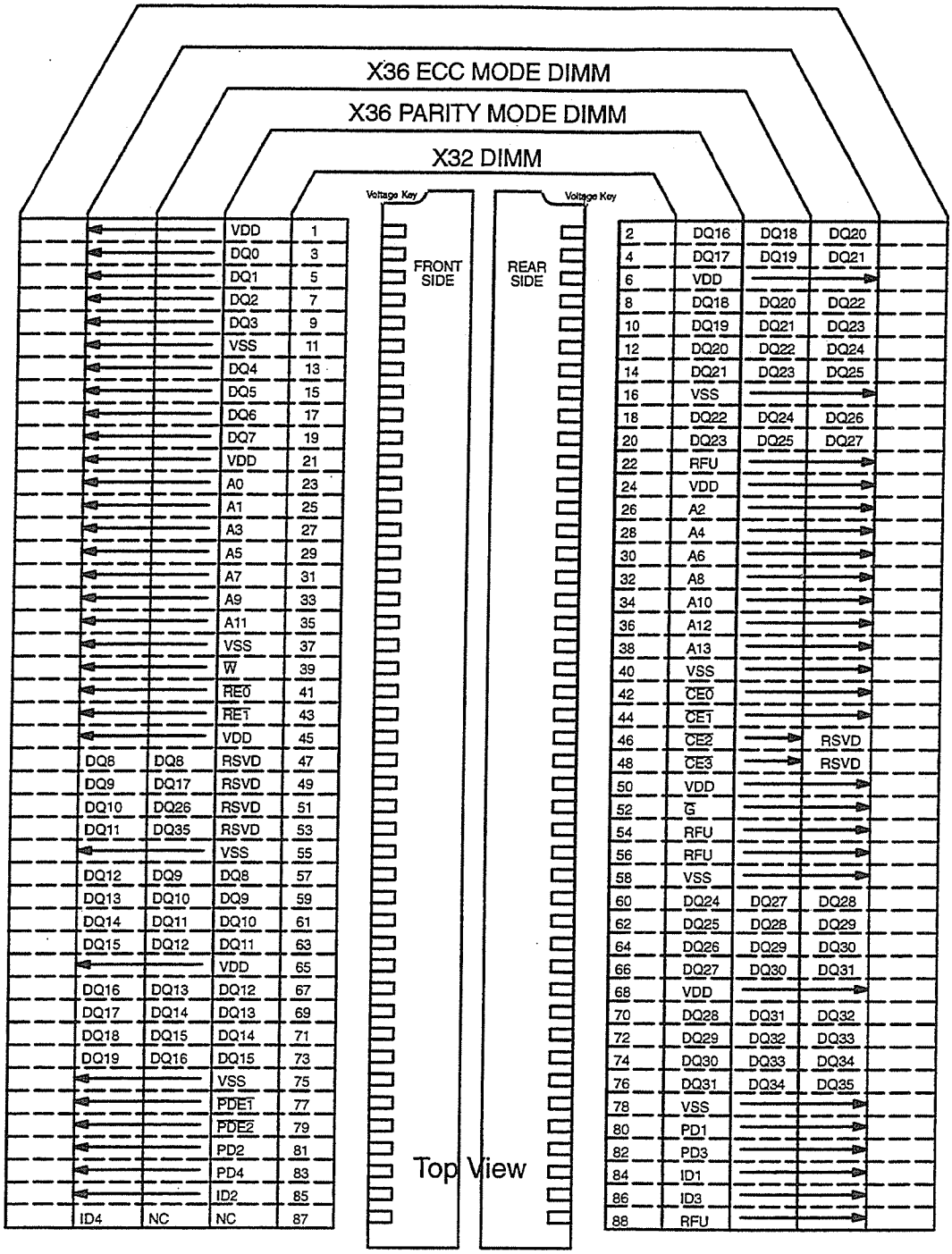


FIGURE 4.4.5–A
X32 and X36 DRAM SO–DIMM PINOUT

Release 6c7

PREOENCE DETECT TRUTH TABLE							
MOD CONFIG	DEVICE	ADDR		PD14	PD13	PD12	PD11
		ROW	COL				
NO MODULE				1	1	1	1
512K X 32/36	512K X 8/9	10	9	1	0	0	0
1M X 32/36	512K X 8/9	10	9	0	0	0	0
1M X 32/36	1M X 1/4/16/18	10	10	1	0	0	1
1M X 32/36	1M X 16/18	12	8	1	0	1	0
2M X 32/36	1M X 1/4/16/18	10	10	0	0	0	1
2M X 32/36	1M X 16/18	12	8	0	0	1	0
2M X 32/26	2M X 1/2/8/9	11	10	1	0	1	1
4M X 32/36	2M X 1/2/8/9	11	10	0	0	1	1
4M X 32/36	4M X 4/16/18	12	10	1	1	0	0
4M X 32/36	4M X 1/4/16/18	11	11	1	1	0	1
8M X 32/36	4M X 4/16/18	12	10	0	1	1	1
8M X 32/36	4M X 1/4/16/18	11	11	0	1	0	1
8M X 32/36	8M X 1/2/8/9	12	11	1	1	1	0
16M X 32/36	8M X 1/2/8/9	12	11	0	1	1	0
16M X 32/36	16M X 1/4/16/18	13/12*	11/12*	1	0	0	0
32M X 32/36	16M X 1/4/16/18	13/12*	11/12*	0	0	0	0
32M X 32/36	32M X 1/2/8/9	TBD	TBD	1	0	0	1
64M X 32/36	32M X 1/2/8/9	TBD	TBD	0	0	0	1
64M X 32/36	64M X 1/4	TBD	TBD	1	0	1	0
128M X 32/36	64M X 1/4	TBD	TBD	0	0	1	0

NOTE 1 – * This addressing includes a redundant address to allow mixing of 13/11 and 12/12 devices.

NOTE 2 – The PDmn & IDn values given in the tables have the following significance: 1 = Driven to LOGIC HIGH for PD, OPEN CIRCUIT FOR ID
0 = Driven to LOGIC LOW for PD, SHORT TO VSS FOR ID

NOTE 3 – #The PDmn values are multiplexed onto the PDn pins under the control of $\overline{PDE1}$ and $\overline{PDE2}$ as follows:
PD11 ⇒ PD14 to PD1 ⇒ PD4 WITH $\overline{PDE1}$ = LOW
PD21 ⇒ PD24 to PD1 ⇒ PD4 WITH $\overline{PDE2}$ = LOW

NOTE4: This standard allows for the use of different values of VDD depending on the memory device requirements. A mechanical key is used to define the voltage as described in the package registration document.

&

	ID3
PARITY	
X32 NO–PAR.	0
X36 PARITY	1
PARITY STRUCTURE	

	ID2
REFRESH MODE	
NORMAL	0
SELF–REFRESH	1
REFRESH MODE	

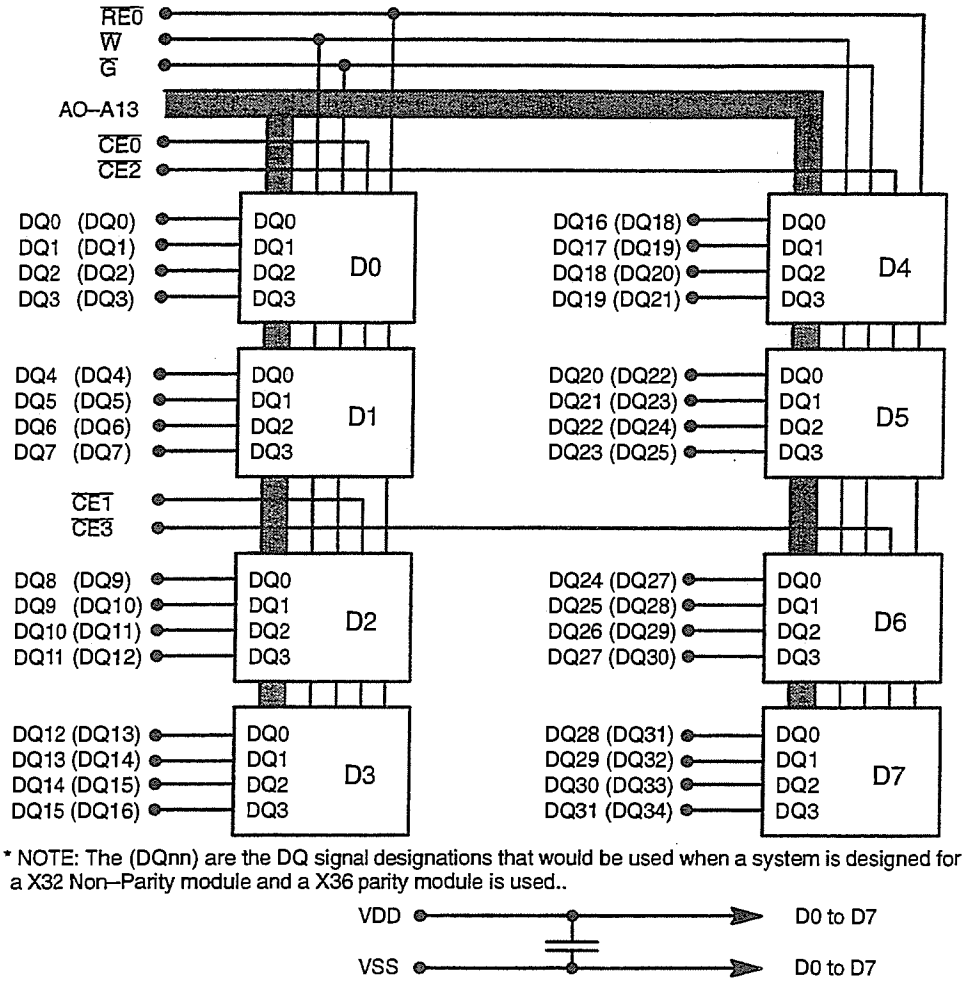
	ID1
REFRESH	
NORMAL	0
SLOW	1
REFRESH PERIOD	

	PD24
ECC	
X32/X36 PARITY	1
X36 ECC	0
DATA STRUCTURE	

	PD23
MODE	
FAST PAGE	1
EDO/BURST EDO	0
DATA I/O MODE	

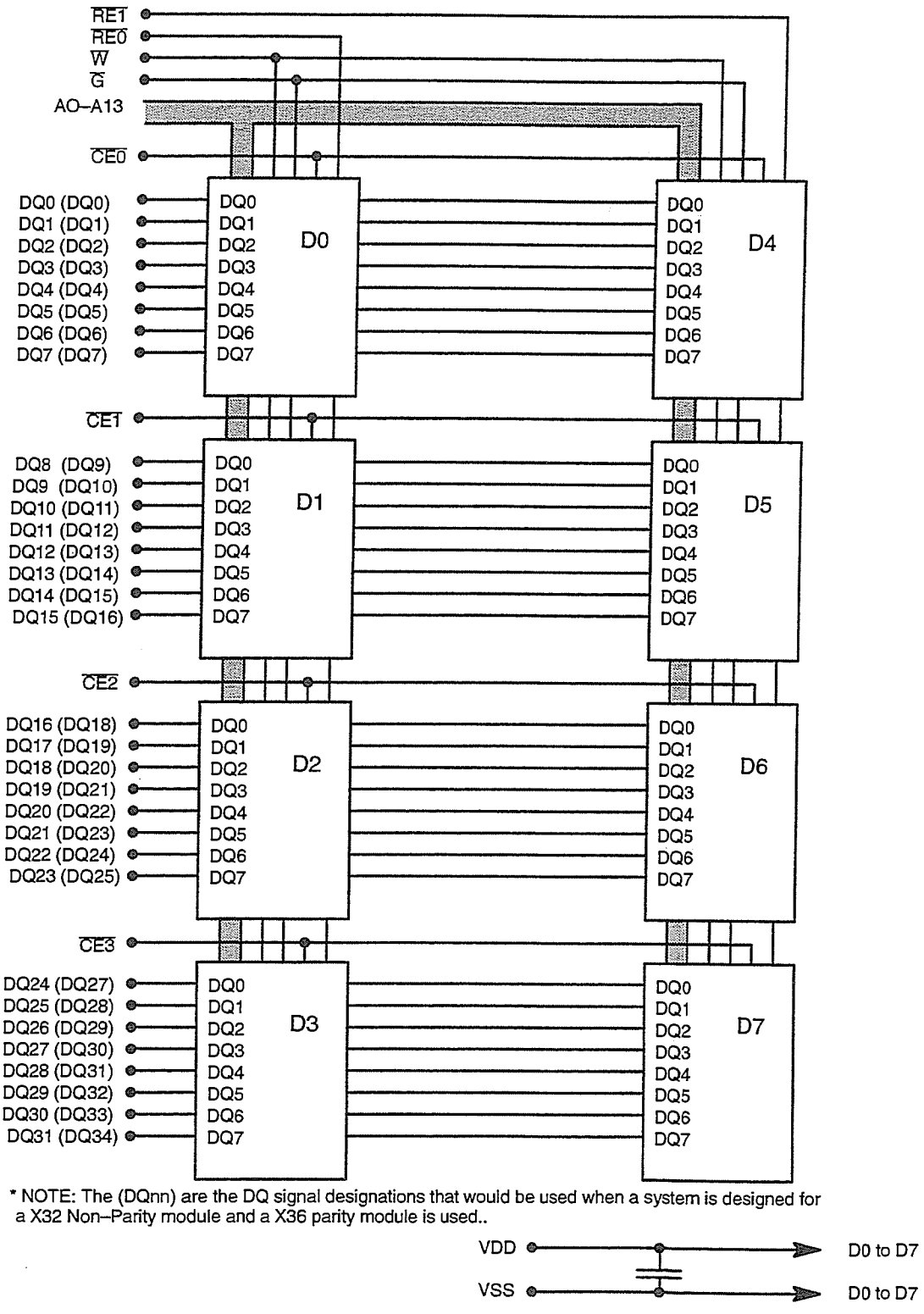
	PD22	PD21
SPEED (tRAC)	81	80
80 ns	0	1
70 ns	1	0
60 ns	1	1
50 ns	0	0
40 ns	0	1
PD SPEED TABLE		

FIGURE 4.4.5–B
X32 and X36 DRAM SO–DIMM PD and ID TRUTH TABLES



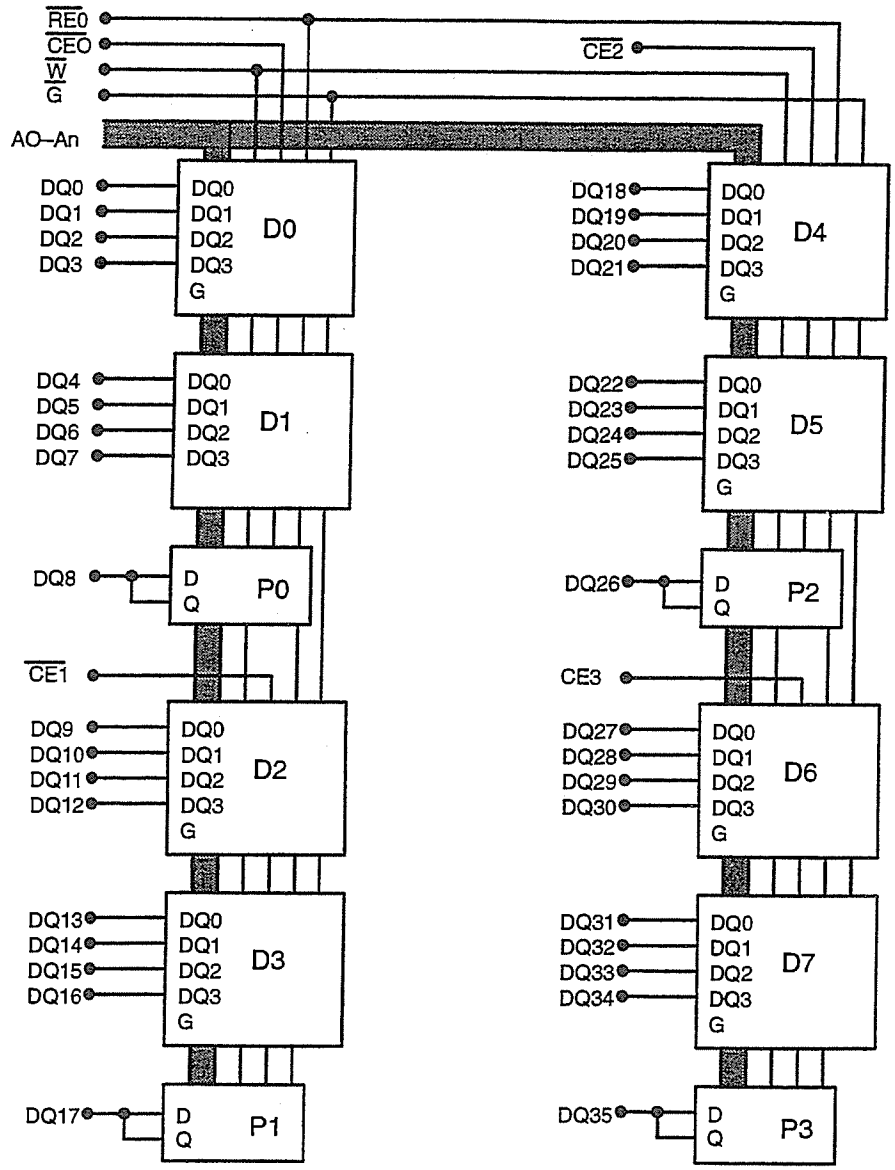
* NOTE: The (DQnn) are the DQ signal designations that would be used when a system is designed for a X32 Non–Parity module and a X36 parity module is used..

FIGURE 4.4.5–C
X 32 DRAM SO–DIMM USING X4 DEVICES



* NOTE: The (DQnn) are the DQ signal designations that would be used when a system is designed for a X32 Non–Parity module and a X36 parity module is used..

FIGURE 4.4.5–D
X 32 DRAM SO–DIMM USING X8 DEVICES



* NOTE: For the parity bit devices, P0 ⇒ P3, X1 DRAMs are showed, but Multi $\overline{CE}$ DRAM may be used.

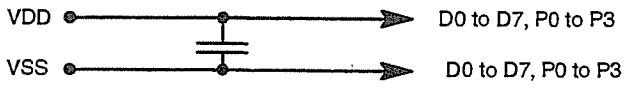


FIGURE 4.4.5–E
X 36 DRAM PARITY SO–DIMM USING X4/X1 DEVICES

Release 6–7

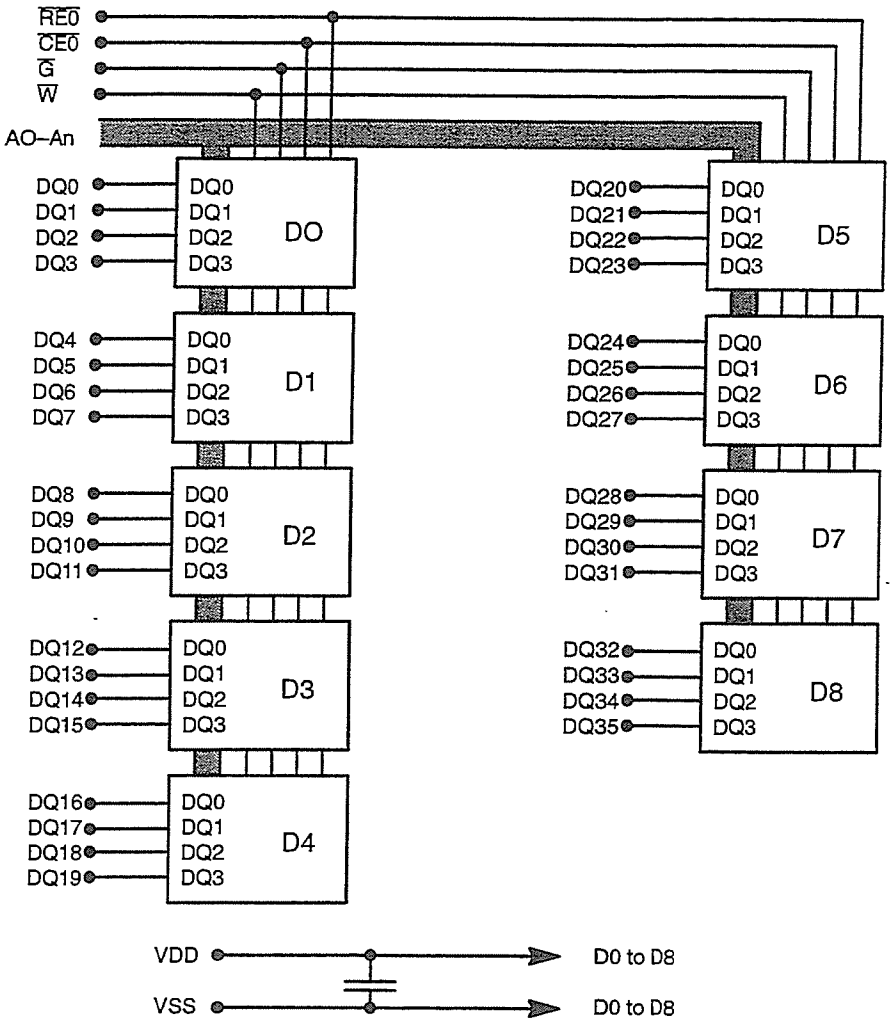
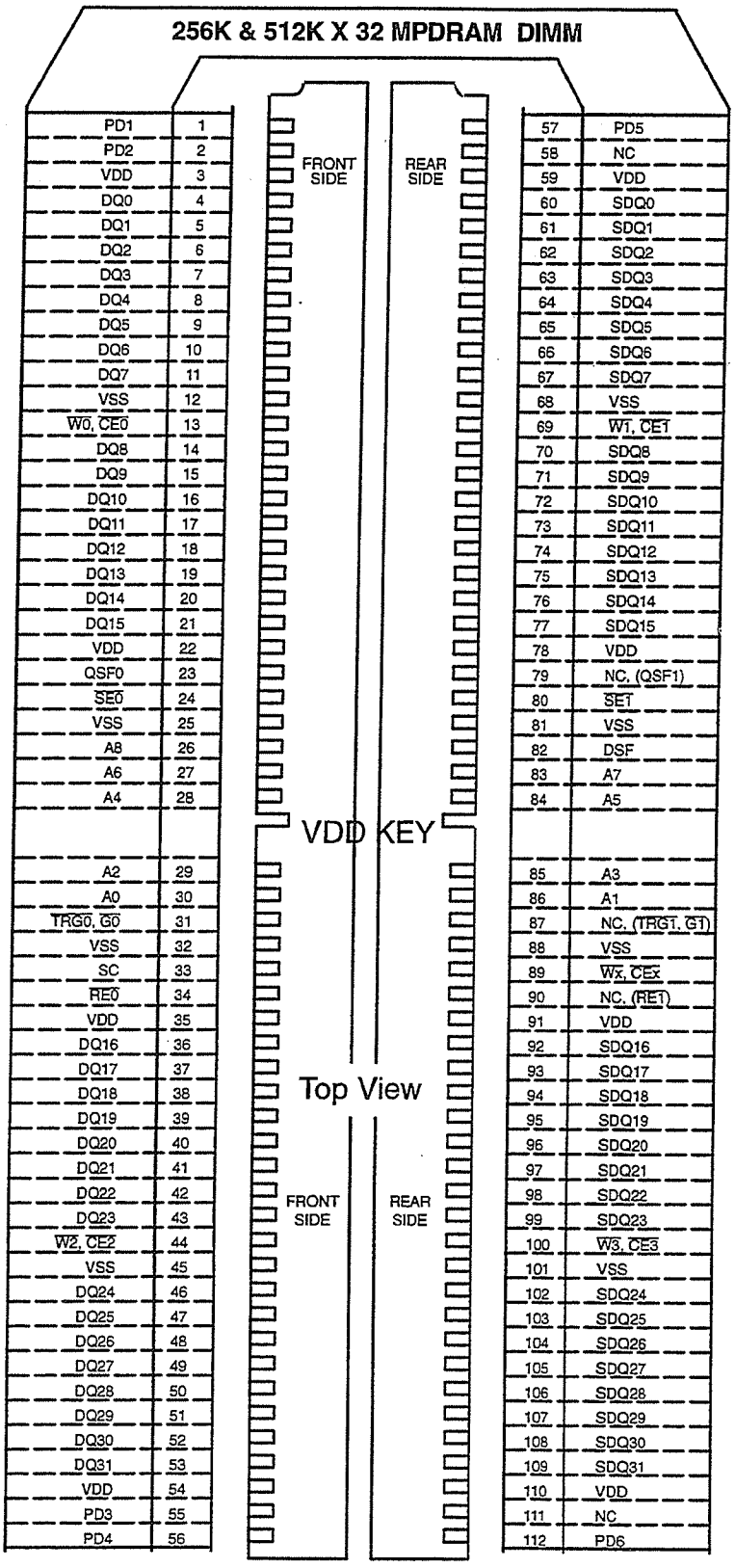


FIGURE 4.4.5–F
X 36 DRAM ECC SO–DIMM USING X4 DEVICES

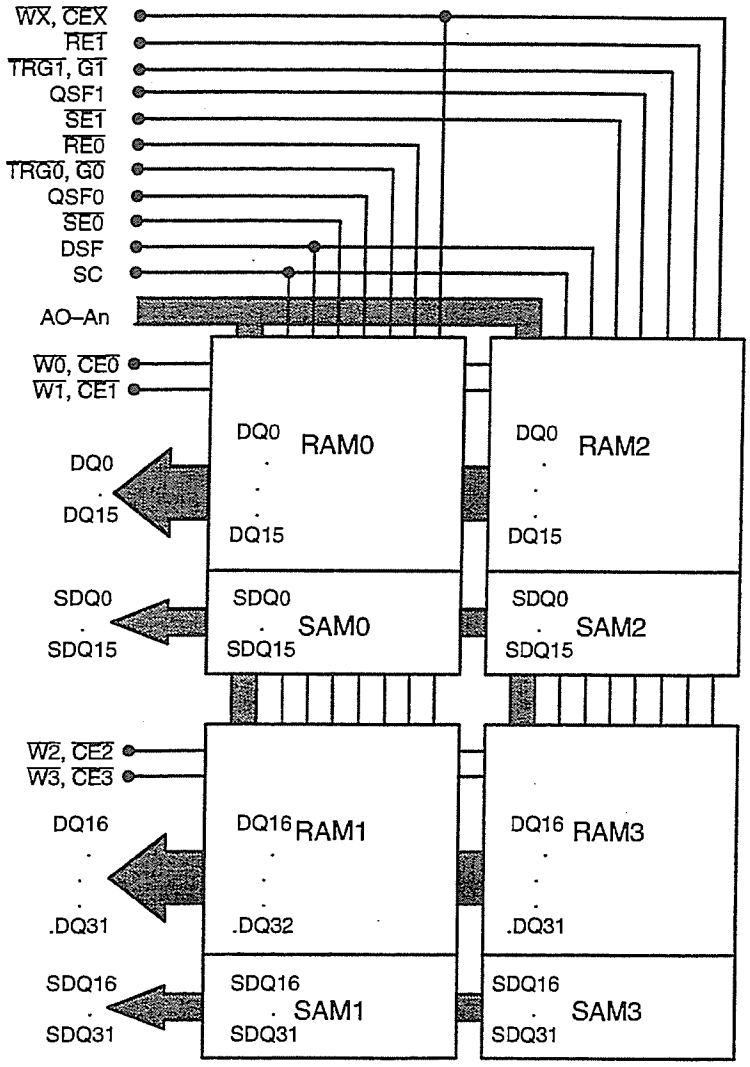
4.4.6 – 112 PIN MPDRAM DIMM FAMILY

CAPACITY—256K, and 512K WORDS OF 32 BITS ON THE SERIAL AND PARALLEL PORTS.
DATA CONFIGURATIONS—Two DEVICE configurations are defined: using X8 and X16 MPDRAM
CONFIGURATION—2 Different Configurations are defined using X4 & X8 memories with 2 banks.
LOGIC FEATURES—The modules contain independent clock control of the 4 separate BYTE groups of data bits and "PRESENCE DETECT" features that consists of output pins in the PDn field which supplies encoded values that define the storage capacity, SAM length, read mode, refresh mode, $\overline{CE}/\overline{W}$ logic configuration, and speed of the module.
PACKAGE—112 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS AND PD TABLES—Figs. 4.4.6–A
PRESENCE DETECT TABLES—Fig. 4.4.6–B
CONFIGURATION BLOCK DIAGRAM—Figs. 4.4.6–B & 4.4.6–C



NOTE: Pin functions in ( ) may be re;quired on certain 2–bank 512K X 32 module implementations

FIGURE 4.4.6–A
256K & 512K MPDRAM DIMM



BLOCK DIAGRAM for 256K/512K X 32 DIMM WITH 256K BY 16 MPDRAM

CAPACITY	
	PD1
	Pin 1
1MB	S
2MB	O

SAM LENGTH	
	PD2
	Pin 2
256	S
512	O

OPERATIONAL MODE	
	PD3
	Pin 55
Fast Page	S
EDO	O

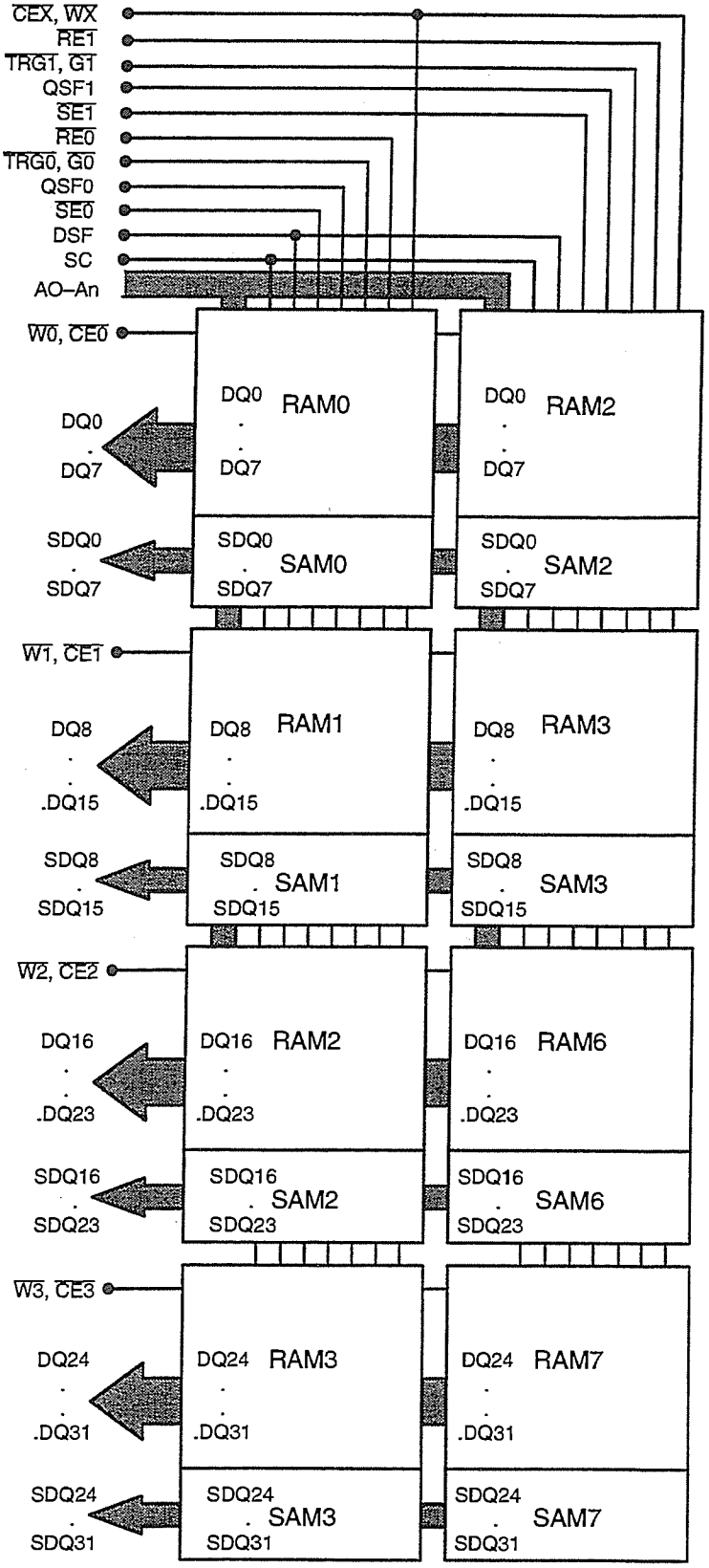
BYTE CONTROL	
	PD6
	Pin 112
4 $\overline{CE}$	S
4 $\overline{W}$	O

PD SPEED TABLE		
	PD4	PD5
SPEED (tRELQV)	Pin 56	Pin 57
80 ns	O	O
70 ns	S	O
60 ns	O	S
50 ns	S	S

S = CONNECTED TO VSS
O = NO CONNECTION

PD TRUTH TABLES for 256K/512K X 32 DIMM WITH 256K BY 8 or 16 MPDRAM

FIGURE 4.4.6–B
256K/512K BY 32 MPDRAM DIMM WITH 256K BY 16 MPDRAM



BLOCK DIAGRAM for 256K/512K X 32 DIMM WITH 256K BY 8 MPDRAM

FIGURE 4.4.6–C

256K/512K BY 32 MPDRAM DIMM WITH 256K BY 8 MPDRAM

4.4.7 – 80 PIN EEPROM SIMM FAMILY

CAPACITY—128K, 256K, 512K, 1M, 2M, 4M, & 8M WORDS OF 32 BITS
CONFIGURATION—Fifteen Different Configurations Using 1mb, 4mb, & 16mb Devices.
LOGIC FEATURES—The modules contain a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the module.
PACKAGE—88 PIN JEDEC MEMORY MODULE
PIN ASSIGNMENTS AND PD TABLES—Fig. 4.4.7–A
CONFIGURATION BLOCK DIAGRAM—Figs. 4.4.7–B

PIN #	PIN NAME	PIN #	PIN NAME
1	VSS	41	A11
2	VDD	42	A10
3	VPP/NC	43	A9
4	$\overline{G}$	44	A8
5	$\overline{W0}$	45	A7
6	$\overline{W1}$	46	A6
7	RFU	47	A5
8	DQ16	48	A4
9	DQ17	49	A3
10	DQ18	50	A2
11	DQ19	51	A1
12	DQ20	52	A0
13	DQ21	53	$\overline{W3}$
14	DQ22	54	VSS
15	DQ23	55	DQ15
16	DQ24	56	DQ14
17	DQ25	57	DQ13
18	DQ26	58	DQ12
19	DQ27	59	DQ11
20	DQ28	60	DQ10
21	$\overline{E3}$	61	DQ9
22	$\overline{E2}$	62	DQ8
23	$\overline{E1}$	63	DQ7
24	$\overline{E0}$	64	DQ6
25	VSS	65	DQ5
26	DQ29	66	DQ4
27	DQ30	67	DQ3
28	DQ31	68	DQ2
29	$\overline{W2}$	69	DQ1
30	A22	70	DQ0
31	A21	71	VPP/NC
32	A20	72	VDD
33	A19	73	PD1
34	A18	74	PD2
35	A17	75	PD3
36	A16	76	PD4
37	A15	77	PD5
38	A14	78	PD6
39	A13	79	PD7
40	A12	80	VSS

PRESENCE DETECT TRUTH TABLE							
Module Organization	Device Density	# of Dev.	Module Capacity	PD1	PD2	PD3	PD4
No Module				1	1	1	1
.128K X 32	1M	4	512KB	0	1	1	1
256K X 32	1M	8	1MB	1	0	1	1
512K X 32	1M	16	2MB	0	0	1	1
256K X 32	2M	4	1MB	1	1	0	1
512K X 32	2M	8	2MB	0	1	0	1
1M X 32	2M	16	4MB	1	0	0	1
512K X 32	4M	4	2MB	0	0	0	1
1M X 32	4M	8	4MB	1	1	1	0
2M X 32	4M	16	8MB	0	1	1	0
1M X 32	8M	4	4MB	1	0	1	0
2M X 32	8M	8	8MB	0	0	1	0
4M X 32	8M	16	16MB	1	1	0	0
2M X 32	16M	4	8MB	0	1	0	0
4M X 32	16M	8	16MB	1	0	0	0
8M X 32	16M	16	32MB	0	0	0	0

1 = OPEN CIRCUIT (NO CONNECTION)
0 = CONNECTED TO VSS

MODULE SPEED IDENTIFICATION			
MAX ACCESS TIME	PRESENCE DETECT PIN		
	PD5	PD6	PD7
NOT DEFINED	1	1	1
45 nS	0	1	1
55 nS	1	0	1
70 nS	0	0	1
90 nS	1	1	0
120 nS	0	1	0
150 nS	1	0	0
200 nS	0	0	0

NOTE – This family of pinouts is approved for use in SIMM package that is nominally 4.65" long and a height of 0.85" See JEDEC Publication 95, section MO–XXX.

FIGURE 4.4.7–A
128K TO 8M BY 32 EEPROM SIMM, PINOUT AND PD TABLES

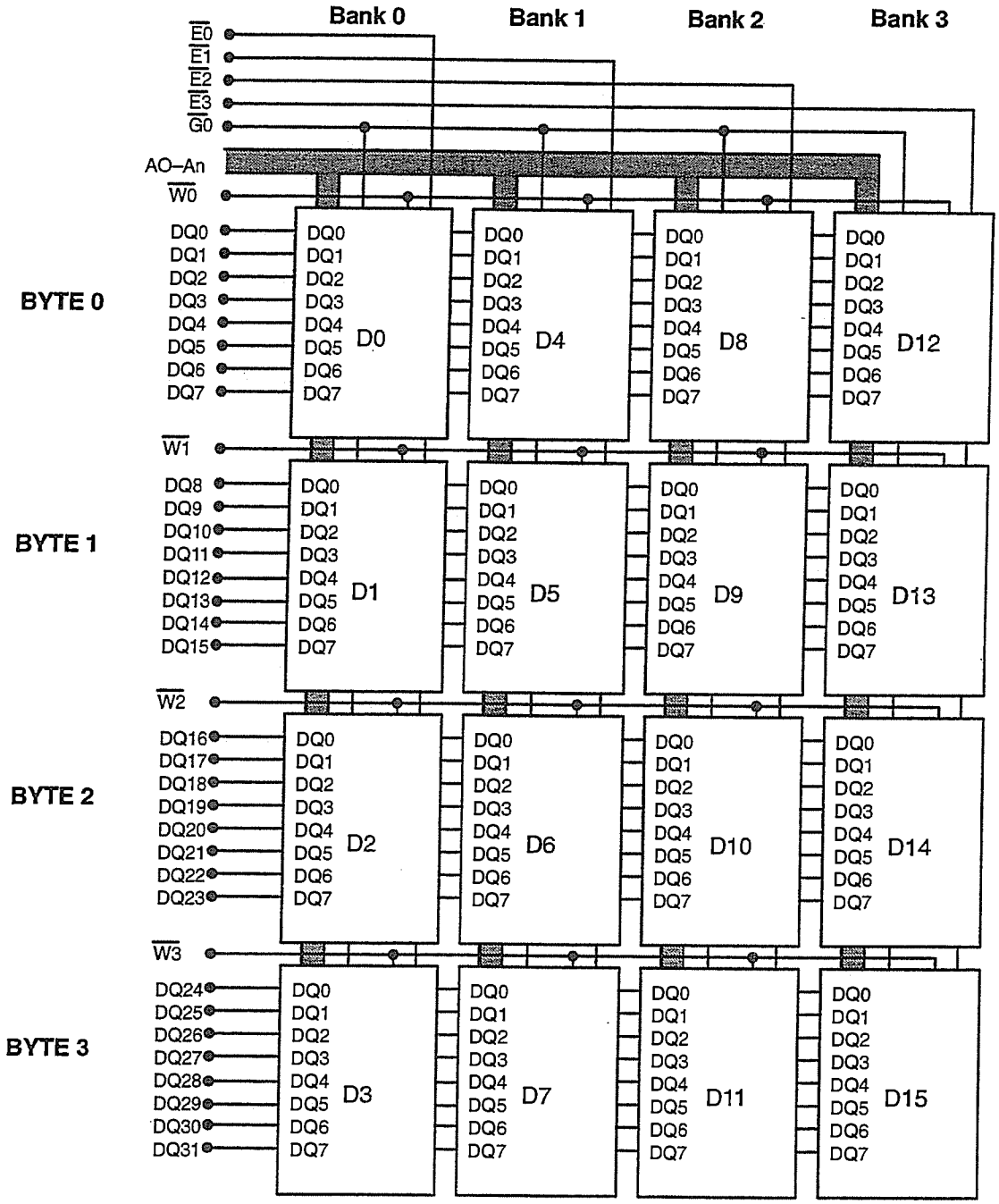


FIGURE 4.4.7–B
128K TO 8M BY 32 EEPROM SIMM BLOCK DIAGRAM

4.4.8 – 100 PIN DRAM, SDRAM & ROM DIMM FAMILY

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 32, 36, & 40 bits.
DATA CONFIGURATIONS—Seven DATA Word configurations are defined:
—32 BIT DRAM & SDRAM without PARITY
—36 BIT DRAM & SDRAM for ECC CODES
—40 BIT DRAM & SDRAM for ECC CODES
—32 BIT MULTIPLEXED ROM without PARITY.
CONFIGURATION—26 Different Configurations are defined using various combinationa of X1, X4, X8, and X16 DRAM & SDRAM memories including 2 bank configurations, 5 for DRAM and 21 for SDRAM.
LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that conist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—100 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS —Figs. 4.4.8–A & 4.4.8–B
TECHNOLOGY COMPARISON TABLE — Fig. 4.4.8–C
SDRAM CLOCK WIRING DIAGRAMS — Fig. 4.4.8–D
SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.4.8–E through 4.4.8–Z
DRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.4.8–AA through 4.4.8–AE

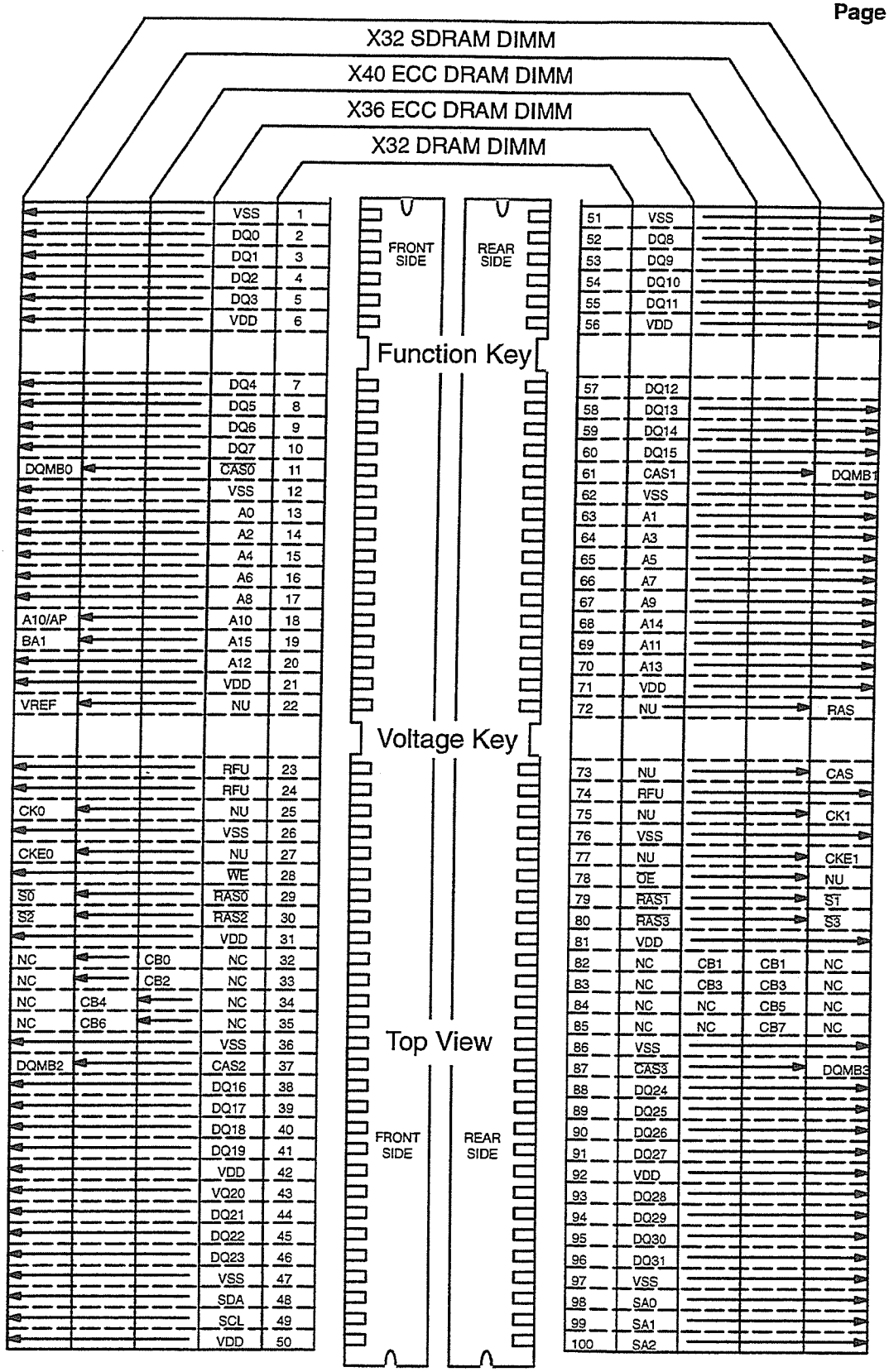


FIGURE 4.4.8– B

100 Pin 32, 36, or 40 BIT DRAM, 32 BIT SDRAM DIMM PINOUT

Release 7

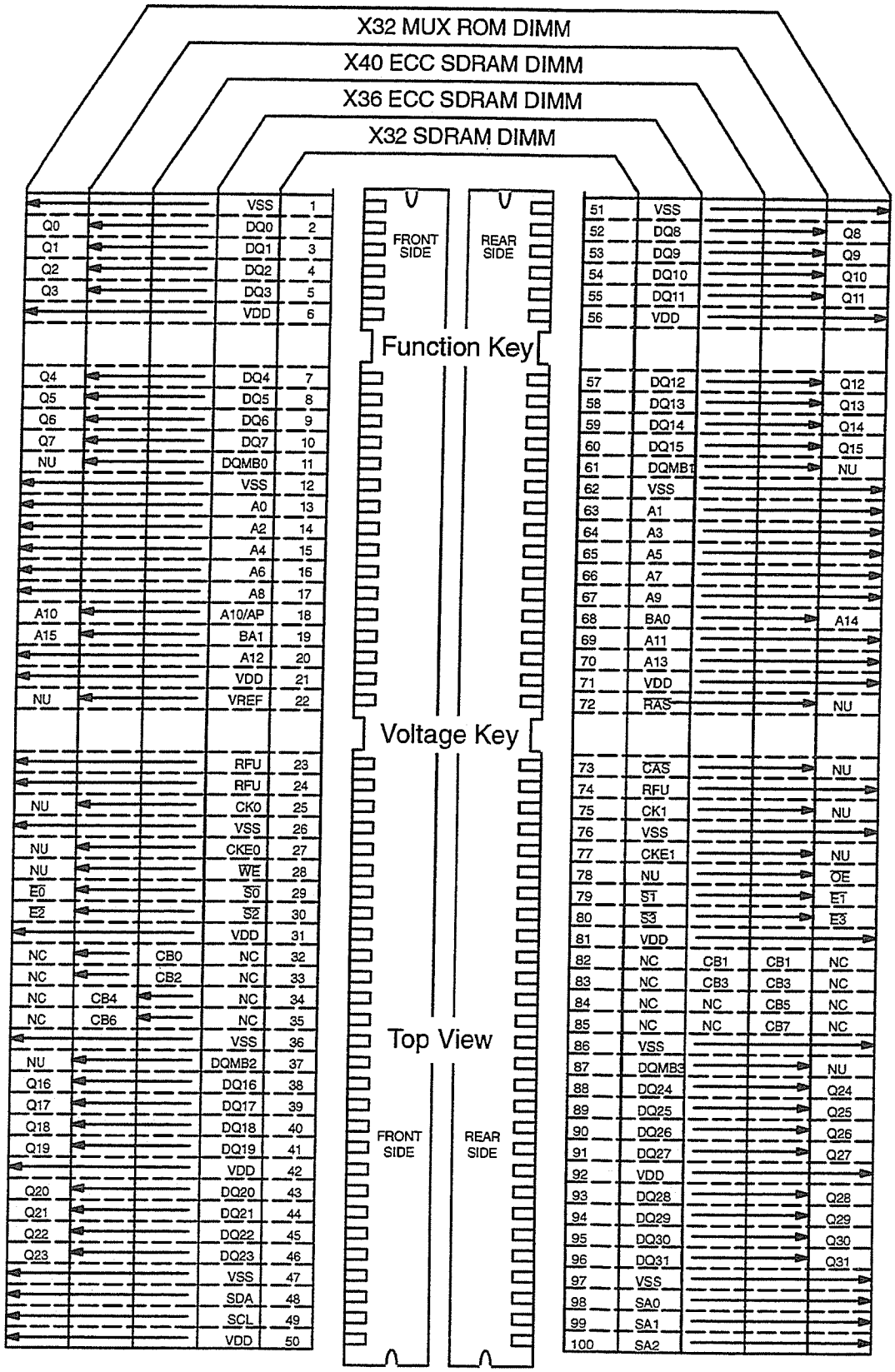


FIGURE 4.4.8– C

100 Pin 32, 36, or 40 BIT DRAM, 32 BIT SDRAM DIMM PINOUT

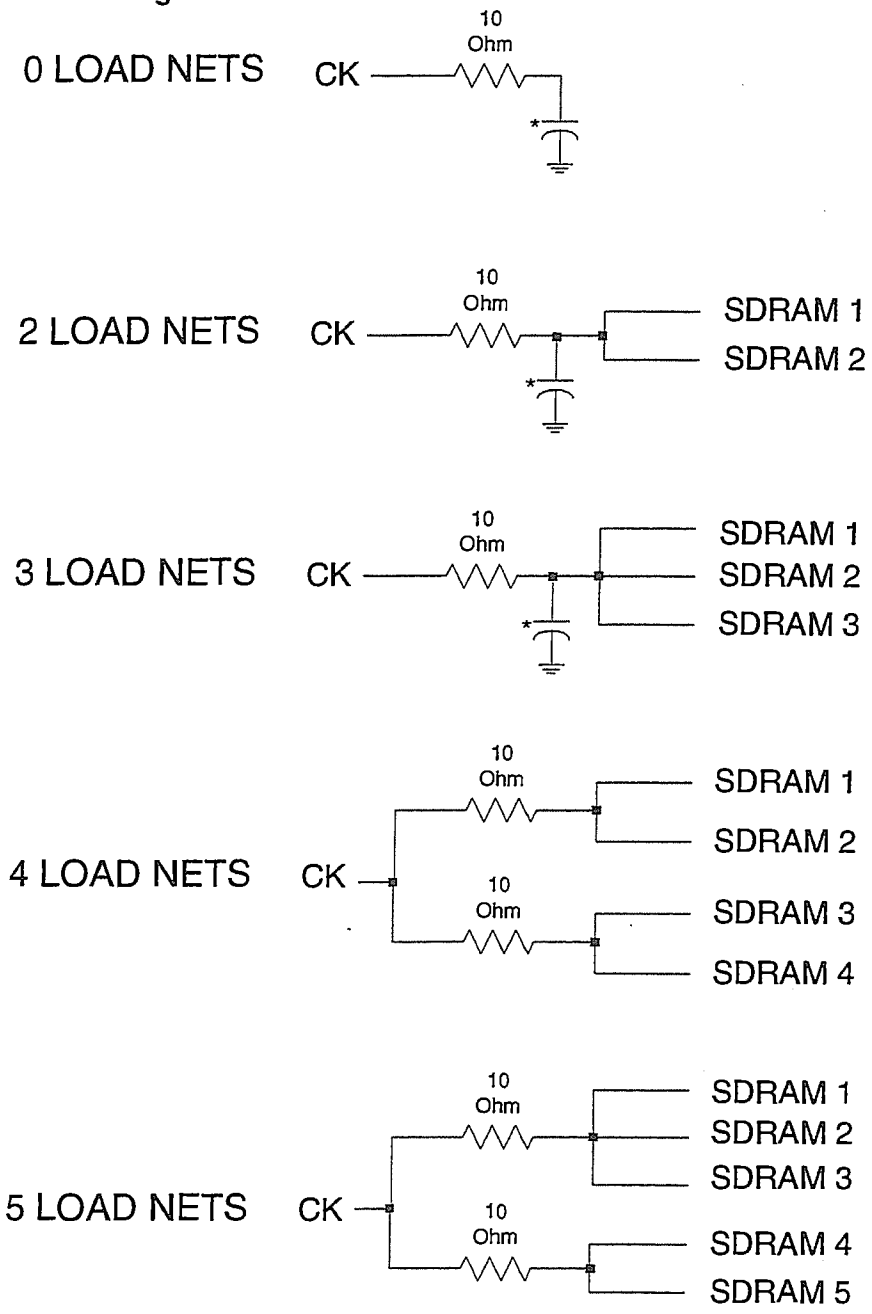
100 PIN DRAM/SDRAM DIMM PINOUT COMPARISON

PIN	DRAM DIMM	SDRAM DIMM	MUX ROM
11	$\overline{CAS0}$	DQMB0	NU
18	A10	A10/AP	A10
19	A12	BA1	A12
20	NU	A12	A14
22	NU	Vref	NU
25	NU	CK0	NU
27	NU	CKE0	NU
28	$\overline{WE}$	$\overline{WE}$	NU
29	$\overline{RAS0}$	$\overline{S0}$	$\overline{E0}$
30	$\overline{RAS2}$	$\overline{S2}$	$\overline{E2}$
37	$\overline{CAS2}$	DQMB2	NU
61	$\overline{CAS1}$	DQMB1	NU
68	A11	BA0	A11
69	A13	A11	A13
70	NU	A13	A15
72	NU	$\overline{RAS}$	NU
73	NU	$\overline{CAS}$	NU
75	NU	CK1	NU
77	NU	CKE1	NU
78	$\overline{OE}$	NU	$\overline{OE}$
79	$\overline{RAS1}$	$\overline{S1}$	$\overline{E1}$
80	$\overline{RAS3}$	$\overline{S3}$	$\overline{E3}$
87	$\overline{CAS3}$	DQMB3	NU

Notes:

1. A10 on DRAM DIMM is also AP on SDRAM DIMM
2. A14 on DRAM DIMM is also BA0 on SDRAM DIMM
3. A15 on DRAM DIMM is also BA1 on SDRAM DIMM (for 4 Bank SDRAM).

Figure 4.4.8–D
100 Pin DRAM, SDRAM, & ROM DIMM, PIN COMPARISON

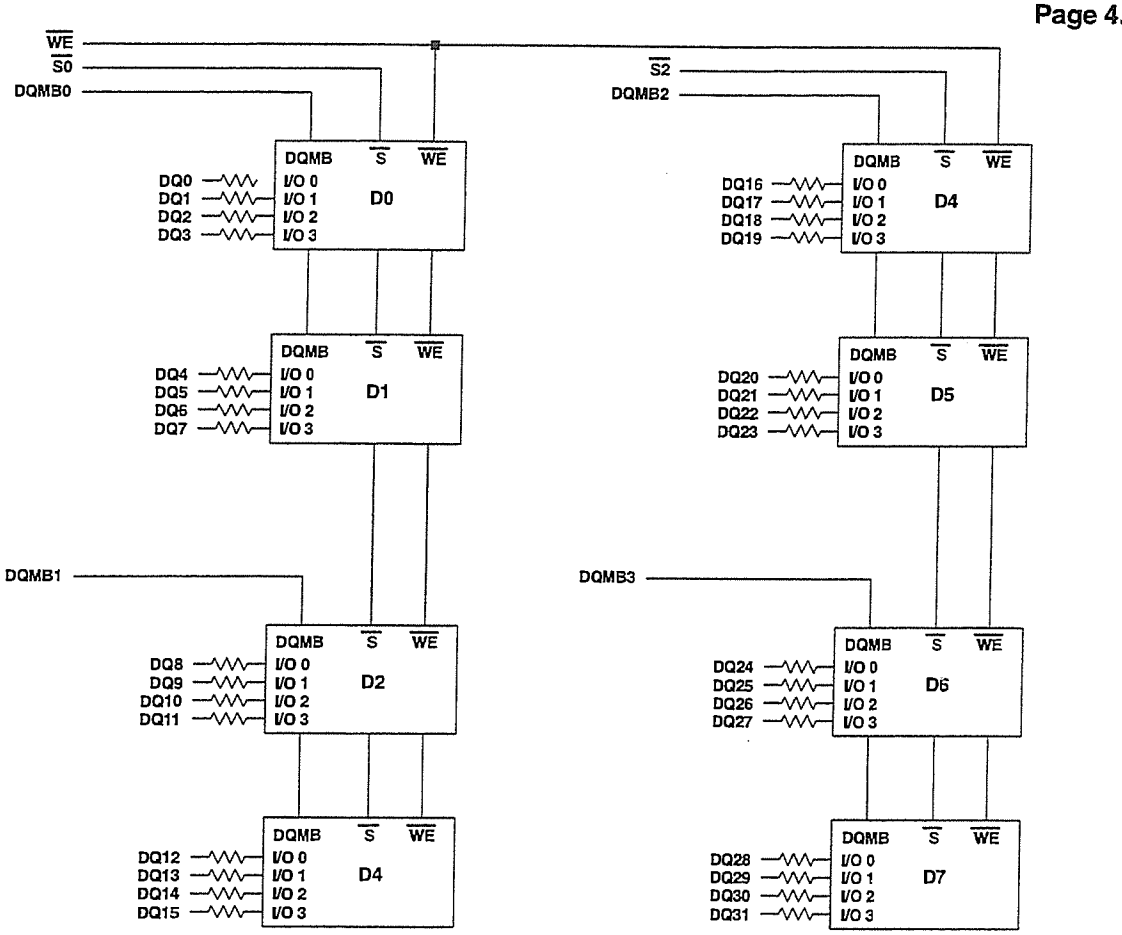


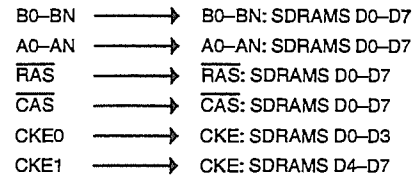
Notes:

1. THE CK INPUTS SHOULD HAVE A NOMINAL DELAY OF .4ns MEASURED FROM THE CK INPUT AT THE DIMM TAB TO THE CK INPUT OF THE SDRAM (OR PADDING CAPACITOR). (EG: THIS IS APPROXIMATELY 2" OF PCB WIRE AND 2.5pf OF INPUT CAPACITANCE).

2.) THE VARIATION OF CK INPUT DELAY WILL BE +/– .1NS FOR BOTH CK INPUTS. (EG: IF THE WIRE IMPEDANCE IS APPROX. 65 ohms, THIS CORRESPONDS TO A CAPACITANCE VARIATION OF +/– 3p IN TOTAL CK INPUT CAPACITANCE).

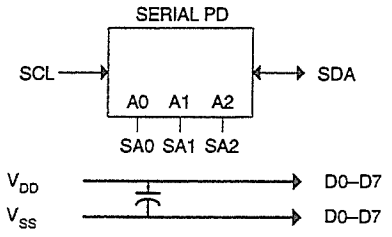
Figure 4.4.8–E
100 Pin SDRAM DIMM, CLOCK WIRING





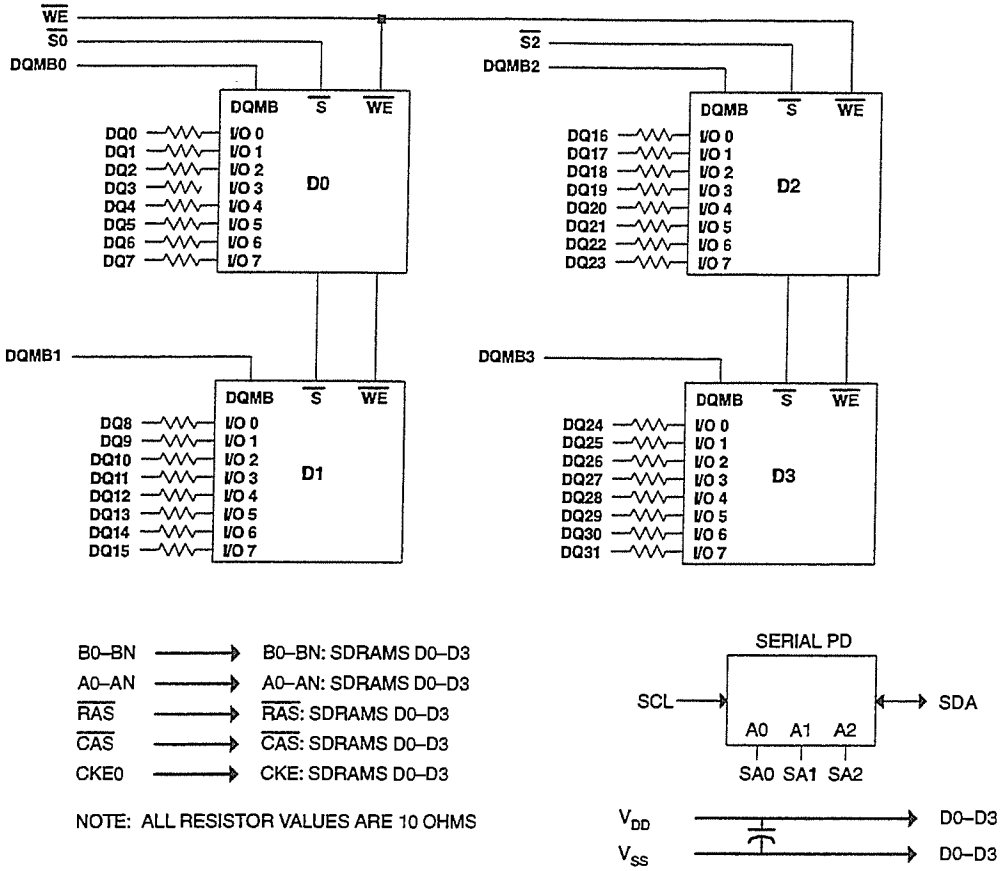
Clock Wiring	
Clock Input	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams



NOTE: ALL RESISTOR VALUES ARE 10 OHMS

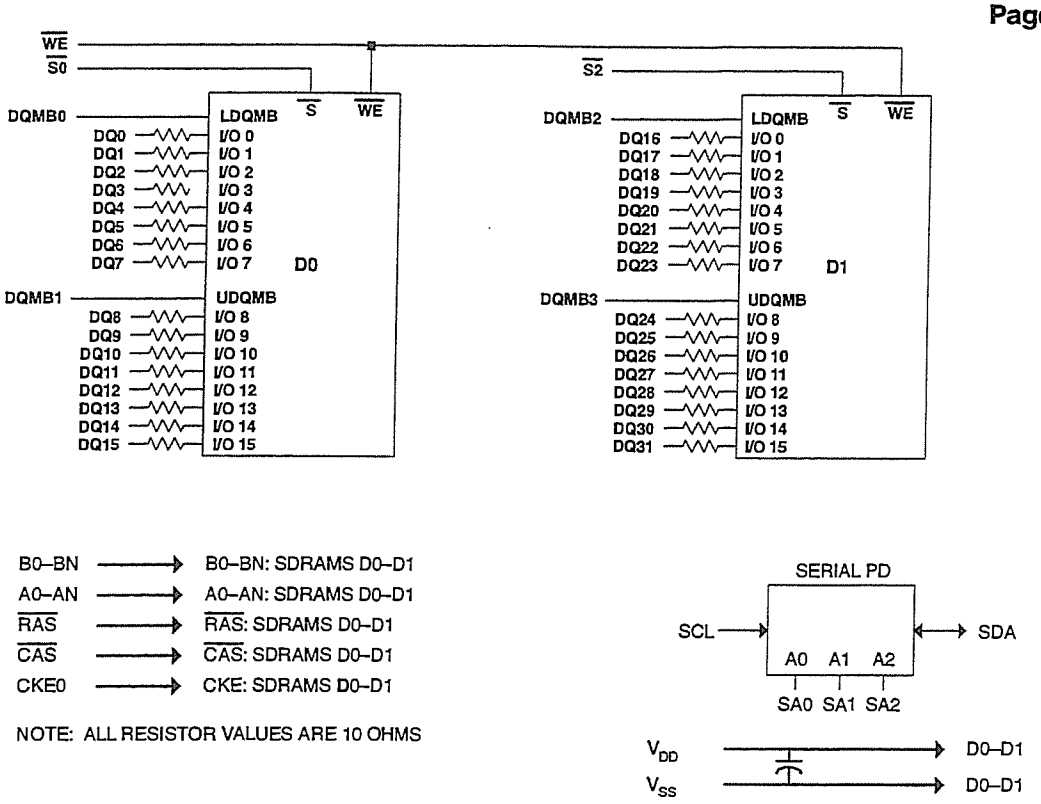
Figure 4.4.8–F
100 Pin X32 SDRAM DIMM, 1 Bank with X4 SDRAMs



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	4 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–G
100 Pin X32 SDRAM DIMM, 1 Bank with X8 SDRAMs



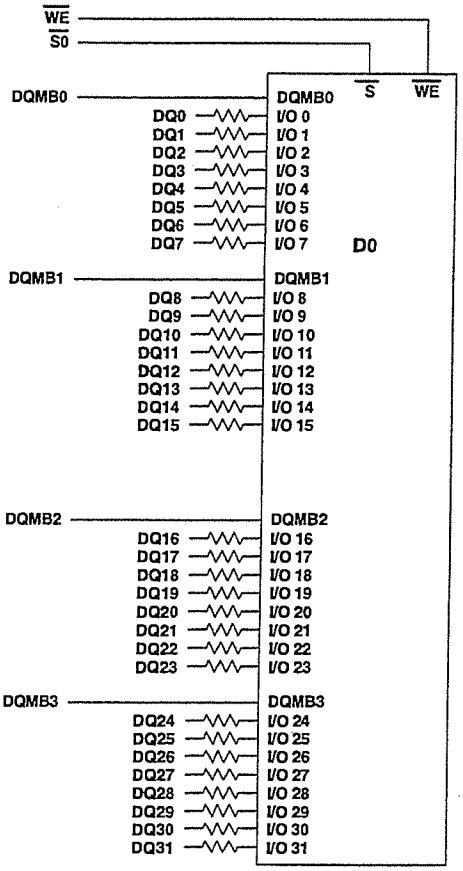
B0–BN → B0–BN: SDRAMS D0–D1
A0–AN → A0–AN: SDRAMS D0–D1
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D1
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D1
CKE0 → CKE: SDRAMS D0–D1

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	2 SDRAMS

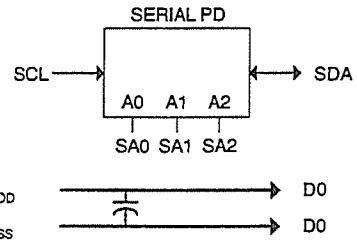
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–H
100 Pin X32 SDRAM DIMM, 1 Bank with X16 SDRAMs



B0–BN → B0–BN: SDRAMS D0
A0–AN → A0–AN: SDRAMS D0
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0
CKE0 → CKE: SDRAMS D0

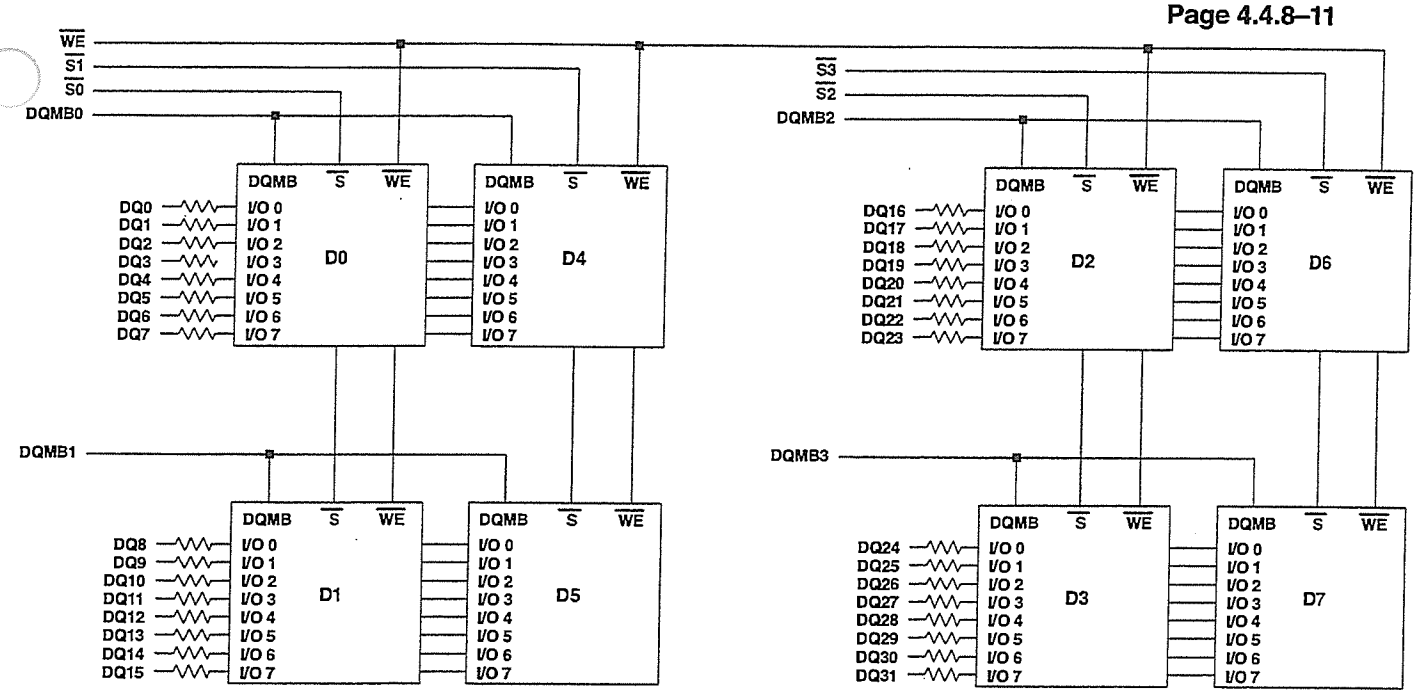
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	1 SDRAMS

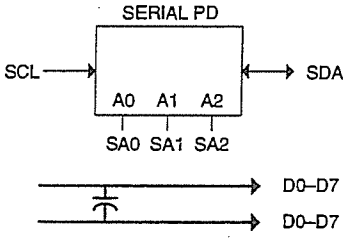
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–I
100 Pin X32 SDRAM DIMM, 1 Bank with X32 SDRAMs



B0–BN ⟶ B0–BN: SDRAMS D0–D7
A0–AN ⟶ A0–AN: SDRAMS D0–D7
$\overline{RAS}$ ⟶ $\overline{RAS}$: SDRAMS D0–D7
$\overline{CAS}$ ⟶ $\overline{CAS}$: SDRAMS D0–D7
CKE0 ⟶ CKE: SDRAMS D0–D3
CKE1 ⟶ CKE: SDRAMS D4–D7

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

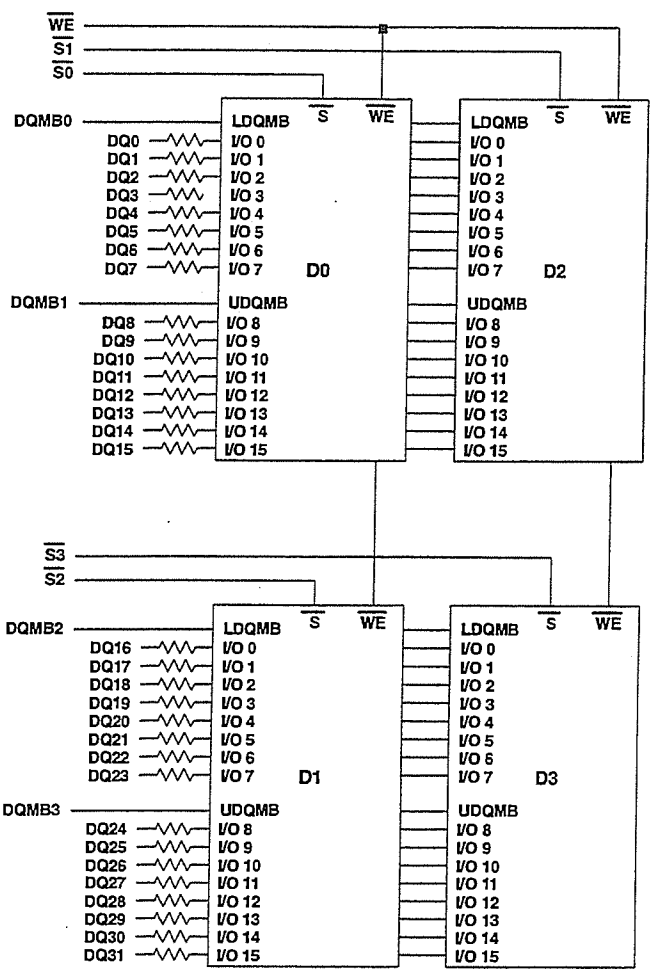


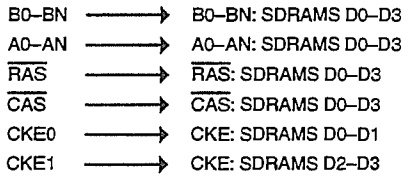
Clock Wiring	
Clock Input	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

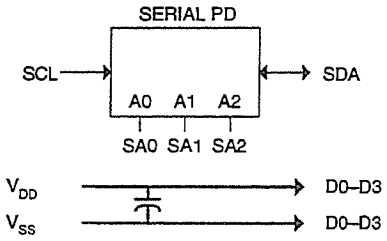
Figure 4.4.8–J
100 Pin X32 SDRAM DIMM, 2 Bank with X8 SDRAMs

4.4.6–1





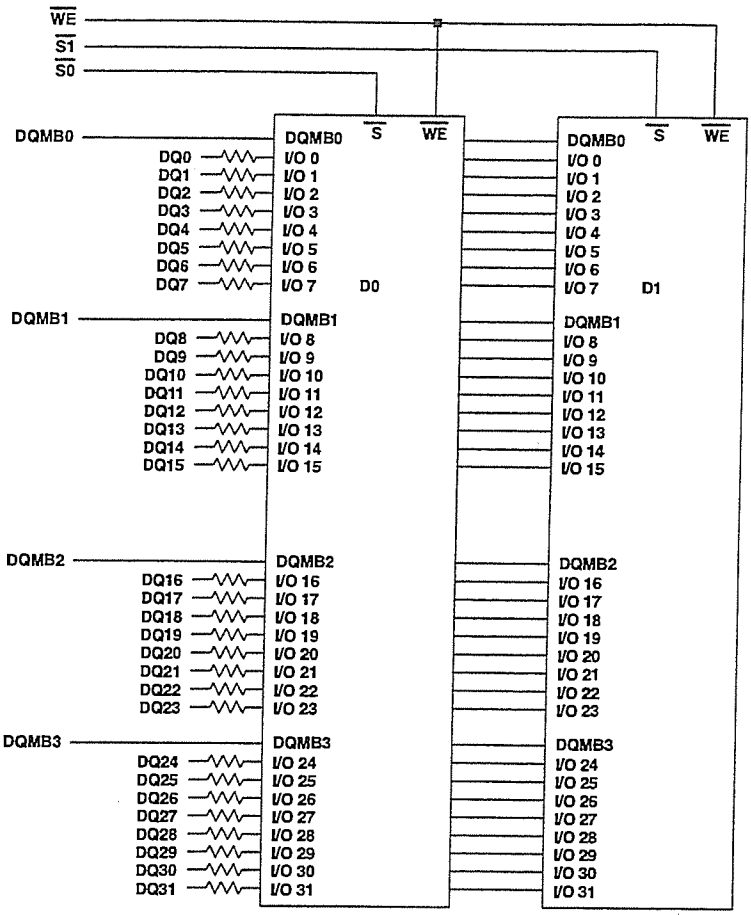
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0	2 SDRAMS
*CK1	2 SDRAMS

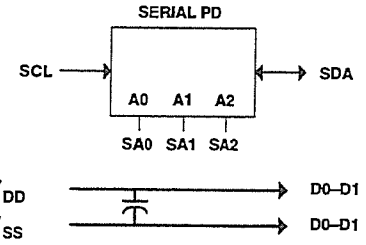
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–K
100 Pin X32 SDRAM DIMM, 2 Bank with X16 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D1
A0–AN → A0–AN: SDRAMS D0–D1
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D1
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D1
CKE0 → CKE: SDRAMS D0
CKE1 → CKE: SDRAMS D1

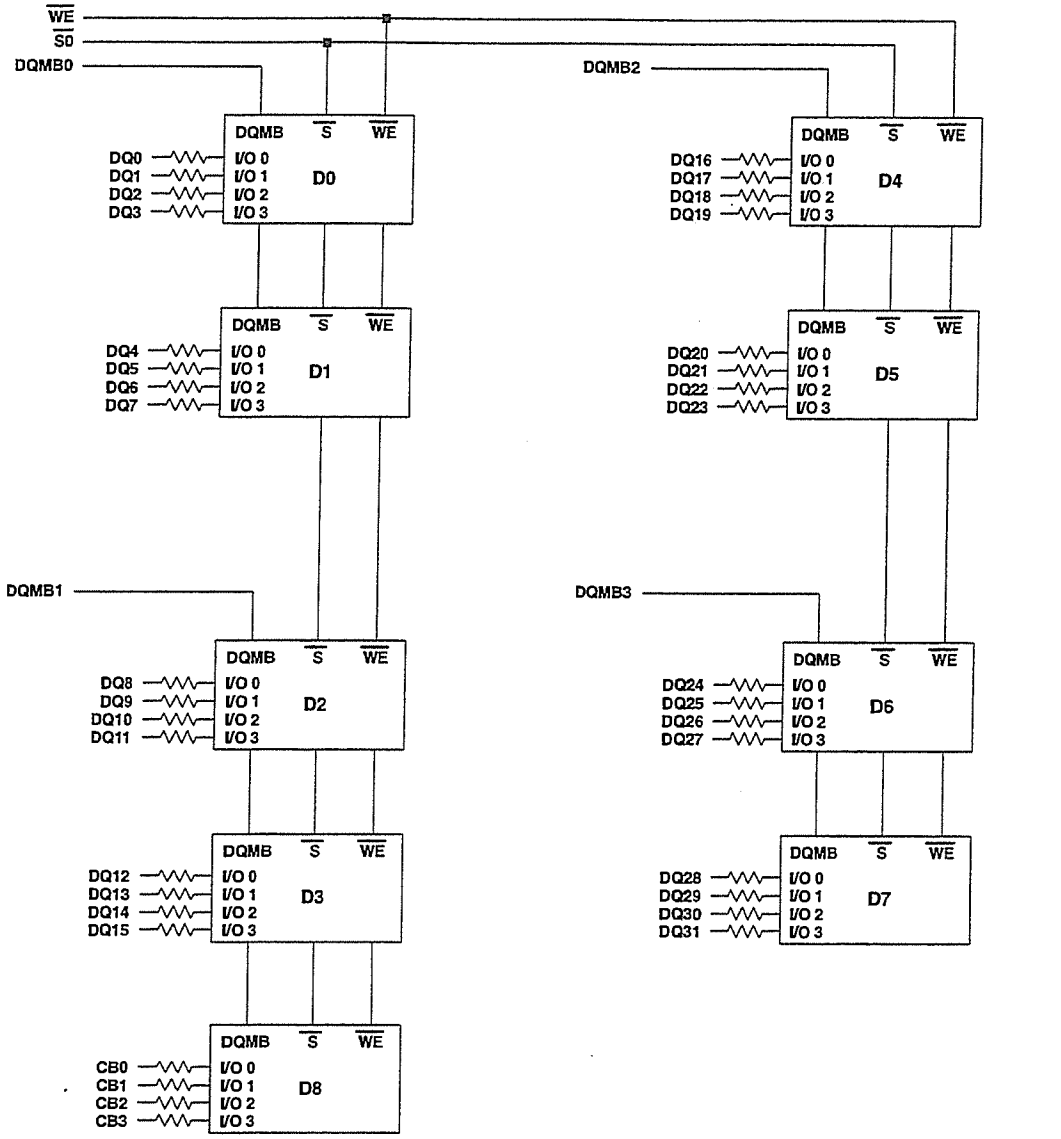
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0	1 SDRAM
*CK1	1 SDRAM

*Wire per Clock Loading Table/Wiring Diagrams

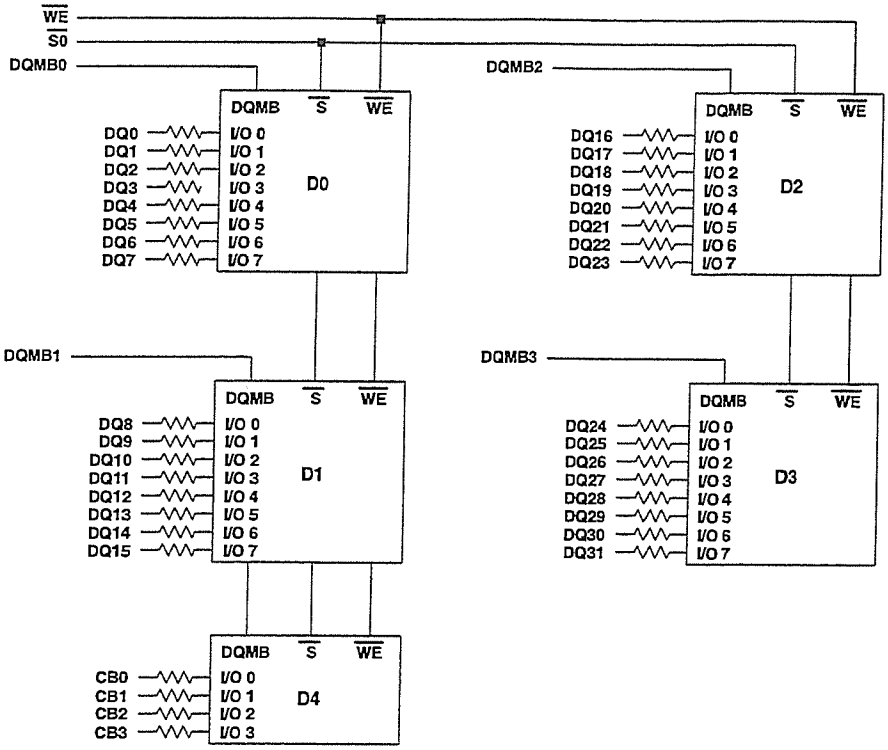
Figure 4.4.8–L
100 Pin X32 SDRAM DIMM, 2 Bank with X32 SDRAMs



Clock Wiring	
Clock Input	SDRAMS
*CK0	4 or 5 SDRAMS
*CK1	4 or 5 SDRAMS

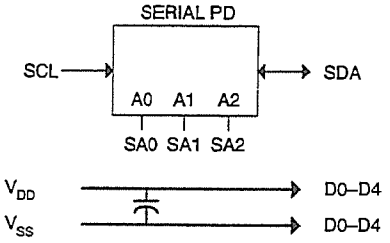
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–M
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D4
A0–AN → A0–AN: SDRAMS D0–D4
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D4
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D4
CKE0 → CKE: SDRAMS D0–D4

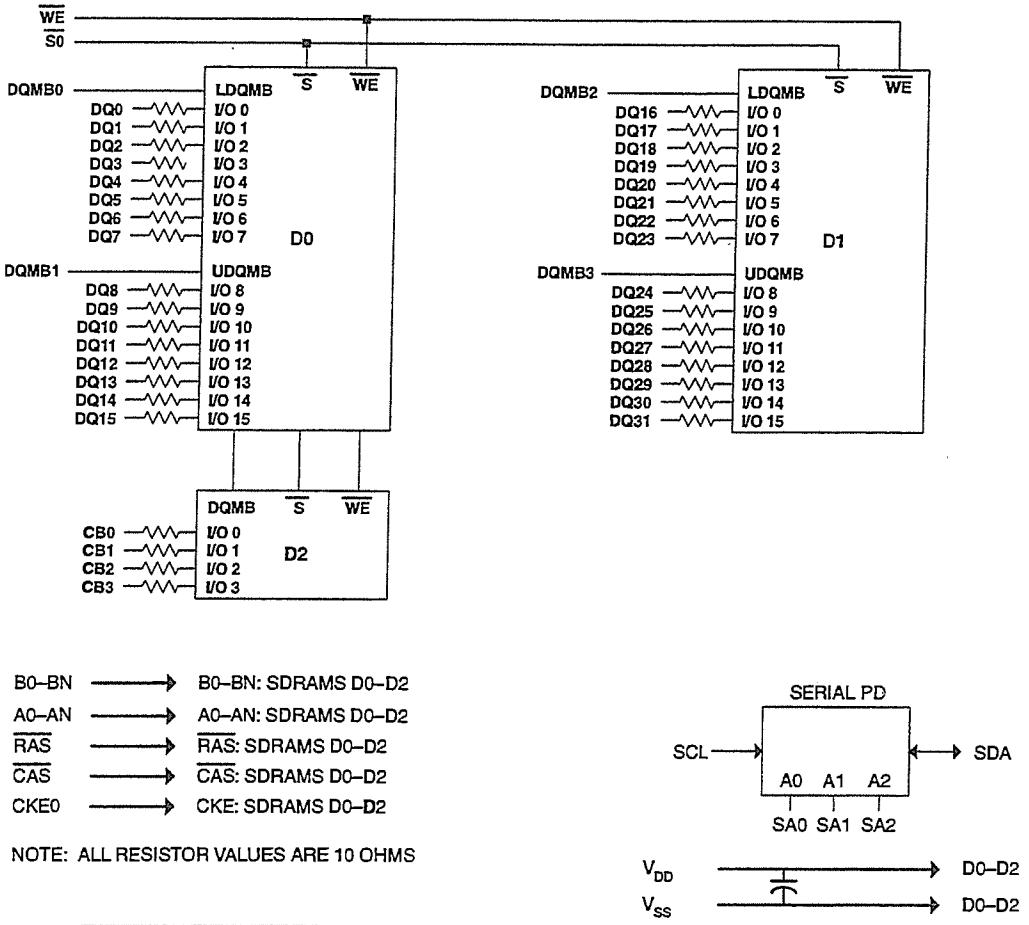
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

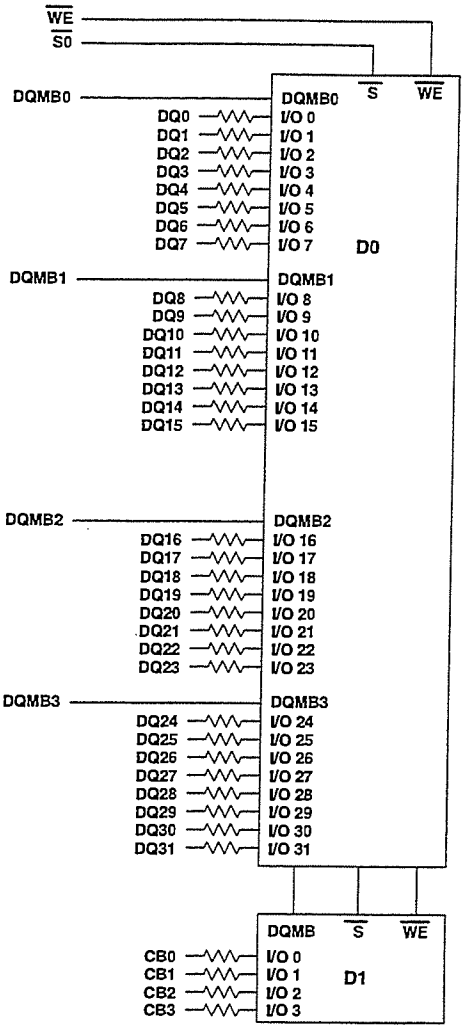
Figure 4.4.8–N
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 & X8 SDRAMs

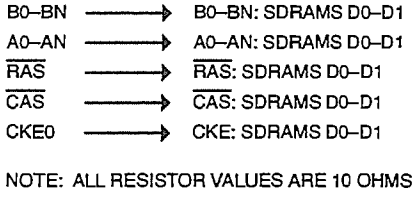


Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	3 SDRAMS

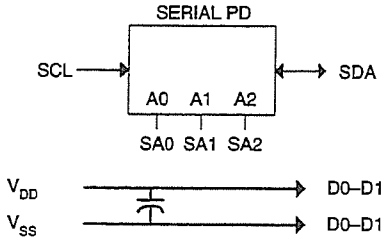
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–O
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 & X16 SDRAMs





NOTE: ALL RESISTOR VALUES ARE 10 OHMS

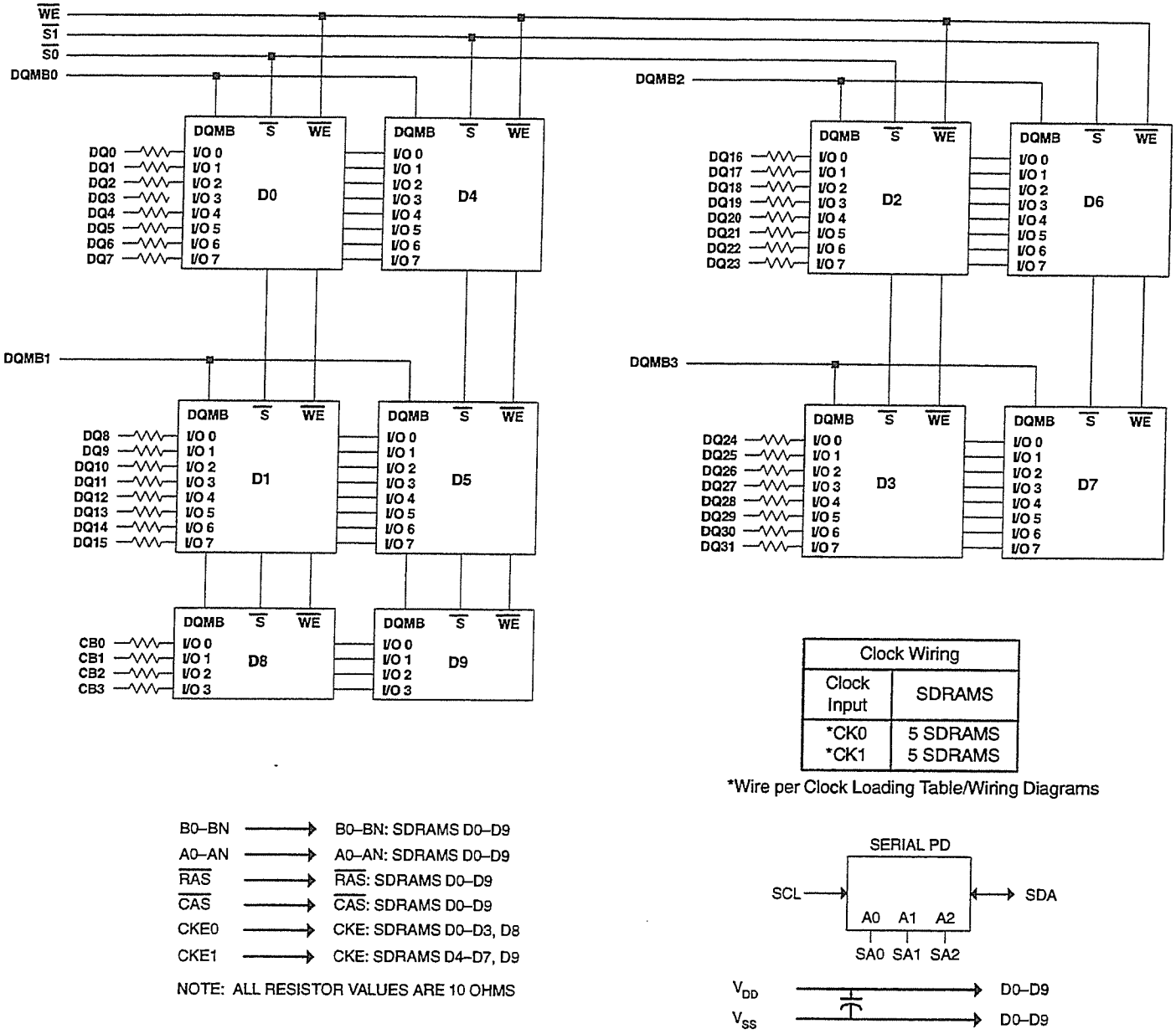


Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–P
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 & X32 SDRAMs

Release 7



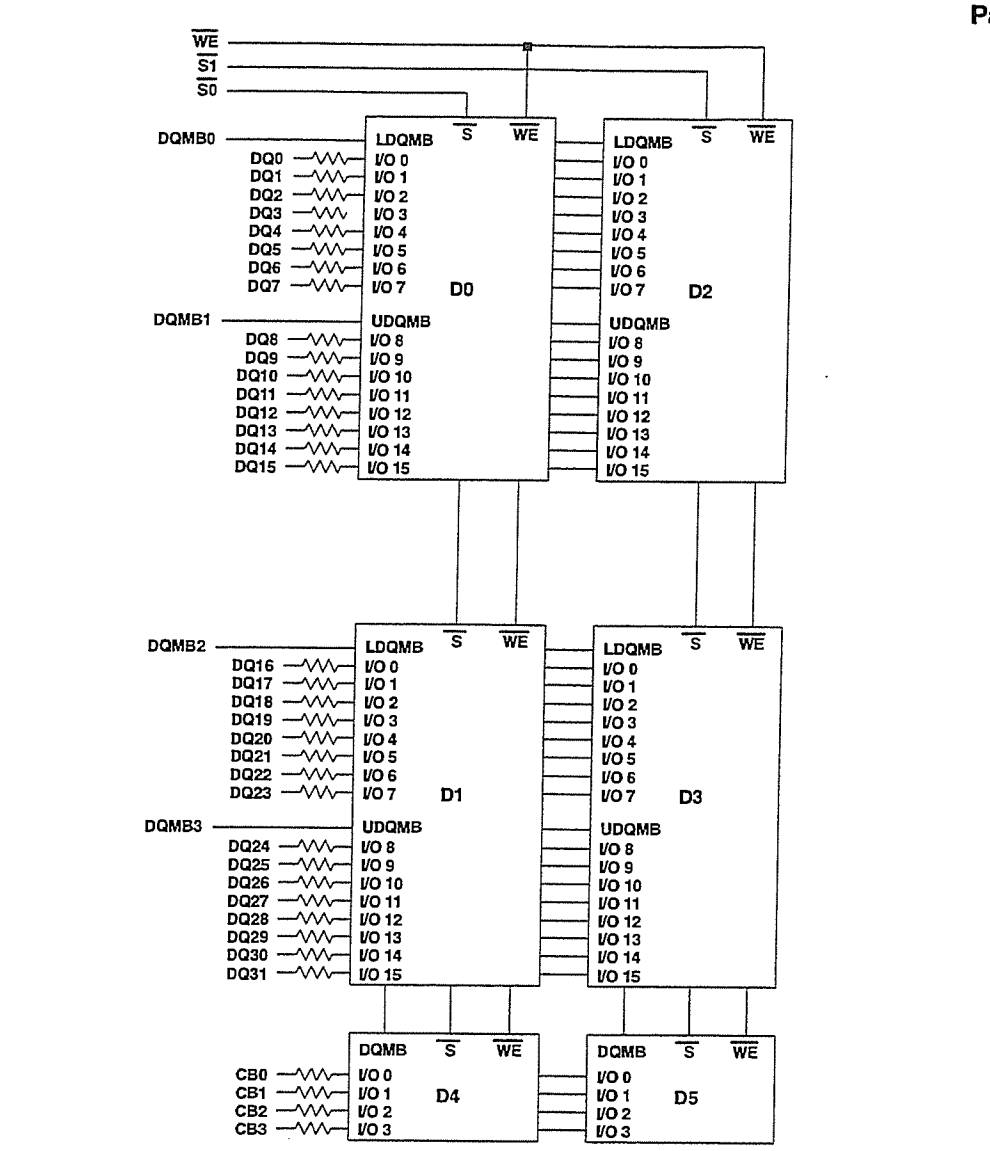
Clock Wiring	
Clock Input	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

B0–BN ⟶ B0–BN: SDRAMS D0–D9
A0–AN ⟶ A0–AN: SDRAMS D0–D9
$\overline{RAS}$ ⟶ $\overline{RAS}$: SDRAMS D0–D9
$\overline{CAS}$ ⟶ $\overline{CAS}$: SDRAMS D0–D9
CKE0 ⟶ CKE: SDRAMS D0–D3, D8
CKE1 ⟶ CKE: SDRAMS D4–D7, D9

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Figure 4.4.8–Q
100 Pin X36 ECC SDRAM DIMM, 2 Bank with X4 & X8 SDRAMs

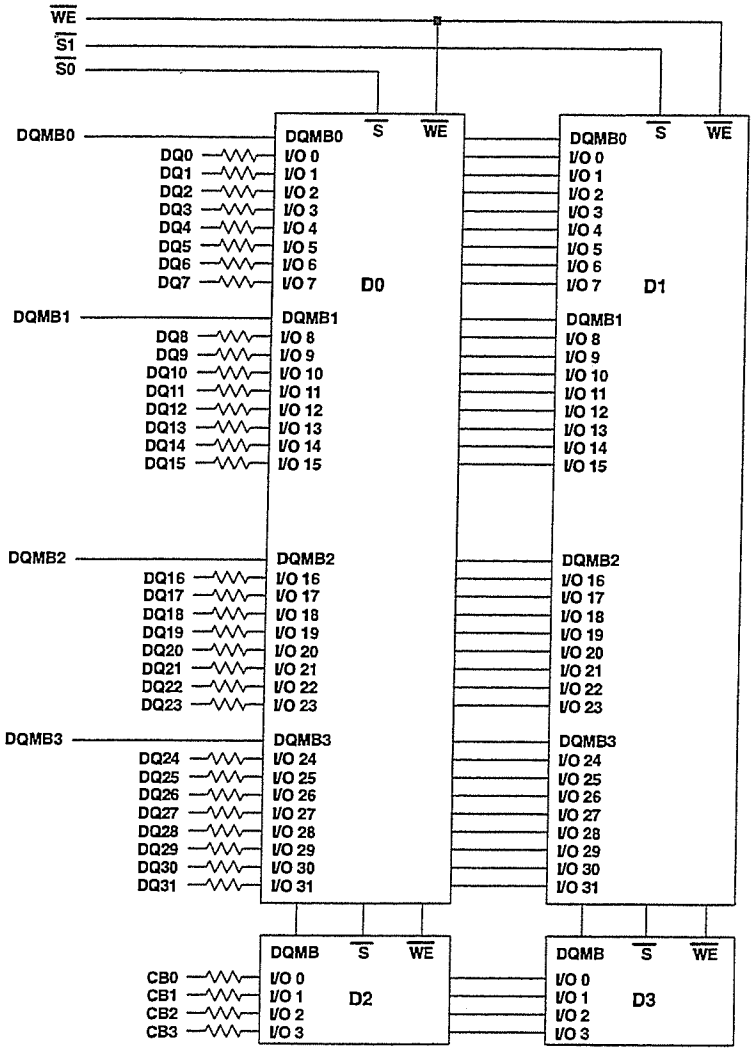


Clock Wiring	
Clock Input.	SDRAMS
*CK0	3 SDRAMS
*CK1	3 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

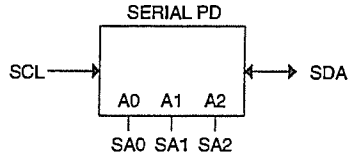
Figure 4.4.8–R
100 Pin X36 ECC SDRAM DIMM, 2 Bank with X4 & X16 SDRAMs

Release 7



B0–BN → B0–BN: SDRAMS D0–D3
A0–AN → A0–AN: SDRAMS D0–D3
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D3
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D3
CKE0 → CKE: SDRAMS D0, D2
CKE1 → CKE: SDRAMS D1, D3

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

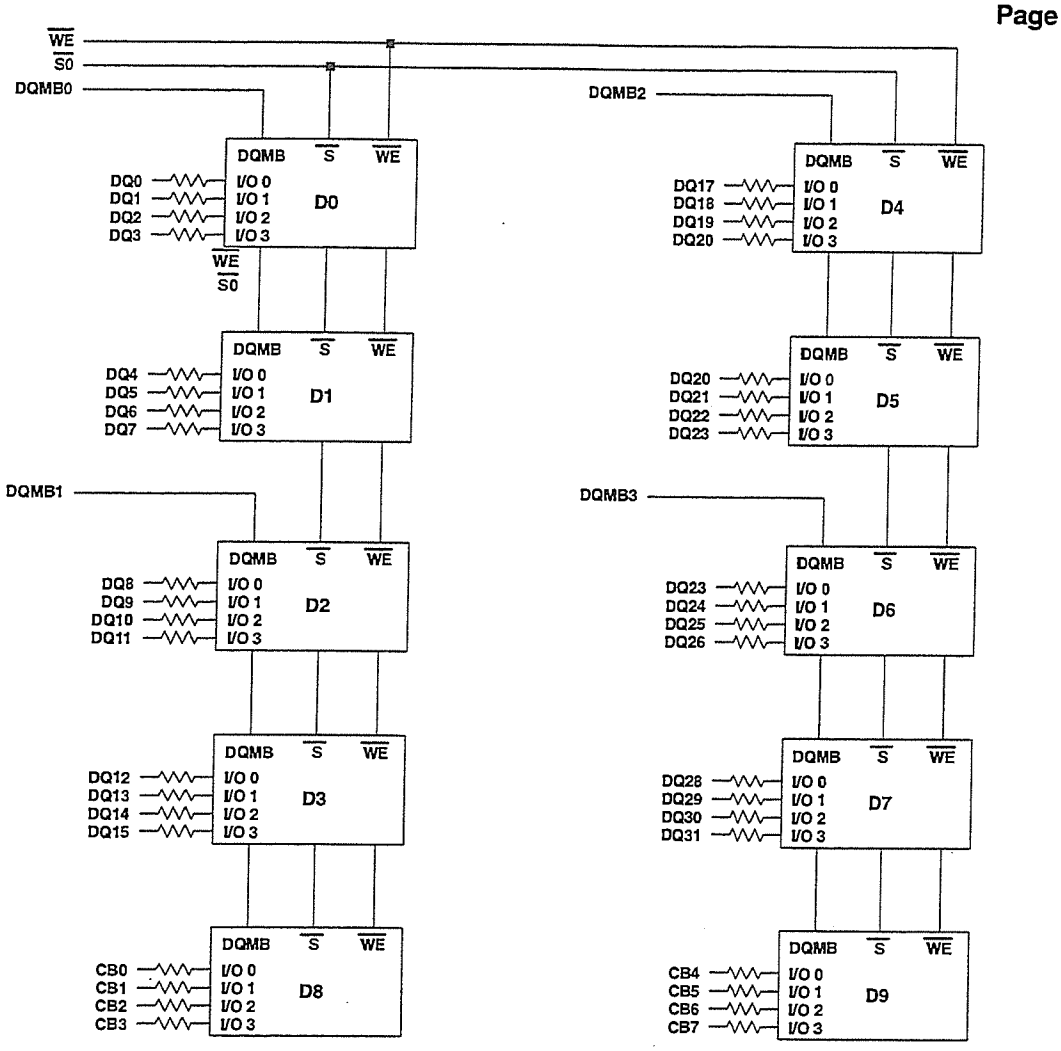


V_{DD} → D0–D3
V_{SS} → D0–D3

Clock Wiring	
Clock Input	SDRAMS
*CK0	2 SDRAMS
*CK1	2 SDRAMS

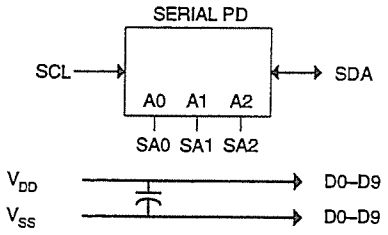
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–S
100 Pin X36 ECC SDRAM DIMM, 2 Bank with X4 & X32 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D9
A0–AN → A0–AN: SDRAMS D0–D9
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D9
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D9
CKE0 → CKE: SDRAMS D0–D3, D8
CKE1 → CKE: SDRAMS D4–D7, D9

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

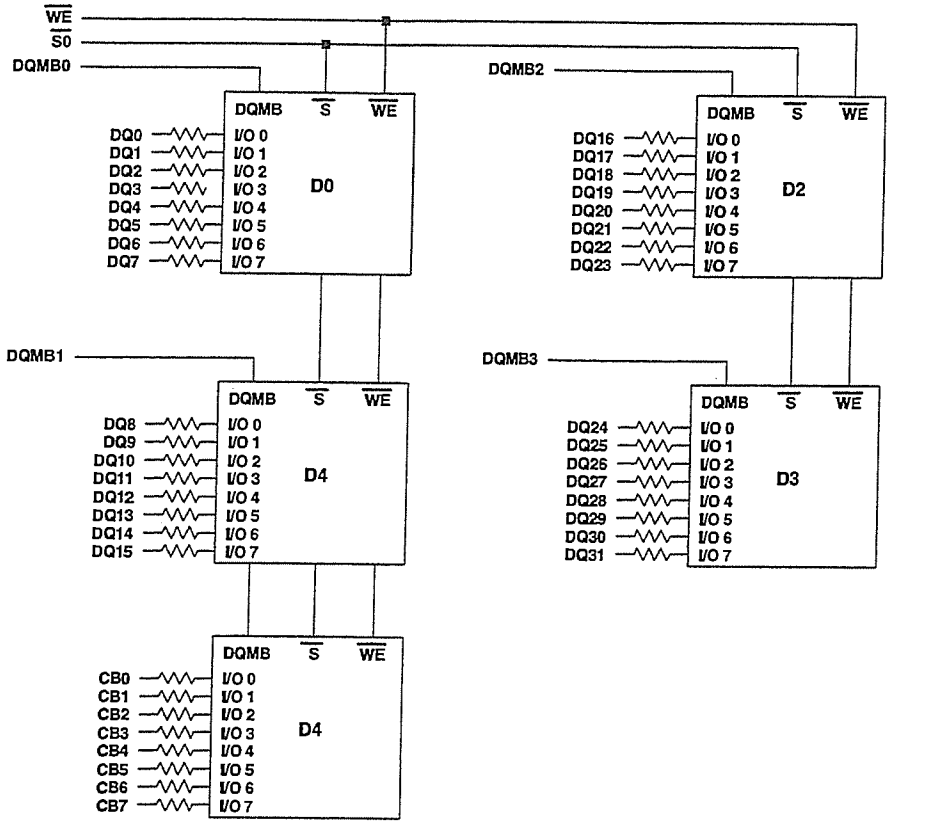


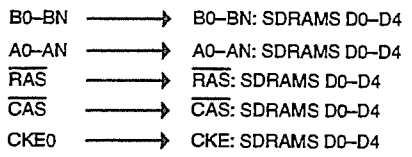
Clock Wiring	
Clock Input	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

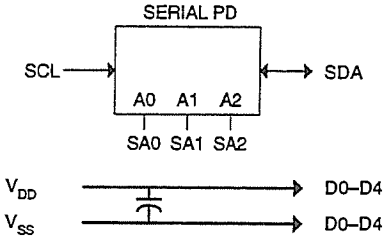
Figure 4.4.8–T
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X4 SDRAMs

Release 7





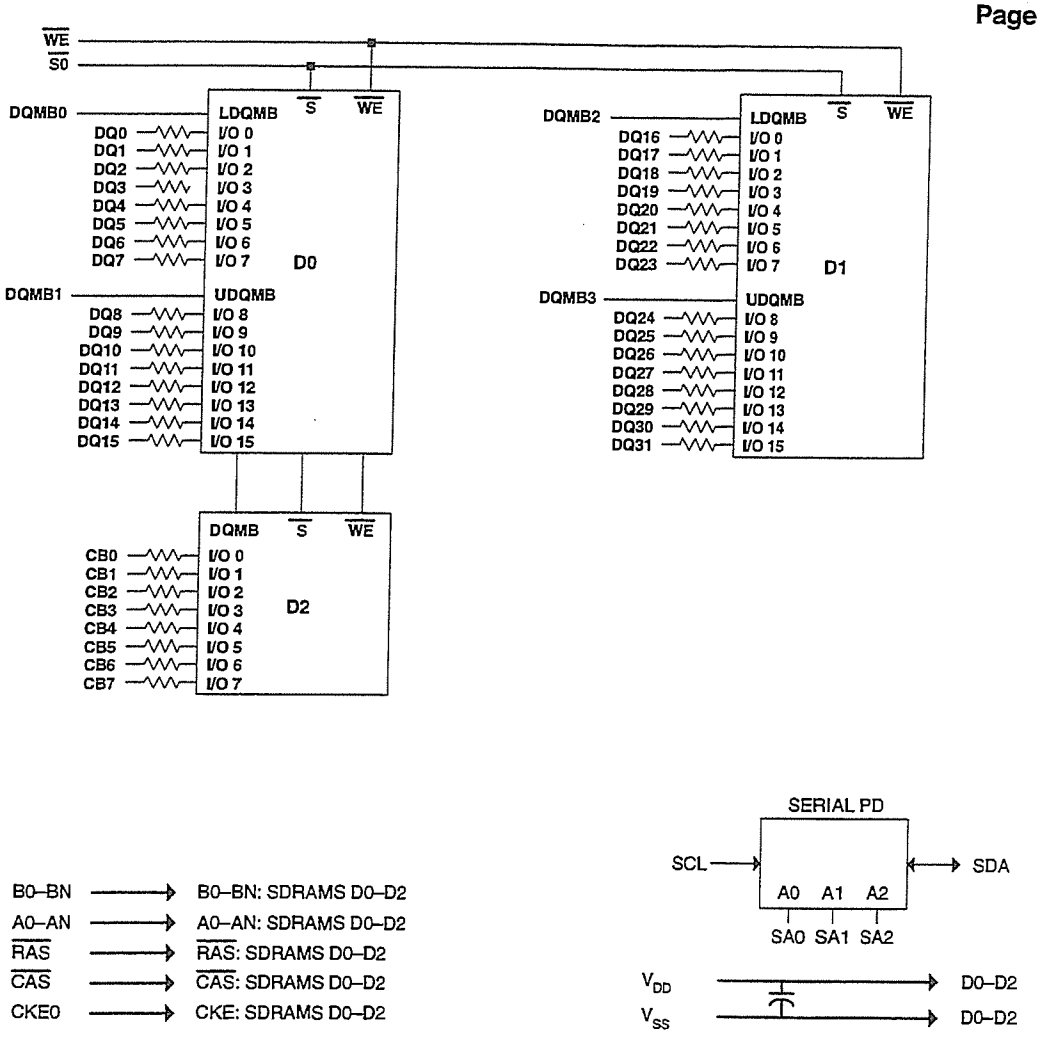
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–U
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X8 SDRAMs

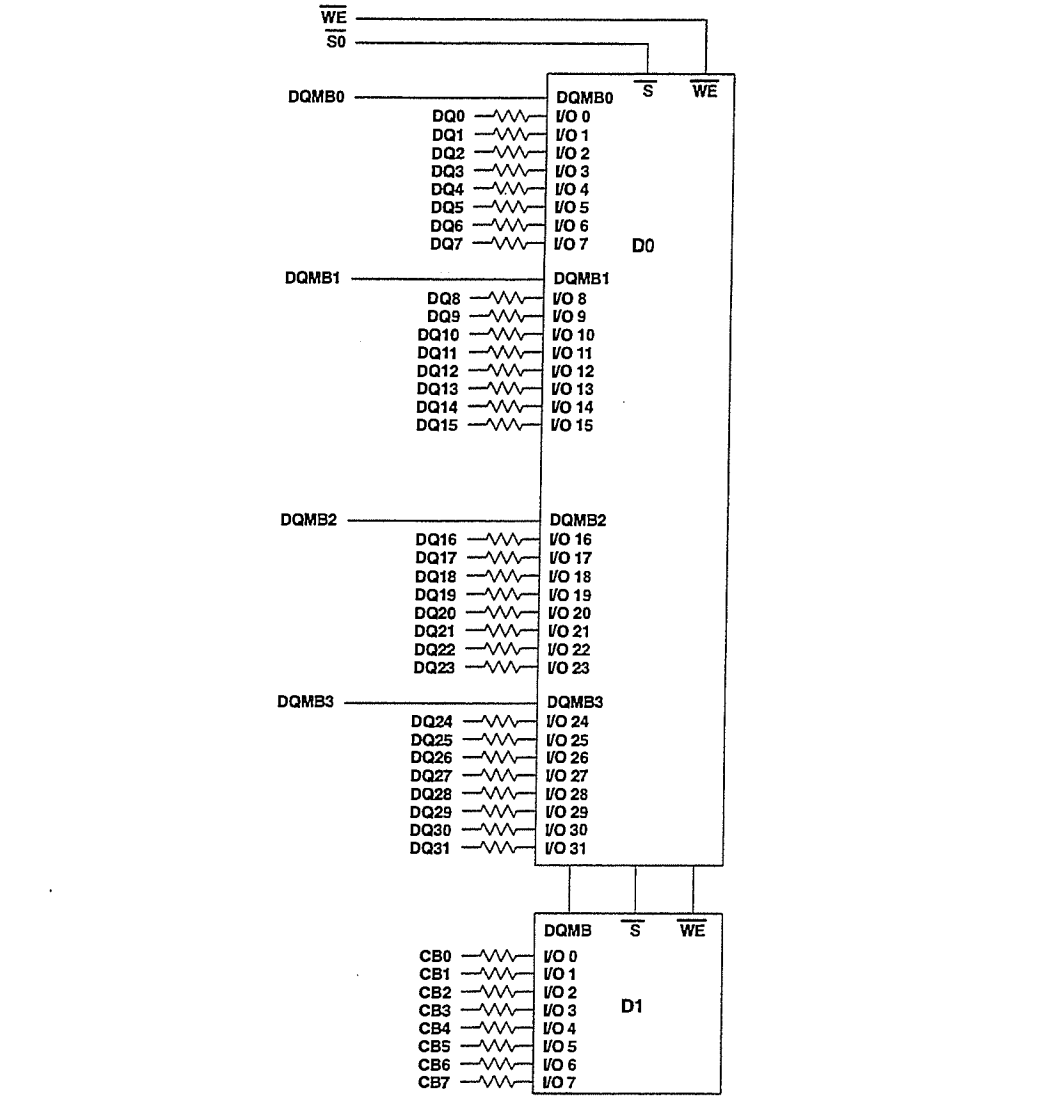


NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	3 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–V
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X8 & X16 SDRAMs



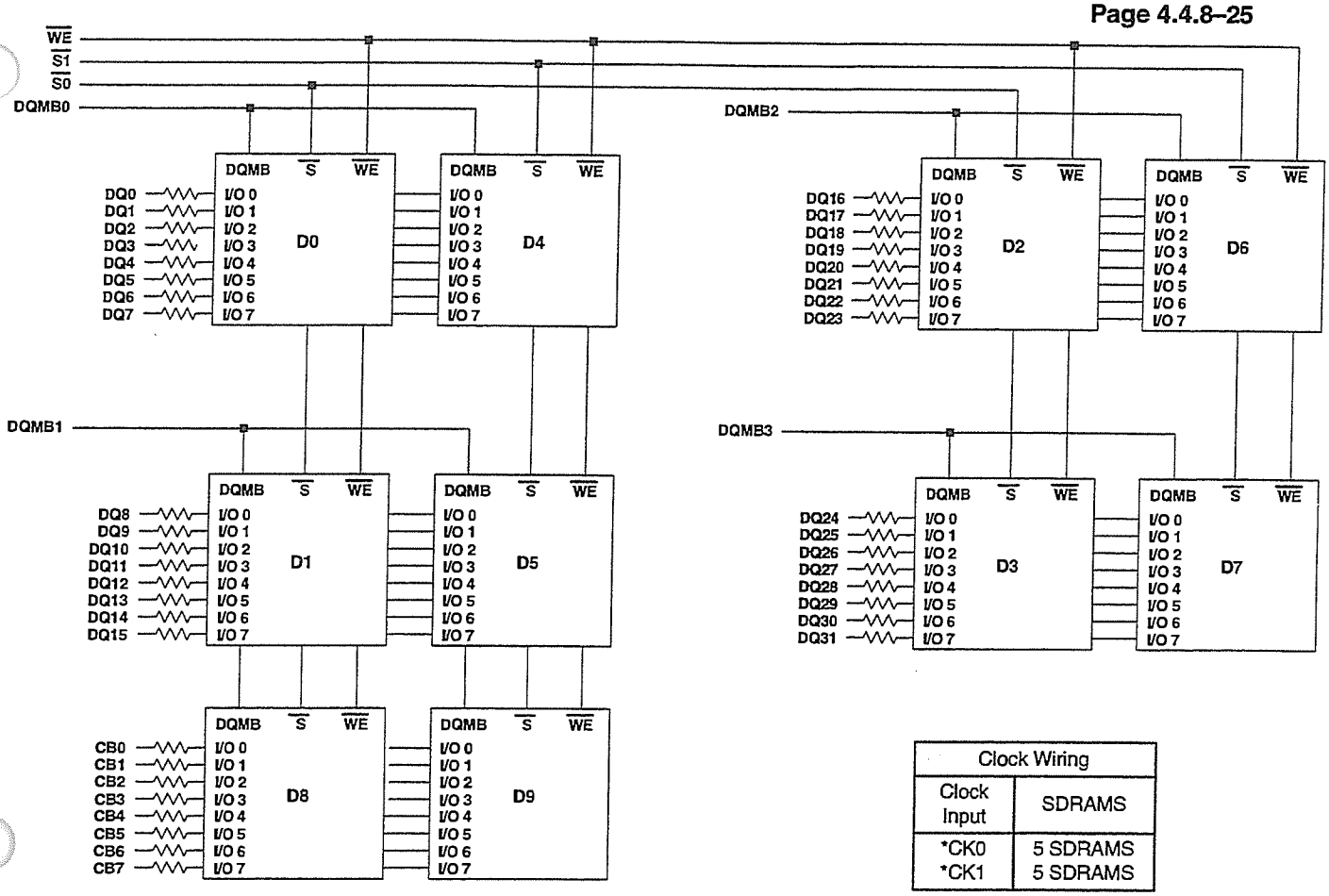
NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–W
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X8 & X32 SDRAMs

Release 7



Clock Wiring	
Clock Input	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

B0–BN → B0–BN: SDRAMS D0–D9
A0–AN → A0–AN: SDRAMS D0–D9
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D9
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D9
CKE0 → CKE: SDRAMS D0–D3, D8
CKE1 → CKE: SDRAMS D4–D7, D9

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

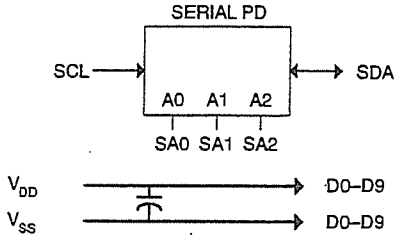
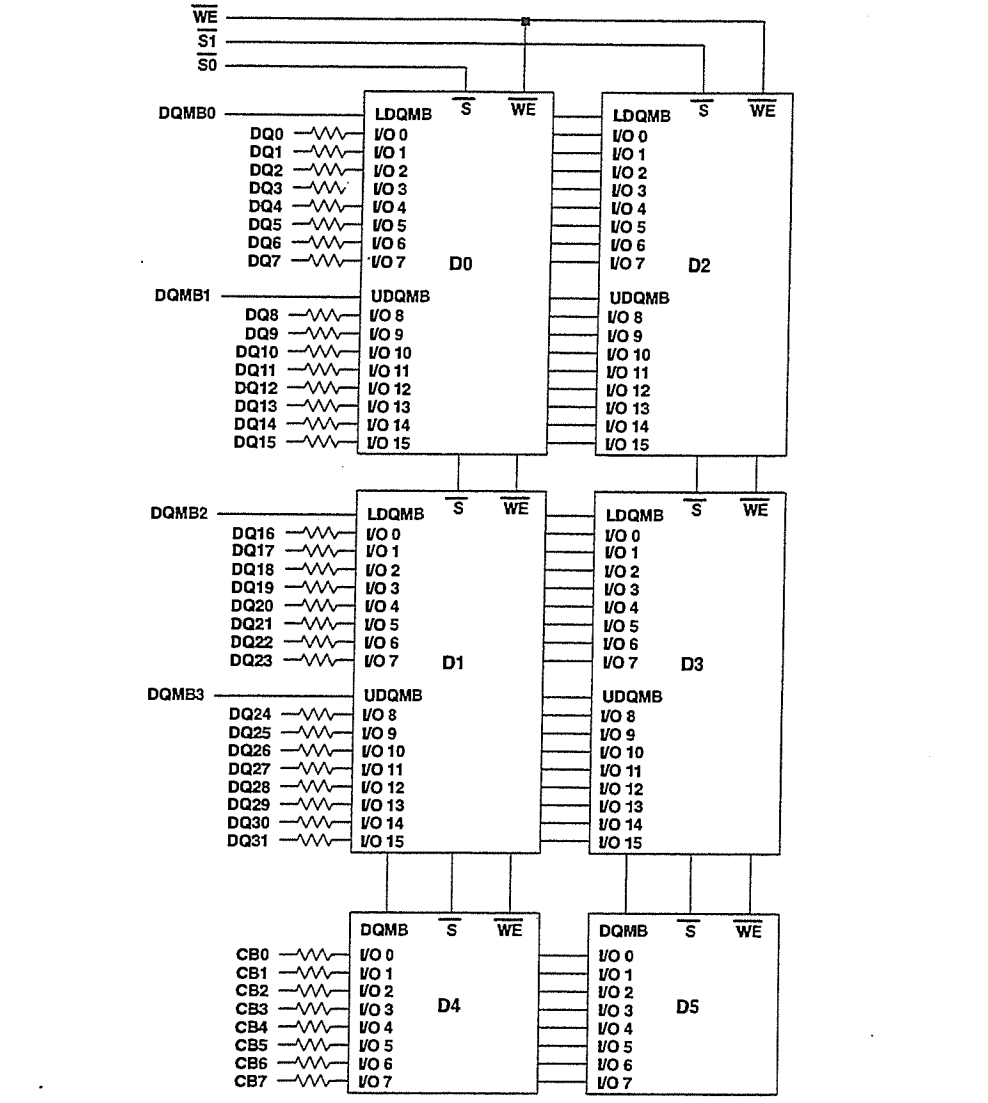


Figure 4.4.8–X
100 Pin X40 ECC SDRAM DIMM, 2 Bank with X8 SDRAMs

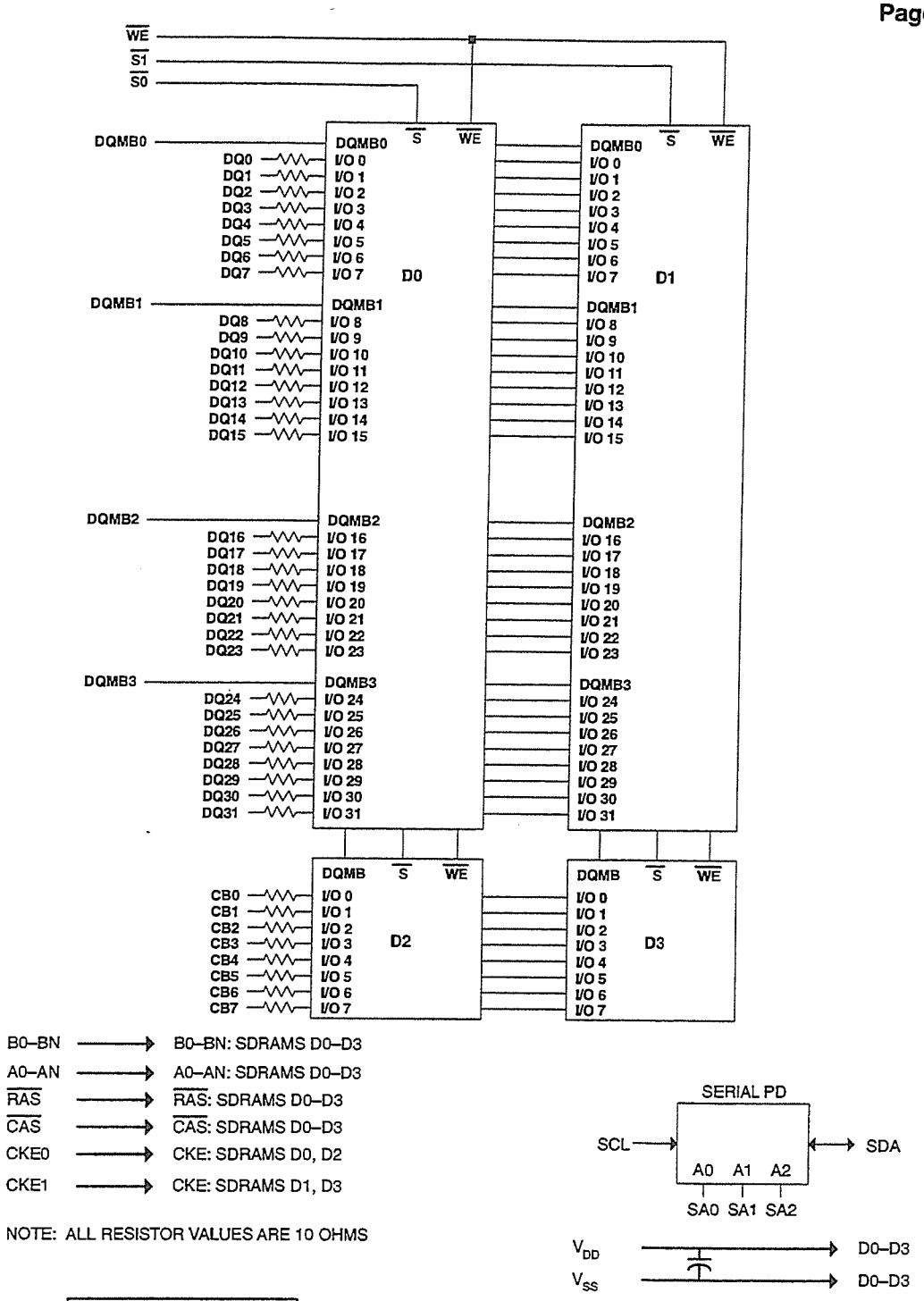


NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0	3 SDRAMS
*CK1	3 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–Y
100 Pin X40 ECC SDRAM DIMM, 2 Bank with X8 & X16 SDRAMs



Clock Wiring	
Clock Input	SDRAMS
*CK0	2 SDRAMS
*CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–Z
100 Pin X40 ECC SDRAM DIMM, 2 Bank with X8 & X32 SDRAMs

Release 7

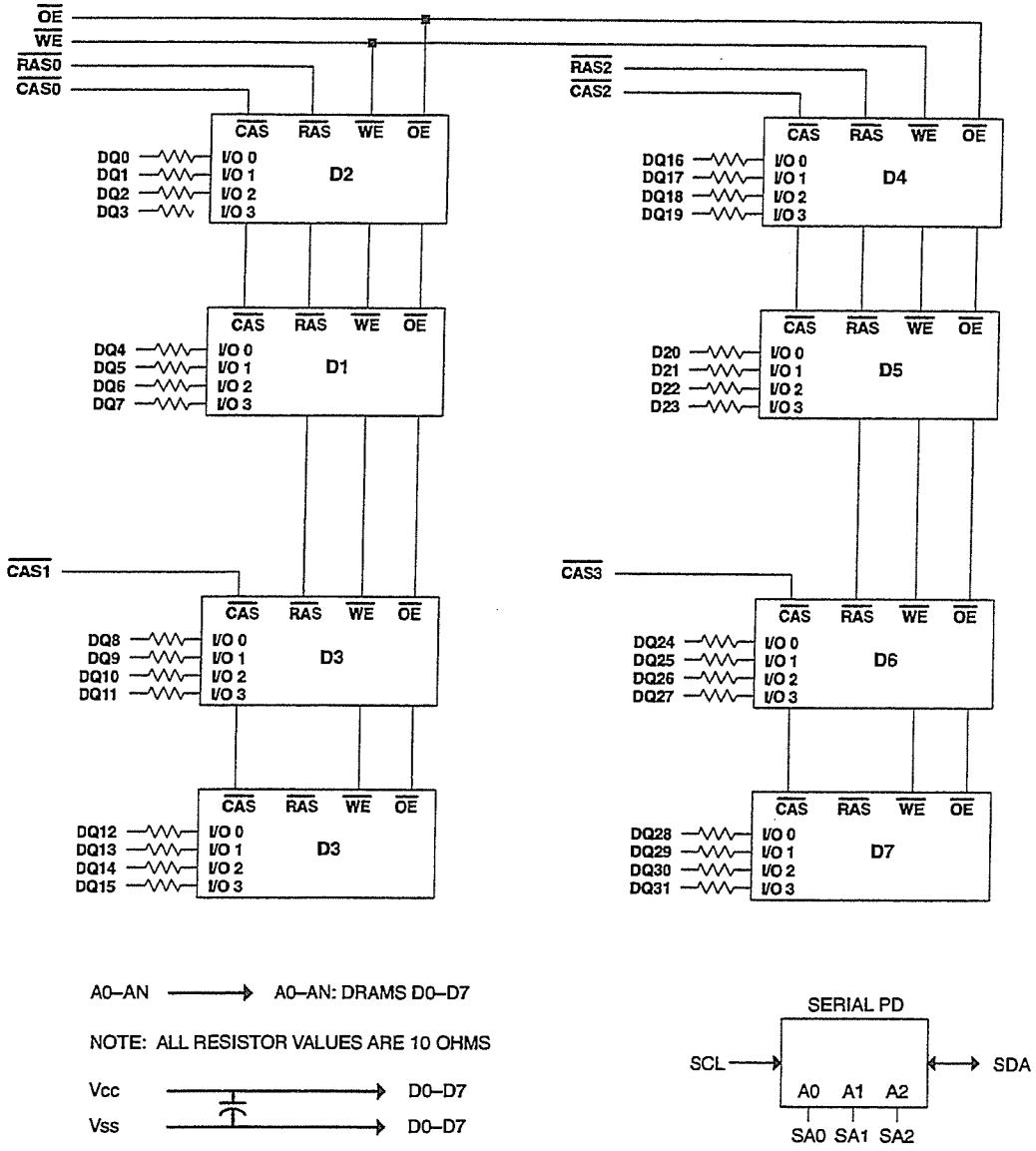


Figure 4.4.8–AA
100 Pin X32 DRAM DIMM, 1 Bank with X4 DRAMs

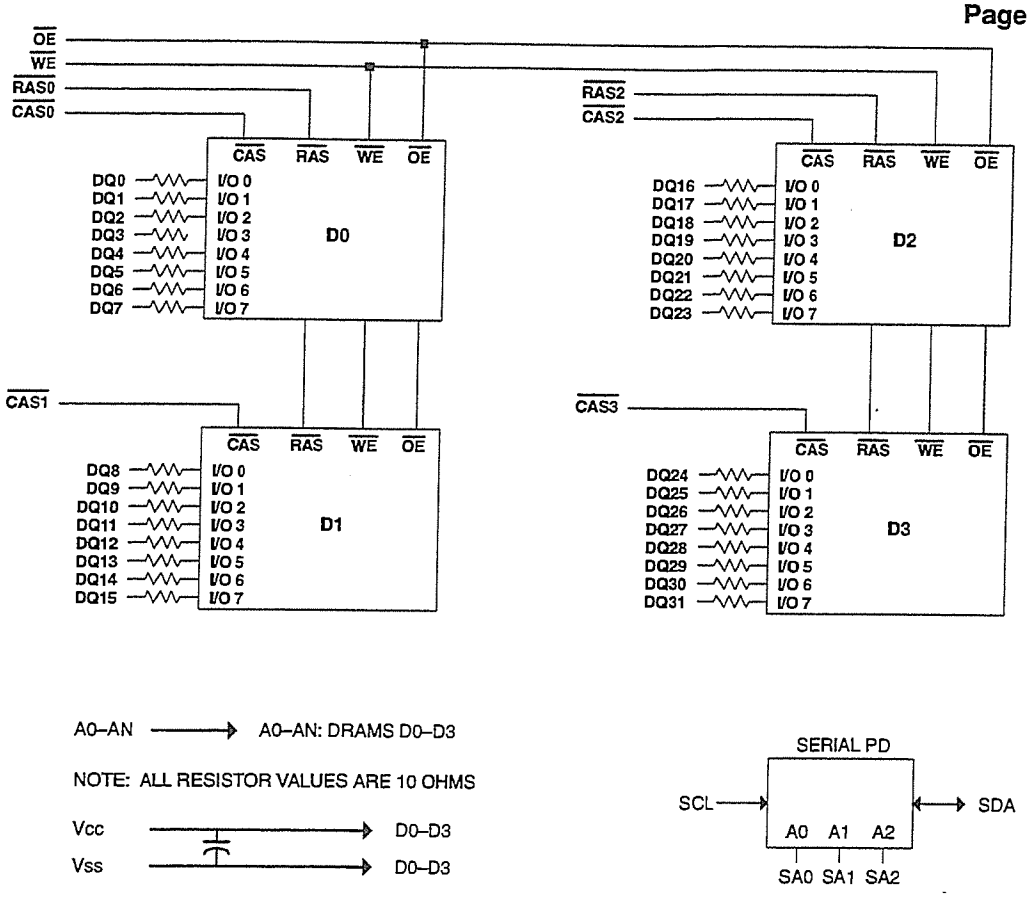


Figure 4.4.8–AB
100 Pin X32 DRAM DIMM, 1 Bank with X8 DRAMs

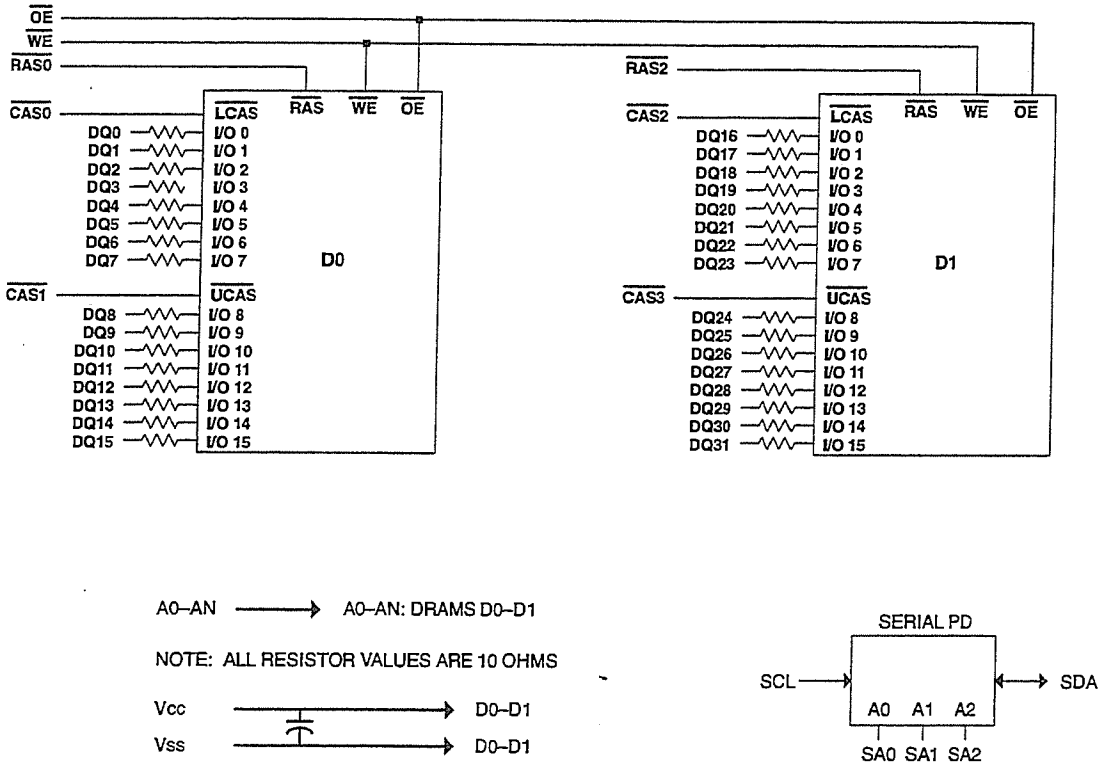


Figure 4.4.8–AC
100 Pin X32 DRAM DIMM, 1 Bank with X16 DRAMs

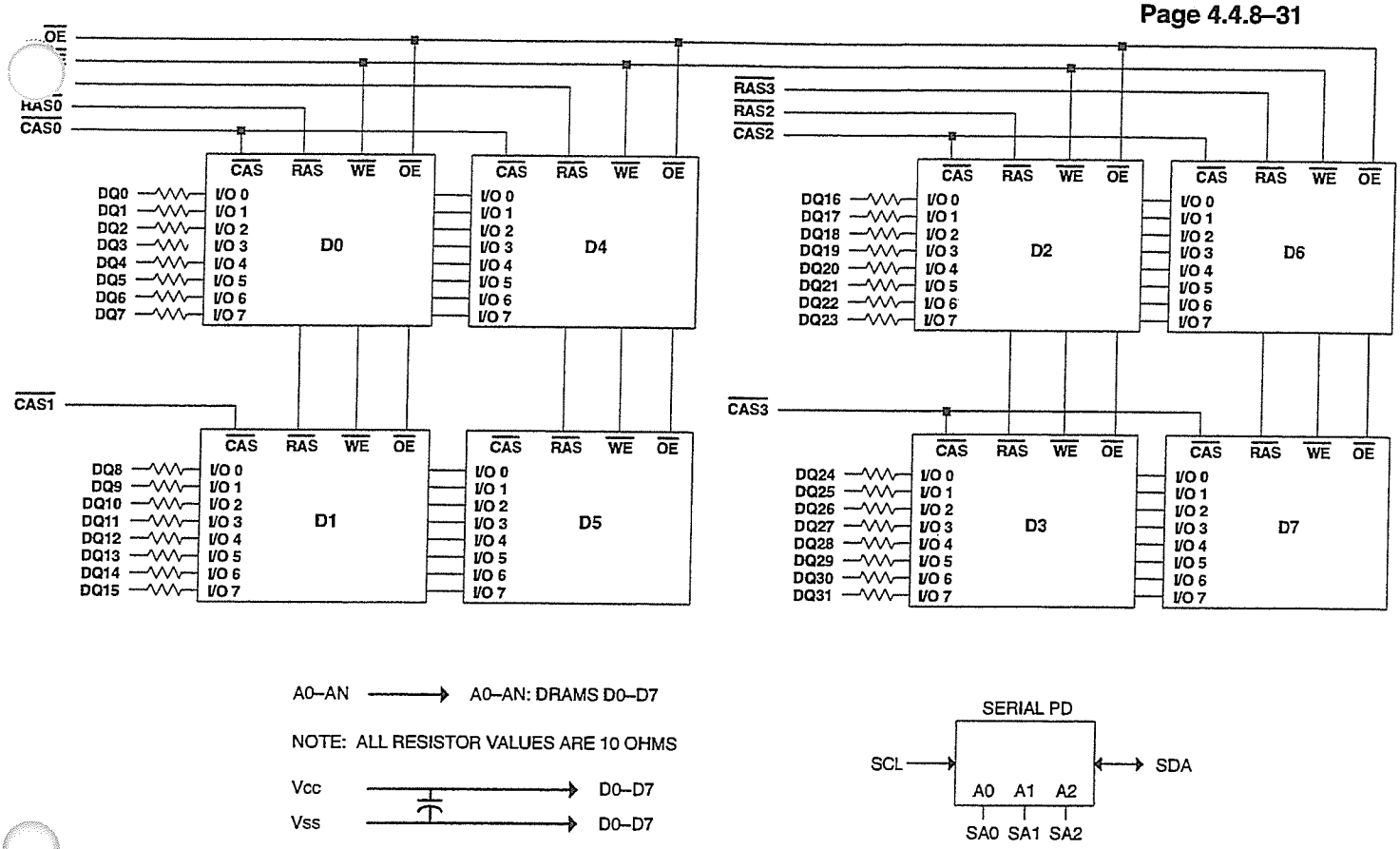


Figure 4.4.8–AD
100 Pin X32 DRAM DIMM, 2 Bank with X8 DRAMs

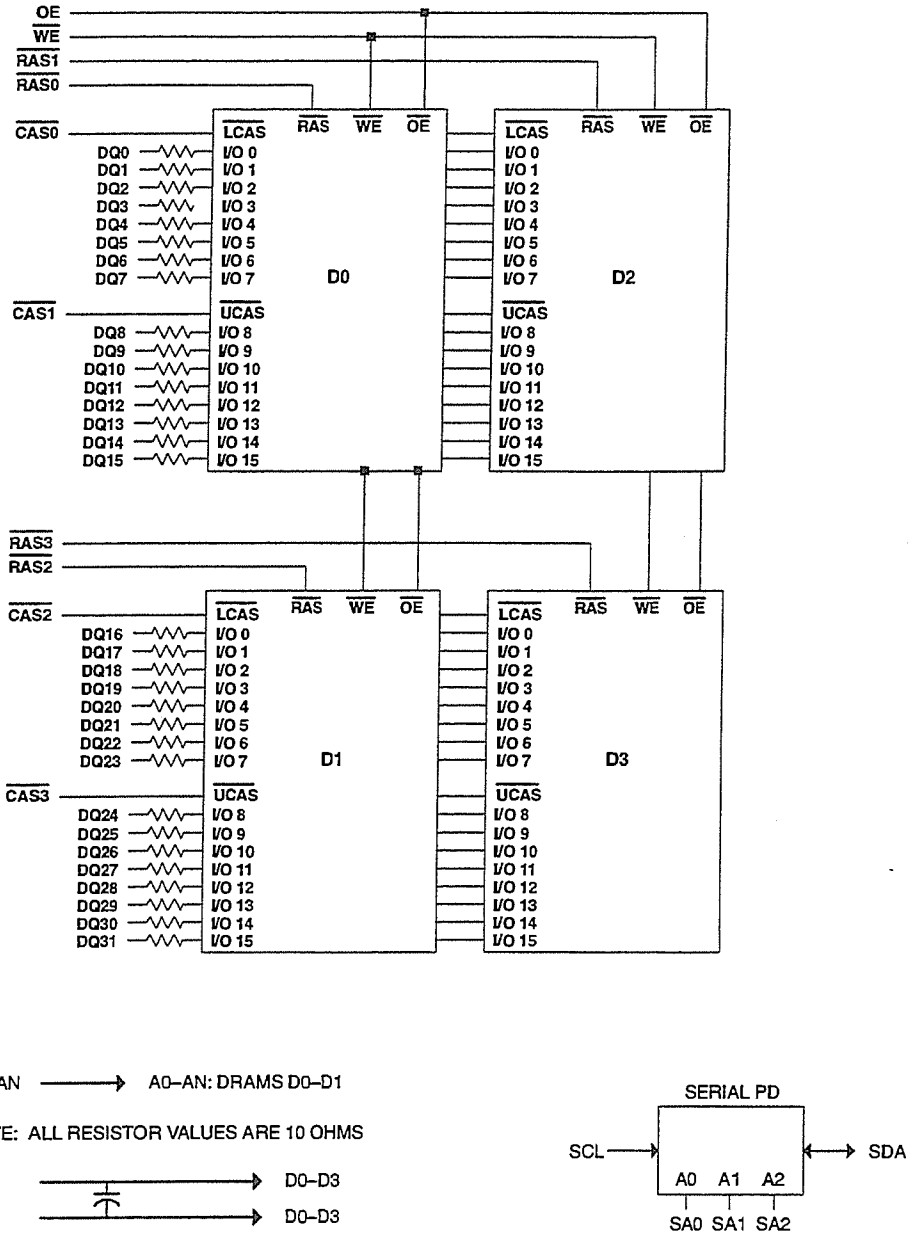


Figure 4.4.8–AE
100 Pin X32 DRAM DIMM, 2 Bank with X16 DRAMs

4.5 Eight Byte Memory Modules

4.5.1 – 168 PIN DRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS
DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES
CONFIGURATION—21 Different Configurations are defined using various combinationa of X1, X4, X8, X9, X16 and X18 memories including 2 bank configurations using X4 devices.
LOGIC FEATURES—The modules contain "PRESENCE DETECT" and "IDENTITY" featurs that conist of output pins in the PDn and IDn fields which supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS AND PD TABLES—Figs. 4.5.1–A, 4.5.1–B, & 4.5.1–C
CAPACITY / DEVICE CONFIGURATION TABLE—Fig. 4.5.1–D
CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.1–E through 4.5.1–AB

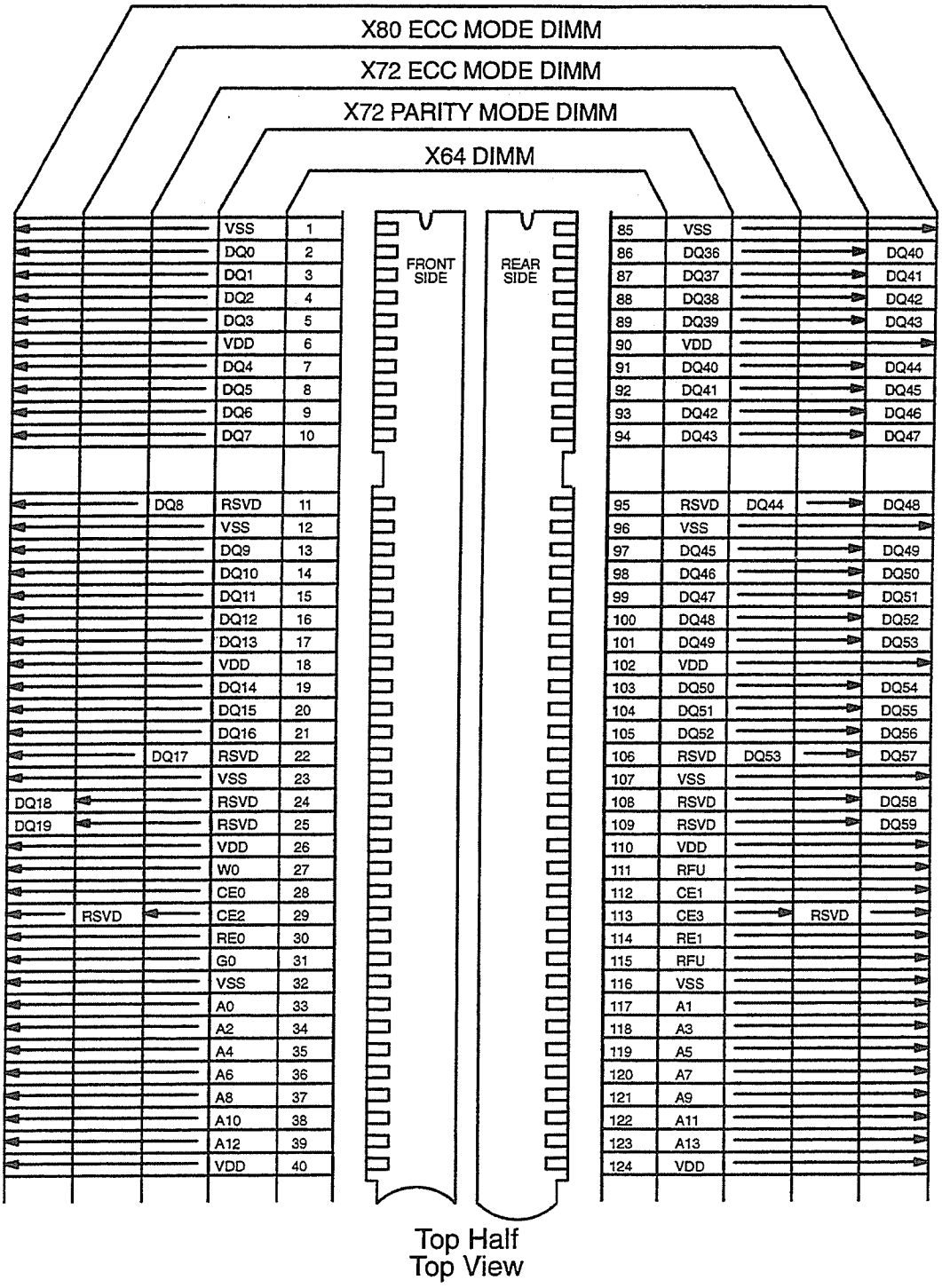


Figure 4.5.1–A
168 PIN, 64, 72, or 80 BIT DIMM PINOUT, TOP HALF

Release 4–7

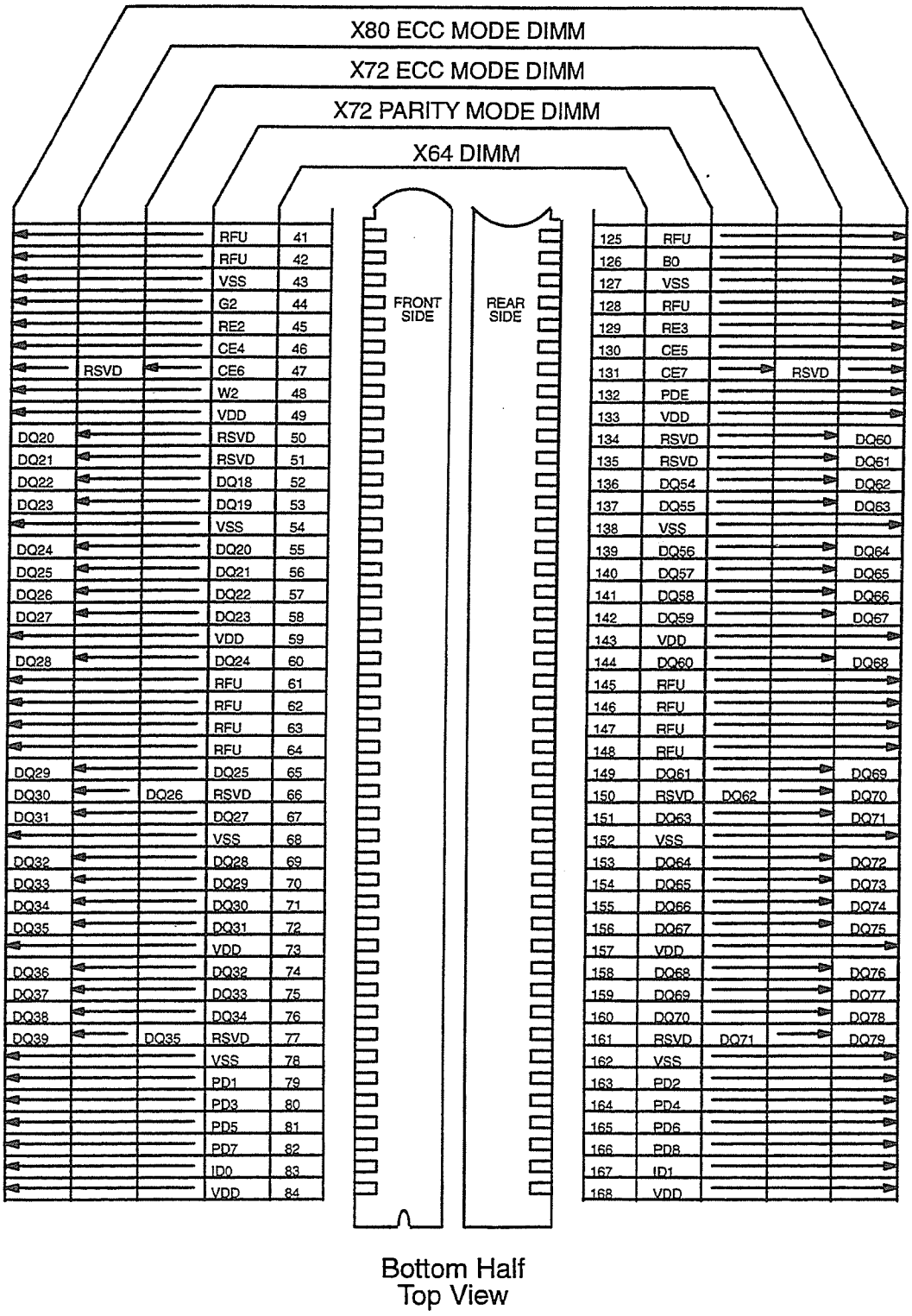


Figure 4.5.1–B
168 PIN, 64, 72, or 80 BIT DIMM PINOUT, BOTTOM HALF

PD 4	PD 3	PD 2	PD 1	DIMM CONFIGURATION (Parity, ECC)	# BANKS	DRAM CONFIGURATION	DRAM ROW ADDR.	DRAM COL. ADDR.	Av. REFRESH INTERVAL NORMAL (µS)	SLOW
0	0	0	0	256K X 64/72, 72	1	256K X 16/18	9	9	15.6	125
0	0	0	1	512K X 64/72, 72	2	256K X 16/18	9	9	15.6	125
0	0	1	0	512K X 64/72, 72/80	1	512K X 8/9	10	9	15.6	125
0	0	1	1	1M X 64/72, 72/80	2	512K X 8/9	10	9	15.6	125
0	1	0	0	1M X 64/72, 72/80	1	1M X 4/16/18	10	10#	15.6	125
0	1	0	1	2M X 64/72, 72/80	2	1M X 4/16/18	10	10#	15.6	125
0	1	1	0	1M X 64/72, 72	1	1M X 16/18	12	8	15.6	31.2
1	0	0	0	2M X 64/72, 72	2	1M X 16/18	12	8	15.6	31.2
1	0	0	1	2M X 64/72, 72/80	1	2M X 8	11	10	15.6	62.5
1	0	1	0	4M X 64/72, 72/80	2	2M X 8	11	10	15.6	62.5
1	0	1	1	4M X 72	1	4M X 1/4	12**	11**	15.6	31.2
1	0	1	1	4M X 64, 72/80	1	4M X 4/16	12/11	10/11	15.6	31.2/62.5
1	1	0	0	8M X 64/72, 72/80	2	4M X 4/16	12/11	10/11	15.6	31.2/62.5
1	1	0	1	8M X 64/72, 72/80	1	8M X 8	12	11	15.6	31.2
1	1	1	0	16M X 64/72, 72/80	2	8M X 8	12	11	15.6	31.2
1	1	1	1	16M X 64/72, 72/80	1	16M X 4	13/12	11/12	15.6	TBD/31.2
0	0	0	0	16M X 64/72, 72	1	16M X 16	13/12	11/12	15.6	TBD/31.2
0	0	0	1	32M X 64/72, 72/80	2	16M X 4/16	13/12	11/12	15.6	TBD/31.2
0	0	1	0	32M X 64/72, 72/80	1	32M X 8	14/13	11/12	7.8/15.6	TBD*
0	0	1	1	64M X 64/72, 72/80	2	32M X 8	14/13	11/12	7.8/15.6	TBD*
0	1	0	0	64M X 64/72, 72/80	1	64M X 4	14/13	12/13	7.8/15.6	TBD*
0	1	1	1	Expansion						

Note 1) * These modules using 256M devices are for reference only and will be further defined in the future.
Note 2) 1 = Logic high ; 0 = Logic low; In Table Information.
Note 3) ** This addressing includes a redundant address to allow mixing of 12/10(X4) and 11/11(X1) DRAMs
Note 4) # 1M X 16/18 DRAMS with 10/10 addressing may dissipate excessive power in many applications. Care must be taken to ensure device thermal limits are not exceeded. 12/8 addressing is provided as a lower power option.
PD Note: PD & ID terminals must each be pulled up through a resistor to VDD at the next higher level assembly. PDs will either be open or driven to VOH or driven to VOL via on–board buffer circuits.
ID Note: IDs will either be open (NC) or connected directly to VSS without a buffer.

	PD7	PD6
SPEED (tRAC)	82	165
80 ns	0	1
70 ns	1	0
60 ns	1	1
50 ns	0	0
40 ns	0	1
PD SPEED TABLE		

	PD8	ID0
CONFIGURATION	166	83
X64	1	0
X72 PARITY	1	1
X72 ECC	0	0
X80 ECC	0	1
DATA CONFIGURATION		

	ID1
REFRESH MODE	167
NORMAL	0
SELF–REFRESH	1
REFRESH MODE	

DATA ACCESS MODE	PD5 81
FAST PAGE	0
FP W/EDO	1
EDO DETECTION	

Figure 4.5.1–C
168 PIN, 64, 72, or 80 BIT DIMM PRESENCE DETECT & CONFIGURATION TABLES

64, 72, & 80 BIT DRAM DIMM CAPACITY IN M BYTE																				
Memory Device / DIMM Configuration	4M DRAM					16M DRAM					64M DRAM					256M DRAM				
	256K		512K		1M	1M		2M		4M	4M		8M		16M	16M		32M		64M
	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4
256K X 64		4																		
256K X 72	4																			
256K X 72 (ECC)	4																			
256K X 80 (ECC)																				
512 X 64		8		8																
512K X 72	8		8																	
512K X 72 (ECC)	8		8	9																
512K X 80 (ECC)				10																
1M X 64				16	16		4													
1M X 72			16		18	4														
1M X 72 (ECC)			16	18	18	4														
1M X 80 (ECC)				20	20															
2M X 64							8		8											
2M X 72						8		8												
2M X 72 (ECC)						8		8	9											
2M X 80 (ECC)									10											
4M X 64									16	16		4								
4M X 72								16		18	4									
4M X 72 (ECC)								16	18	18	4									
4M X 80 (ECC)									20	20										
8M X 64												8		8						
8M X 72											8		8							
8M X 72 (ECC)											8		8	9						
8M X 80 (ECC)														10						
16M X 64														16	16		4			
16M X 72													16		18	4				
16M X 72 (ECC)													16	18	18	4				
16M X 80 (ECC)														20	20					
32M X 64																	8		8	
32M X 72																8		8		
32M X 72 (ECC)																8		8	9	
32M X 80 (ECC)																			10	
64M X 64																			16	16
64M X 72																		16		18
64M X 72 (ECC)																		16	18	18
64M X 80 (ECC)																			20	20

Figure 4.5.1–D
168 PIN, 64, 72, & 80 BIT DRAM DIMM Capacity Table

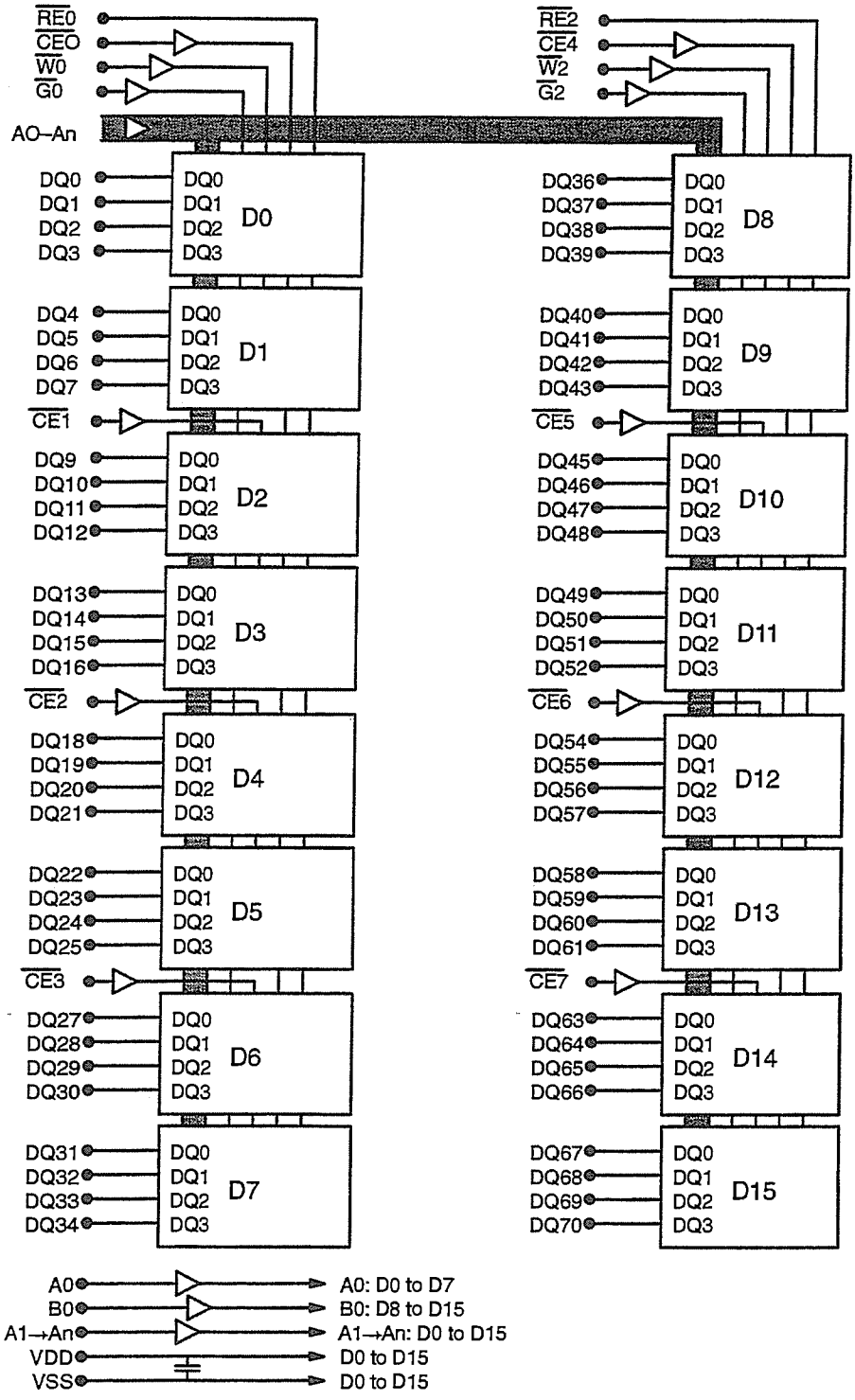


Figure 4.5.1–E
168 PIN, X64 DRAM DIMM, 1 bank with X4 DRAMs

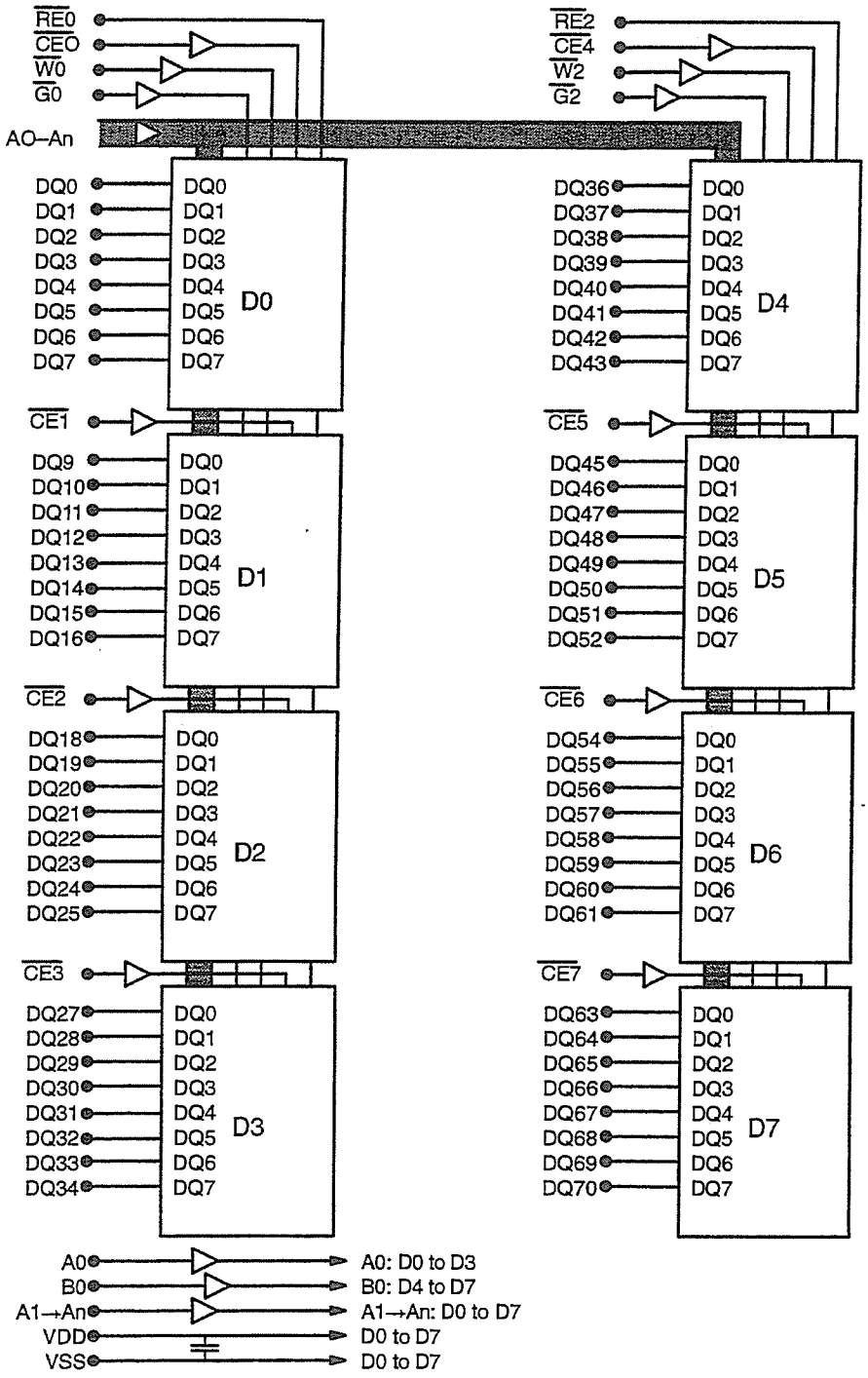


Figure 4.5.1–F
168 PIN, X64 DRAM DIMM, 1 bank with X8 DRAMs

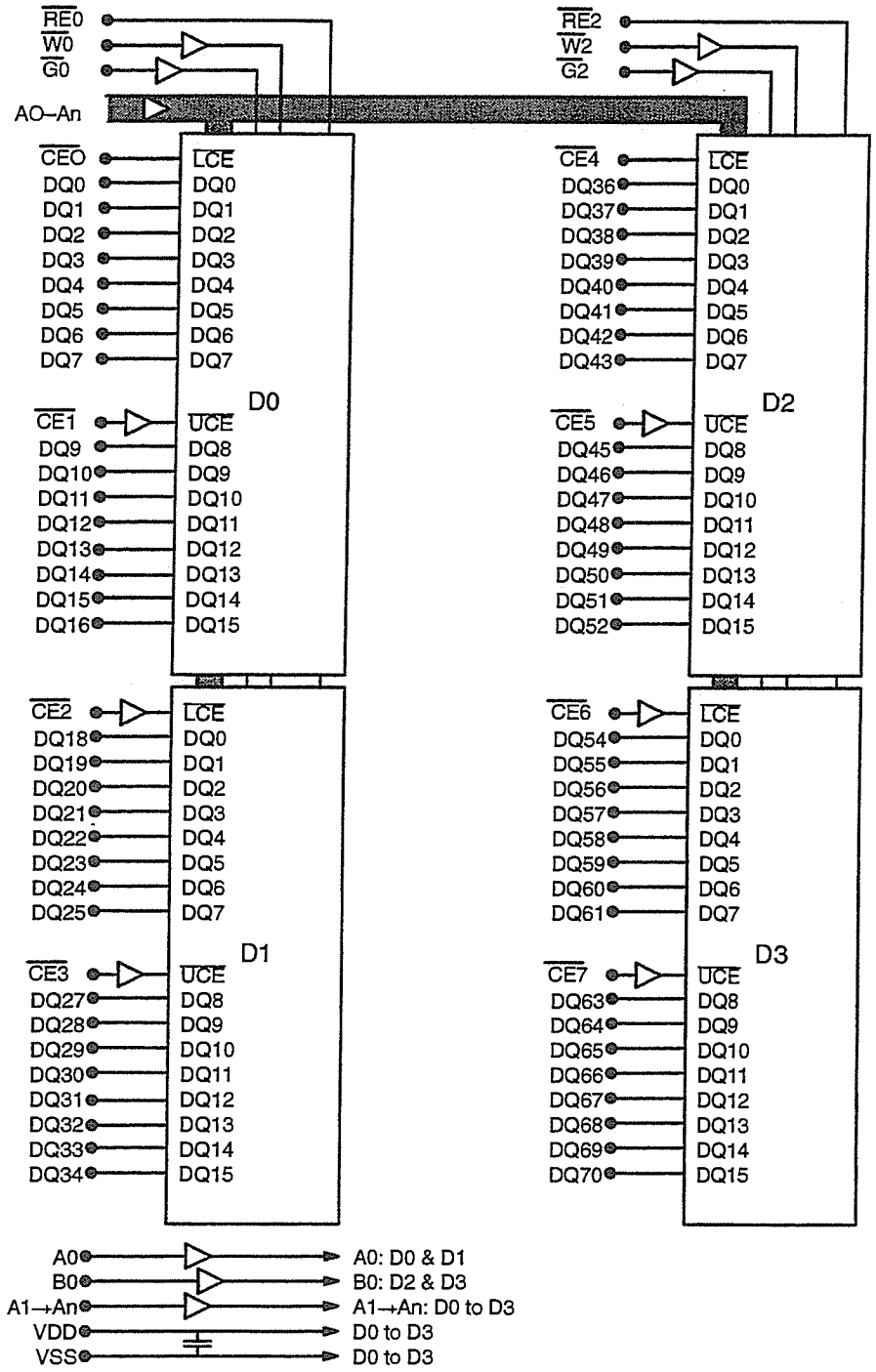


Figure 4.5.1–G
168 PIN, X64 DRAM DIMM, 1 bank with X16 DRAMs

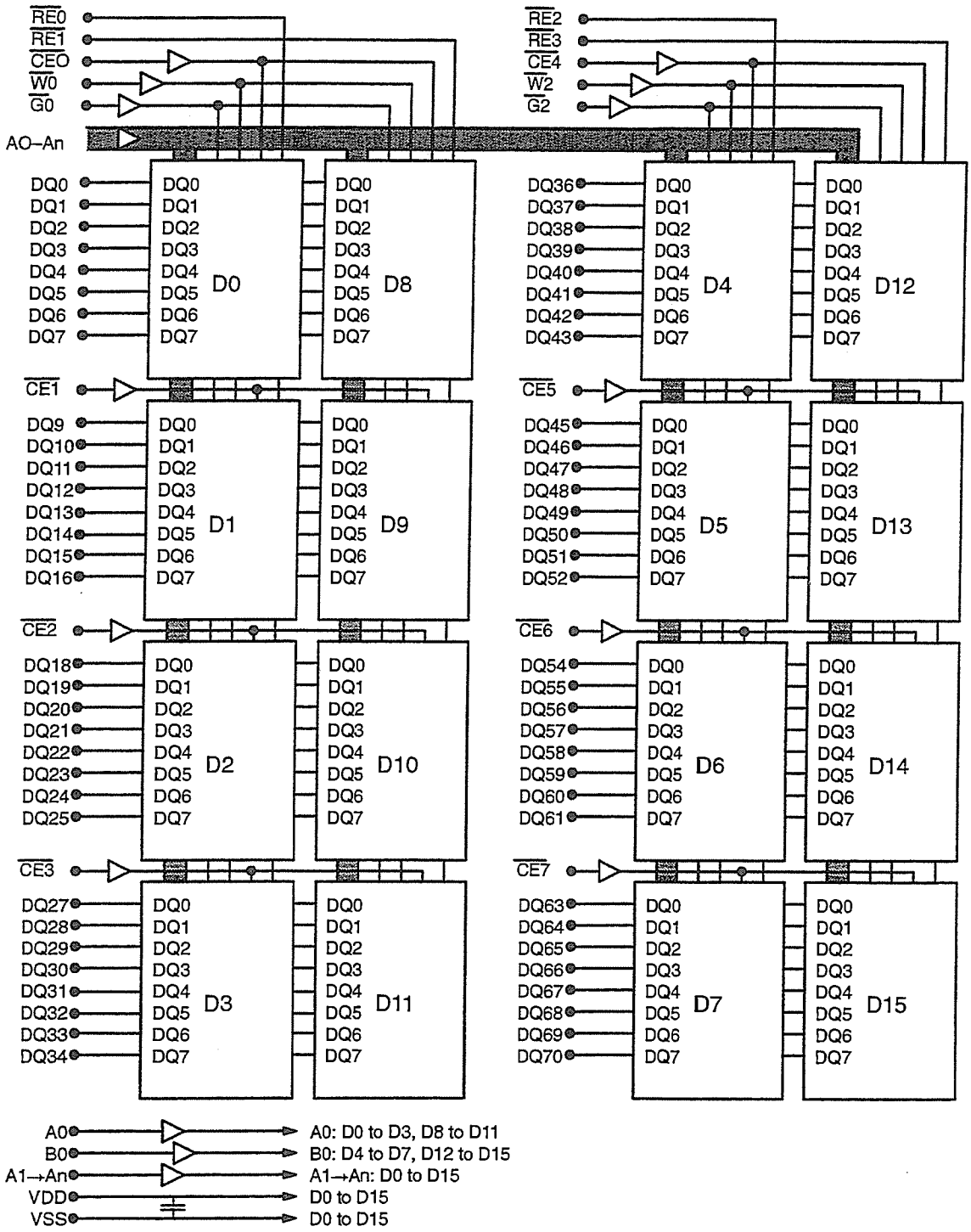


Figure 4.5.1–H
168 PIN, X64 DRAM DIMM, 2 banks with X8 DRAMs

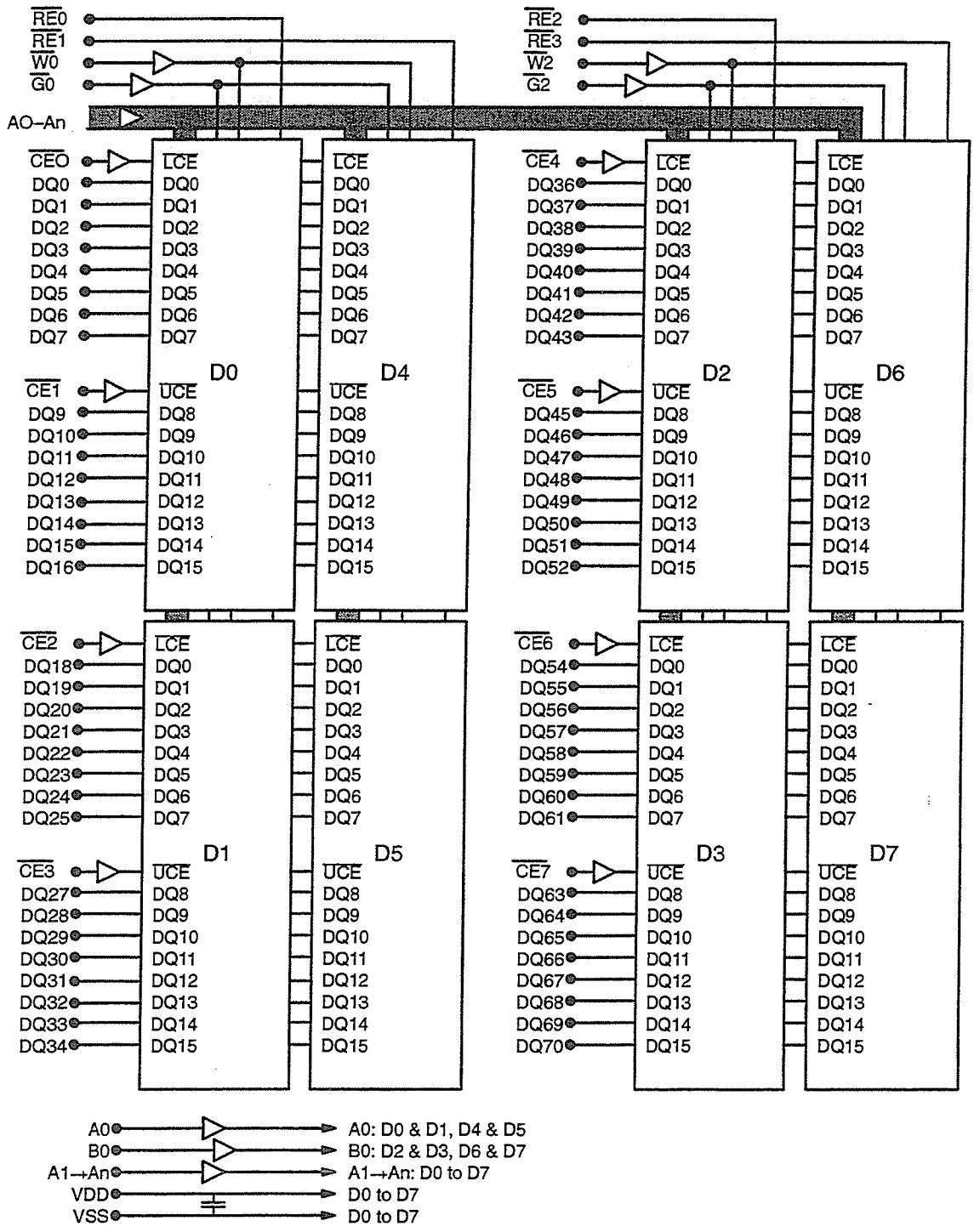


Figure 4.5.1–I
168 PIN, X64 DRAM DIMM, 2 banks with X16 DRAMs
Release 4c7

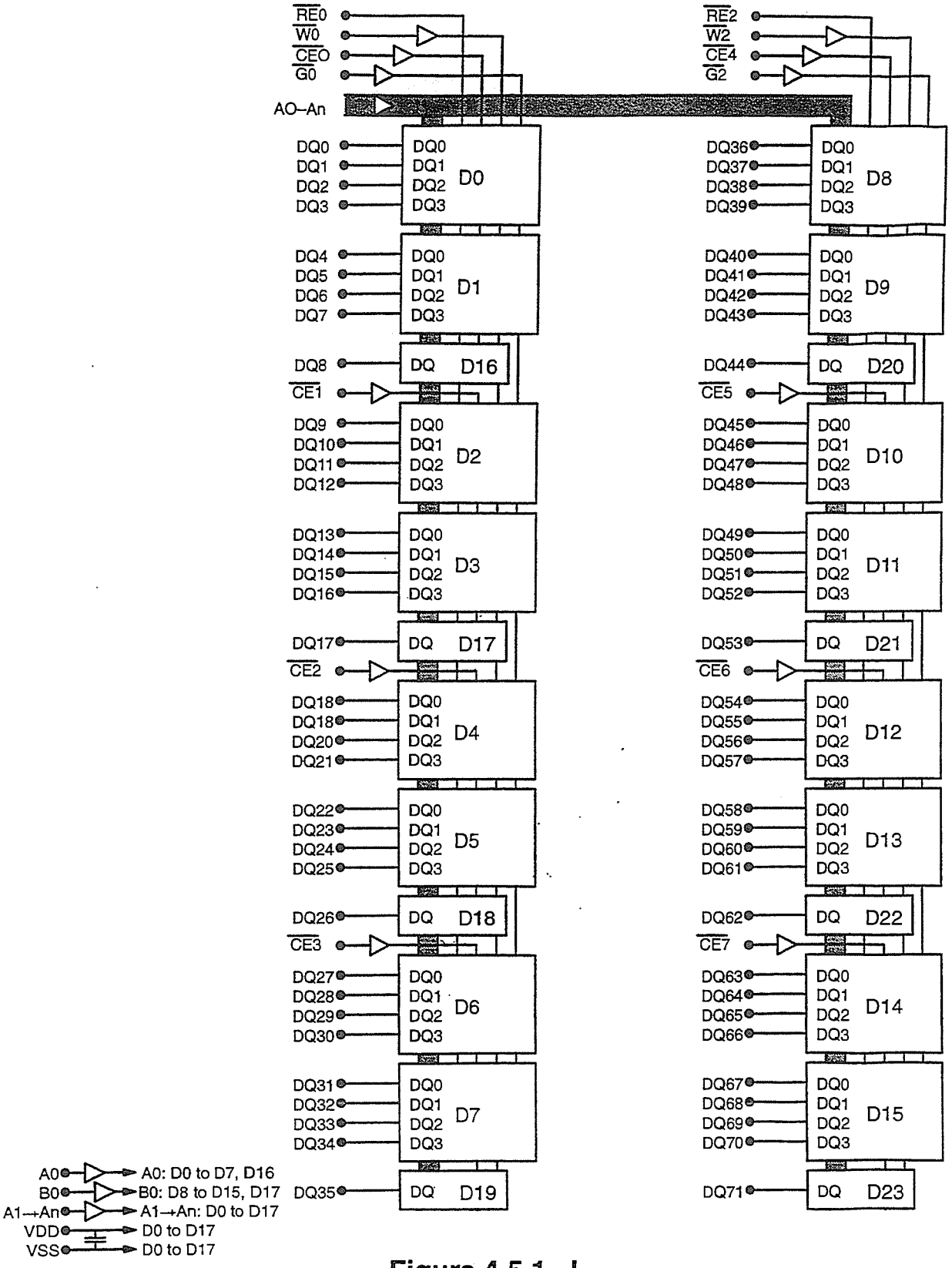


Figure 4.5.1–J

168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X4 & X1 DRAMs

Release 4c7

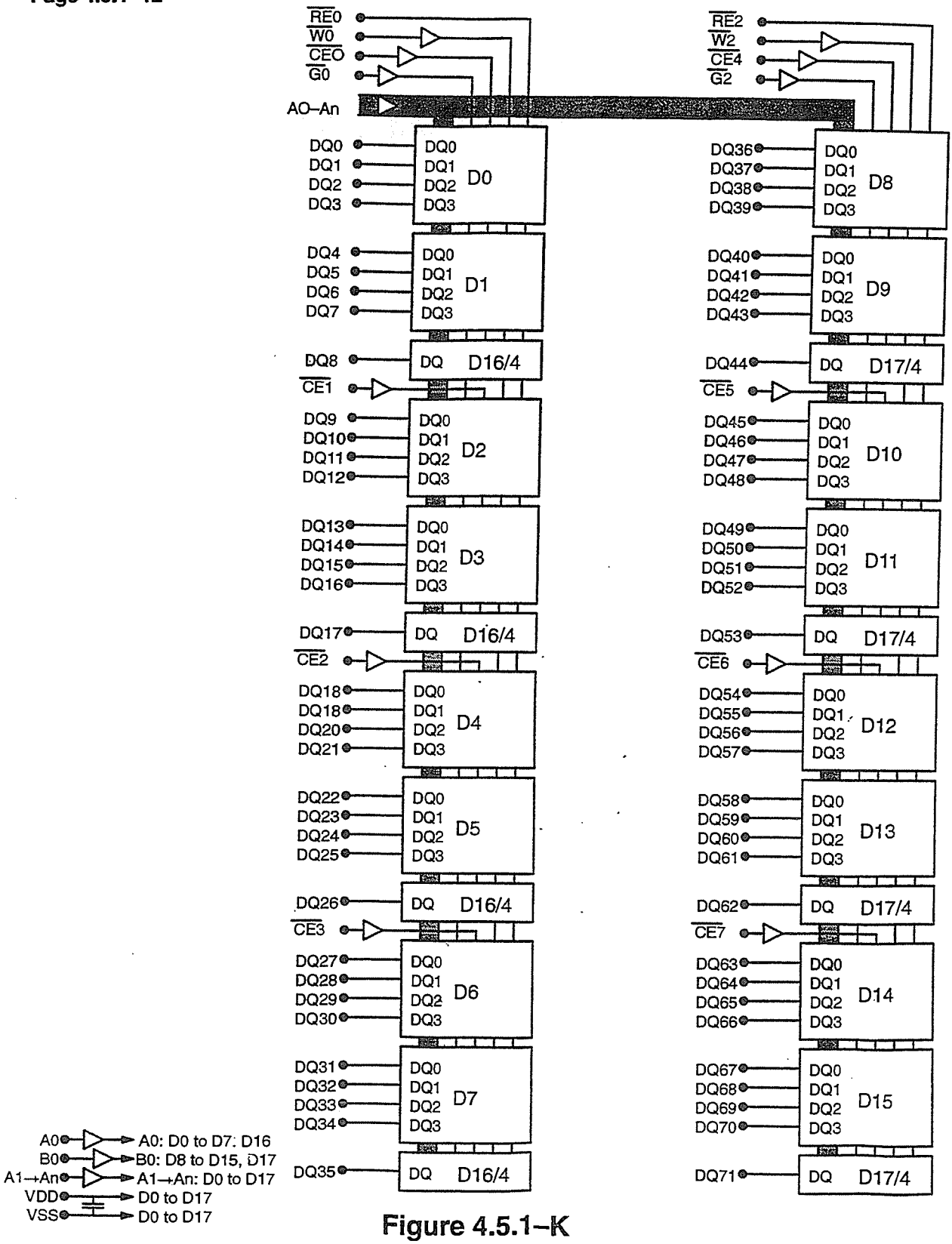


Figure 4.5.1–K
168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X4 & X4 W/4 $\overline{CE}$ DRAMs

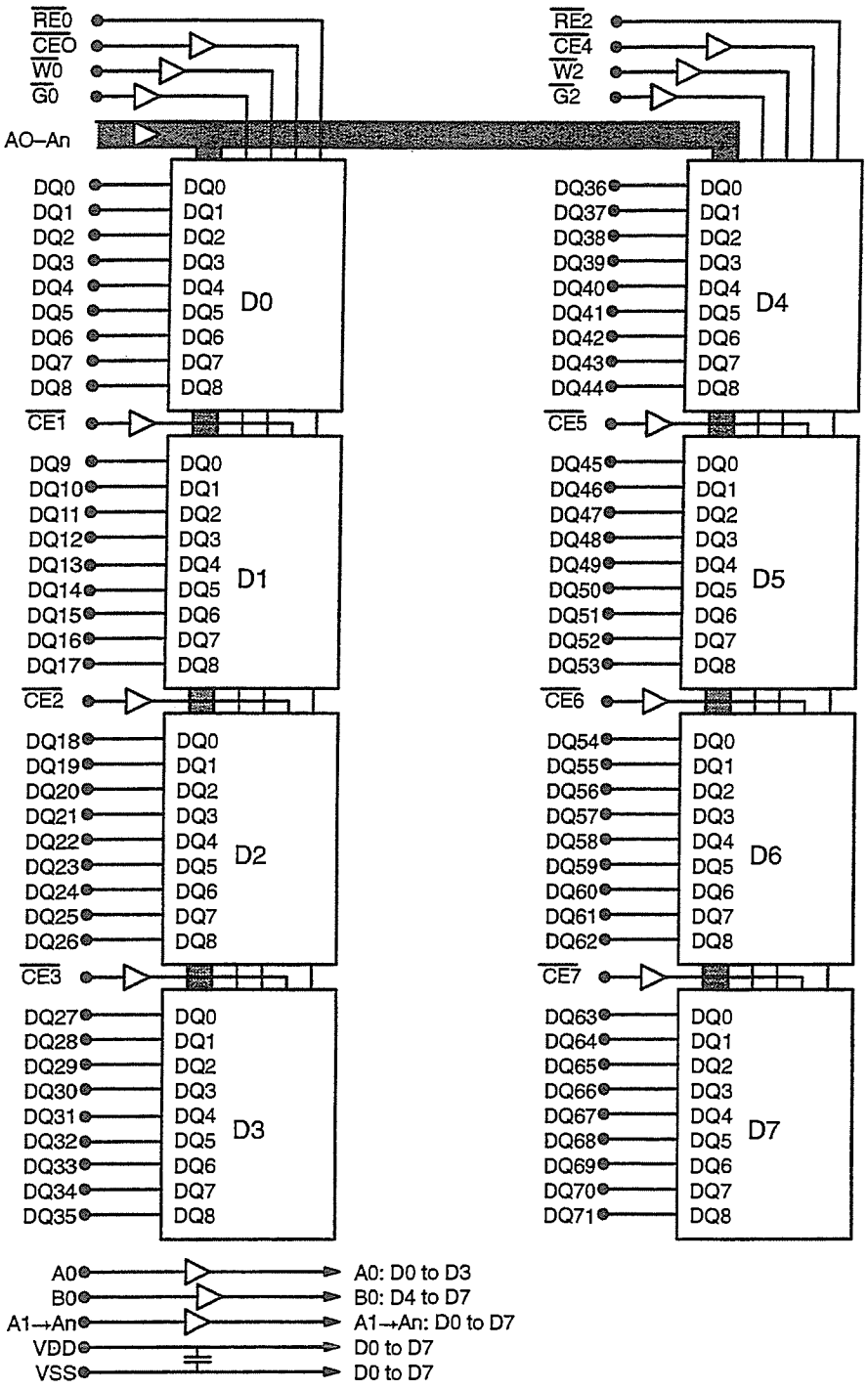


Figure 4.5.1–L
168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X9 DRAMs

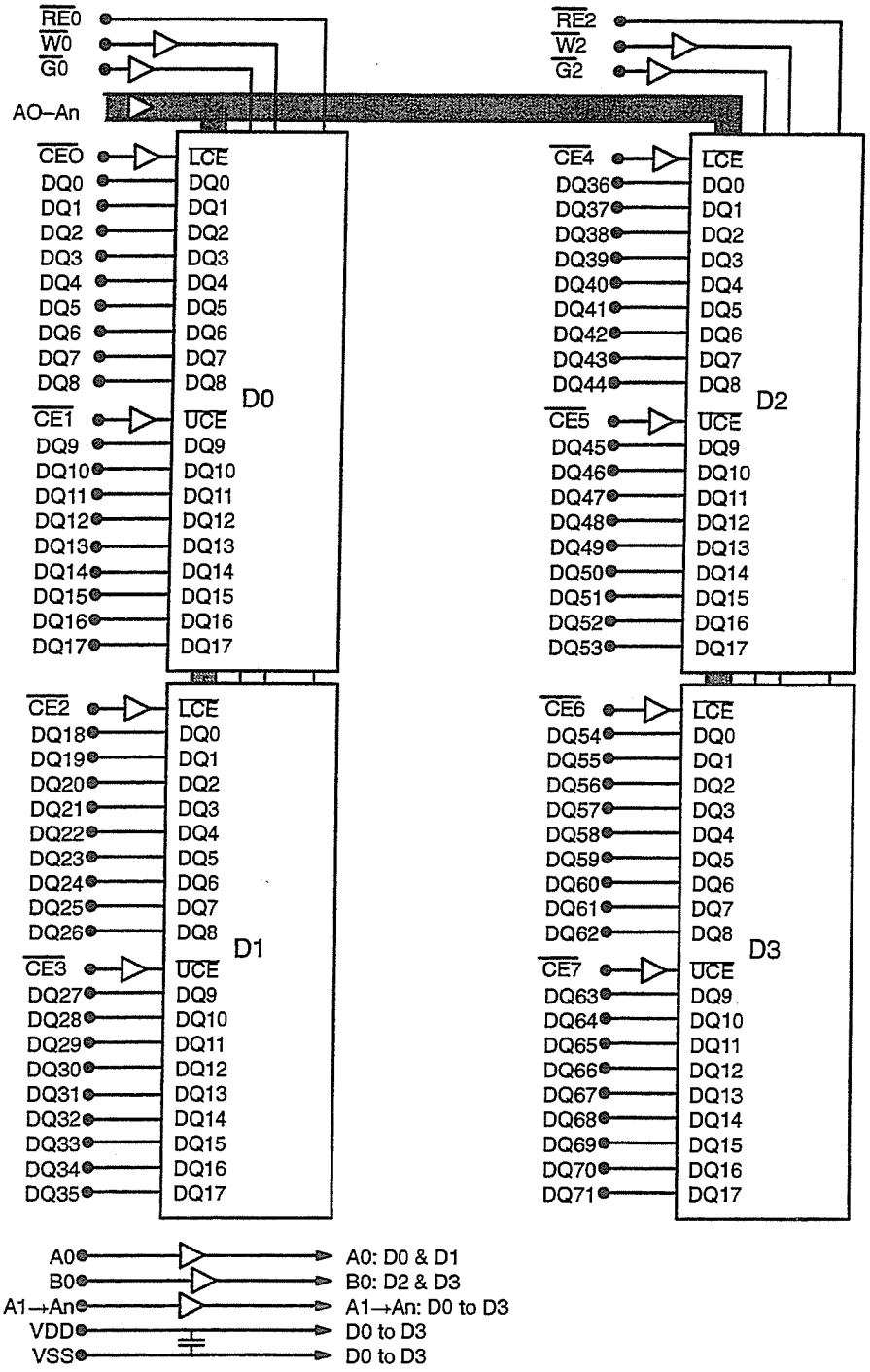


Figure 4.5.1–M
168 PIN, X72 (Parity mode) DRAM DIMM, 1 bank with X18 DRAMs
Release 4c7

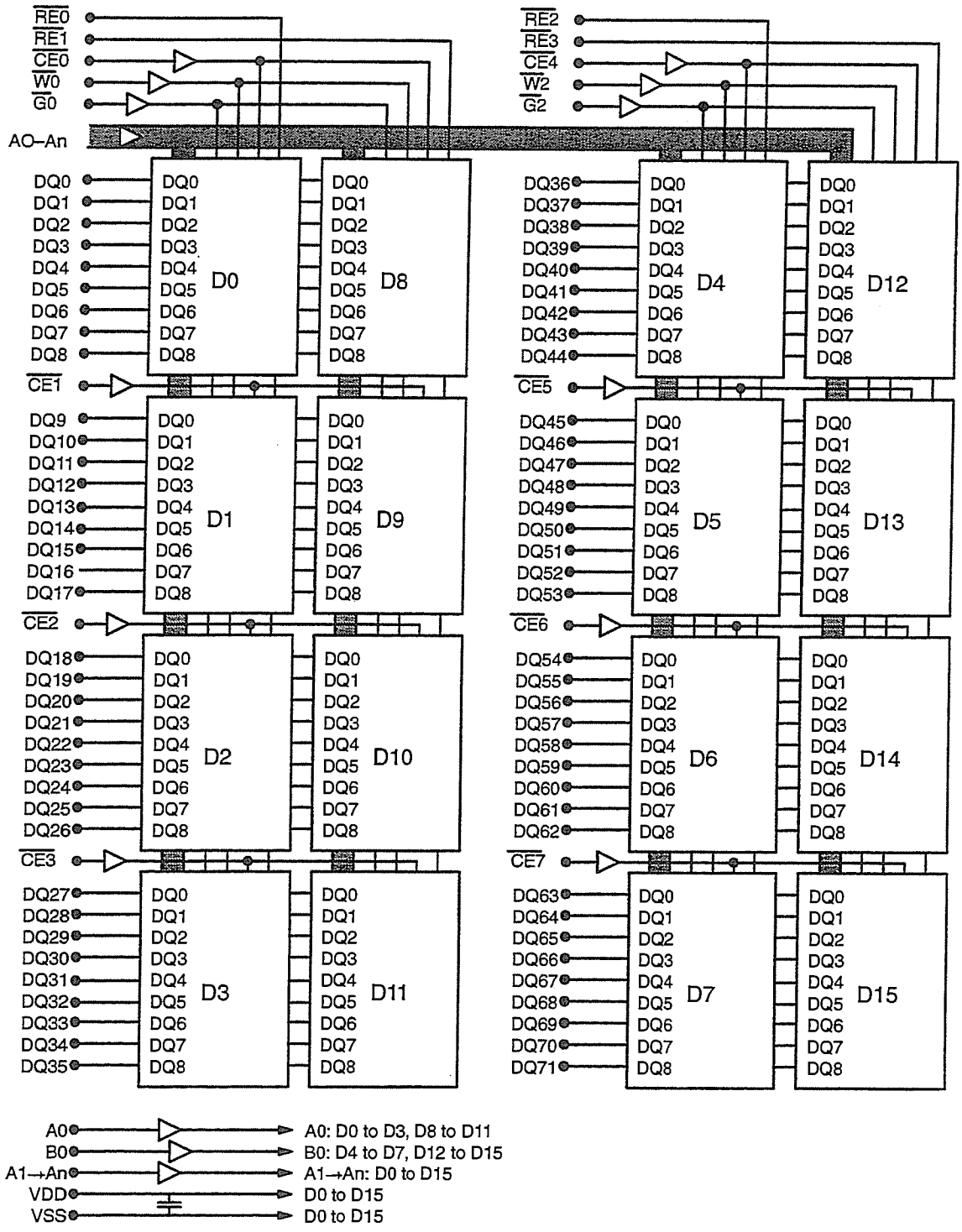


Figure 4.5.1–N
168 PIN, X72 (Parity mode) DRAM DIMM, 2 banks with X9 DRAMs

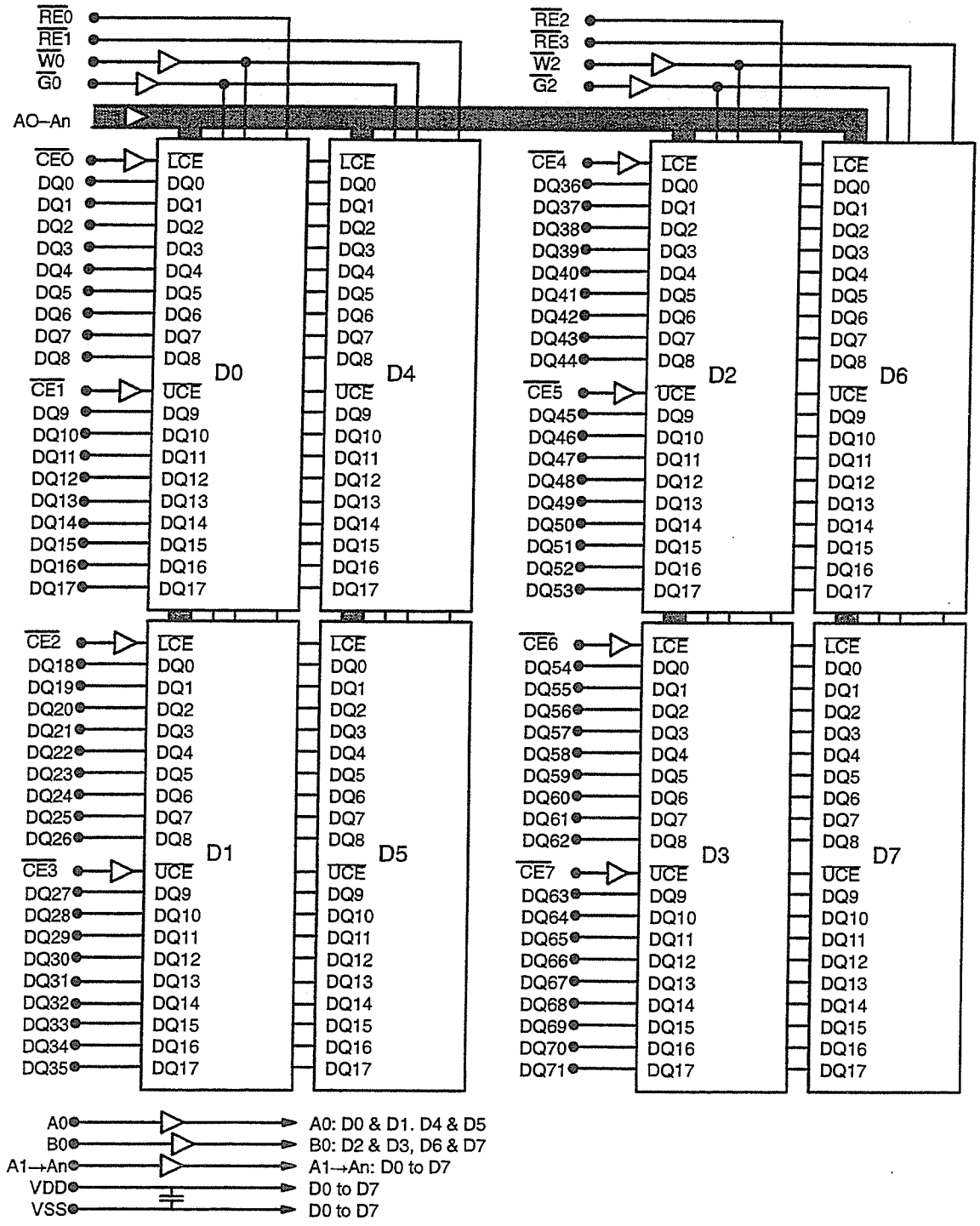


Figure 4.5.1–O
168 PIN, X72 (Parity mode) DRAM DIMM, 2 bank with X18 DRAMs

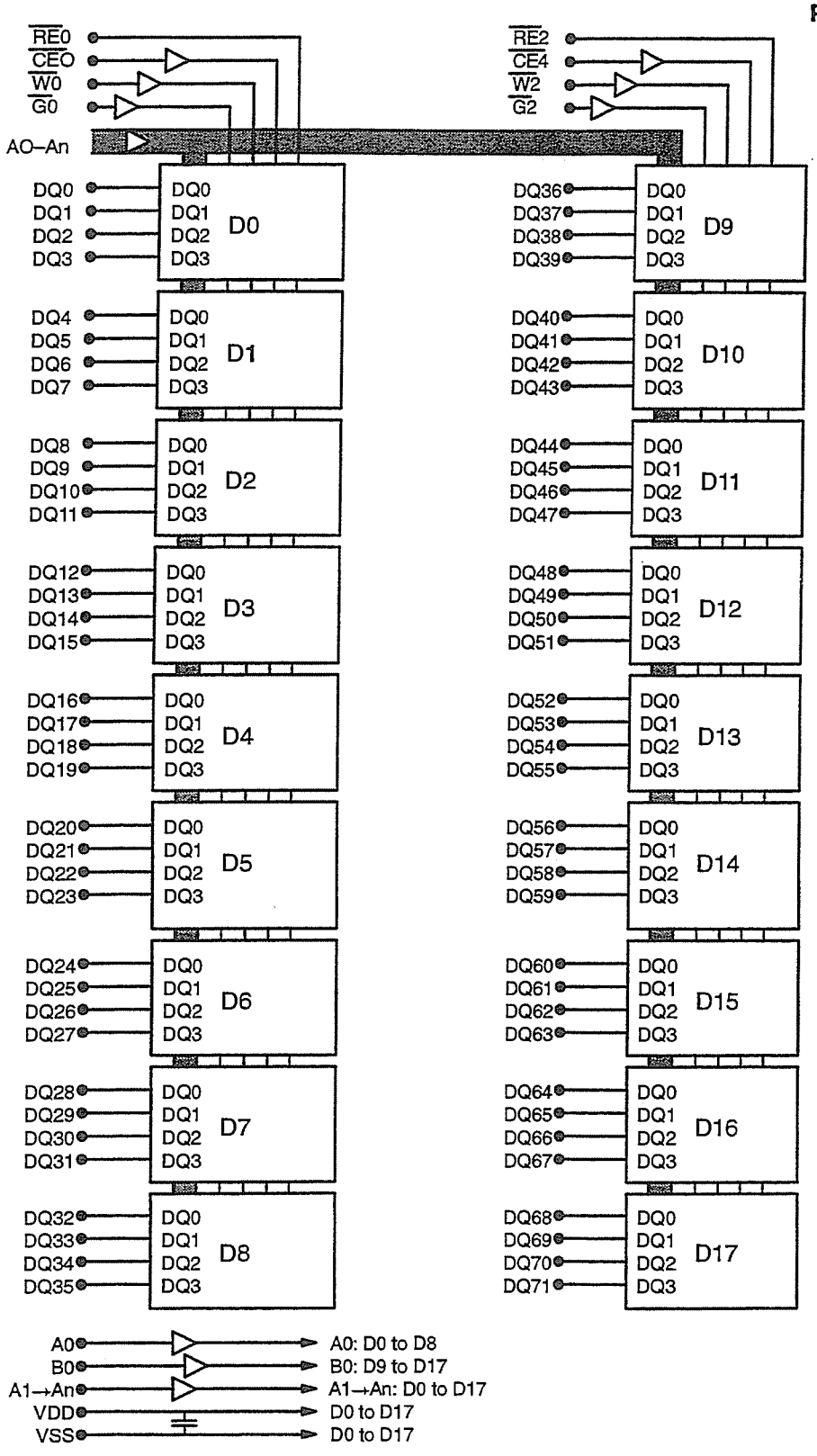
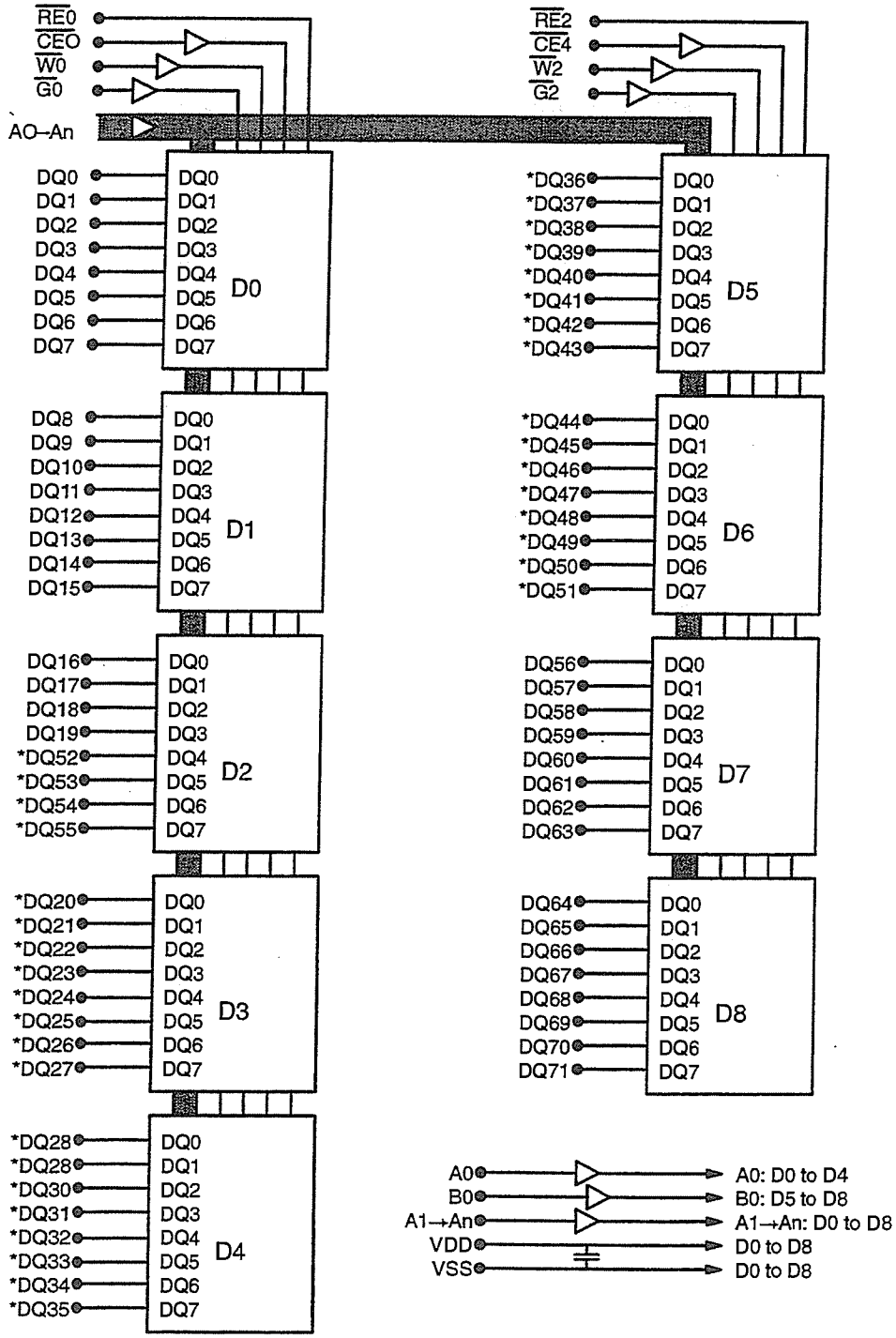


Figure 4.5.1–P
168 PIN, X 72 (ECC mode) DRAM DIMM, 1 bank with X4 DRAMs
Release 4c7



* Note: The location of data pins DQ–20 through DQ–55 have been changed in Release 7

Figure 4.5.1–Q
168 PIN, X72 (ECC mode) DRAM DIMM, 1 bank with X8 DRAMs

Release 4–r7

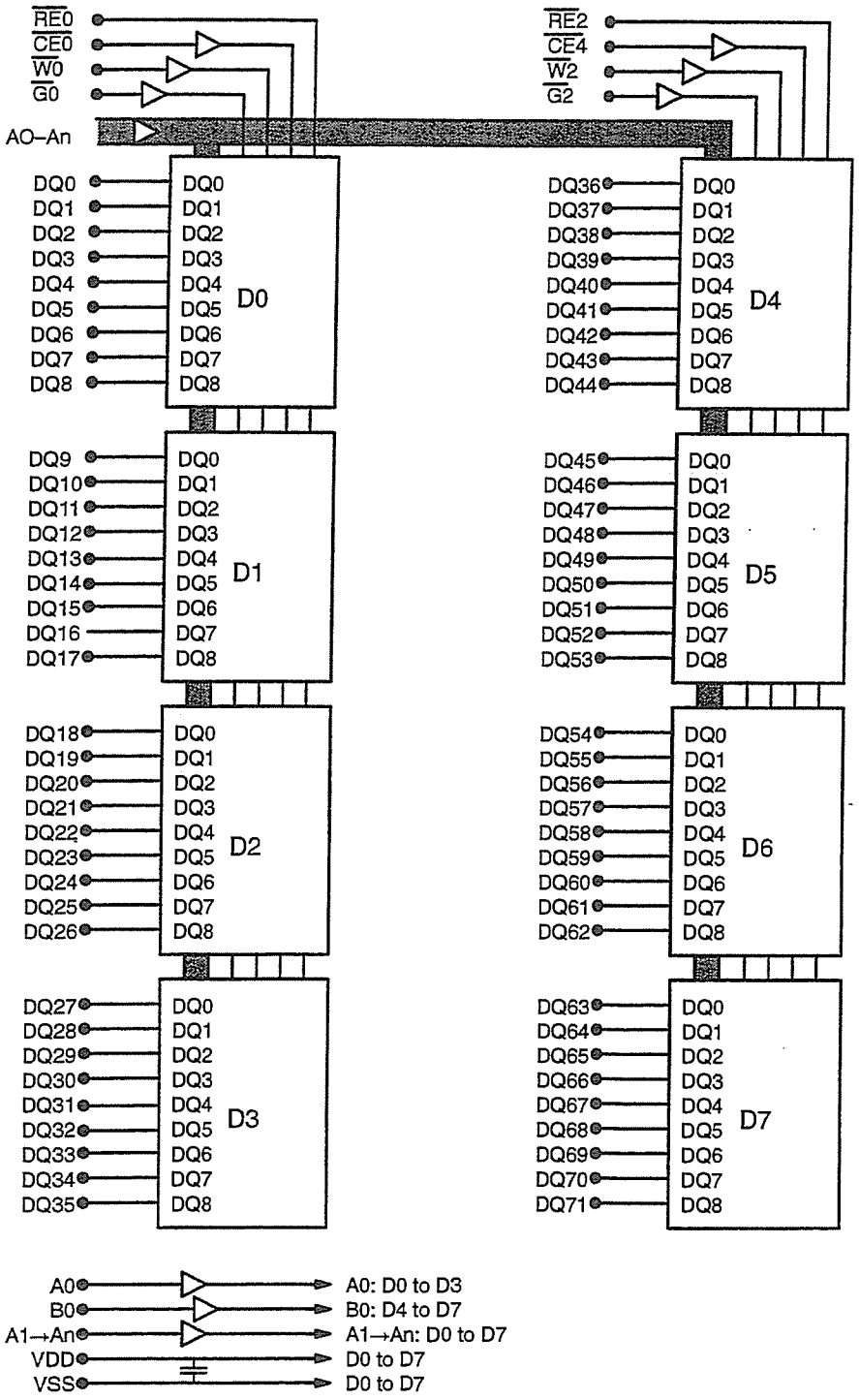


Figure 4.5.1–R
168 PIN, X72 (ECC mode) DRAM DIMM, 1 bank with X9 DRAMs
Release 4c7

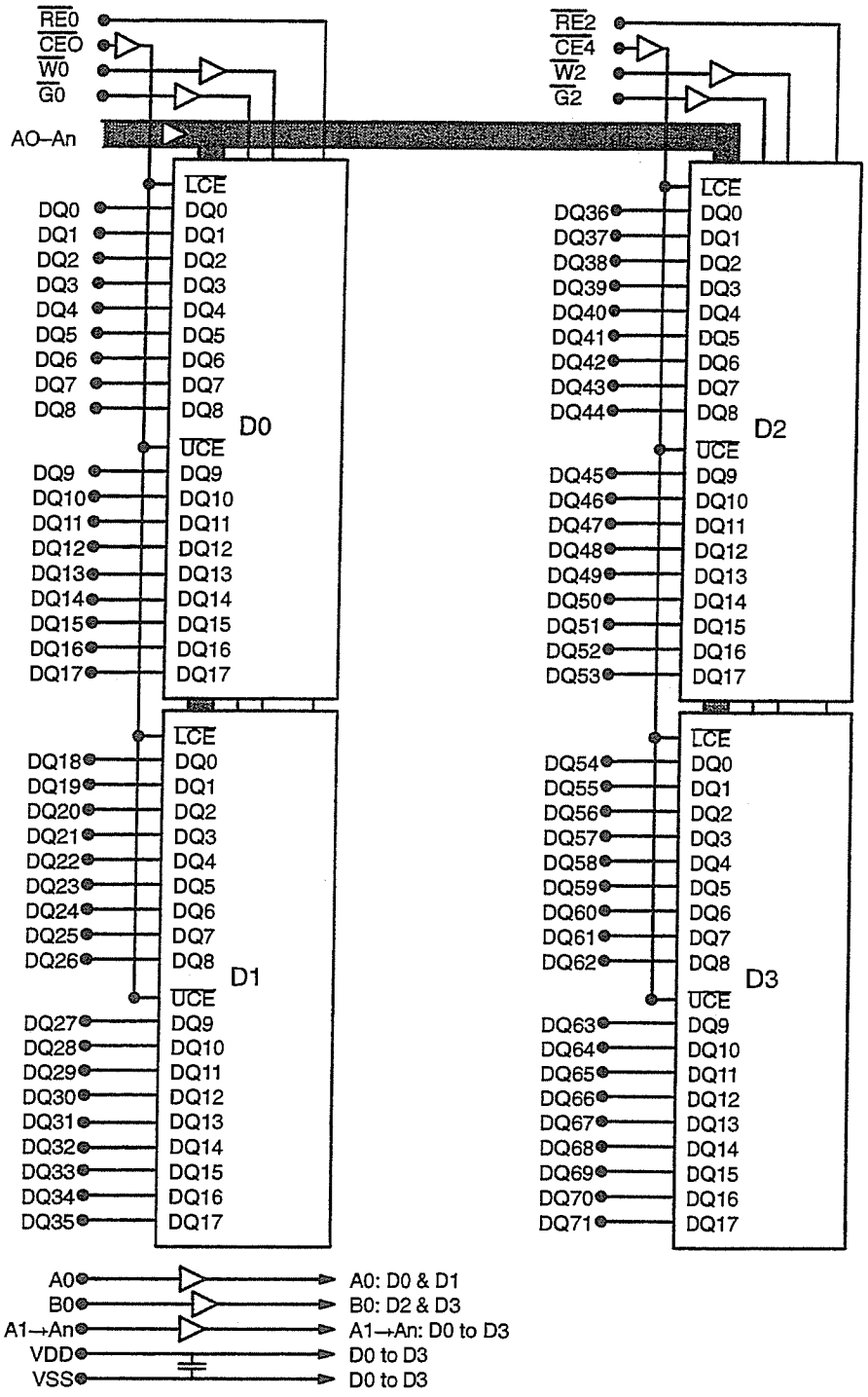


Figure 4.5.1–S
168 PIN, X72 (ECC mode) DRAM DIMM, 1 bank with X18 DRAMs

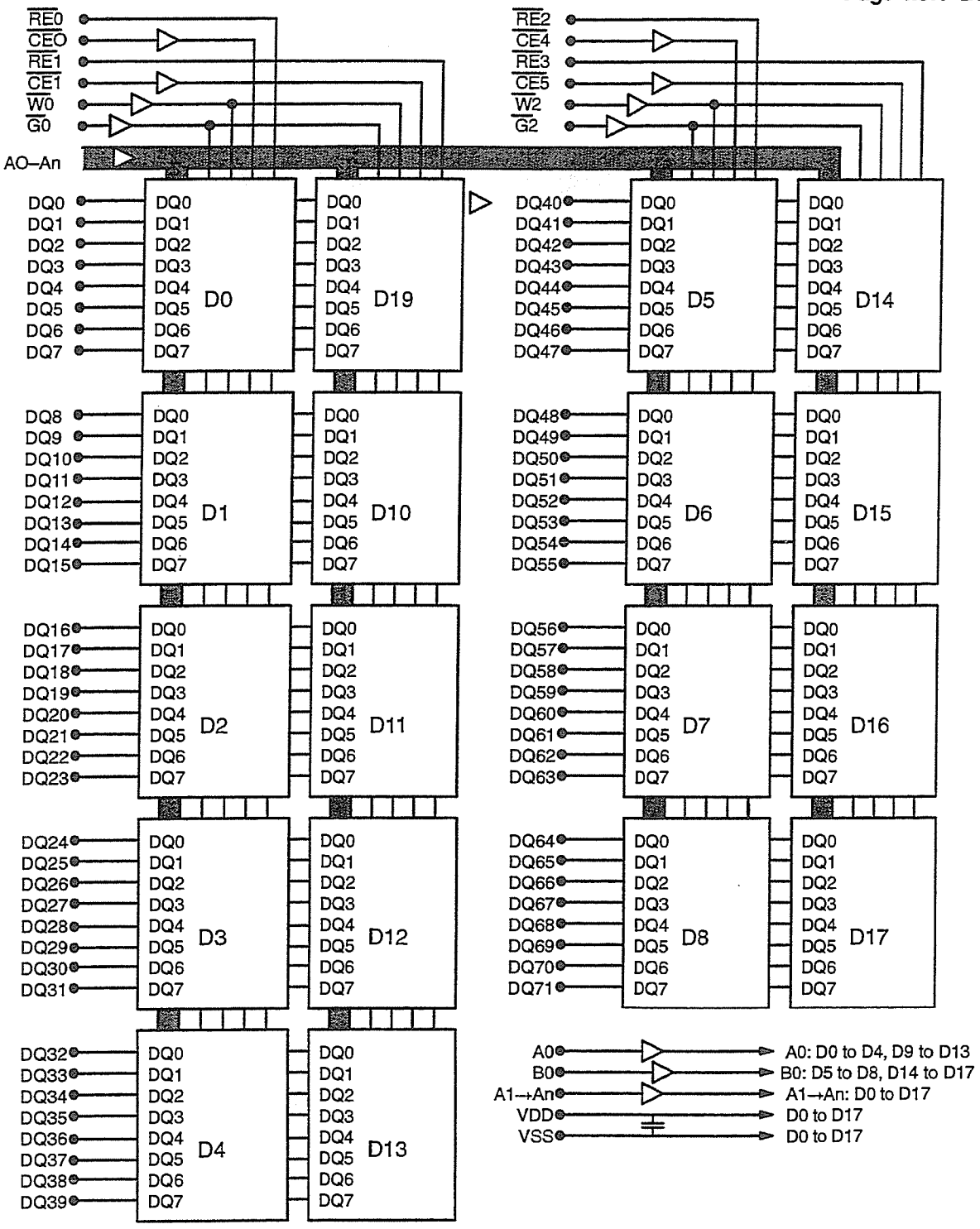


Figure 4.5.1–T
168 PIN, X72 (ECC mode) DRAM DIMM, 2 banks with X8 DRAMs

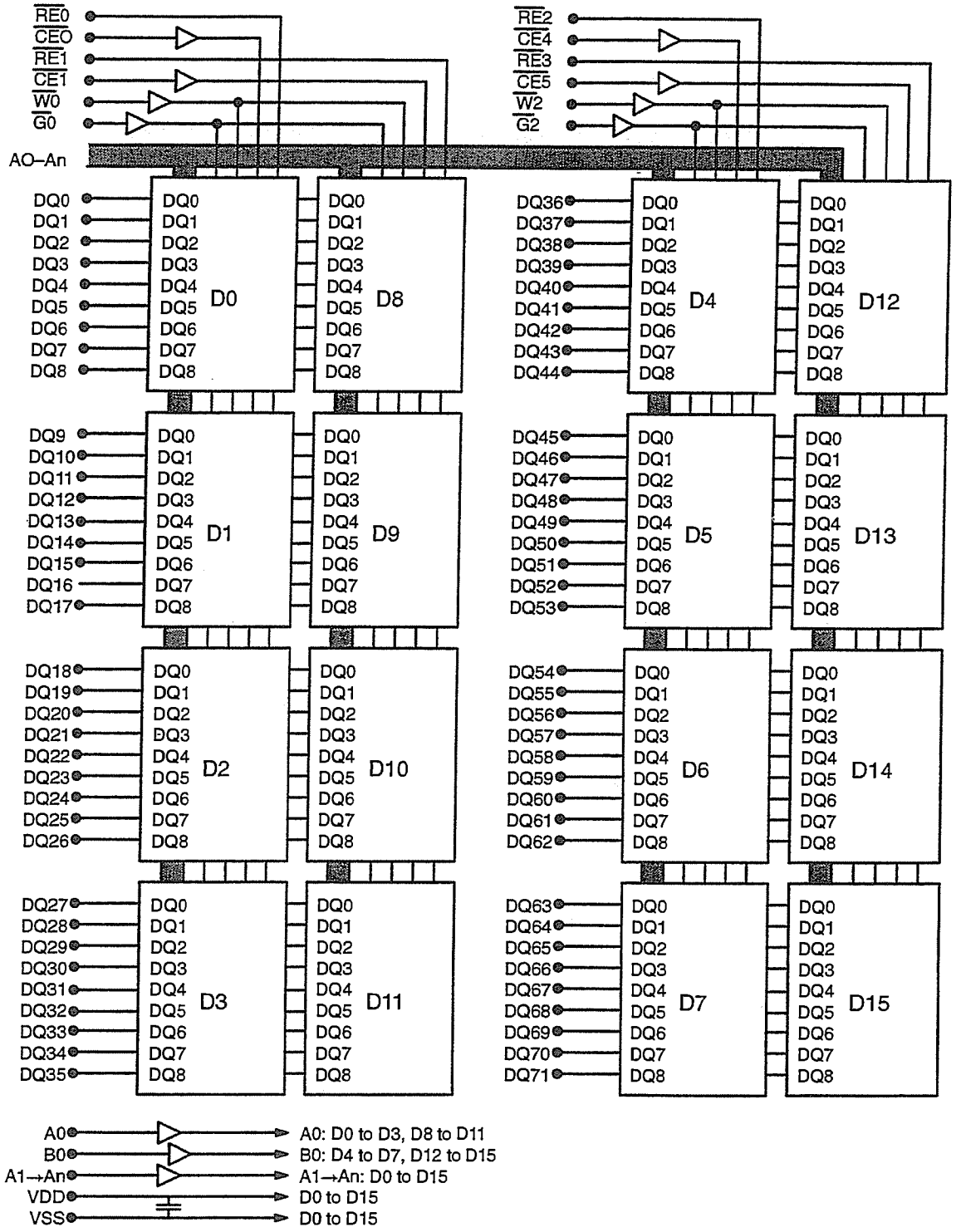


Figure 4.5.1–U
168 PIN, X72 (ECC mode) DRAM DIMM, 2 banks with X9 DRAMs
Release 4–7

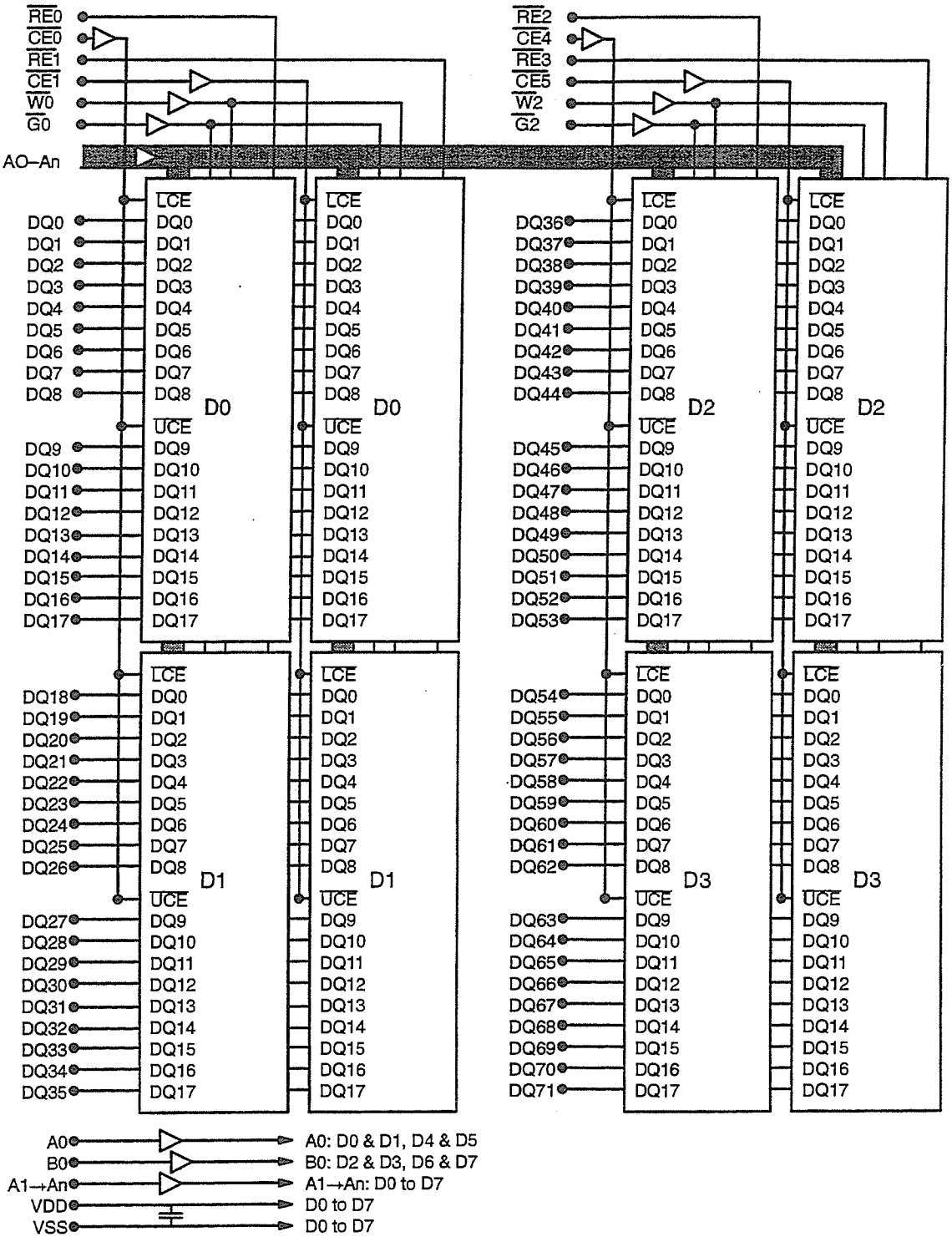


Figure 4.5.1–V

168 PIN, X72 (ECC mode) DRAM DIMM, 2 banks with X18 DRAMs

Release 4–7

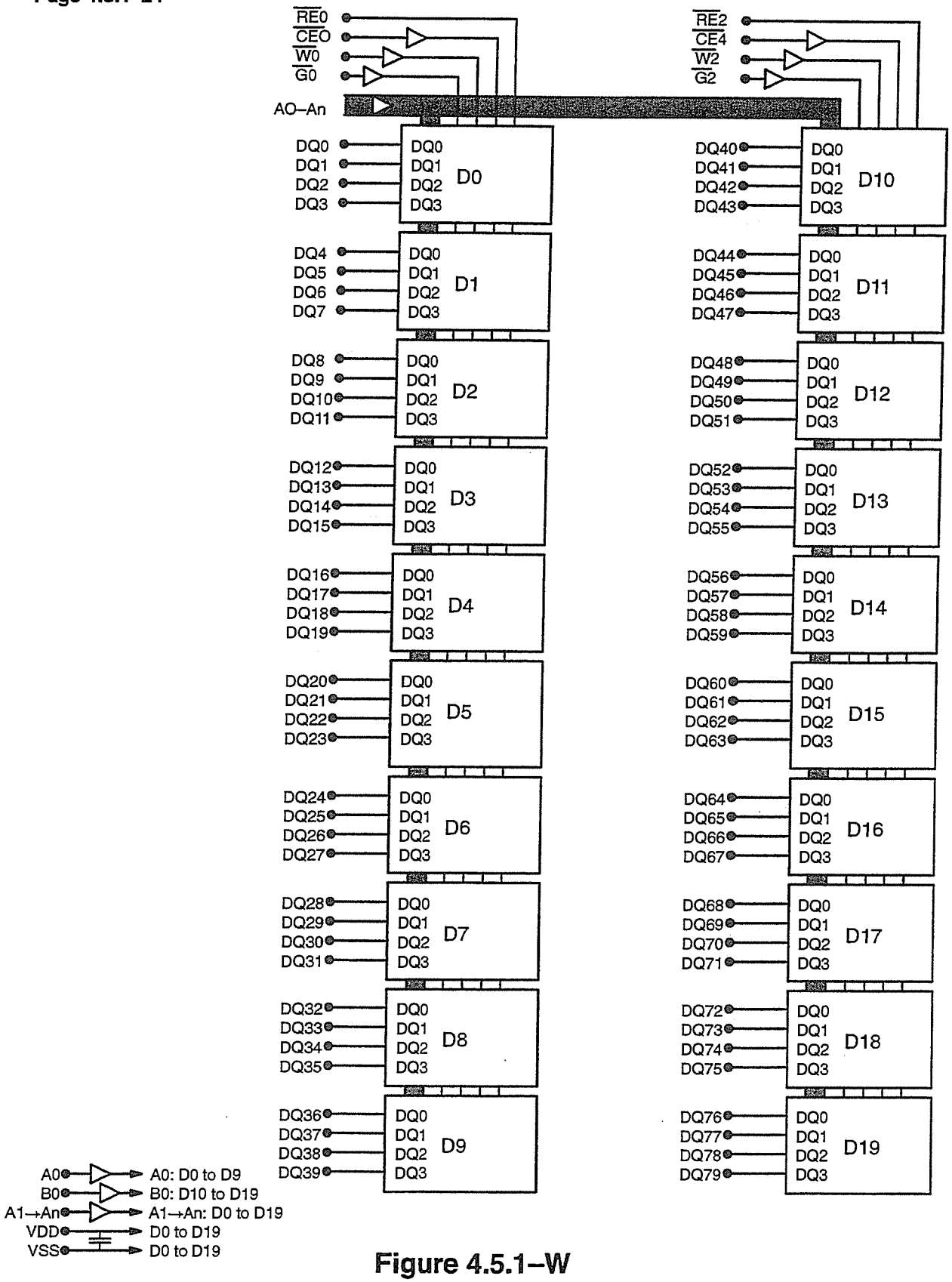


Figure 4.5.1–W

168 PIN, 80 BIT (ECC mode) DRAM DIMM, 1 bank with X4 DRAMs

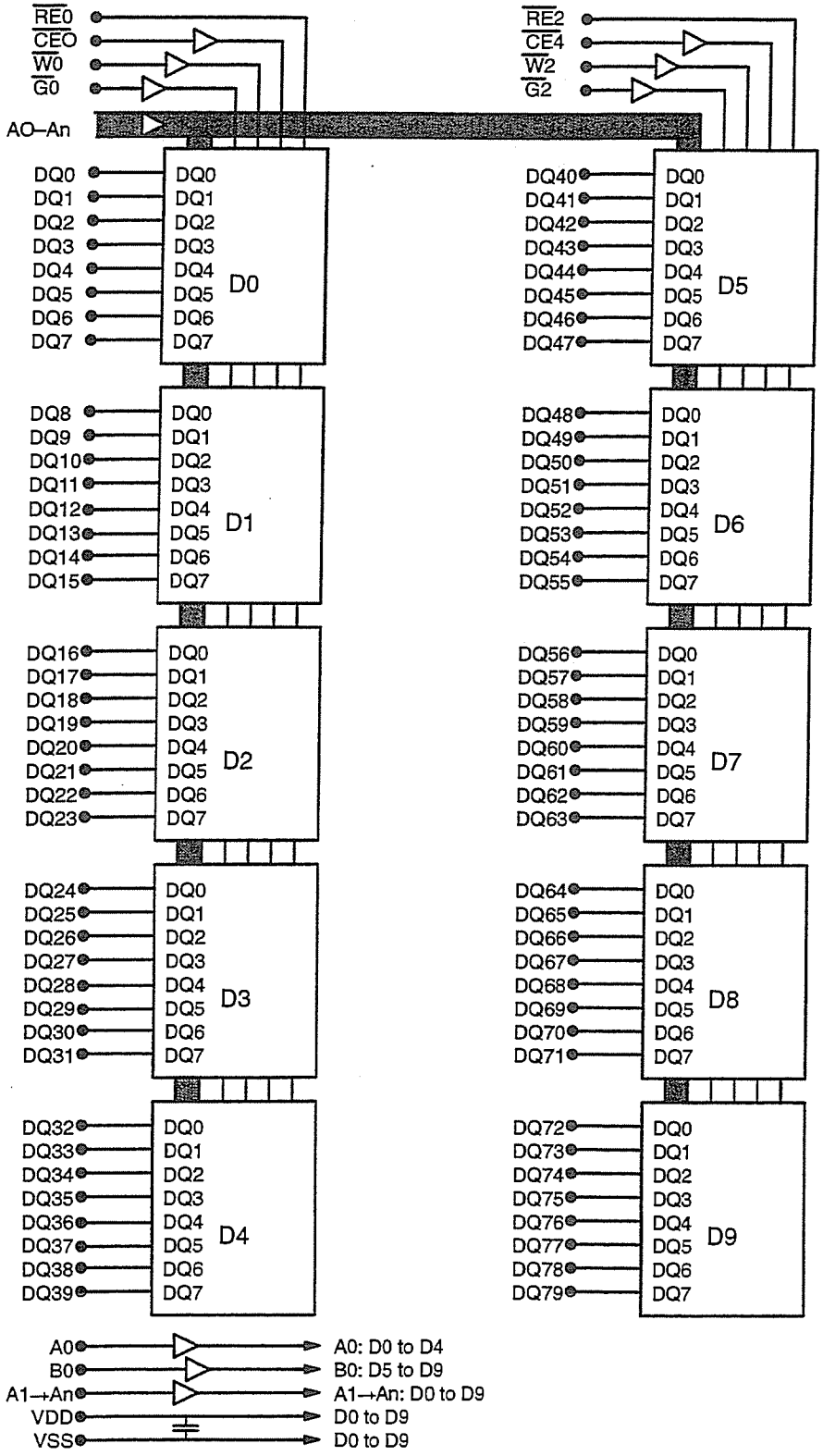


Figure 4.5.1–X
168 PIN, X80 (ECC mode) DRAM DIMM, 1 bank with X8 DRAMs

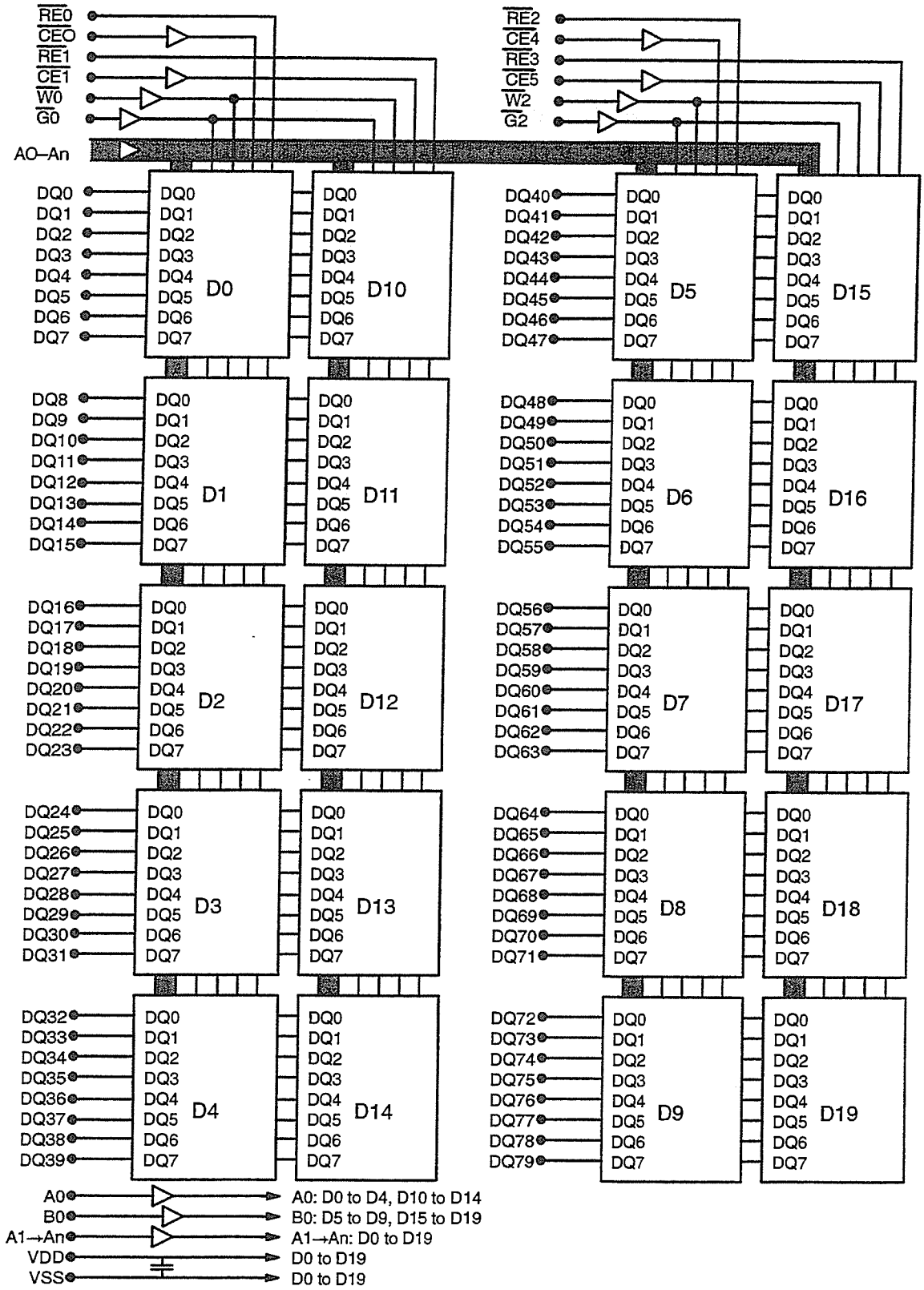


Figure 4.5.1–Y
168 PIN, X80 (ECC mode) DRAM DIMM, 2 banks with X8 DRAMs

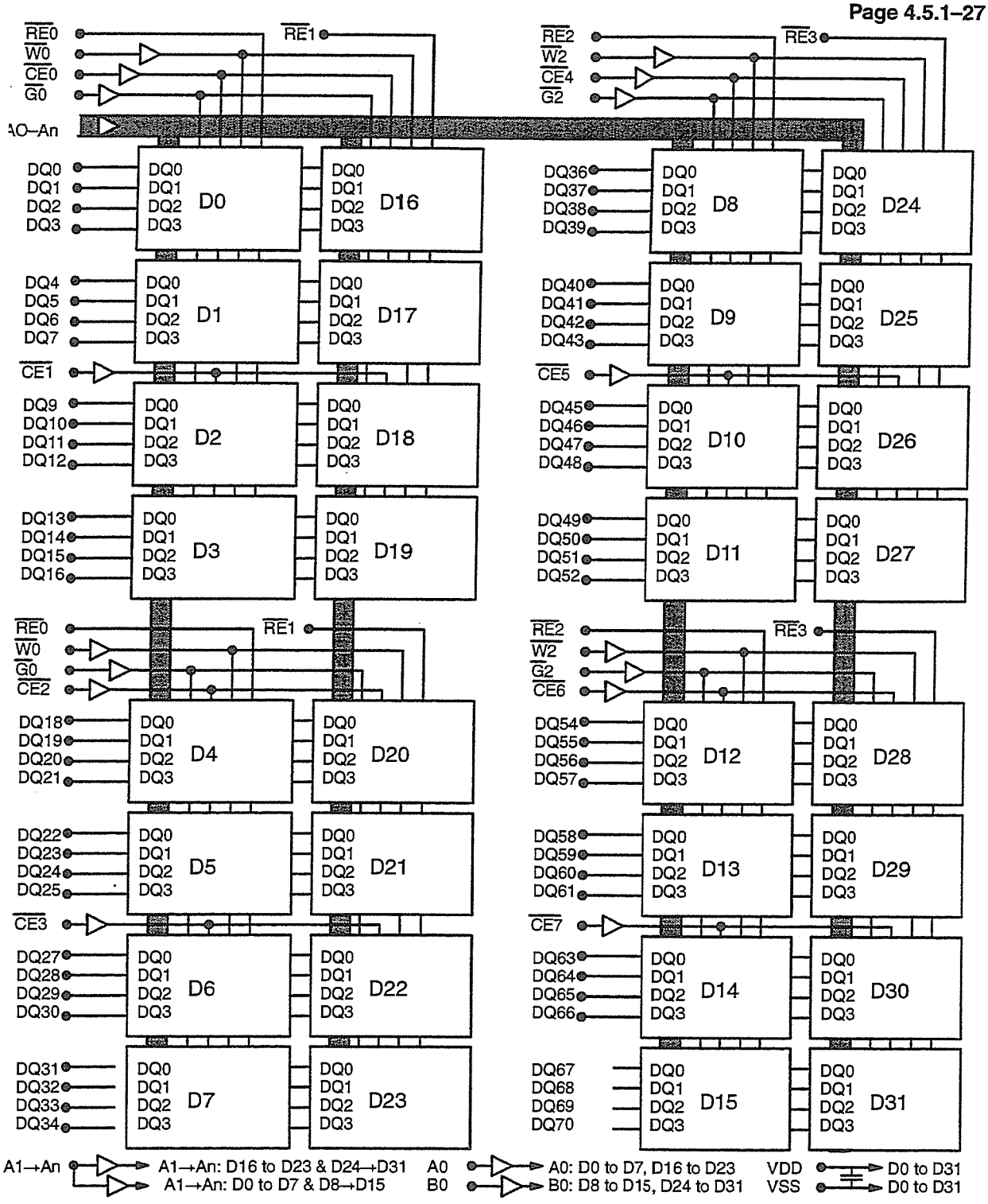


Figure 4.5.1–Z
168 PIN, X64 DRAM DIMM, 2 BANK with X4 DRAMs

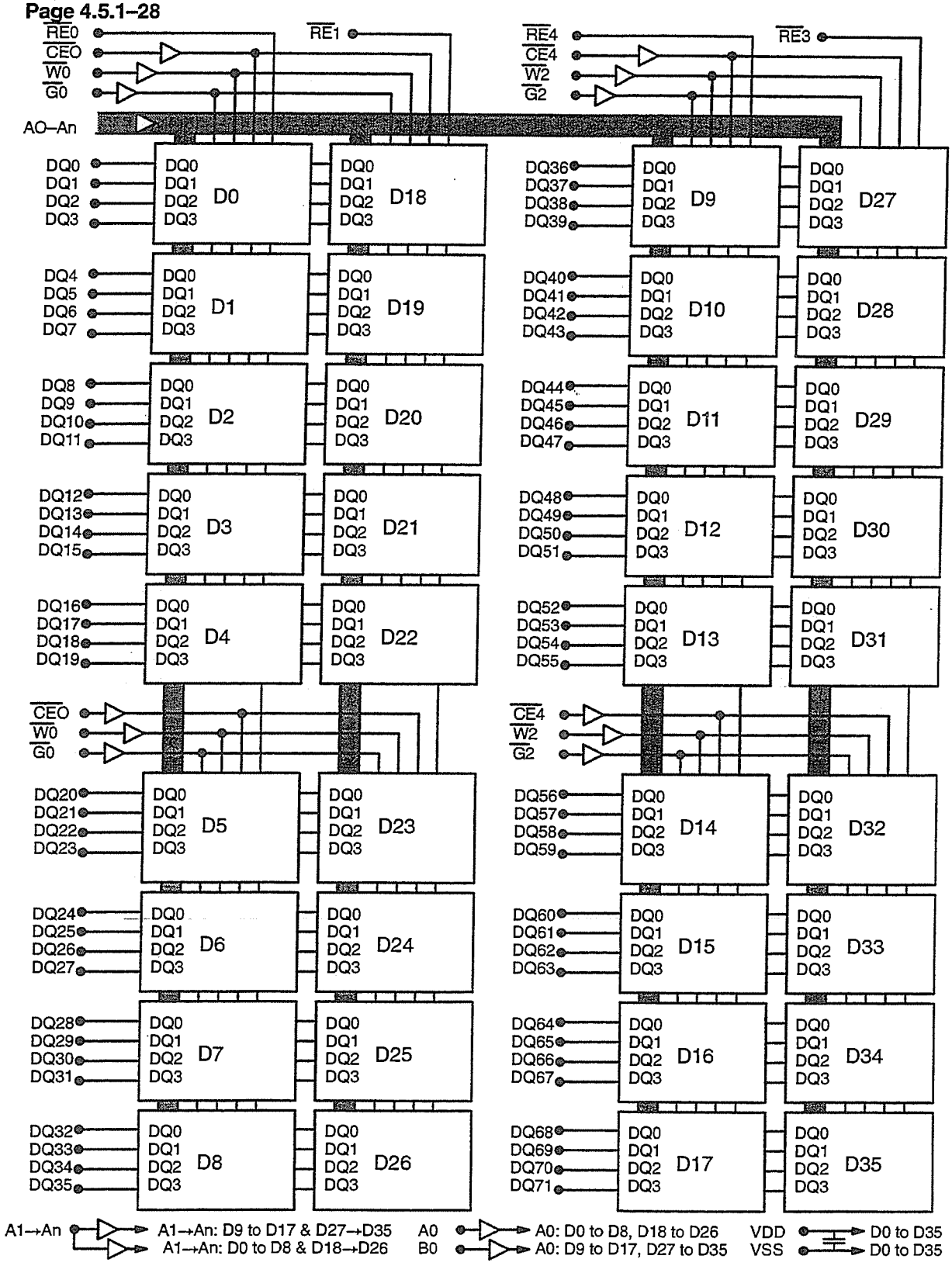


Figure 4.5.1–AA
168 PIN, X72 ECC DRAM DIMM, 2 BANK, X4 DRAMs
Release 6c7

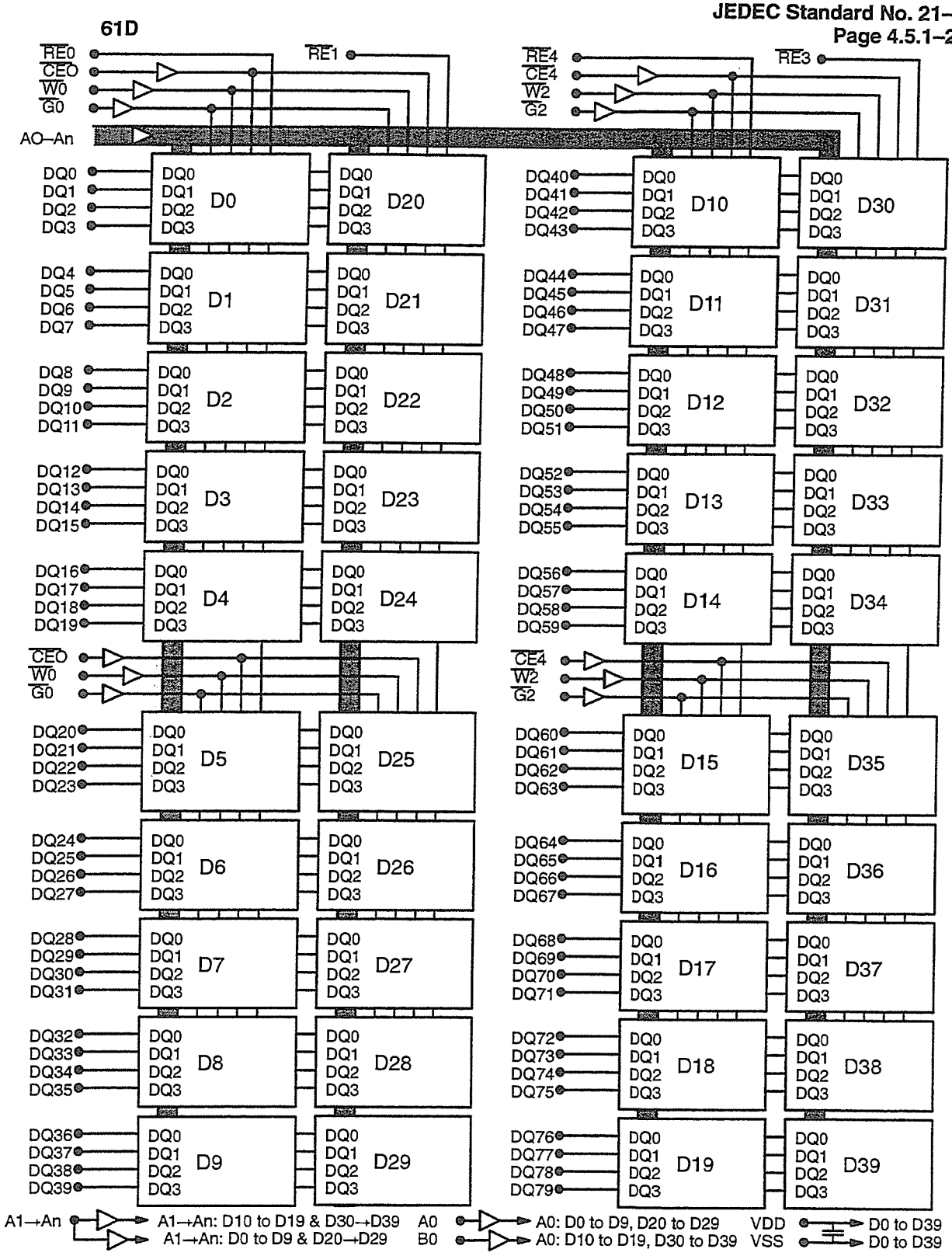


Figure 4.5.1–AB
168 PIN, X80 ECC DRAM DIMM, 2 BANK, X4 DRAMs

4.5.2 – 200 PIN DRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS
DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES
CONFIGURATION—21 Different Configurations are defined using various combinationa of X1, X4, X8, X9, X16 and X18 memory devices.
LOGIC FEATURES—The modules contain "PRESENCE DETECT" and "IDENTITY" featurs that conist of output pins in the PDn and IDn fields which supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS AND PD TABLES—Figs. 4.5.2–A, 4.5.2–B, & 4.5.2–C
MECHANICAL KEY DEFINITION—Fig. 4.5.2–D
PIN DEFINITIONS—Fig. 4.5.2–E
CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.2–F through 4.5.2–M

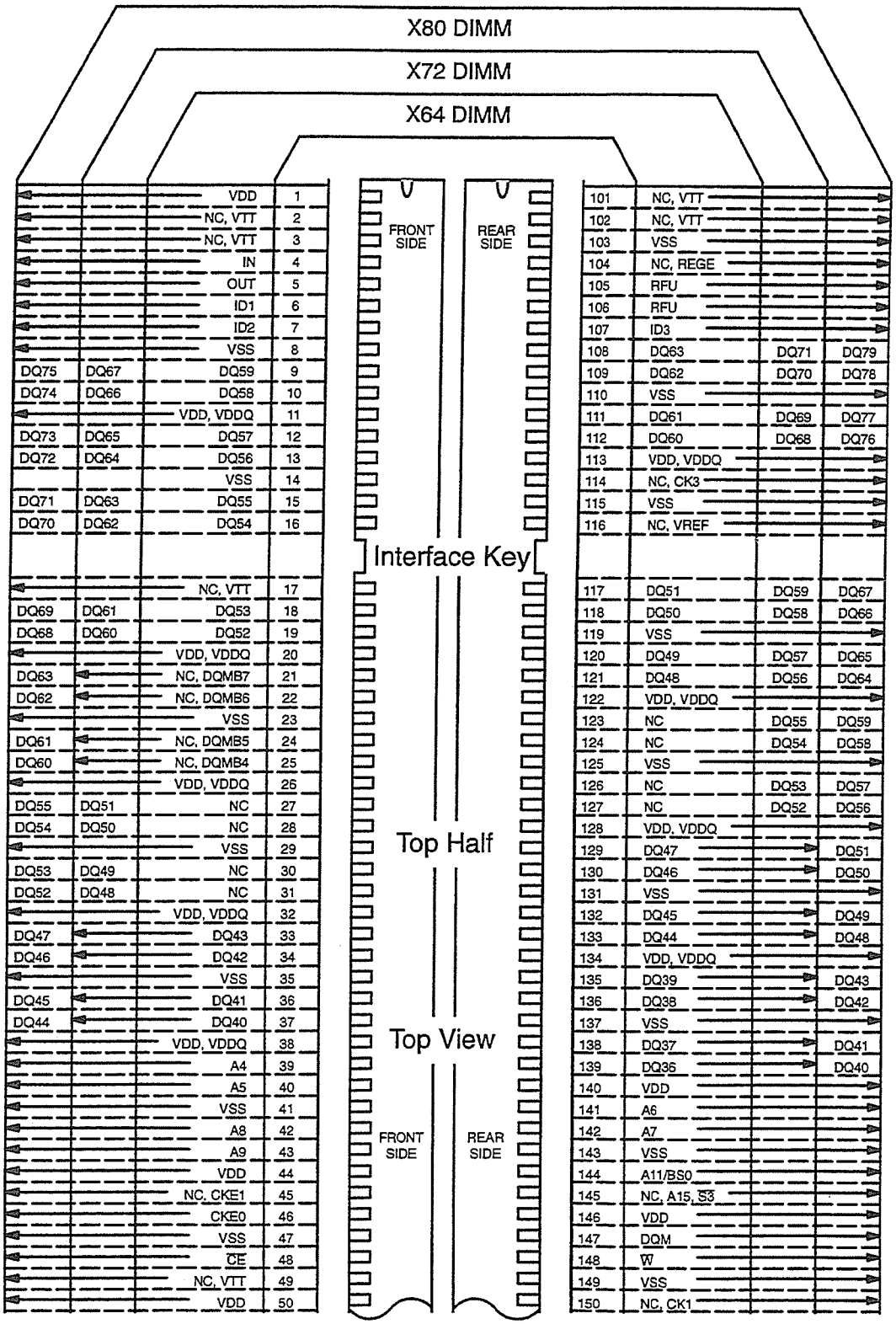


Figure 4.5.2–A
200 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, TOP HALF

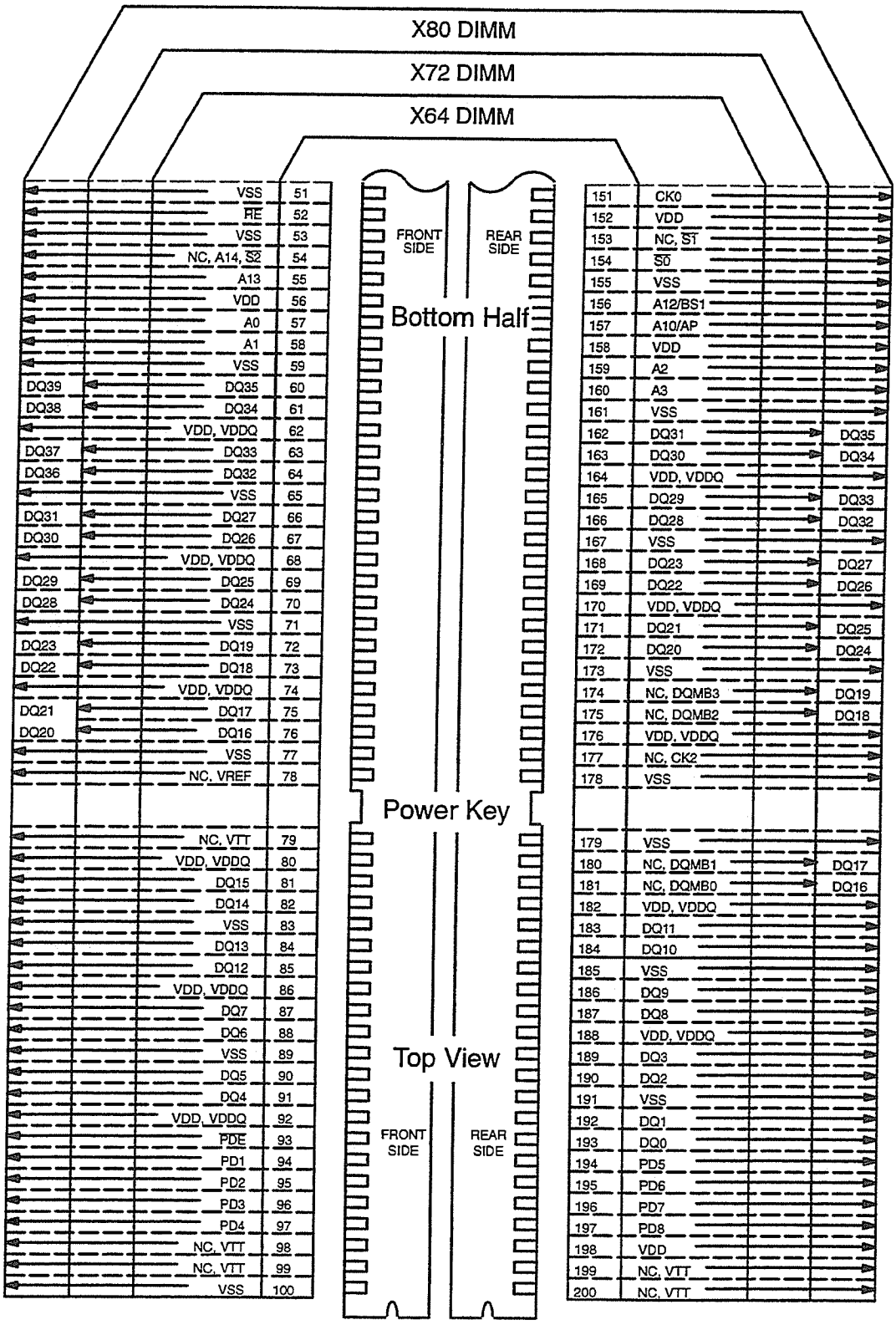


Figure 4.5.2–B
200 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, BOTTOM HALF

PD BITS 4 3 2 1	MODULE CONFIGURATION	SDRAM ORGANIZATION	RE ADDR.	CE ADDR
1 1 1 1	NO MODULE			
1 0 0 0 0 0 0 0	1M X 64/72/80 2M X 64/72/80	1M X 16 1M X 16	12 12	8 8
1 0 0 1 0 0 0 1	2M X 64/72/80 4M X 64/72/80	2M X 8 2M X 8	12 12	9 9
1 0 1 0 0 0 1 0	4M X 64/72/80 8M X 64/72/80	4M X 4/16 4M X 4/16	12 12	10 10
1 0 1 1 0 0 1 1	8M X 64/72/80 16M X 64/72/80	8M X 8 8M X 8	TBD TBD	TBD TBD
1 1 0 0 0 1 0 0	16M X 64/72/80 32M X 64/72/80	16M X 4 16M X 4	TBD TBD	TBD TBD
1 1 0 1 0 1 0 1	RFU RFU	TBD TBD	TBD TBD	TBD TBD
1 1 1 0 0 1 1 0	RFU RFU	TBD TBD	TBD TBD	TBD TBD
0 1 1 1	Expansion			

Note 1 Presence Detect pins PD1—PD8 are buffered and enabled by $\overline{PDE}$. The "1" outputs are NC and the "0" outputs are driven low by on–module drivers when $\overline{PDE}$ is asserted active low.

Note 2 Buffered DIMMs (PD7=1) with PD8=0 (Byte–Write) shall be capable of both Word–Write and Byte–Write operations

	PD6	PD5
SPEED (tCYC)	195	194
15 ns	1	1
12 ns	1	0
10 ns	0	1
8 ns	0	0
PD SPEED TABLE		

	PD7
INTERFACE	196
UNBUFFERED	0
BUFFERED	1
MODULE INTERFACE	

	PD8
WRITE MODE	197
BYTE	0
WORD	1
WRITE MODE DETECT	

	ID3
POWER	107
NORMAL	0
LOW–POWER	1
POWER LEVEL DETECT	

	ID2
RAS TIMING	7
NO EARLY RAS	0
EARLY RAS	1
READ PRECHARGE TIMING	

	ID1
INTERVAL	6
2 CLOCKS	0
1 CLOCK	1
COMMAND INTERVAL	

Figure 4.5.2–C

200 PIN, 64, 72, or 80 BIT SIMM PRESENCE DETECT & CONFIGURATION TABLES

Release 5–7

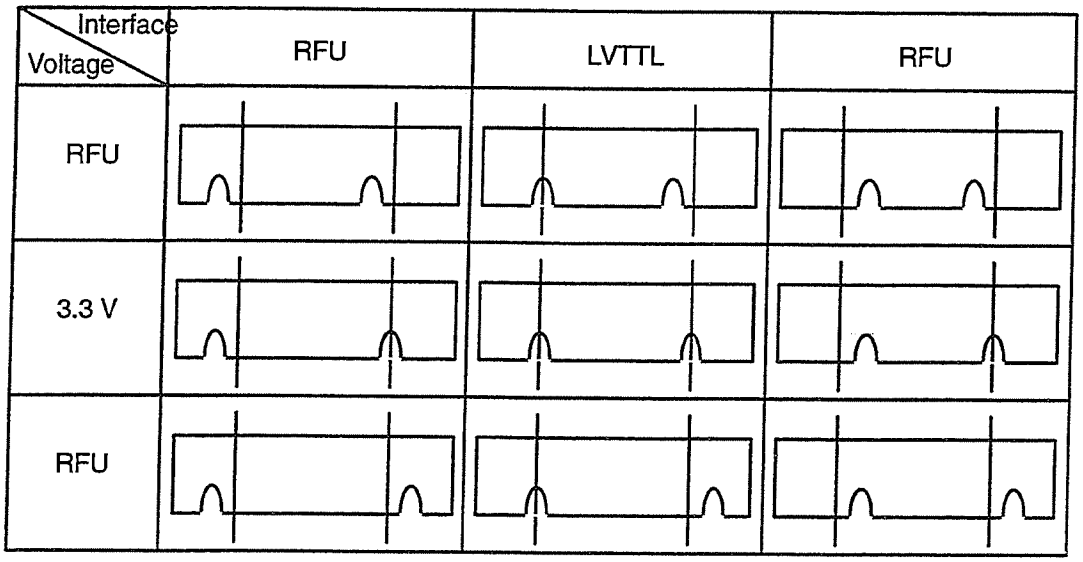


Figure 4.5.2–D

200 PIN, 8 BYTE SDRAM DIMM MECHANICAL KEY DEFINITION

Pin Name	Number	Function
A0....A15	16	Address Input (multiplexed)
DQ0....DQ79	80	Data Input/Output (common)
CK0....CK3	4	Clock Input
CKE0....CKE1	2	Clock Enable Input
$\overline{S0}$....$\overline{S3}$	4	Chip Select Input
$\overline{RE}$	1	Row Enable (RAS) Input
$\overline{CE}$	1	Column Enable (CAS) Input
$\overline{W}$	1	Write Enable Input
DQM	1	Data Mask
DQMB0....DQMB7	8	Byte Data Mask
REGE	1	Buffer/Register Enable
$\overline{PDE}$	1	Presence Detect Enable
PD1....PD8	8	Buffered Logic Presence Detect Output
ID1....ID3	3	Identification Output
IN, OUT	2	Unbuffered Physical Detect Input/Output
VDD	9	Primary Positive Power Supply
VDDQ	20	Posivite Power for Input/Output
VREF	2	Reference Power Supply
VSS	33	Ground
VTT	11	Termination Power Supply
RFU	2	Reserved for Future Use

Notes:

1. Pin A14 is shared with S2, and pin A15 is shared with pin S3.
2 Pins DQMB0...DQMB7 are shared with pins defined as NC for X64 and X72 configurations.
3 REGE (Register Enable) operates similarly to the SAB pin on the 74AC11652 "Octal Bus Transceiver and Register with 3–State Outputs". When it is asserted, active high, the buffer–register operates in Register mode, as opposed to when it is de–asserted, inactive low, the buffer –register operates in "real–time" buffer mode.
4. The unbuffered physical detect pins IN and OUT are shorted together on the DIMM.

Figure 4.5.2–E

8 BYTE SDRAM DIMM PIN DEFINITIONS

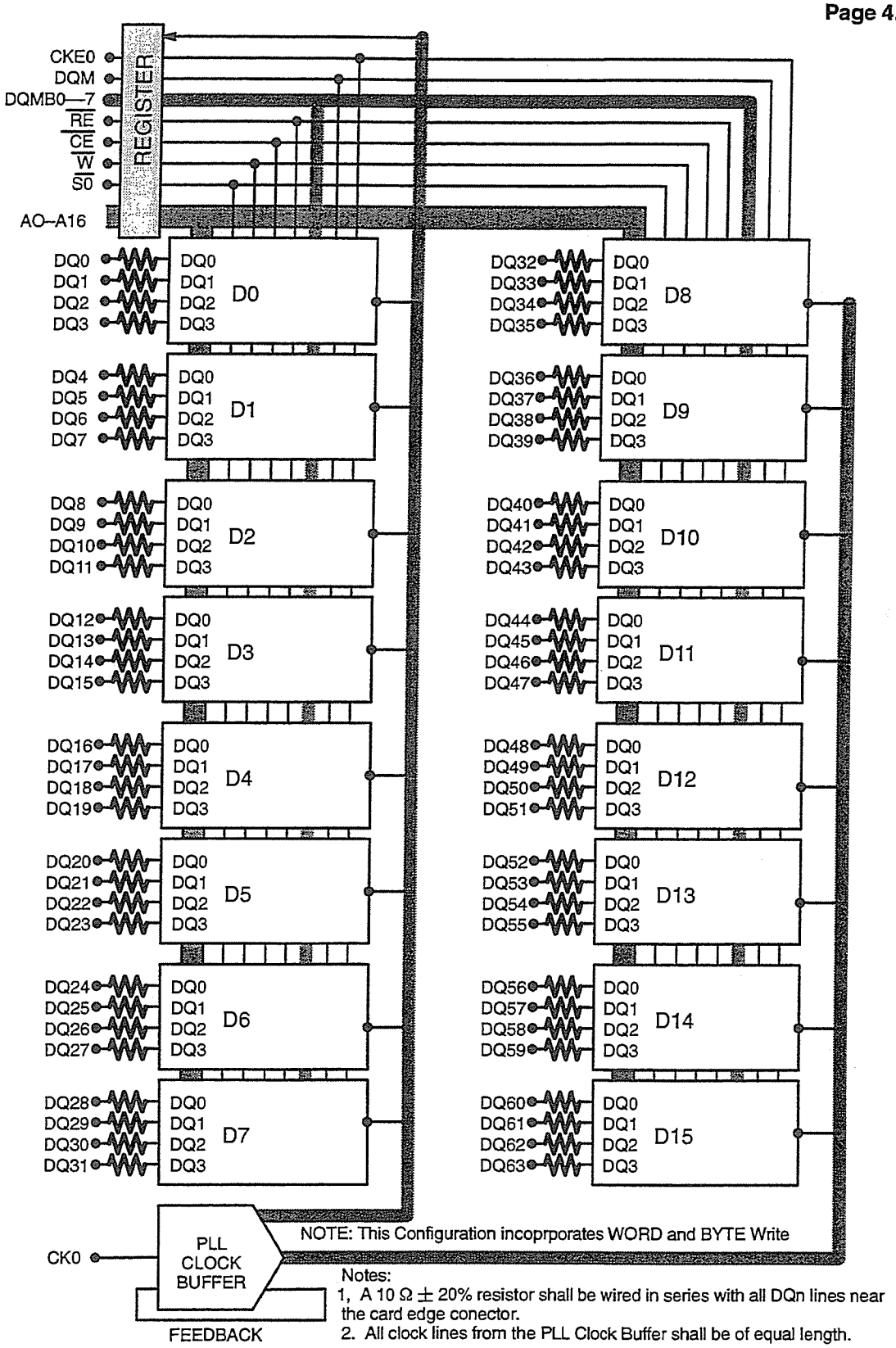


Figure 4.5.2–F

200 PIN, X64 BUFFERED SDRAM DIMM, 1 bank with X4 SDRAMs

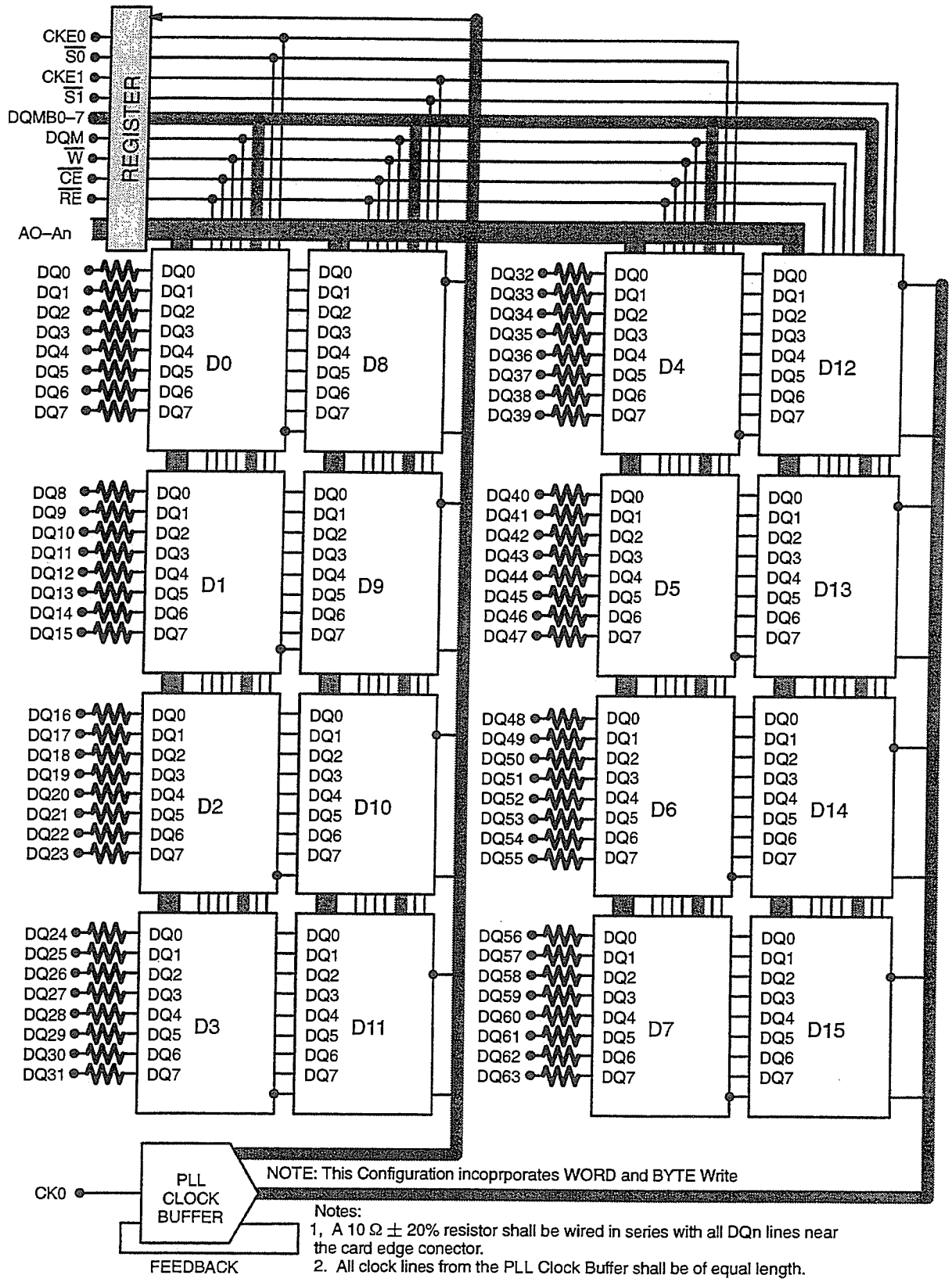


Figure 4.5.2–G

200 PIN, X64 BUFFERED SDRAM DIMM, 2 BANKS with X8 SDRAMs

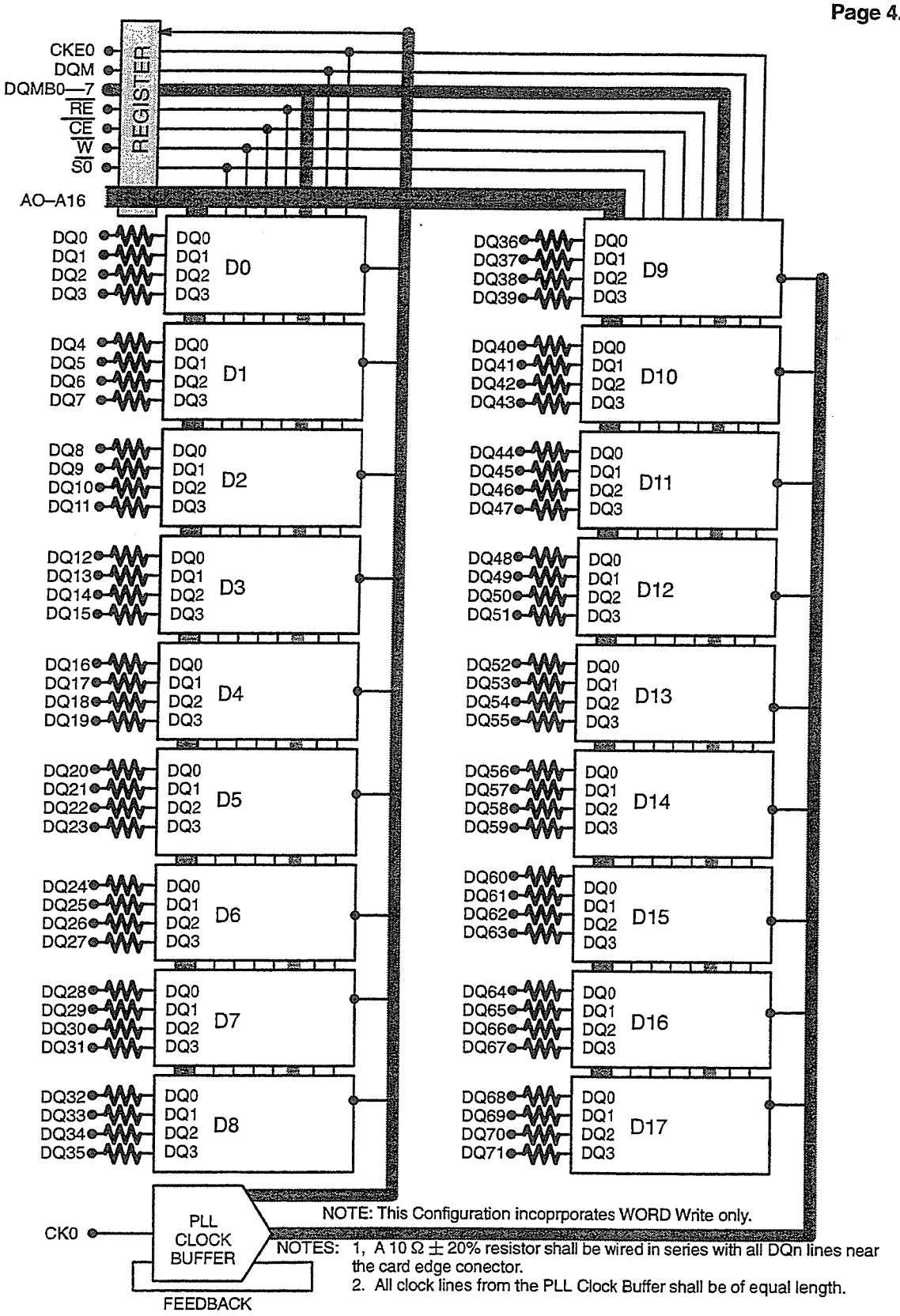
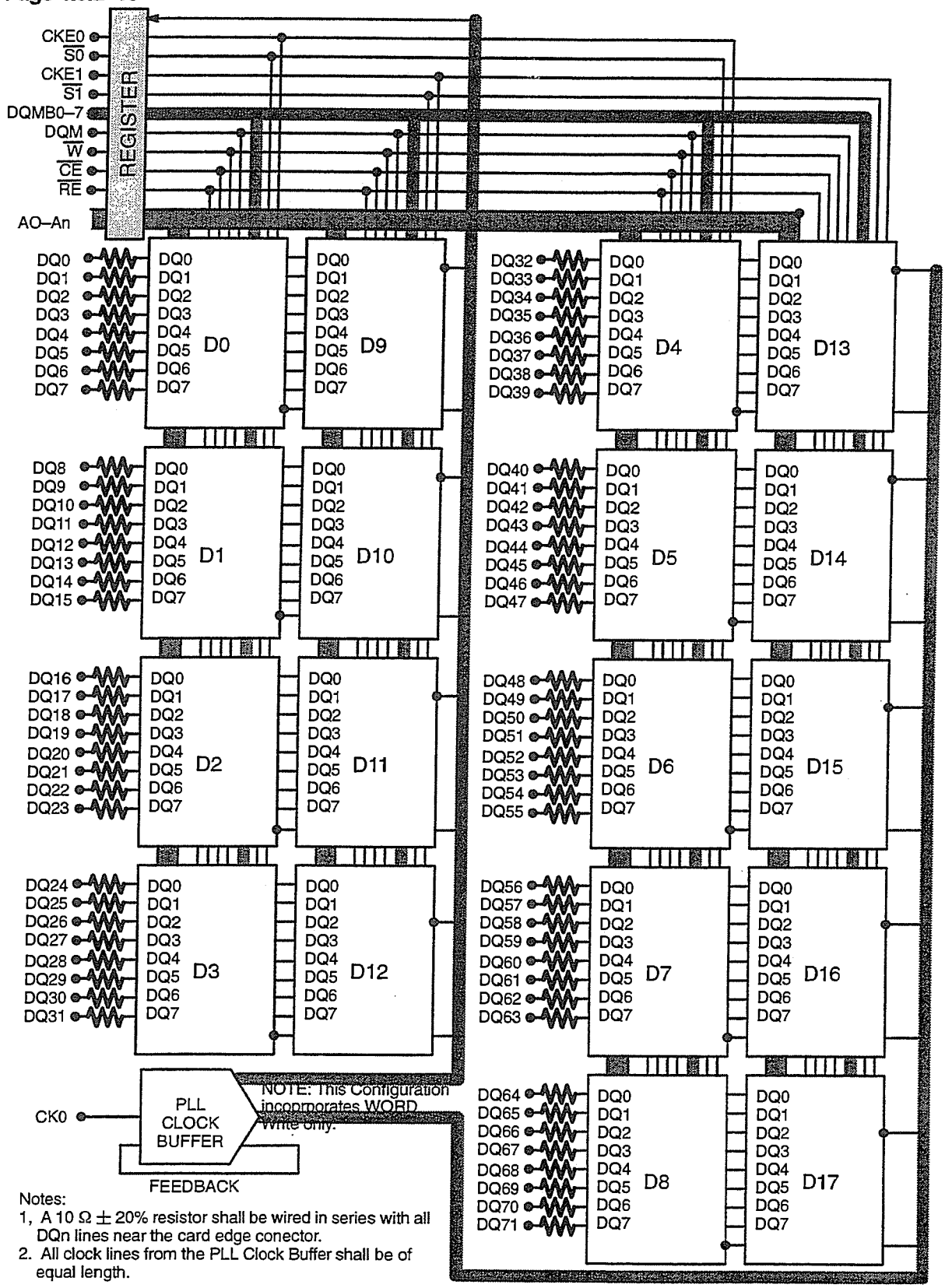


Figure 4.5.2–H

200 PIN, X72 BUFFERED SDRAM DIMM, 1 bank with X4 SDRAMs



Notes:
1, A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.5.2–I

200 PIN, X72 BUFFERED SDRAM DIMM, 2 BANKS with X8 SDRAMs

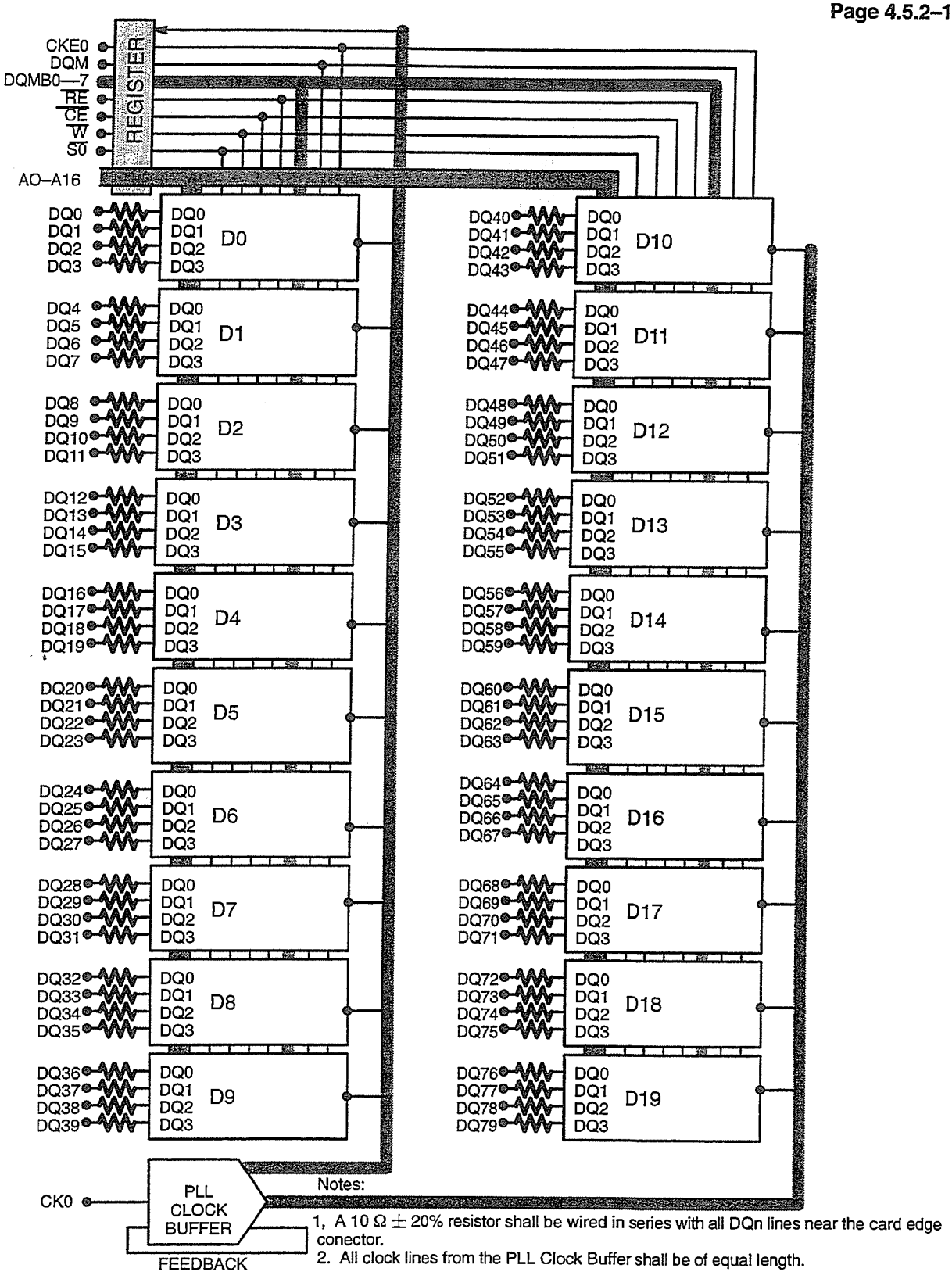
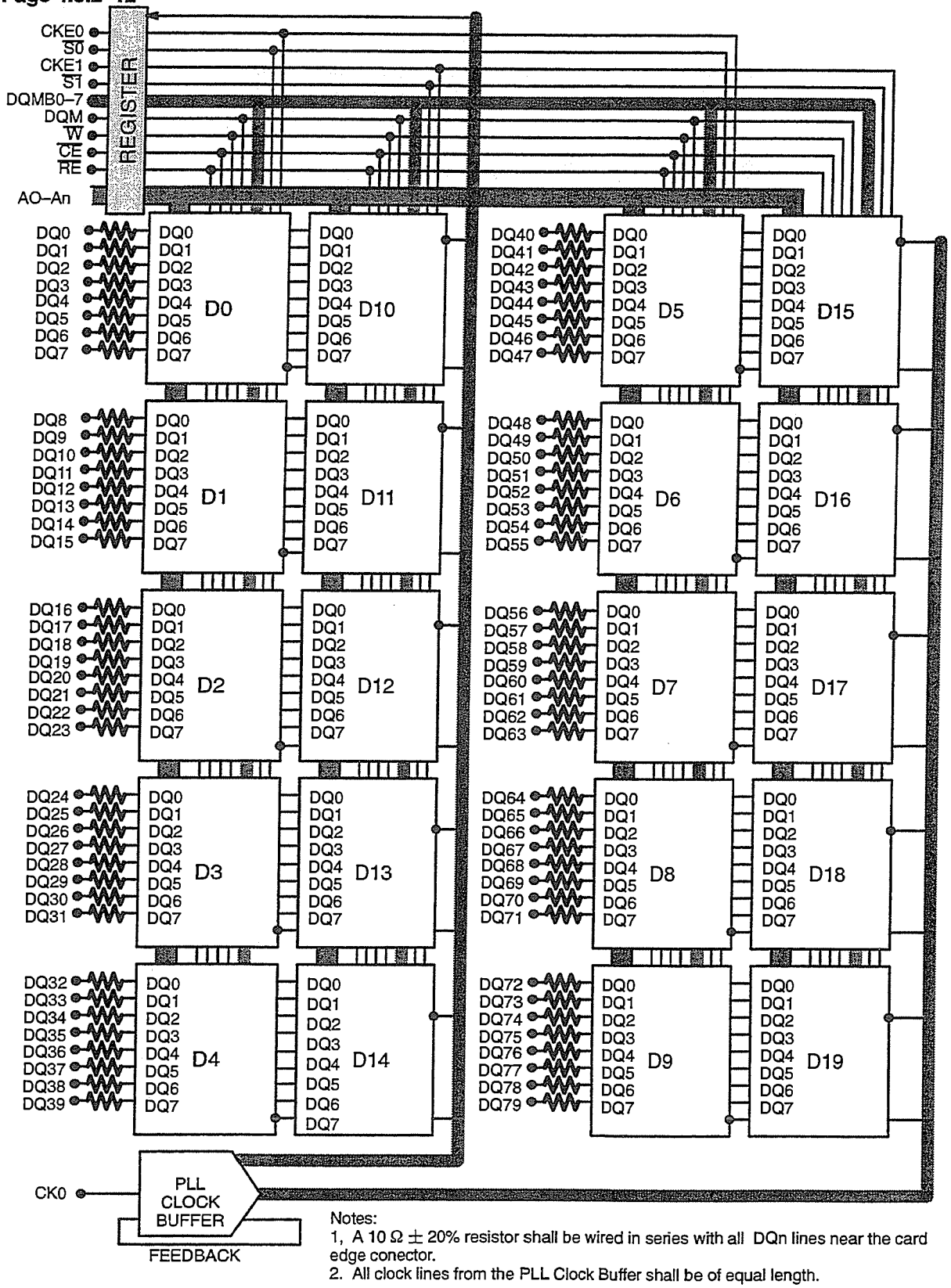


Figure 4.5.2–J

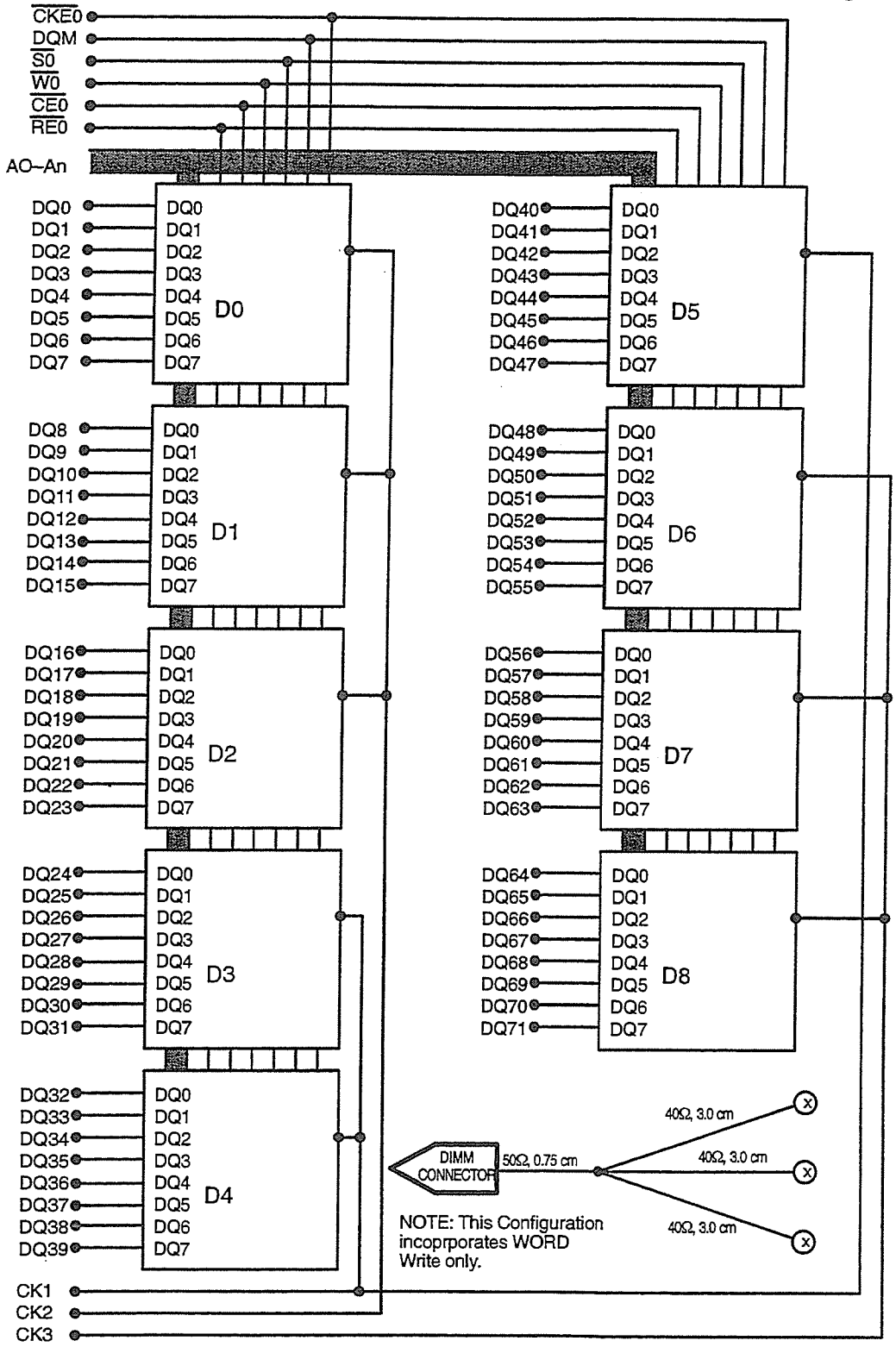
200 PIN, X80 BUFFERED SDRAM DIMM, 1 bank with X4 SDRAMs



Notes:
1, A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.5.2–K

200 PIN, X80 BUFFERED SDRAM DIMM, 2 BANKS with X8 SDRAMs



Note: All clock trees shall be routed as equal–length "stars" from CK1, CK2, & CK3 inputs as shown in the diagram above.

Figure 4.5.2–L

200 PIN, X72 UNBUFFERED SDRAM DIMM, 1 bank with X8 DRAMs

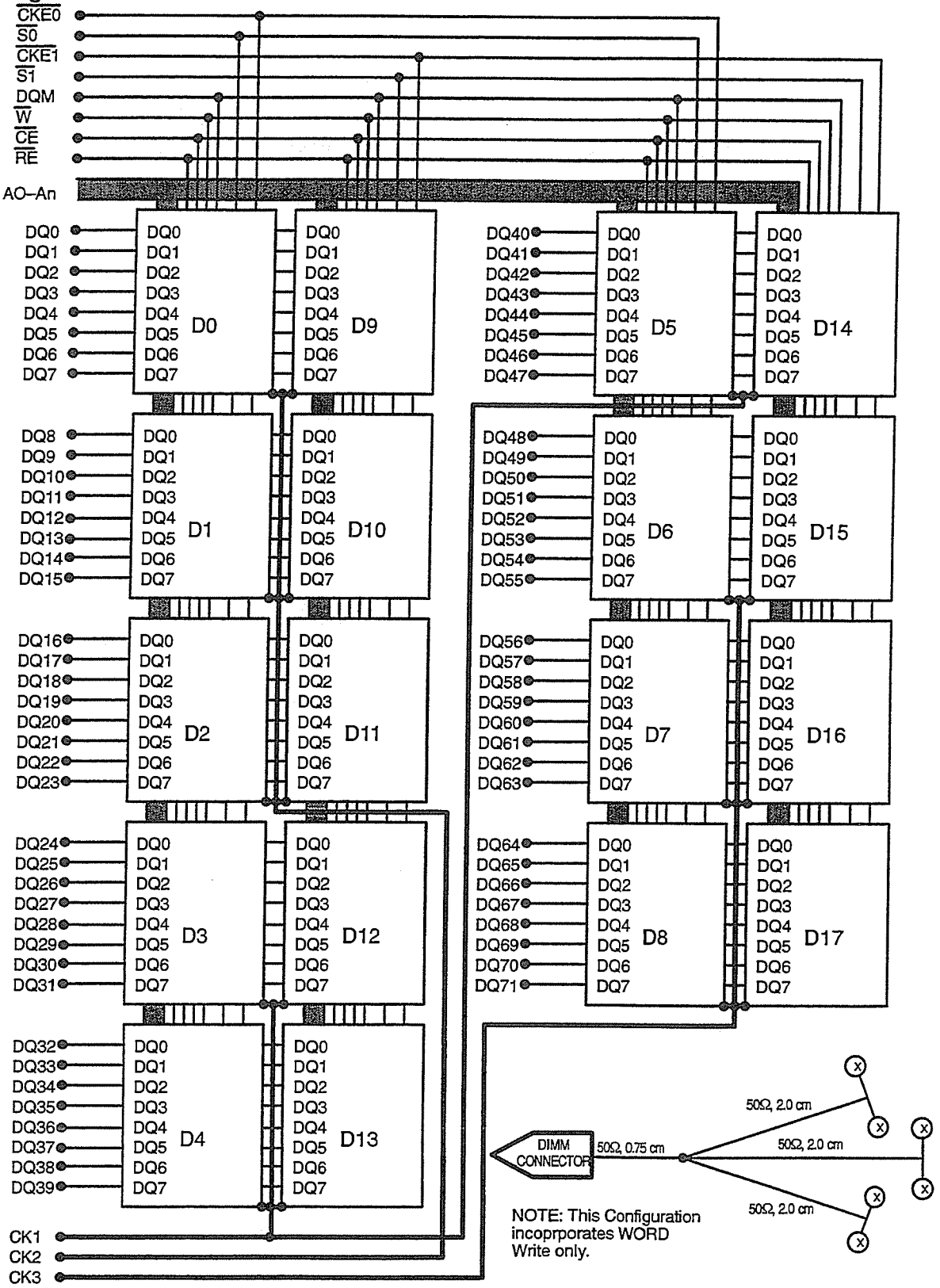


Figure 4.5.2–M

200 PIN, X72 UNBUFFERED SDRAM DIMM, 2 banks with X8 DRAMs

4.5.3 – 168 PIN UNBUFFERED DRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS

DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES

CONFIGURATION—13 Different Configurations are defined using various combinationa of X1, X4, X8, X16 and X18 memories.

LOGIC FEATURES—The modules contain "SERIAL PRESENCE DETECT" features using EEPROM stored information that profided a variety of encoded information regarding the module such as storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
—Check Bit locations are pre–assigned

PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS—Figs. 4.5.3–A, & 4.5.3–B

SPD TABLES—Figs. 4.5.3–C

KEYING METHODOLOGY—Fig. 4.5.3–D

CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.3–E through 4.5.3–S

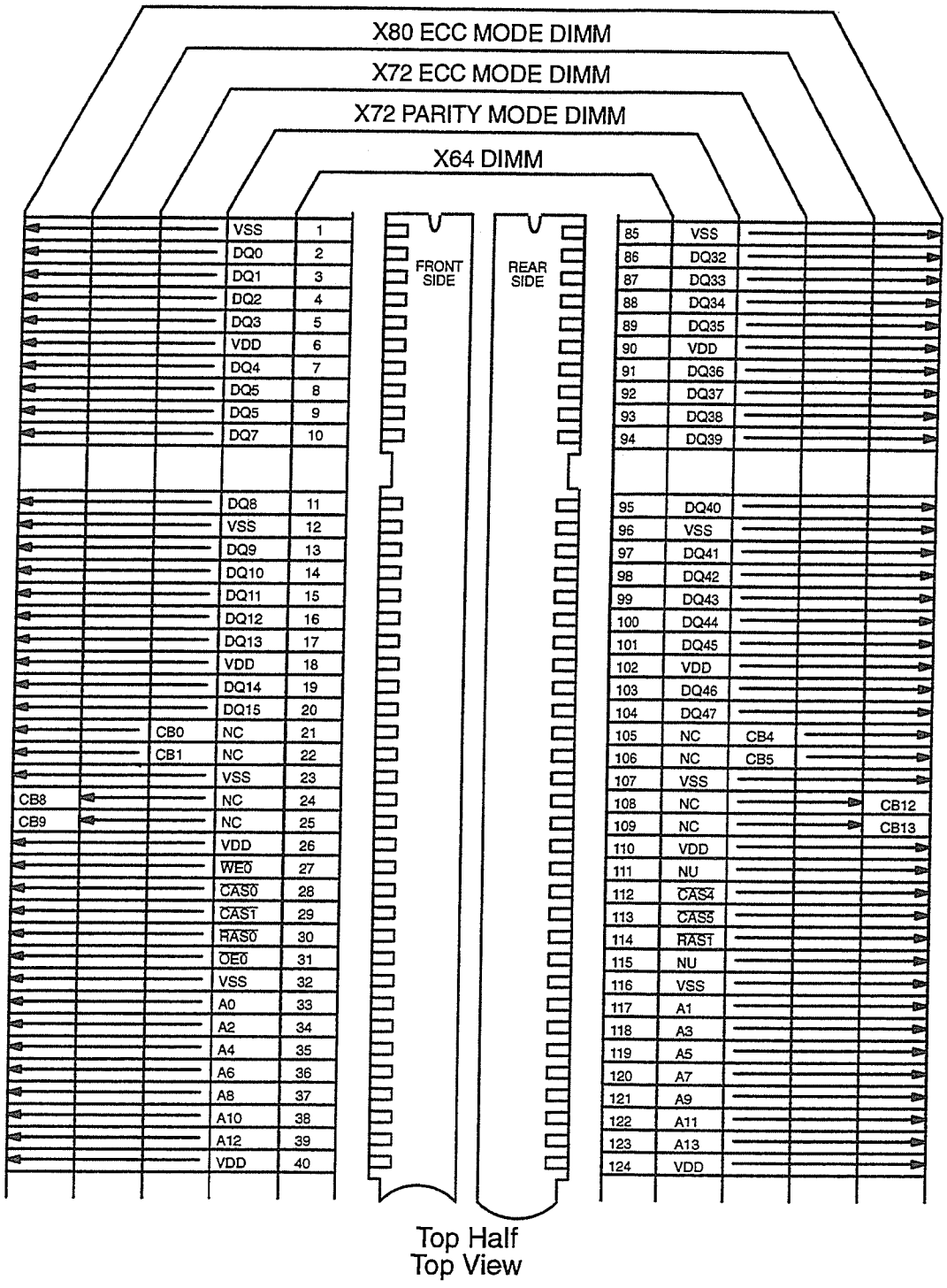


FIGURE 4.5.3–A
64, 72, or 80 BIT DIMM PINOUT, TOP HALF

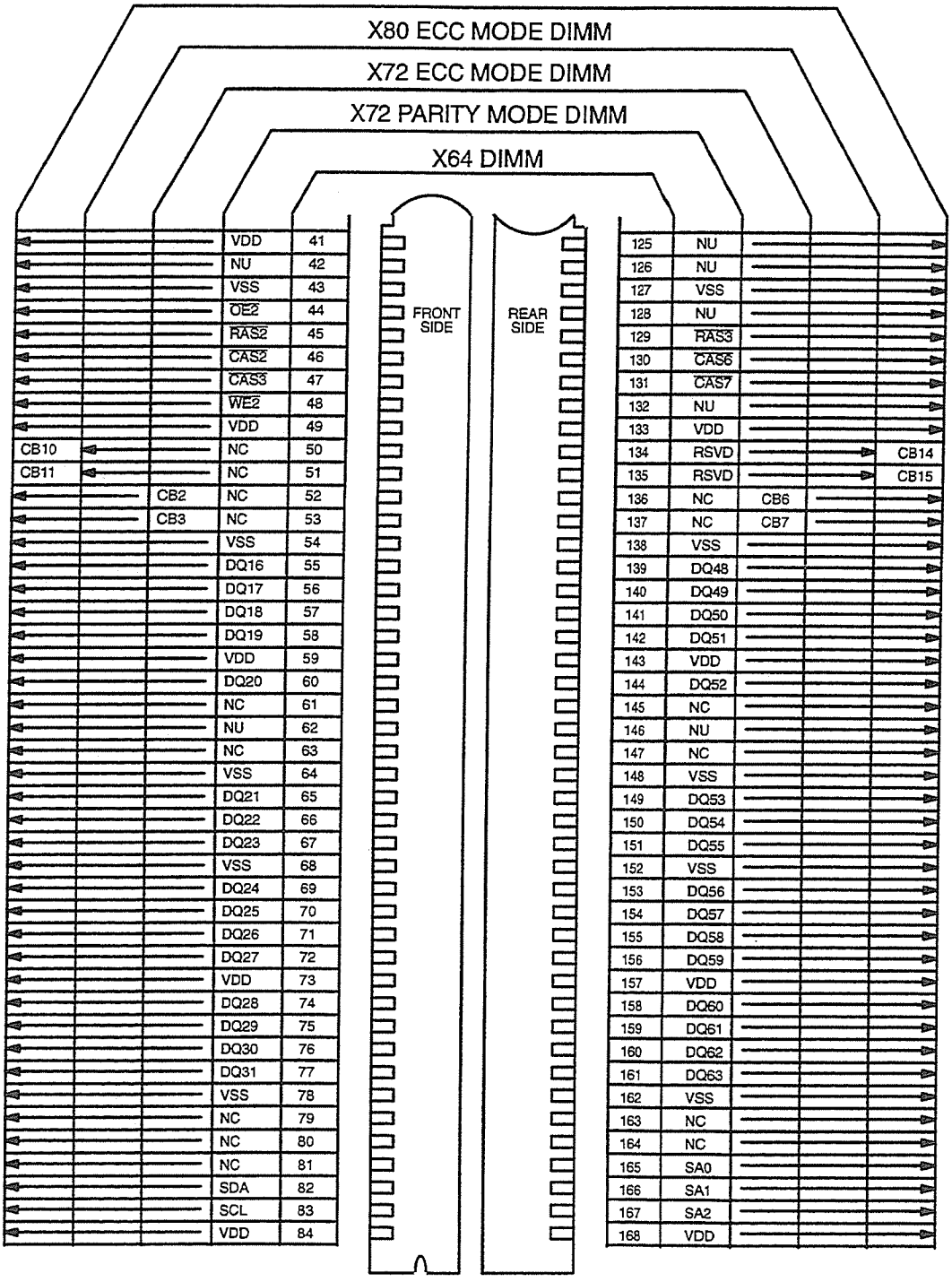
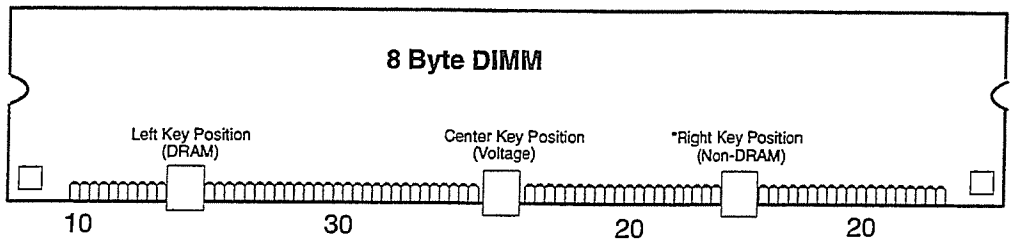
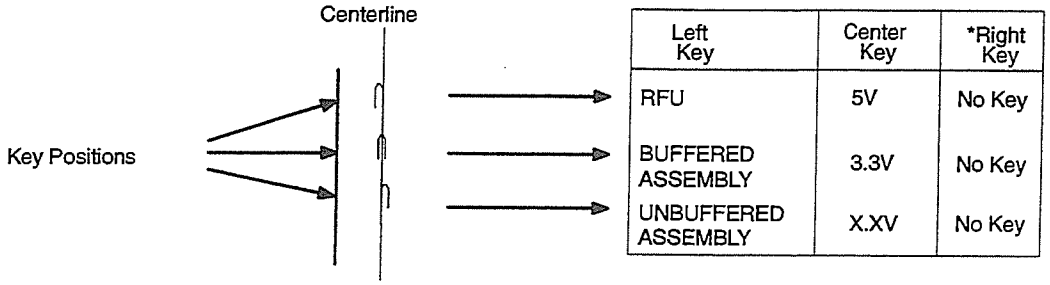


FIGURE 4.5.3–B
64, 72, or 80 BIT DIMM PINOUT, BOTTOM HALF

Buffered	Unbufffered
All signals except RAS and Data are buffered	No buffers, all DRAM signals are connected directly to DIMM tab pins
11 Pins are used for DIMM attributes (PDE, PD1-8, ID0-1)	5 pins are used for DIMM attributes (SDA, SCL, SA0-2)
CAS Pin assignment sequence optimized for buffer placement 0, 1 2, 3 4, 5 6, 7	CAS Pin signals are re-assigned for optimal DRAM placement 0, 4 1, 5 2, 6 3, 7
ECC DIMMs use subset of CAS signals for word selection (CAS0/1 and CAS4/5)	All DIMM types use byte selection (CAS0-7)
Address 0 to the DRAMs is sourced from separate pins (A0, B0) for 4 byte interleave	Single address pin (A0)
Data pin assignment uses both X64/X72 and X80 numbering schemes	Data pin assignment is changed to single x80 numbering scheme with x64 and x72 as subsets
Non-Parity is subset of Parity with inter-mixed Parity bits unconnected (PQ8, 17, 26, 35, 44, 53, 62, 71)	All DIMM types use the same sequential 64 data pins (DQ0-63). Eight center pins (CB0-7) are used as Parity/Check Bits for x72 Parity/ECC DIMMs. An additional 8 center pins (CB8-15) are used for the x80 ECC DIMMs.
32 Power/Gnd Pins V_{CC} - 16 V_{SS} - 16	35 Power/Gnd Pins V_{CC} - 17 (1 additional pin) V_{SS} - 18 (2 additional pins)
Unused Pins - 18	Unused Pins - 14
Left Key Definition SDRAM STD DRAM RFU	Left Key Definition modified RFU Buffered Assembly (DRAM/SDRAM) Unbuffered Assembly (DRAM/SDRAM)

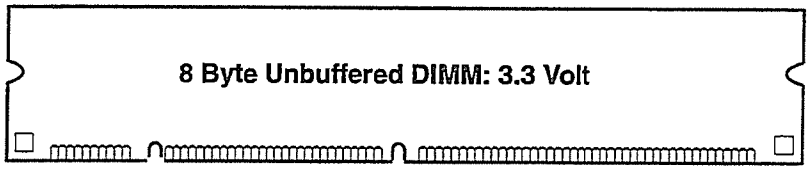
FIGURE 4.5.3–C
Comparison of 168 Pin Buffered & Unbuffered DRAM & SDRAM DIMM





Left Key	Center Key	*Right Key
RFU	5V	No Key
BUFFERED ASSEMBLY	3.3V	No Key
UNBUFFERED ASSEMBLY	X.XV	No Key

* For DRAM/SDRAM assemblies, this area is poplulated with pads.



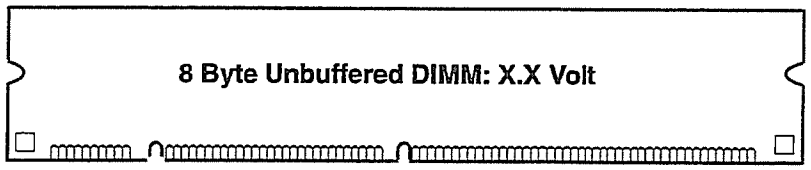


FIGURE 4.5.3–D
168 Pin DRAM DIMM Keying Methodology

31	$\overline{OE0}$	DU
42	DU	CK0
44	$\overline{OE2}$	DU
45	$\overline{RAS2}$	$\overline{S2}$
46	$\overline{CAS2}$	DQMB2
47	$\overline{CAS3}$	DQMB3
48	$\overline{WE2}$	DU
62	DU	V_{REF} (IF APPLICABLE)
111	DU	$\overline{CAS}$
112	$\overline{CAS4}$	DQMB4
113	$\overline{CAS5}$	DQMB5
114	$\overline{RAS1}$	$\overline{S1}$
115	DU	$\overline{RAS}$
125	DU	CK1
126	DU	A14
128	DU	CKE
129	$\overline{RAS3}$	$\overline{S3}$
130	$\overline{CAS6}$	DQMB6
131	$\overline{CAS7}$	DQMB7
132	DU	A15
146	DU	V_{REF} (IF APPLICABLE)

Notes:
1. A10 on DRAM DIMM is also AP on SDRAM DIMM
2. A11 on DRAM DIMM is also BS0 on SDRAM DIMM
3. A12 on DRAM DIMM is also BS1 on SDRAM DIMM (for 4 Bank SDRAMs)

FIGURE 4.5.3–E
Pinout Comparison, 168 Pin DRAM & SDRAM DIMM

8 Byte Presence Detect Information

- Serial PD Interface Protocol: IIC (Synchronous 2-Wire Bus)
- The following information is to be written into EEPROM device during module production:

a. Module Configurations, Addressing: (Bytes 3-7)

Module Configuration	DRAM Organization	Option 1		Option 2		Option 3	
		$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.
256K x 64/72/80	256K x 16	9	9				
512K x 64/72/80	256K x 16	9	9				
512K x 64/72/80	512K x 8	10	9				
1M x 64/72/80	512K x 8	10	9				
1M x 64/72/80	1M x 4/16	10	10	12	8		
2M x 64/72/80	1M x 4/16	10	10	12	8		
2M x 64/72/80	2M x 8	11	10	12	9		
4M x 64/72/80	2M x 8	11	10	12	9		
4M x 64/72/80	4M x 4/16	11	11	12	10	*13	9
8M x 64/72/80	4M x 4/16	11	11	12	10	*13	9
8M x 64/72/80	8M x 8	12	11	13	10		
16M x 64/72/80	8M x 8	12	11	13	10		
16M x 64/72/80	16M x 4/16	12	12	13	11	*14	10
32M x 64/72/80	16M x 4/16	12	12	13	11	*14	10
32M x 64/72/80	32M x 8	TBD	TBD				
64M x 64/72/80	32M x 8	TBD	TBD				
64M x 64/72/80	64M x 4	TBD	TBD				

(Note: All options possible with DRAM standards are shown)
* This addressing option applies to x16 DRAM configuration

b. Allowable configurations: (Byte 11)
- x64 (Non-parity, Byte controls)
- x72 (Parity, Byte controls)
- x72 (ECC-optimized, Byte controls)
- x80 (ECC-optimized, Byte controls)

c. Functional Attributes:
- Power Supply Voltage/Interface levels (Byte 8)
- $\overline{RAS}$ access (Byte 9)
- $\overline{CAS}$ access (Byte 10)
- Refresh rate/type (Byte 12)

Figure 4.5.3-F
168 Pin UNBUFFERED DRAM DIMM SPD ASSIGNMENTS

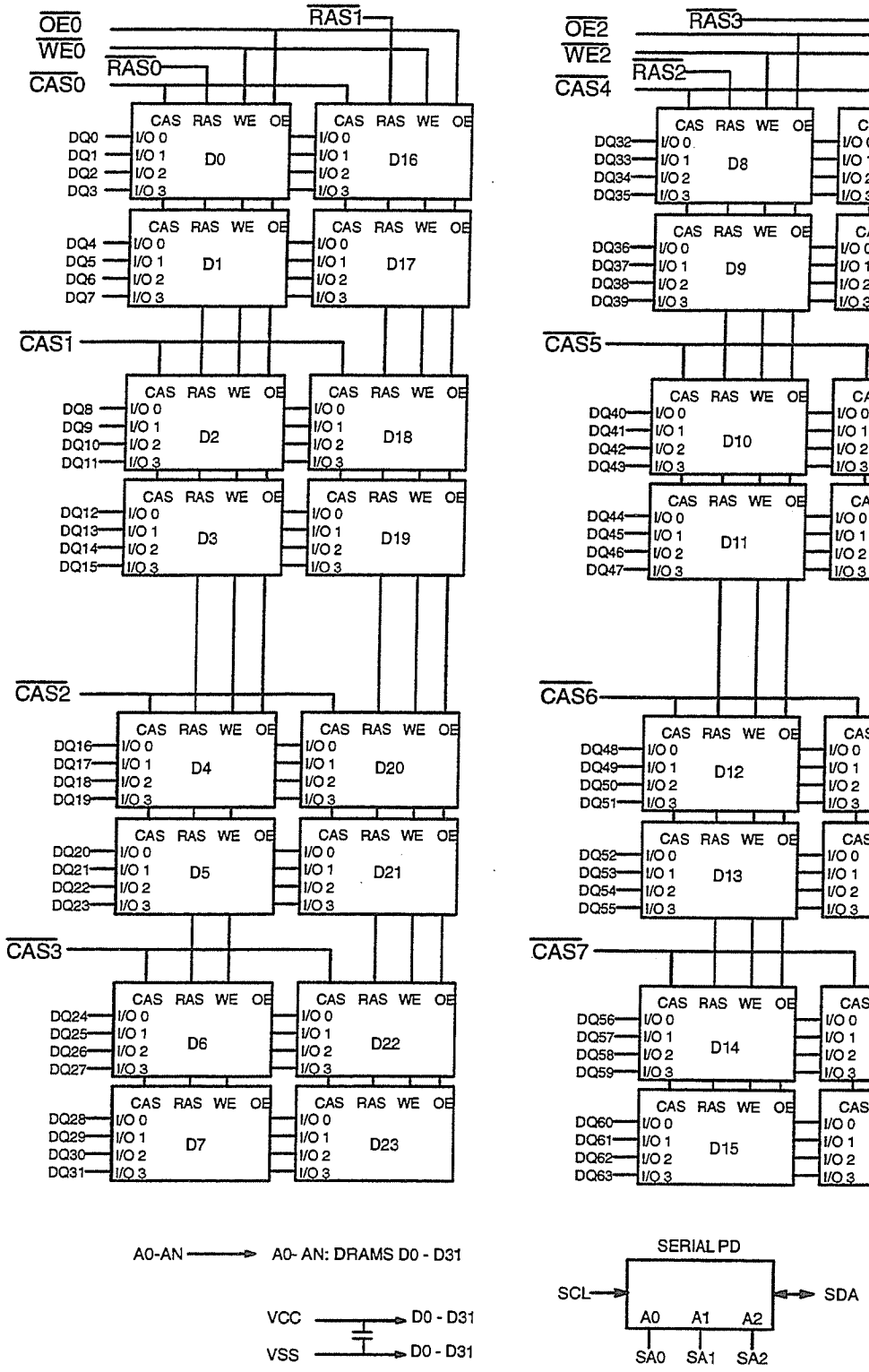


Figure 4.5.3–G
X64 DRAM DIMM, 2 Banks with X4 DRAMs

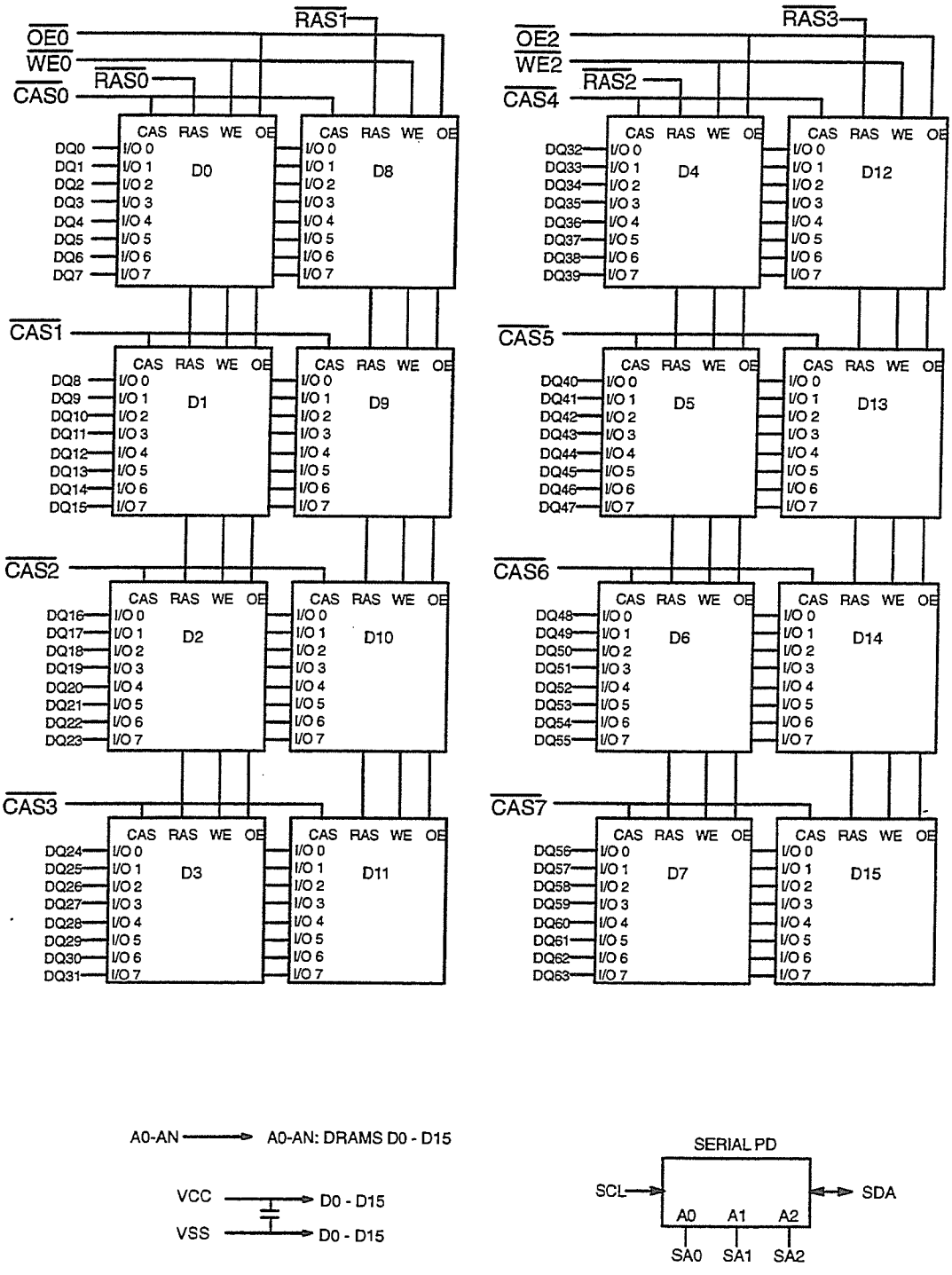


Figure 4.5.3–H
X64 DRAM DIMM, 2 Banks with X8 DRAMs

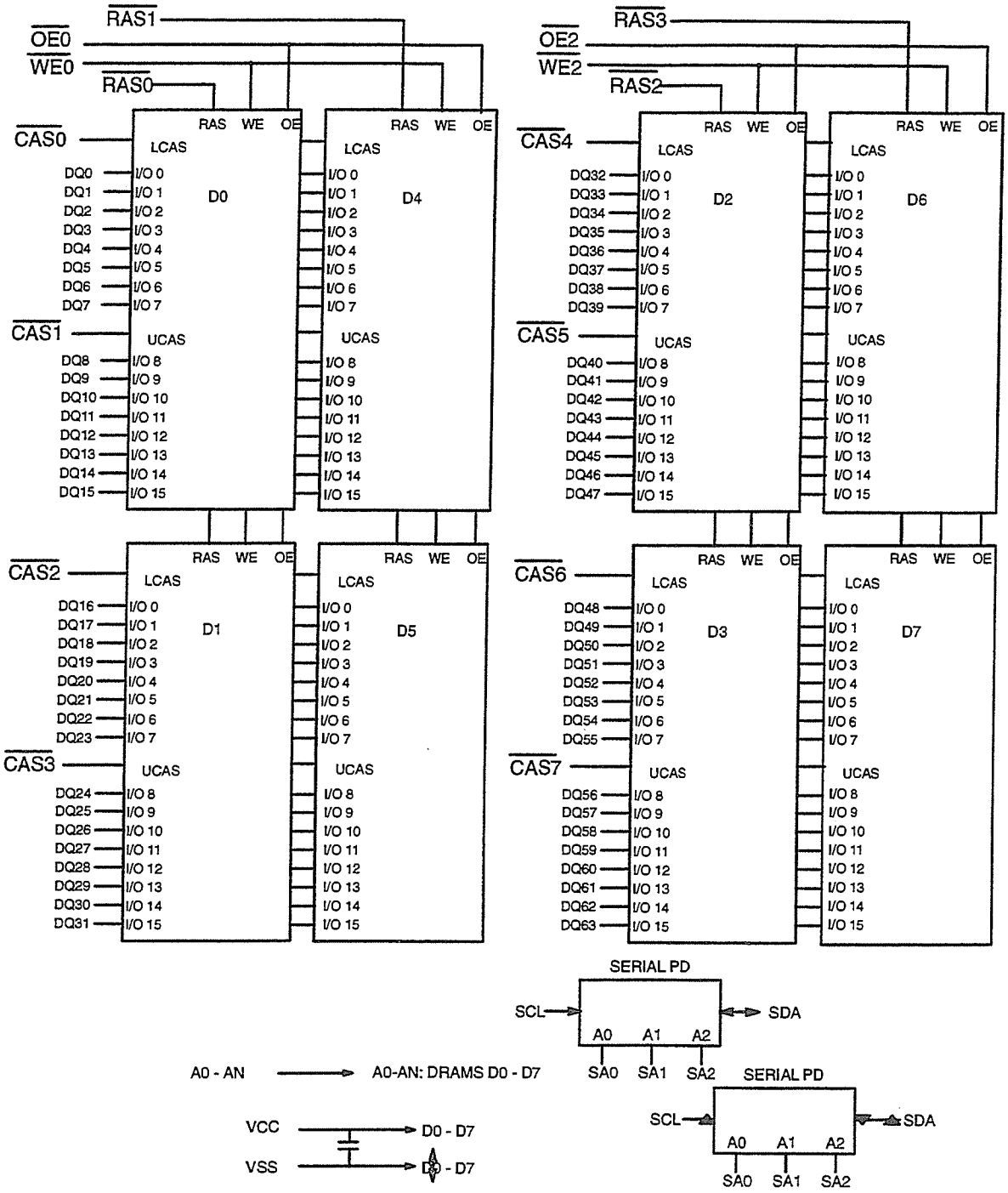


Figure 4.5.3–I
X64 DRAM DIMM, 2 Banks with X16 DRAMs

Release 7

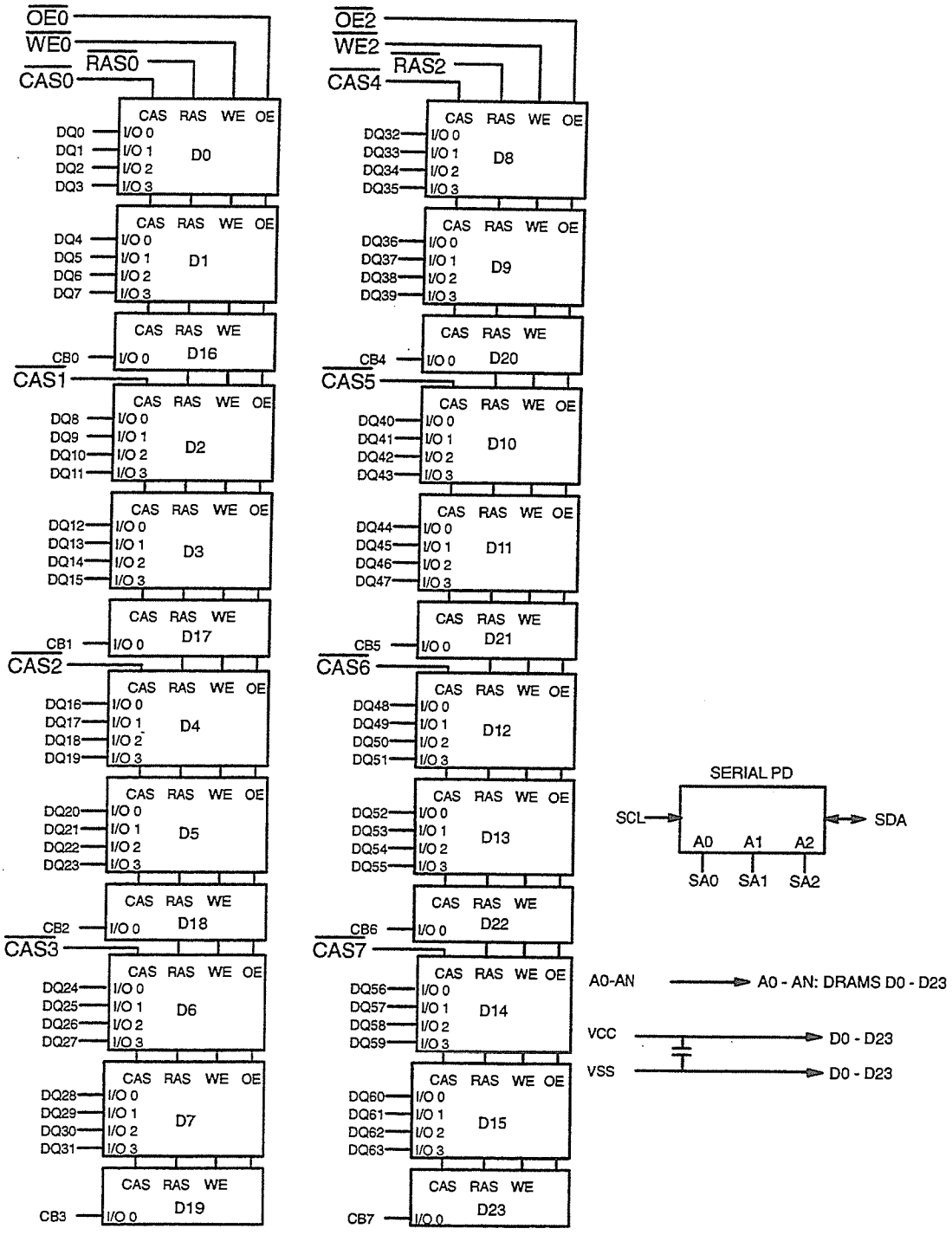


Figure 4.5.3–J
X64 DRAM DIMM, 2 Banks with X4/X1 DRAMs

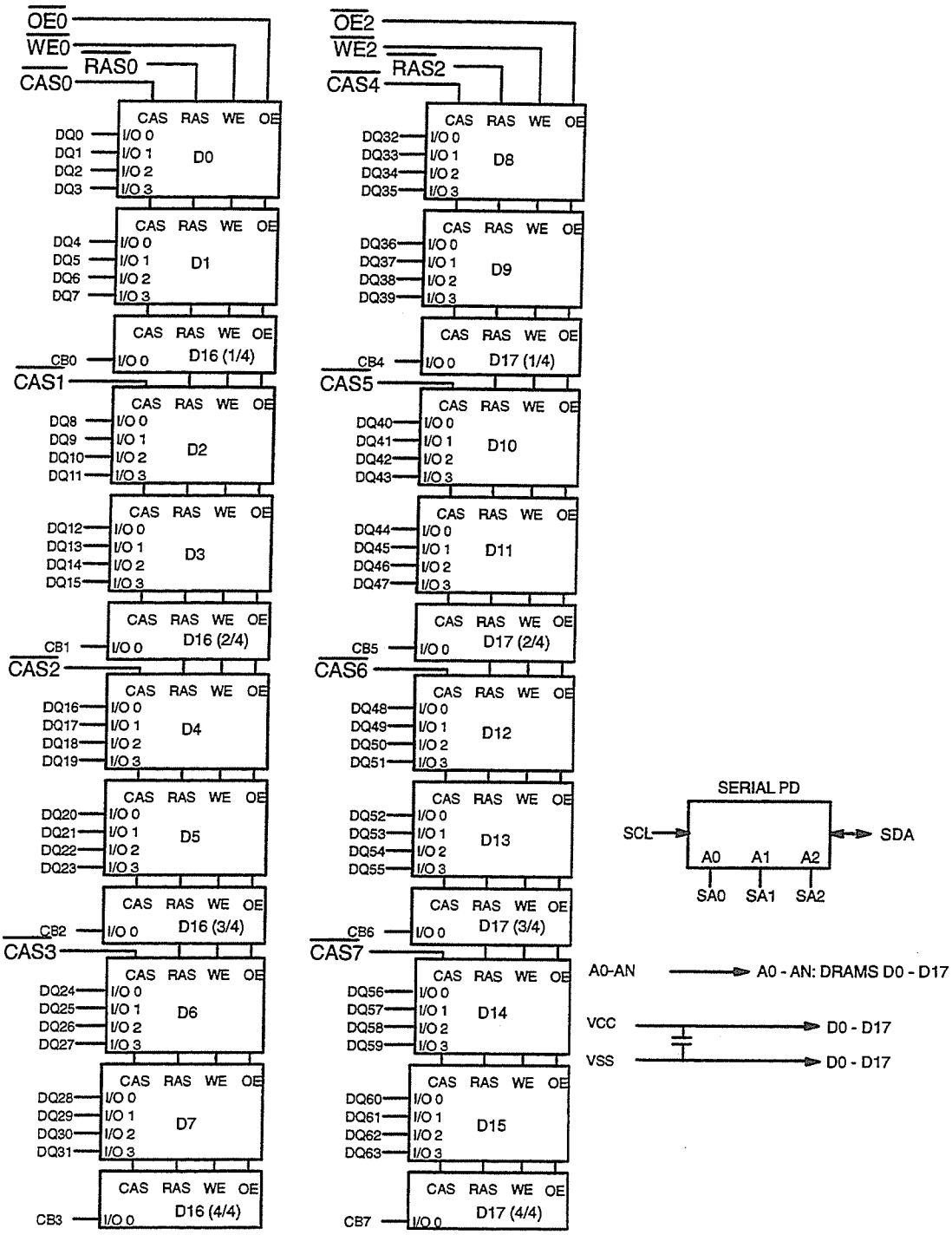


Figure 4.5.3–K
X72 Parity DRAM DIMM, 2 Banks with X4 & X4 W/4 CAS DRAMs

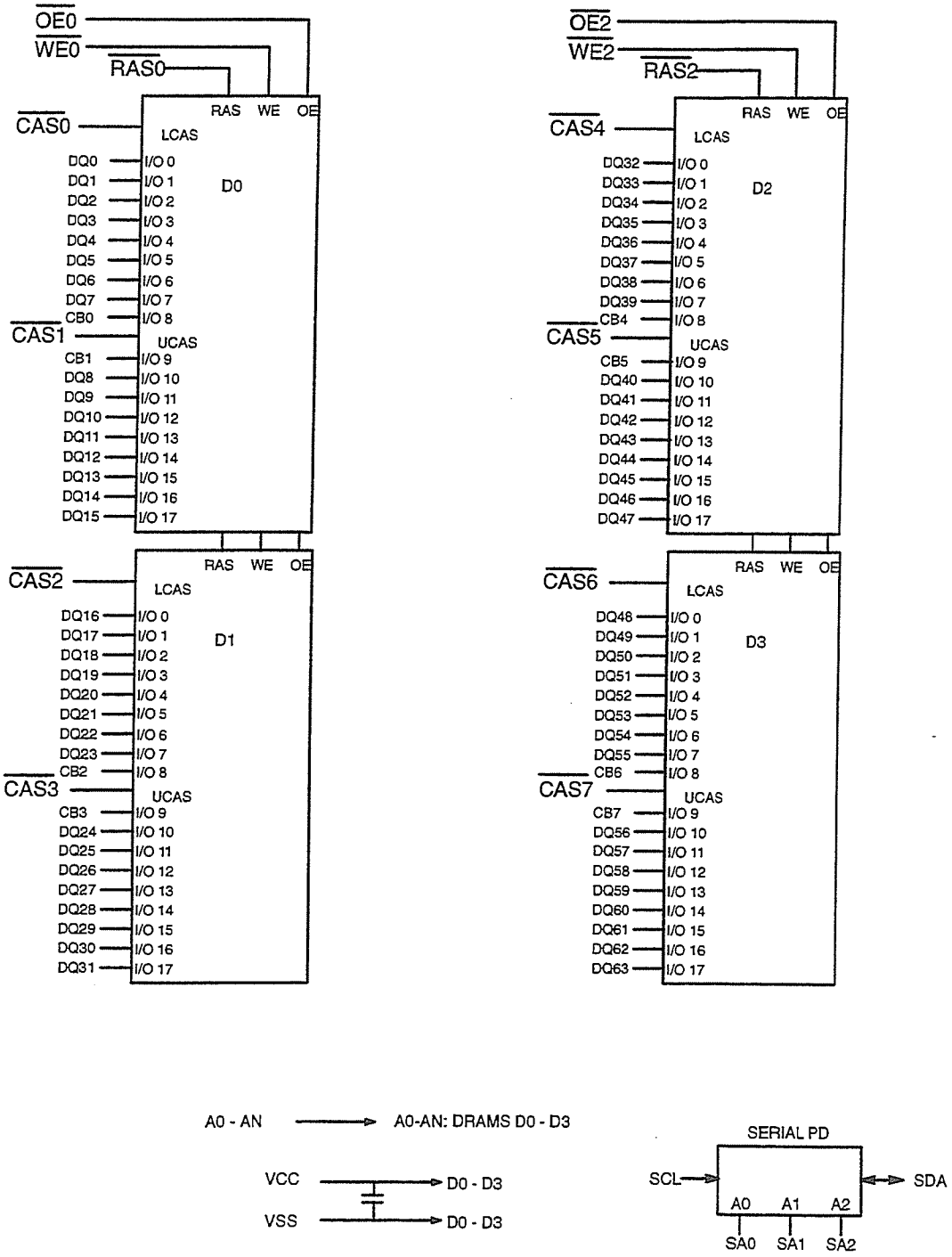


Figure 4.5.3–L
X72 Parity DRAM DIMM, 2 Banks with X16 DRAMs

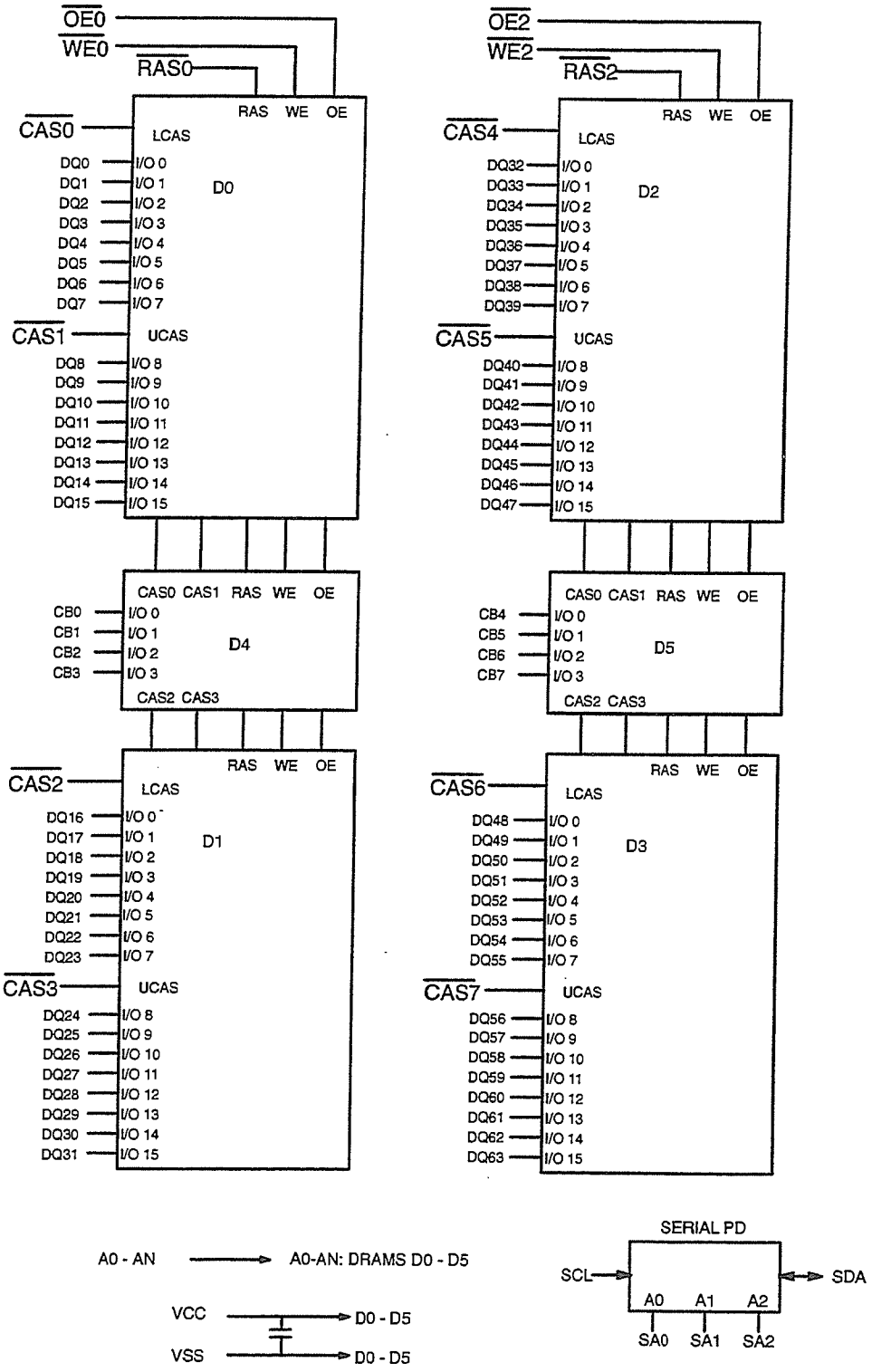


Figure 4.5.3–M
X72 Parity DRAM DIMM, 2 Banks with X16 & X4 W/4 CAS DRAMs

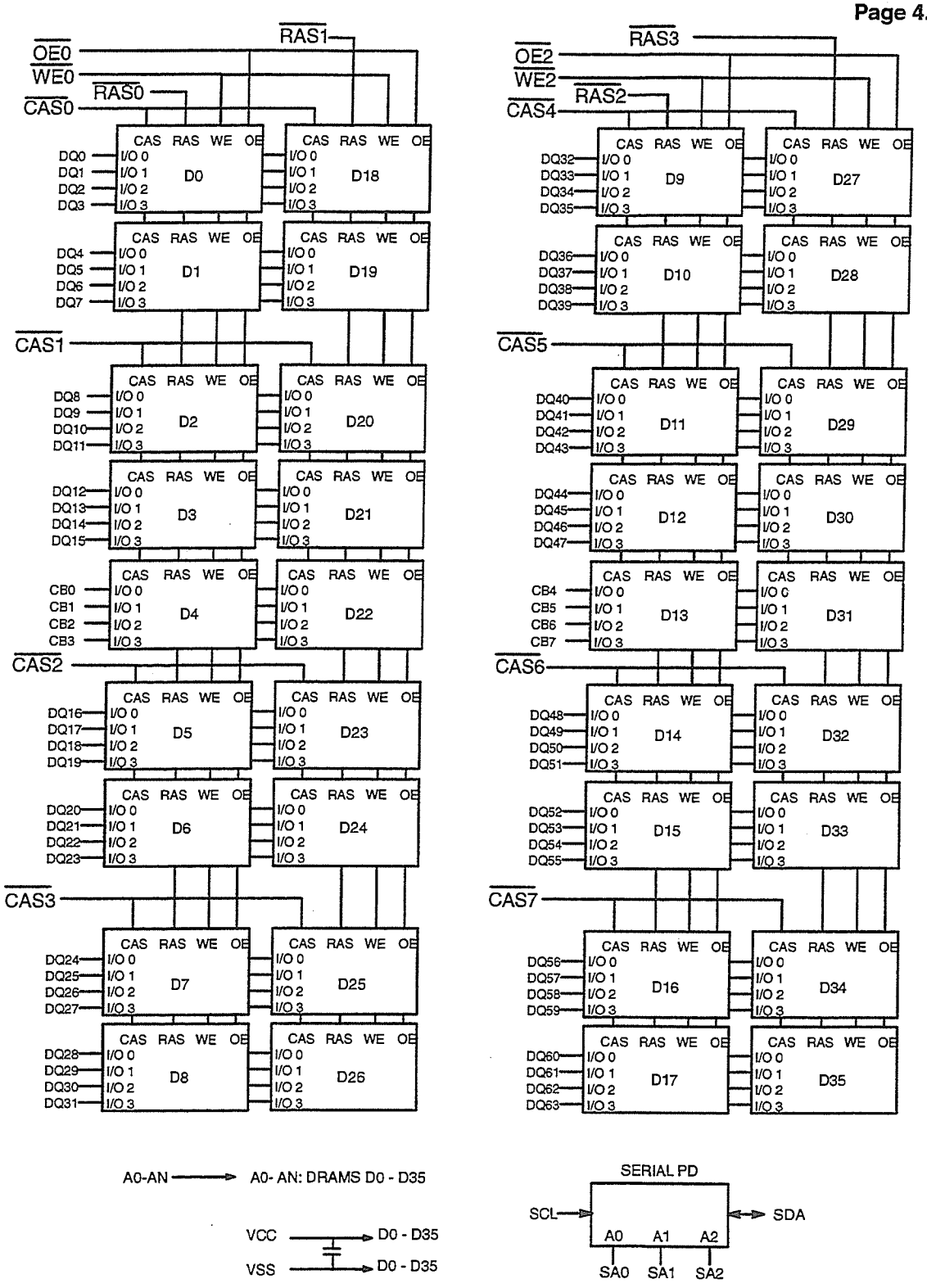


Figure 4.5.3–N
X72 ECC DRAM DIMM, 2 Banks with X4 DRAMs

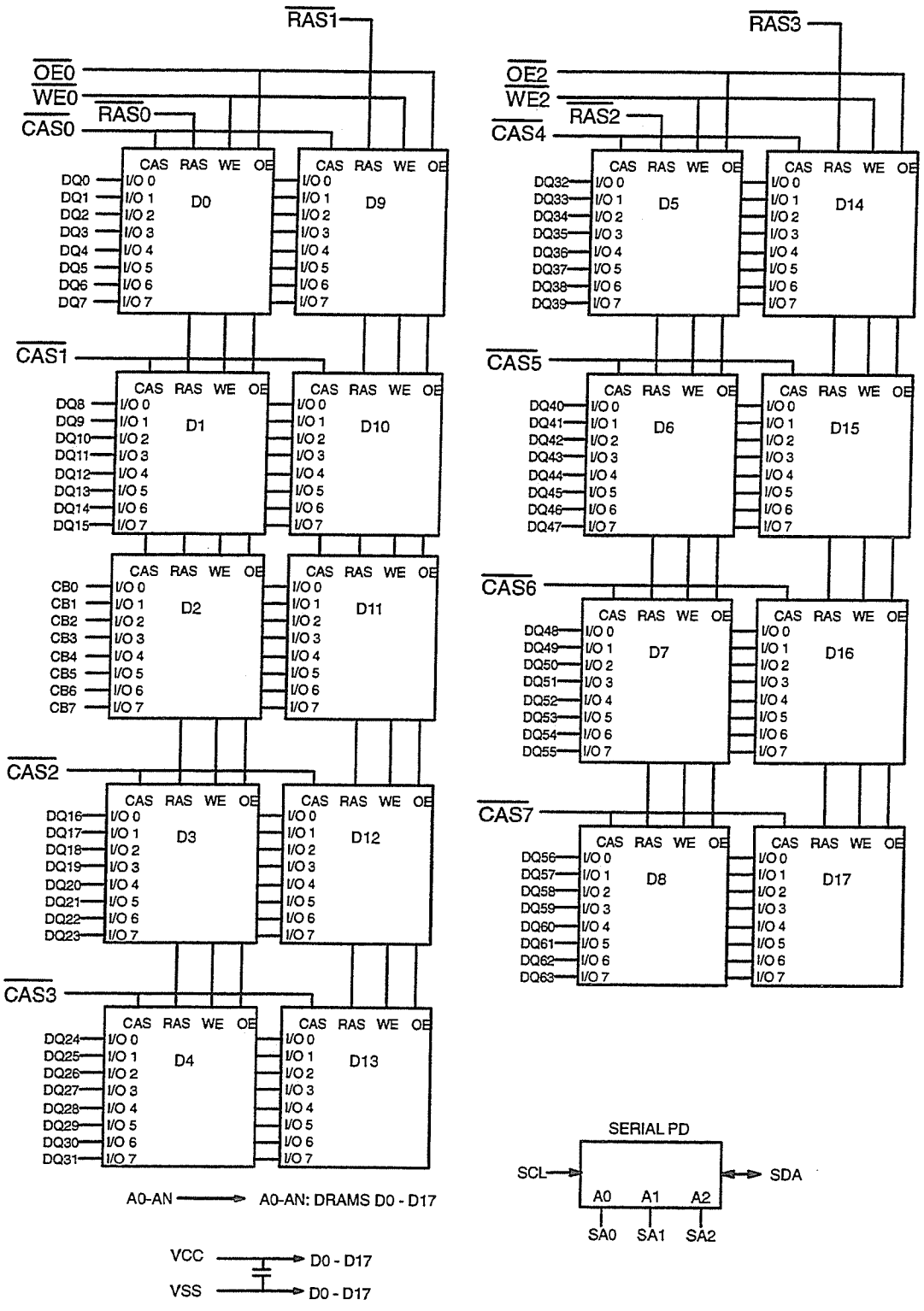


Figure 4.5.3–O
X72 ECC DRAM DIMM, 2 Banks with X8 DRAMs

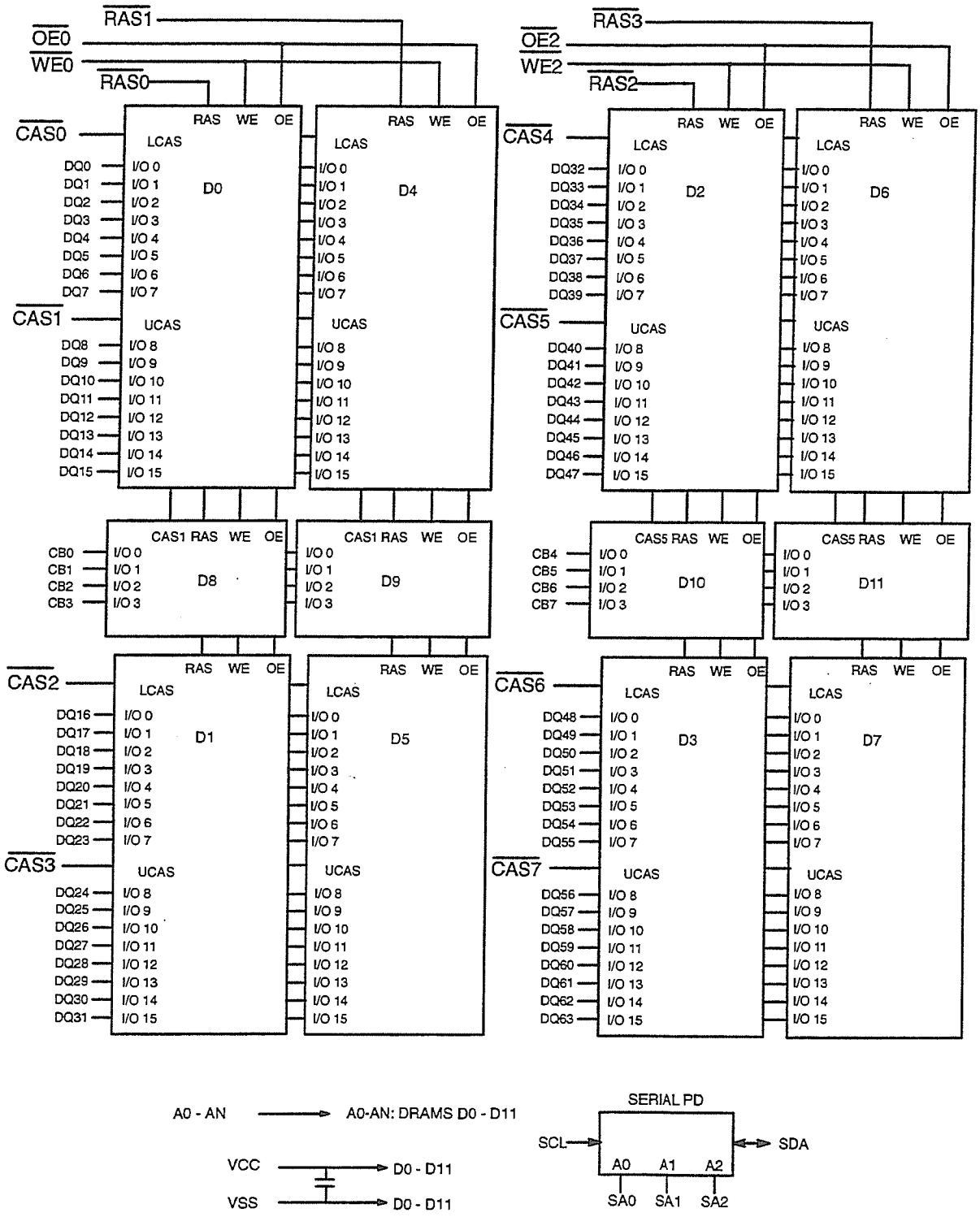


Figure 4.5.3–P
X72 ECC DRAM DIMM, 2 Banks with X16 & X4 DRAMs

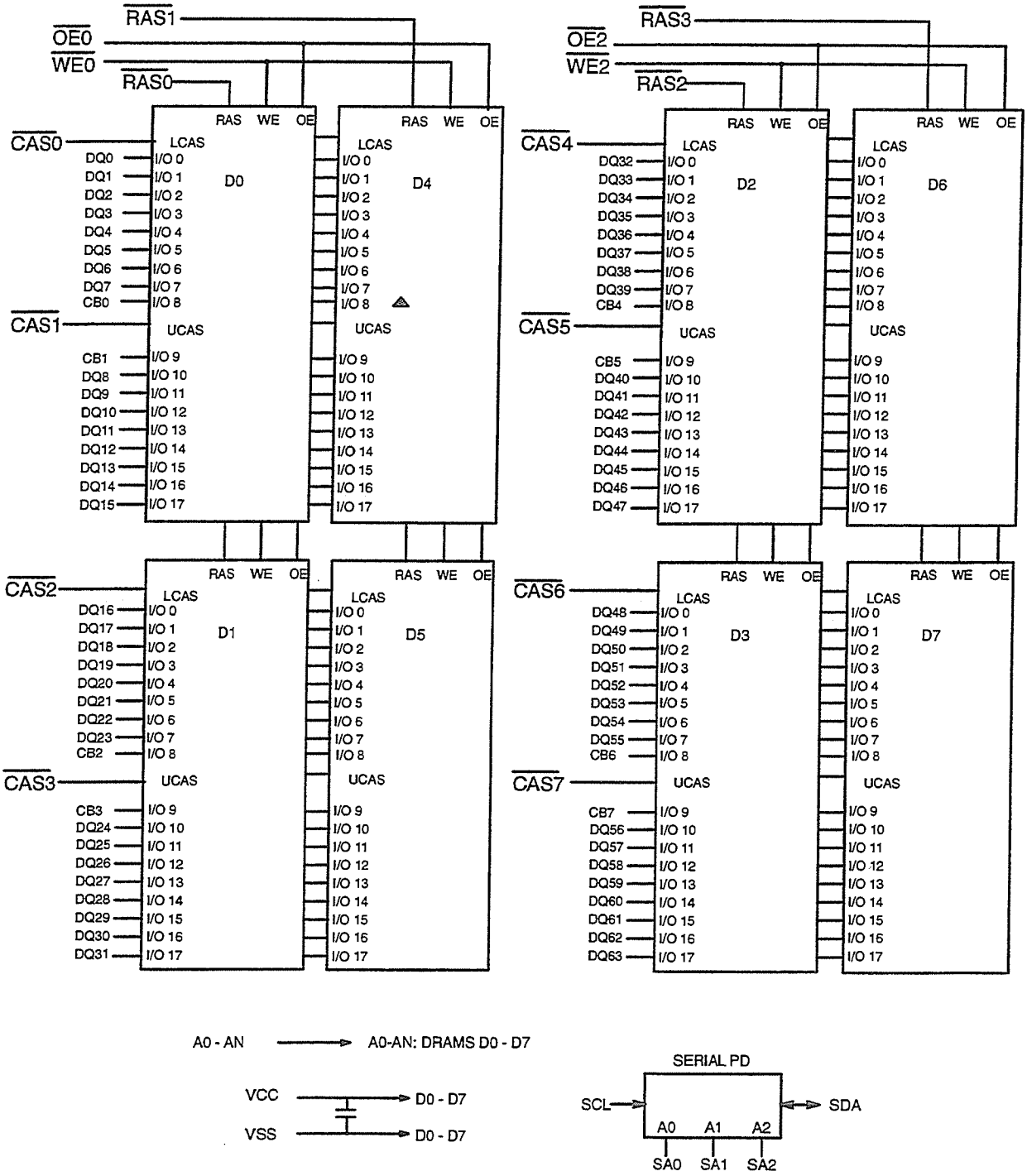


Figure 4.5.3–Q
X72 ECC DRAM DIMM, 2 Banks with X18 DRAMs

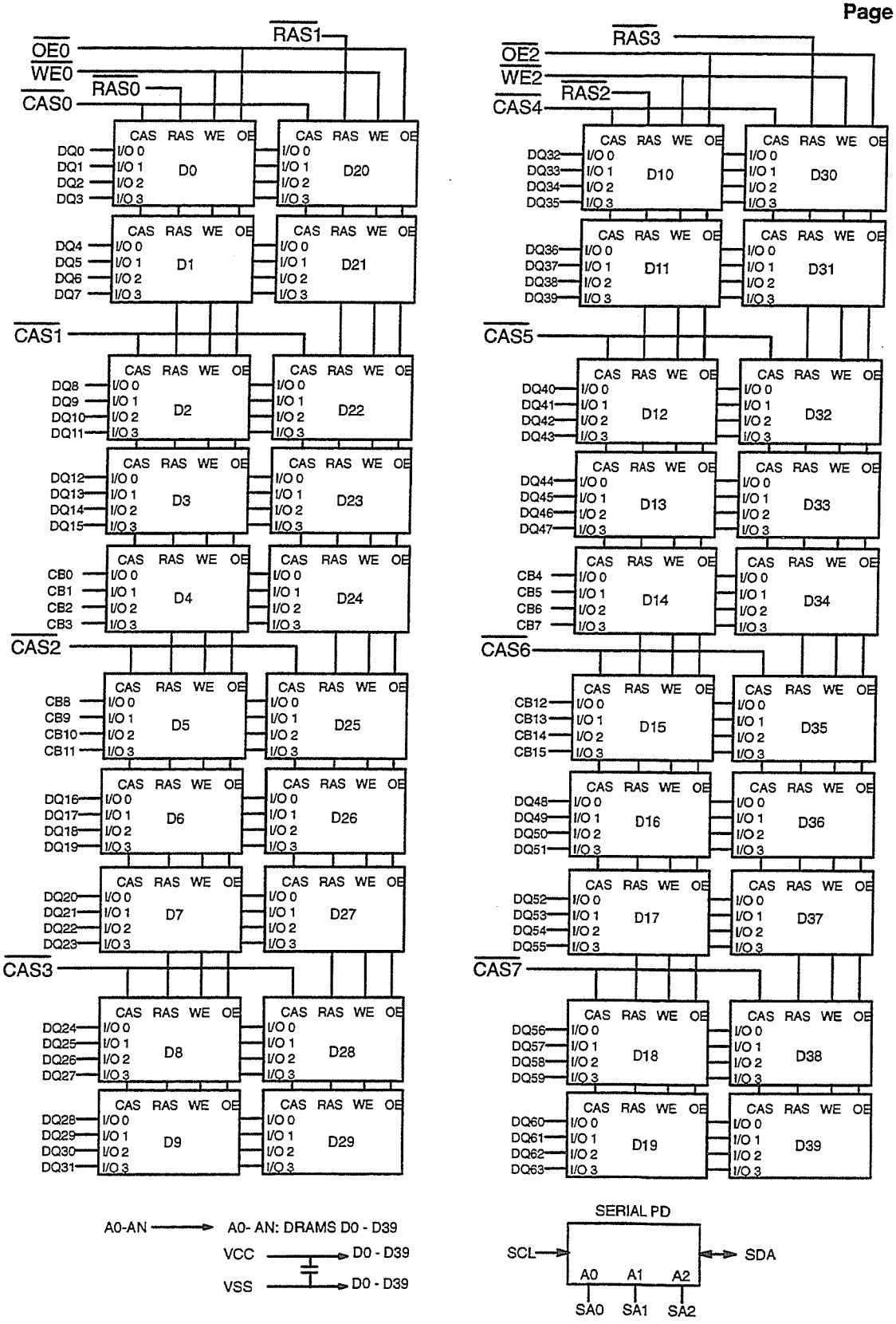


Figure 4.5.3–R
X80 DRAM DIMM, 2 Banks with X4 DRAMs

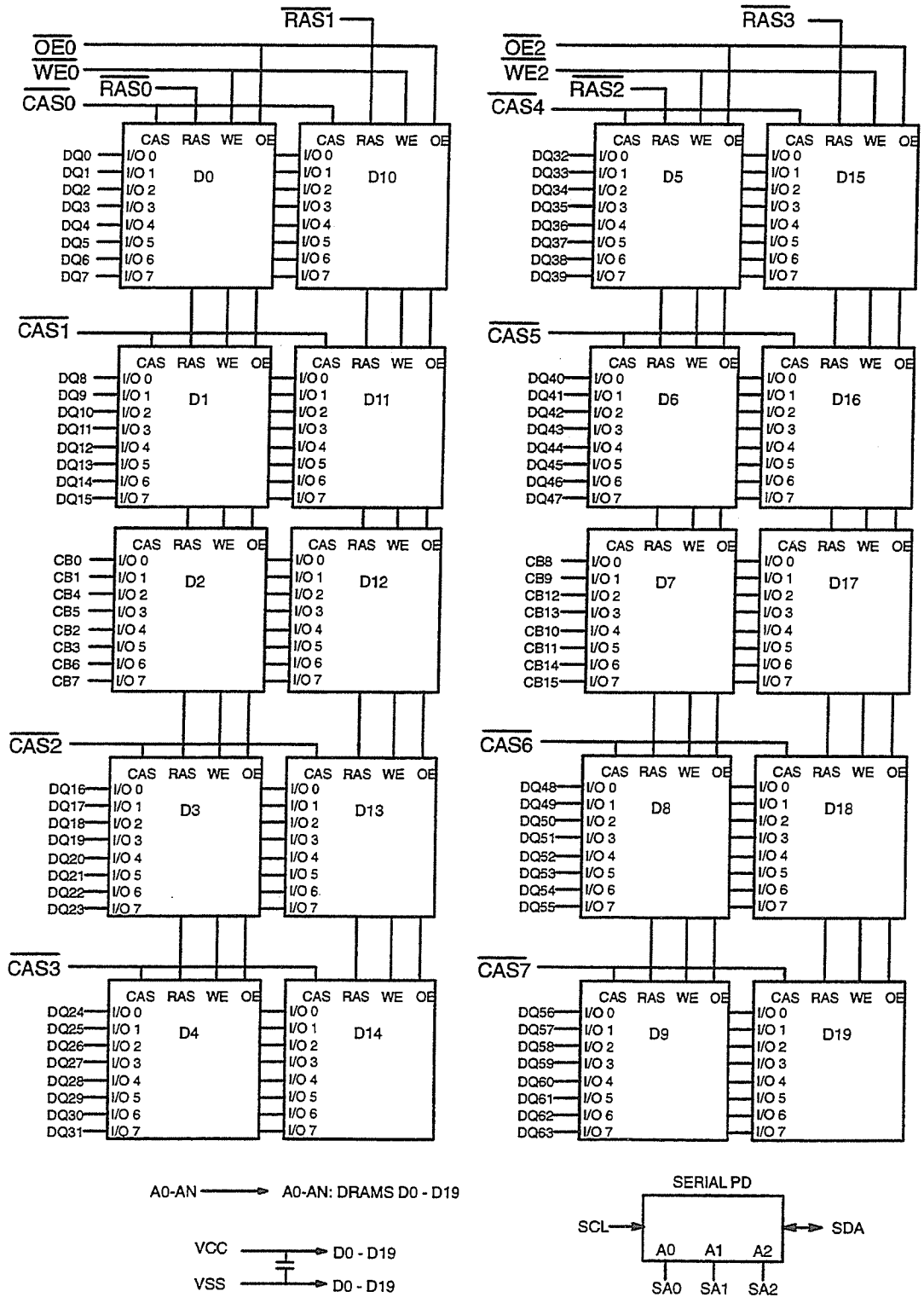


Figure 4.5.3–S
X80 ECC DRAM DIMM, 2 Banks with X8 DRAMs

4.5.4 – 168 PIN UNBUFFERED SDRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS
DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES
CONFIGURATION—21 Different Configurations are defined using various combinationa of X1, X4, X8, X9, X16 and X18 memories including 2 bank configurations using X4 devices.
LOGIC FEATURES—The modules contain "PRESENCE DETECT" and "IDENTITY" featurs that conist of output pins in the PDn and IDn fields which supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS—Figs. 4.5.4–A, & 4.5.4–B,
SPD TABLE & INFORMATION—Fig. 4.5.4–C
Comparison of 168 Pin Buffered & Unbuffered DRAM & SDRAM DIMM—Fig. 4.5.4–D
KEYING METHODOLOGY—Fig. 4.5.4–E
PINOUT COMPARISON DRAM & SDRAM DIMM—Fig. 4.5.4–F
SDRAM CLOCK LOADING—Fig. 4.5.4–G
SDRAM CLOCK WIRING—Fig. 4.5.4–H
CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.4–I through 4.5.4–Y

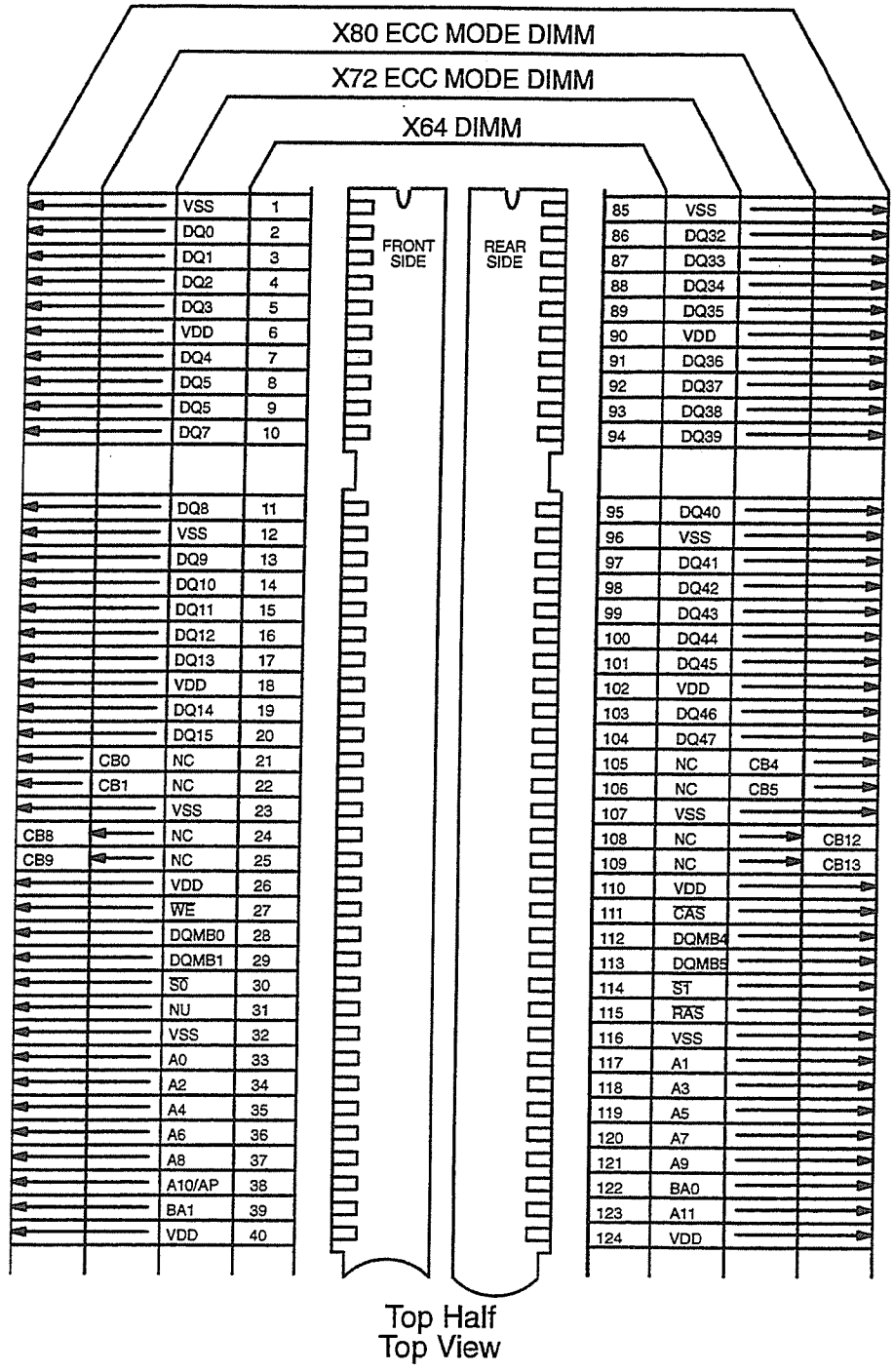


FIGURE 4.5.4–A

168 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, TOP HALF

Release 7

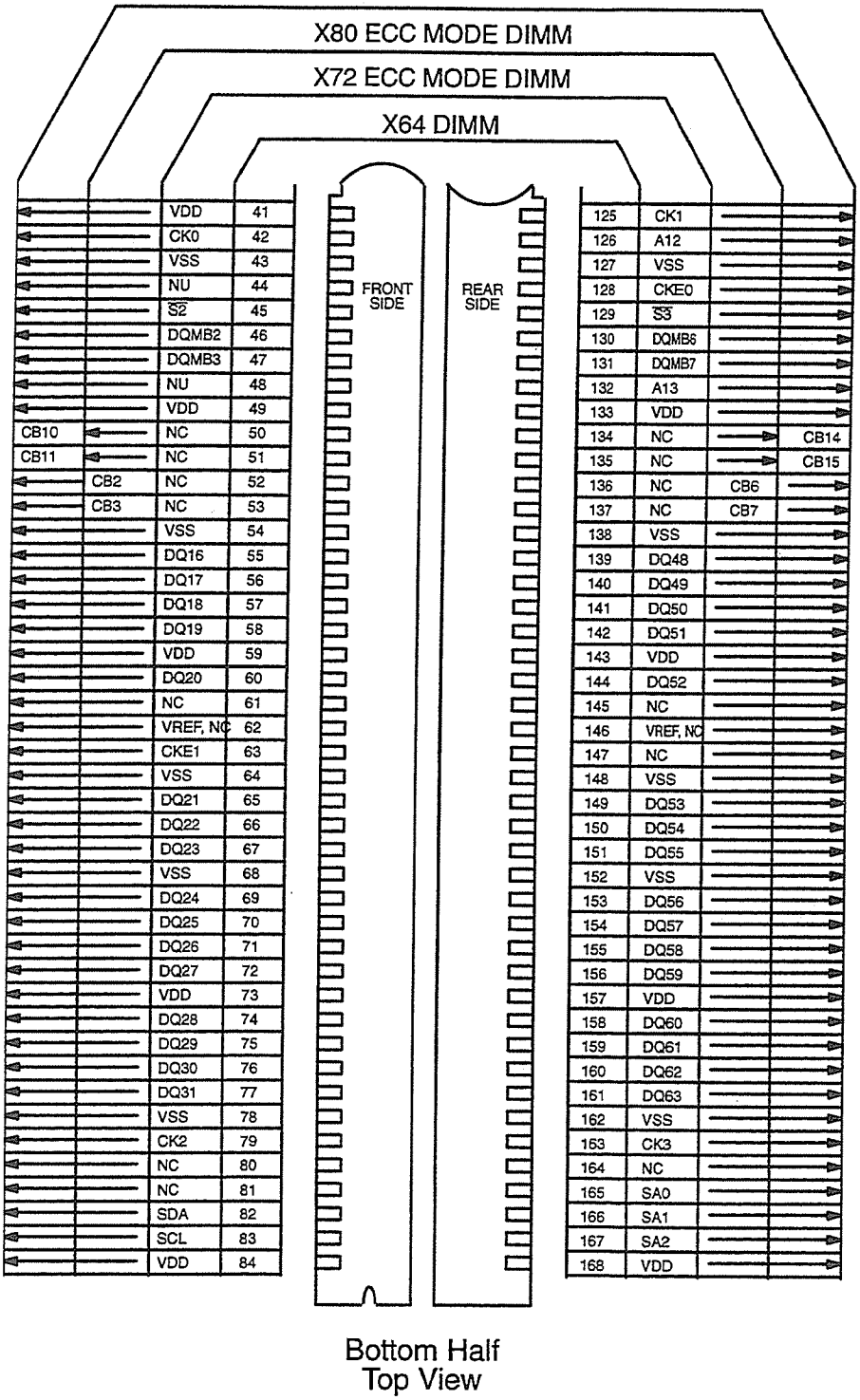


FIGURE 4.5.4–B
168 PIN, 64, 72, or 80 BIT SDRAM DIMM PINOUT, BOTTOM HALF

Module Configuration	SDRAM Organization	Option 1			Option 2			Option 3		
		# Bank accr.	$\overline{RAS}$ accr.	$\overline{CAS}$ accr.	# Bank accr.	$\overline{RAS}$ accr.	$\overline{CAS}$ accr.	# Bank accr.	$\overline{RAS}$ accr.	$\overline{CAS}$ accr.
1M x 64/72/80	1M x 16	1	11	8						
2M x 64/72/80	1M x 16	1	11	8						
2M x 64	2M x 32	2	11	8						
2M x 64/72/80	2M x 8	1	11	9						
4M x 64/72/80	2M x 8	1	11	9						
4M x 64	2M x 32	2	11	8						
4M x 64/72/80	4M x 4	1	11	10						
4M x 64/72/80	4M x 16	2	12	8	1	13	8			
8M x 64/72/80	4M x 16	2	12	8	1	13	8			
8M x 64	8M x 32	2	13	8	2	12	9			
8M x 64/72/80	8M x 8	2	12	9	1	13	9			
16M x 64/72/80	8M x 8	2	12	9	1	13	9			
16M x 64	8M x 32	2	13	8	2	12	9			
16M x 64/72/80	16M x 4	2	12	10	1	13	10			
16M x 64/72/80	16M x 16	2	13	9						
32M x 64/72/80	16M x 16	2	13	9						
32M x 64/72/80	32M x 8	2	13	10						
64M x 64/72/80	32M x 8	2	13	10						
64M x 64/72/80	64M x 4	2	13	11						
(Note: All options possible with SDRAM standards are shown)										

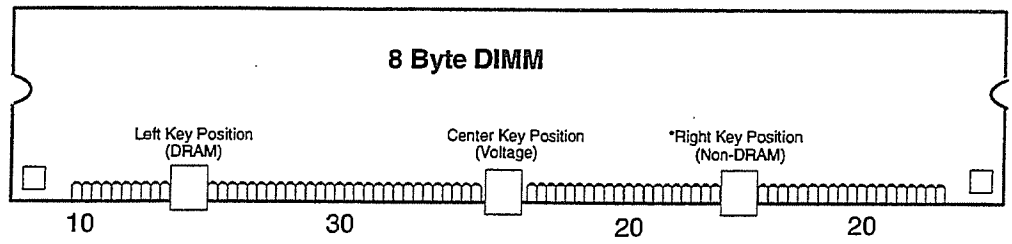
b. Allowable configurations: (Byte 11)
   - x64 (Non-parity, Byte controls)
   - x72 (ECC-optimized, Byte controls)
   - x80 (ECC-optimized, Byte controls)

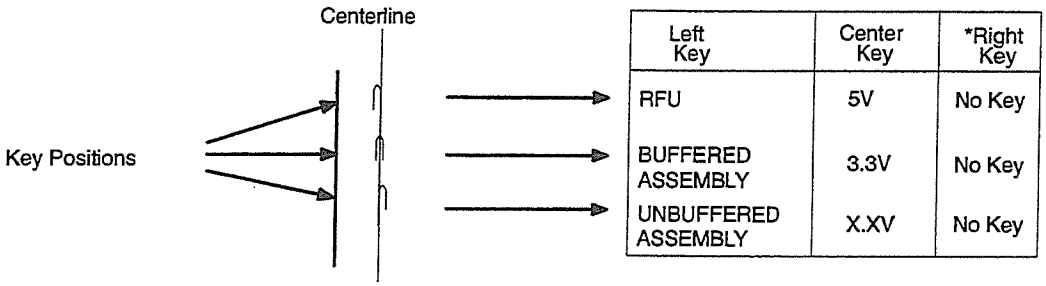
c. Functional Attributes:
   - Power Supply Voltage/Interface levels (Byte 8)
   - SDRAM cycle time (Byte 9)
   - SDRAM access from Clock (Byte 10)
   - Refresh rate/type (Byte 12)
   - SDRAM module attributes (Byte 13)
   - SDRAM device attributes (Bytes 14 - 20)
   - Primary/Secondary DRAM (Bytes 21 - 22)

Figure 4.5.4–C
168 Pin UNBUFFERED DRAM DIMM SPD ASSIGNMENTS

Buffered	Unbufffered
All signals except RAS and Data are buffered	No buffers, all DRAM signals are connected directly to DIMM tab pins
11 Pins are used for DIMM attributes (PDE, PD1-8, ID0-1)	5 pins are used for DIMM attributes (SDA, SCL, SA0-2)
CAS Pin assignment sequence optimized for buffer placement 0, 1 2, 3 4, 5 6, 7	CAS Pin signals are re-assigned for optimal DRAM placement 0, 4 1, 5 2, 6 3, 7
ECC DIMMs use subset of CAS signals for word selection (CAS0/1 and CAS4/5)	All DIMM types use byte selection (CAS0-7)
Address 0 to the DRAMs is sourced from separate pins (A0, B0) for 4 byte interleave	Single address pin (A0)
Data pin assignment uses both X64/X72 and X80 numbering schemes	Data pin assignment is changed to single x80 numbering scheme with x64 and x72 as subsets
Non-Parity is subset of Parity with inter-mixed Parity bits unconnected (PQ8, 17, 26, 35, 44, 53, 62, 71)	All DIMM types use the same sequential 64 data pins (DQ0-63). Eight center pins (CB0-7) are used as Parity/Check Bits for x72 Parity/ECC DIMMs. An additional 8 center pins (CB8-15) are used for the x80 ECC DIMMs.
32 Power/Gnd Pins VCC - 16 VSS - 16	35 Power/Gnd Pins VCC - 17 (1 additional pin) VSS - 18 (2 additional pins)
Unused Pins - 18	Unused Pins - 14
Left Key Definition SDRAM STD DRAM RFU	Left Key Definition modified RFU Buffered Assembly (DRAM/SDRAM) Unbuffered Assembly (DRAM/SDRAM)

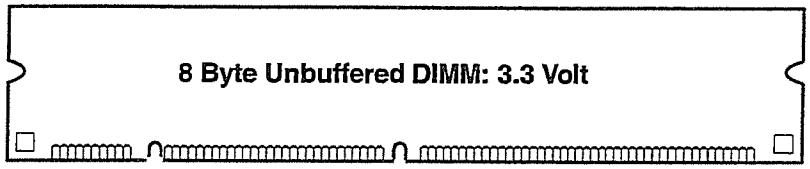
FIGURE 4.5.4–D
Comparison of 168 Pin Buffered & Unbuffered DRAM & SDRAM DIMM





Left Key	Center Key	*Right Key
RFU	5V	No Key
BUFFERED ASSEMBLY	3.3V	No Key
UNBUFFERED ASSEMBLY	X.XV	No Key

* For DRAM/SDRAM assemblies, this area is poplulated with pads.



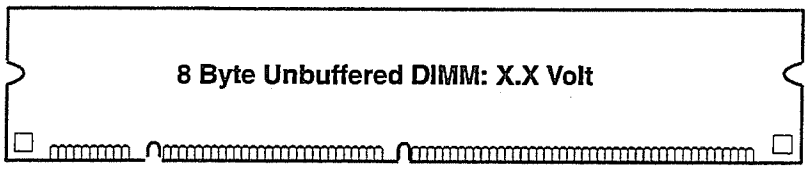


FIGURE 4.5.4–E
168 Pin DRAM DIMM Keying Methodology

Pin number	DRAM DIMM	SDRAM DIMM
39	A12	BA1
42	DU	CK0
44	$\overline{OE}$2	DU
45	$\overline{RAS}$2	$\overline{S}$2
46	$\overline{CAS}$2	DQMB2
47	$\overline{CAS}$3	DQMB3
48	$\overline{WE}$2	DU
62	DU	V_{REF}, NC
63	NC	CKE1
79	NC	CK2
111	DU	$\overline{CAS}$
112	$\overline{CAS}$4	DQMB4
113	$\overline{CAS}$5	DQMB5
114	$\overline{RAS}$1	$\overline{S}$1
115	DU	$\overline{RAS}$
122	A11	BA0
123	A13	A11
125	DU	CK1
126	DU	A12
128	DU	CKE0
129	$\overline{RAS}$3	$\overline{S}$3
130	$\overline{CAS}$6	DQMB6
131	$\overline{CAS}$7	DQMB7
132	DU	A13
146	DU	V_{REF}, NC
163	NC	CK3

Notes:
1. A10 on DRAM DIMM is also AP on SDRAM DIMM

FIGURE 4.5.4–F
Pinout Comparison, 168 Pin DRAM & SDRAM DIMM

X 64 (Non–parity)						
			CLK Loading			
SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CK0	CK1	CK2	CK3
x4	1	16	4	4	4	4
x8	1	8	4	4	*	*
x16	1	4	4	*	*	*
x32	1	2	*2	*	*	*
x8	2	16	4	4	4	4
x16	2	8	4	4	*	*
x32	2	4	4	*	*	*

X 72 (ECC)						
			CLK Loading			
SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CK0	CK1	CK2	CK3
x4	1	18	** 4 or 5	** 4 or 5	** 4 or 5	** 4 or 5
x8	1	9	** 4 or 5	** 4 or 5	*	*
x16/x4	1	6	4 (MAX)	4 (MAX)	*	*
x32/x8	1	3	*3	*	*	*
x8	2	18	** 4 or 5	** 4 or 5	** 4 or 5	** 4 or 5
x16/x4	2	12	4	4	4	
x32/x8	2	6	4 (MAX)	4 (MAX)	*	*

X 80 (ECC)						
			CLK Loading			
SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CK0	CK1	CK2	CK3
x4	1	20	5	5	5	5
x8	1	10	5	5	*	*
x16	1	5	5	*	*	*
x32/x8	1	4	4	*	*	*
x8	2	20	5	5	5	5
x16	2	10	5	5	*	*
x32/x8	2	8	4	4	*	*

Notes:

* add padding capacitance per clock wiring detail.

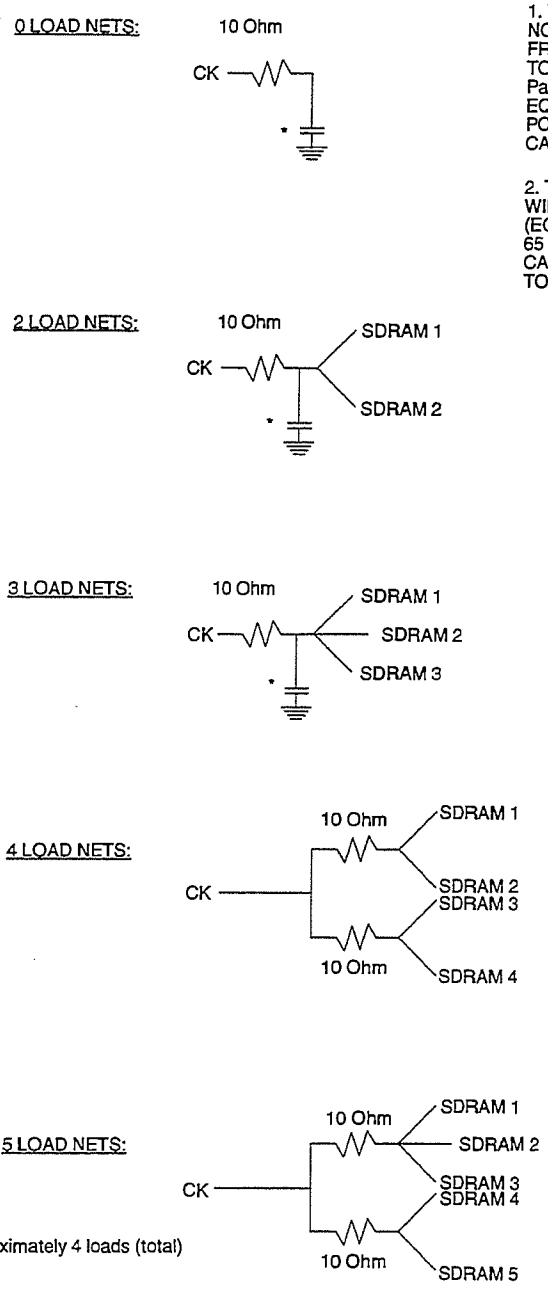
** CK0 + CK2 must total 9 SDRAMs, CK1 + CK3 must total 9 SDRAMs (to allow clock "dotting" at system).

Figure 4.5.4–G
168 Pin UNBUFFERED SDRAM DIMM CLOCK LOADING

TARGET CLOCK (CK) SPECIFICATION:

1. THE CK INPUTS SHOULD HAVE A NOMINAL DELAY OF .6ns MEASURED FROM THE CK INPUT AT THE DIMM TAB TO THE CK INPUT OF THE SDRAM (OR PaccING CAPACITOR). (EG: THIS IS EQUIVALENT TO APPROXIMATELY 3" OF PCB WIRE AND 2.5pf OF INPUT CAPACITANCE).

2. THE VARIATION OF CK INPUT DELAY WILL BE +/- .1ns FOR ALL FOUR CK INPUTS. (EG: IF THE WIRE IMPEDANCE IS APPROX. 65 ohms, THIS CORRESPONDS TO A CAPACITANCE VARIATION OF +/- 3pf IN TOTAL CK INPUT CAPACITANCE).



* add padding capacitance to approximately 4 loads (total)

Figure 4.5.4–H
168 Pin UNBUFFERED DRAM DIMM CLOCK WIRING

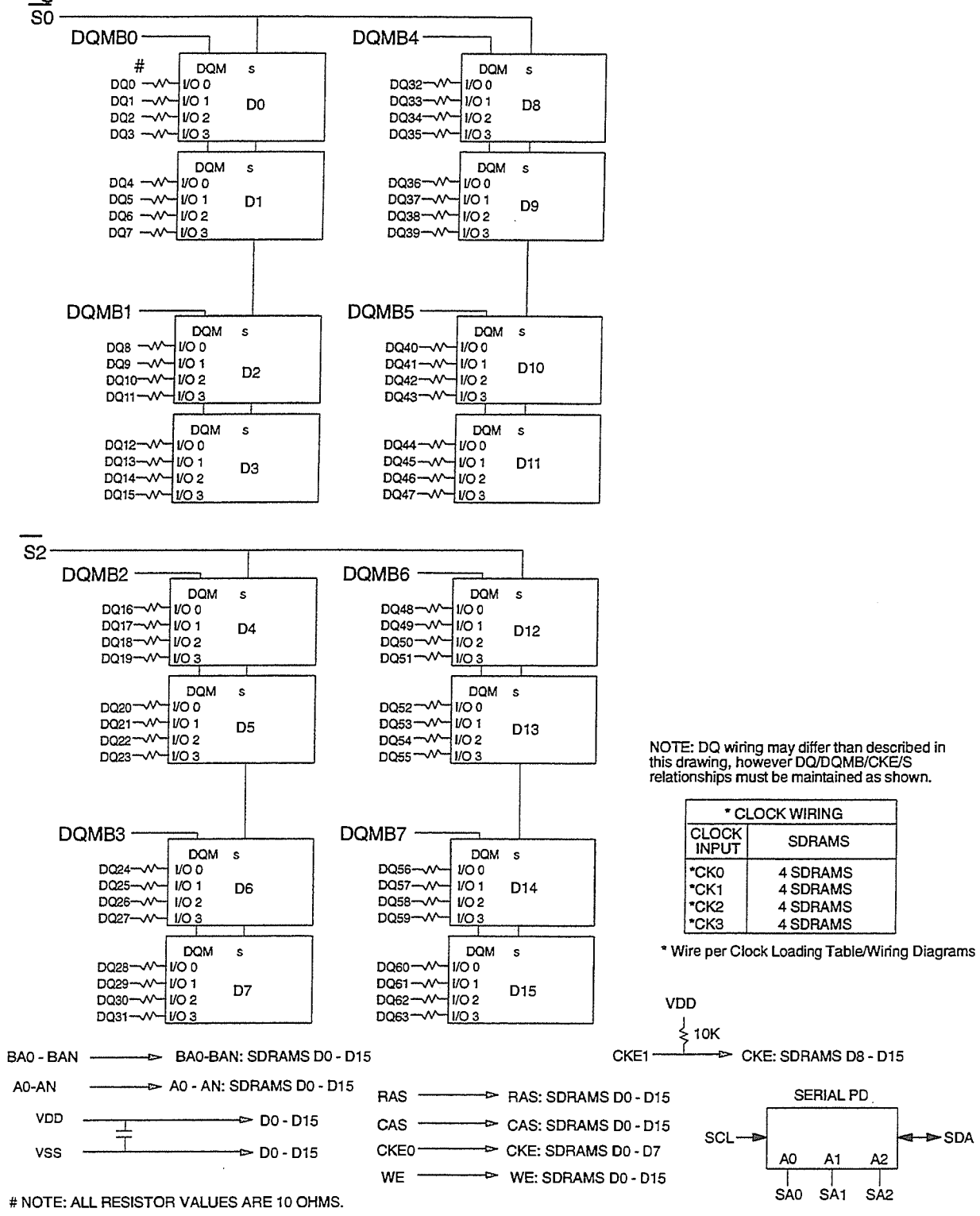


Figure 4.5.4–I
X64 SDRAM DIMM, 1 Bank with X4 SDRAMs

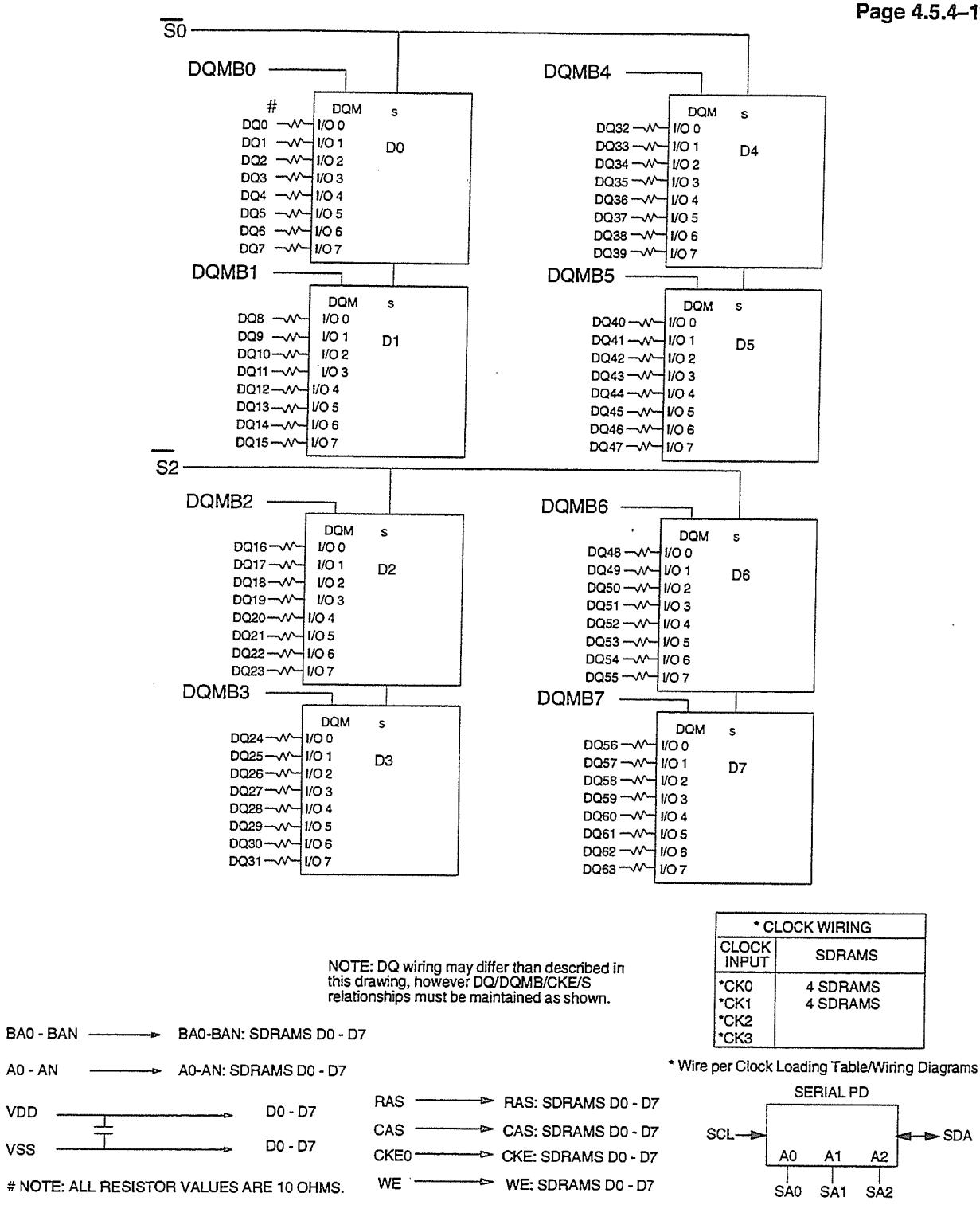
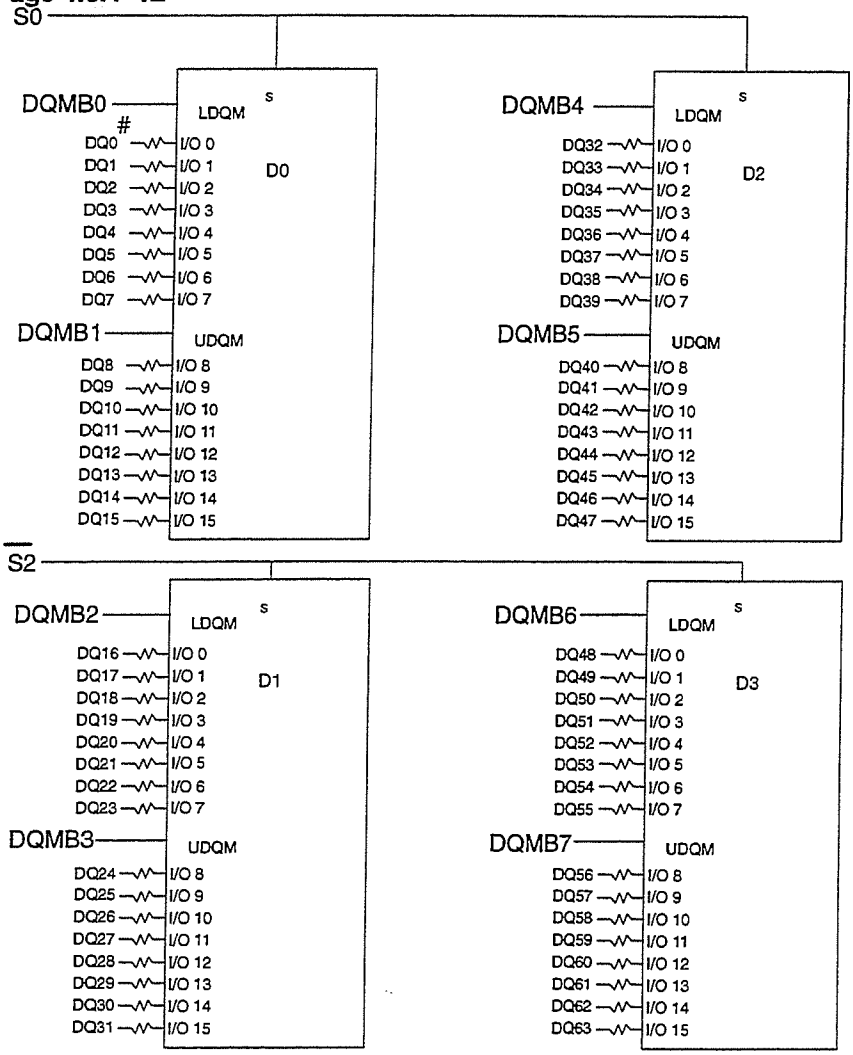
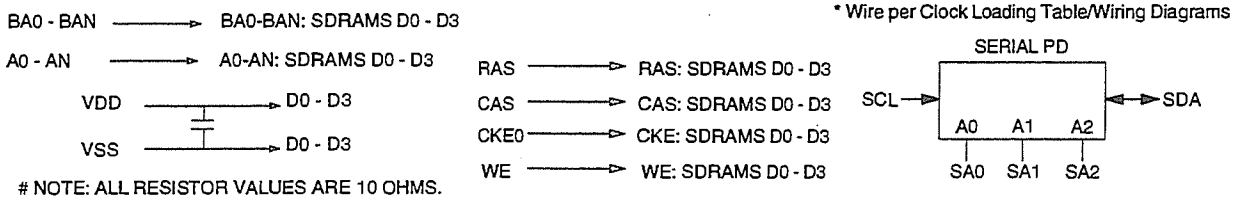


Figure 4.5.4–J
X64 SDRAM DIMM, 1 Bank with X8 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1 *CK2 *CK3	4 SDRAMS



NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.4–K
X64 SDRAM DIMM, 1 Bank with X16 SDRAMs

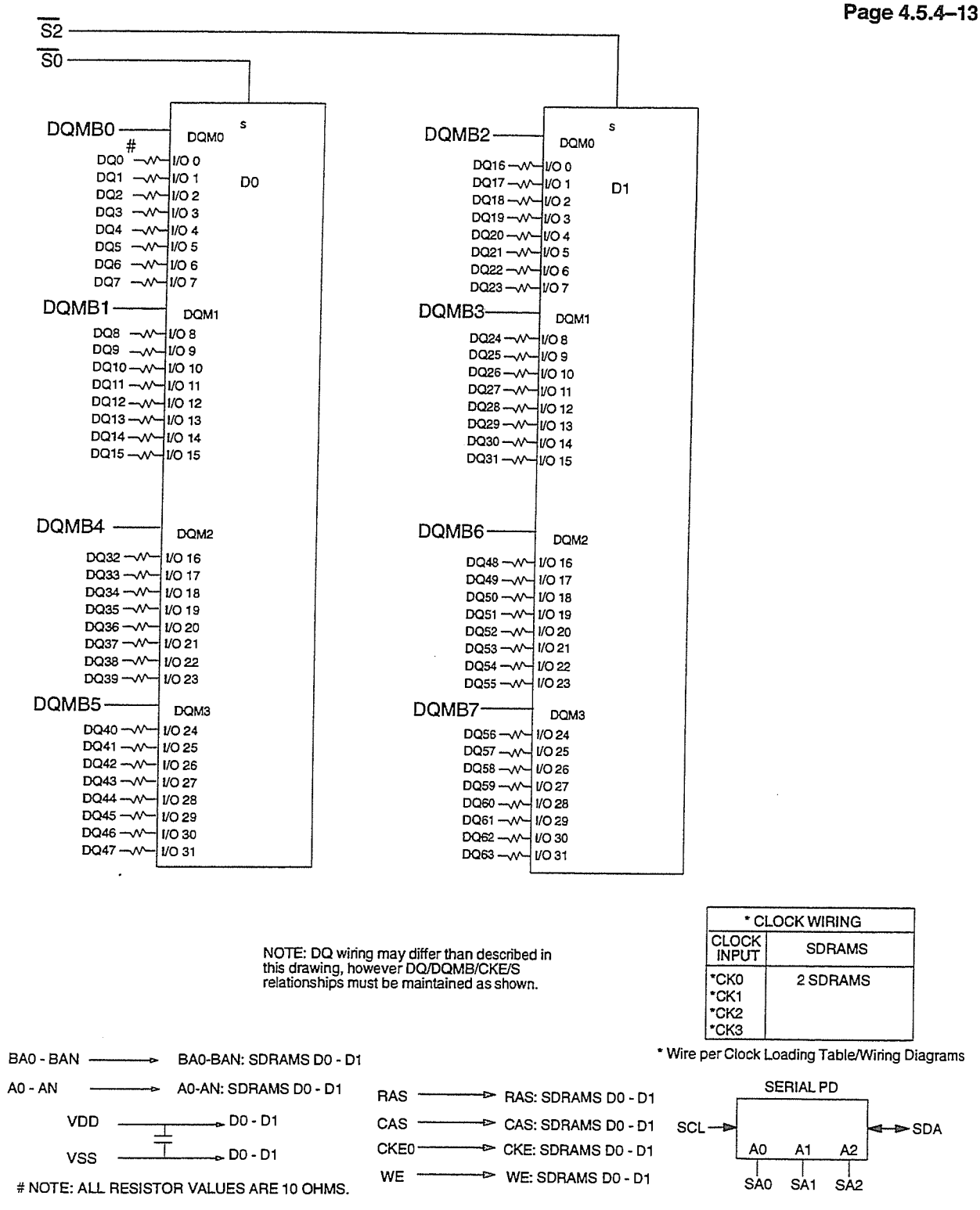


Figure 4.5.4–L
X64 SDRAM DIMM, 1 Bank with X32 SDRAMs

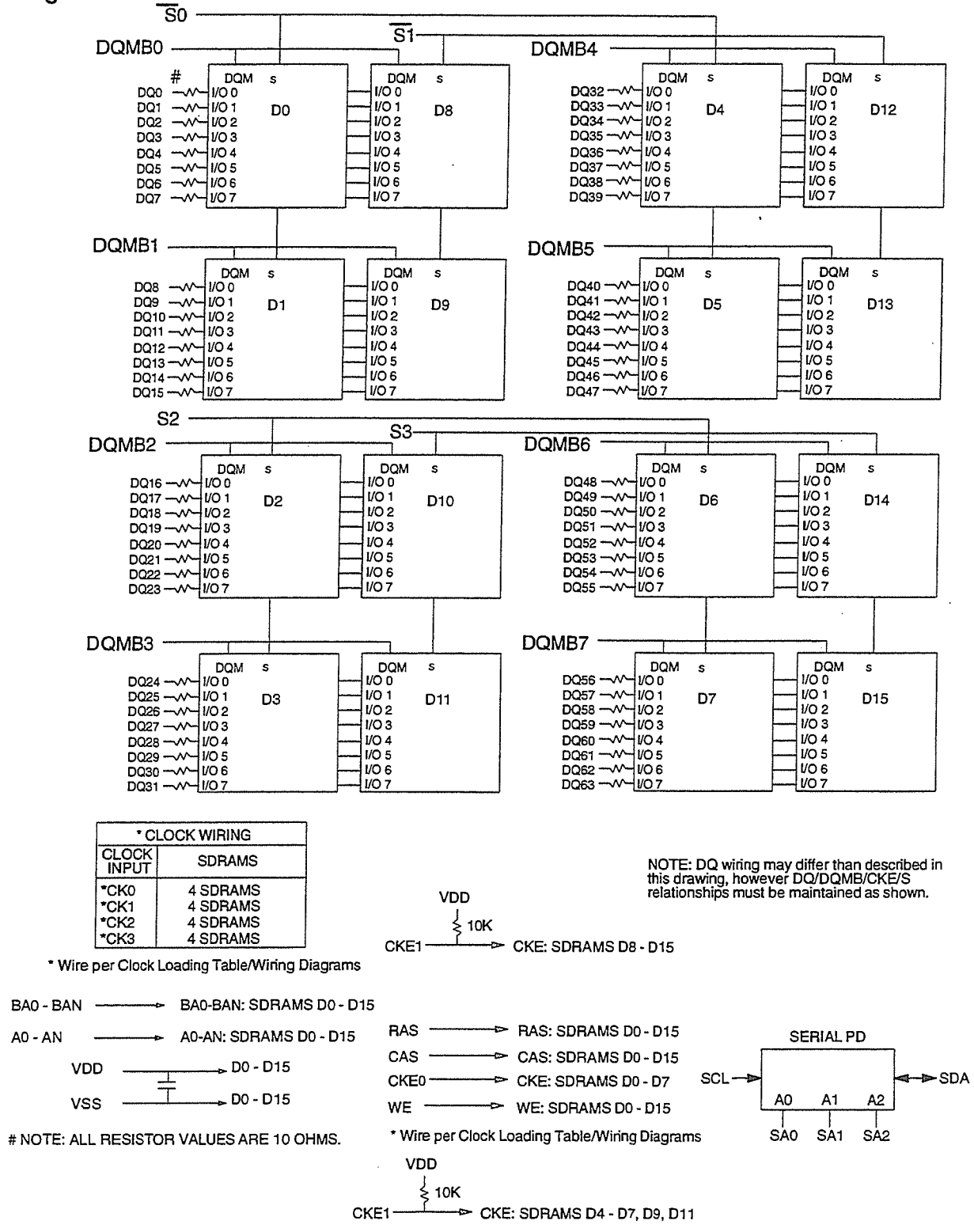


Figure 4.5.4–M
X64 SDRAM DIMM, 2 Banks with X8 SDRAMs

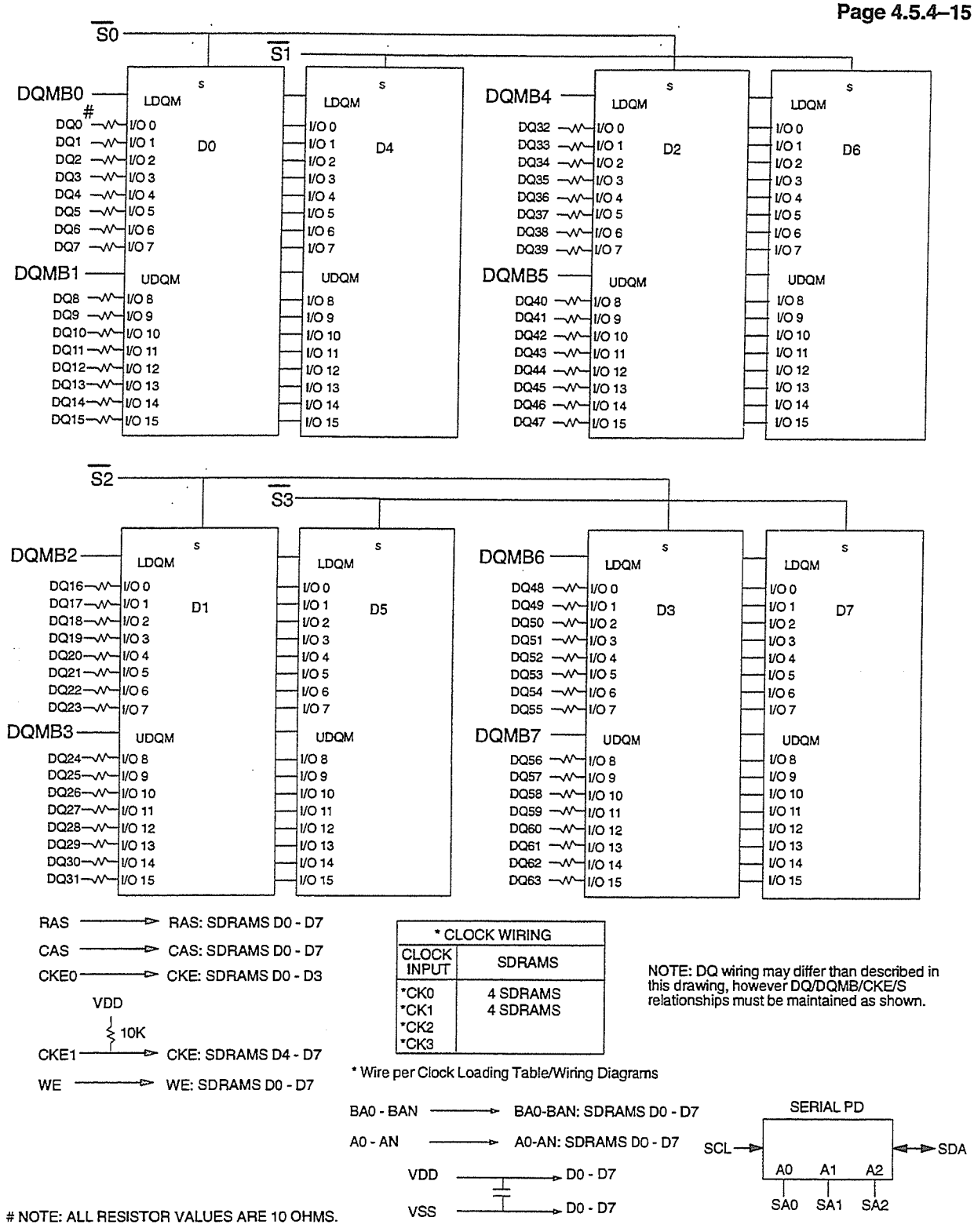


Figure 4.5.4–N
X64 SDRAM DIMM, 2 Banks with X16 SDRAMs

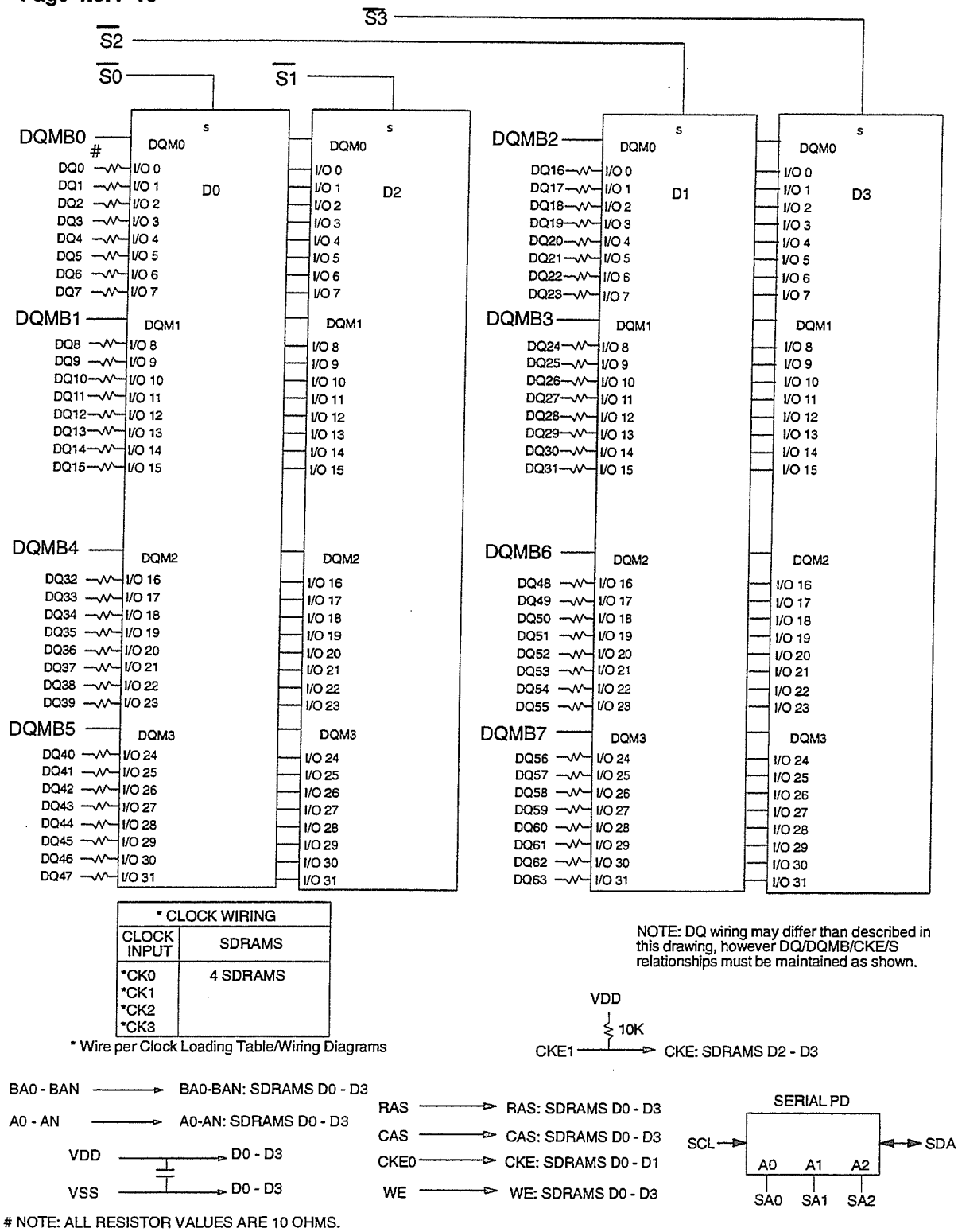


Figure 4.5.4–O
X64 SDRAM DIMM, 2 Banks with X32 SDRAMs

Release 7

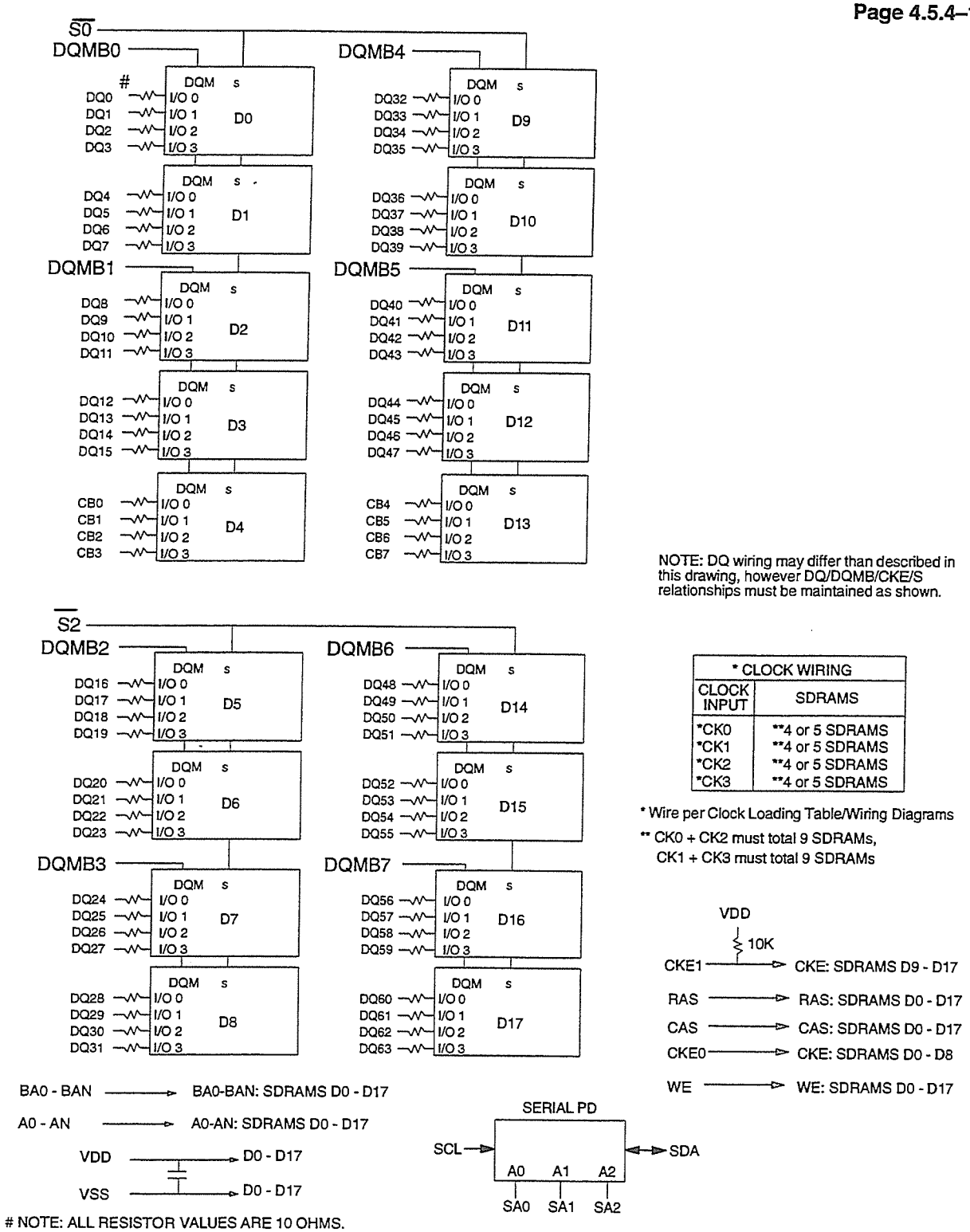


Figure 4.5.4–P
X72 ECC SDRAM DIMM, 1 Banks with X4 SDRAMs

Release 7

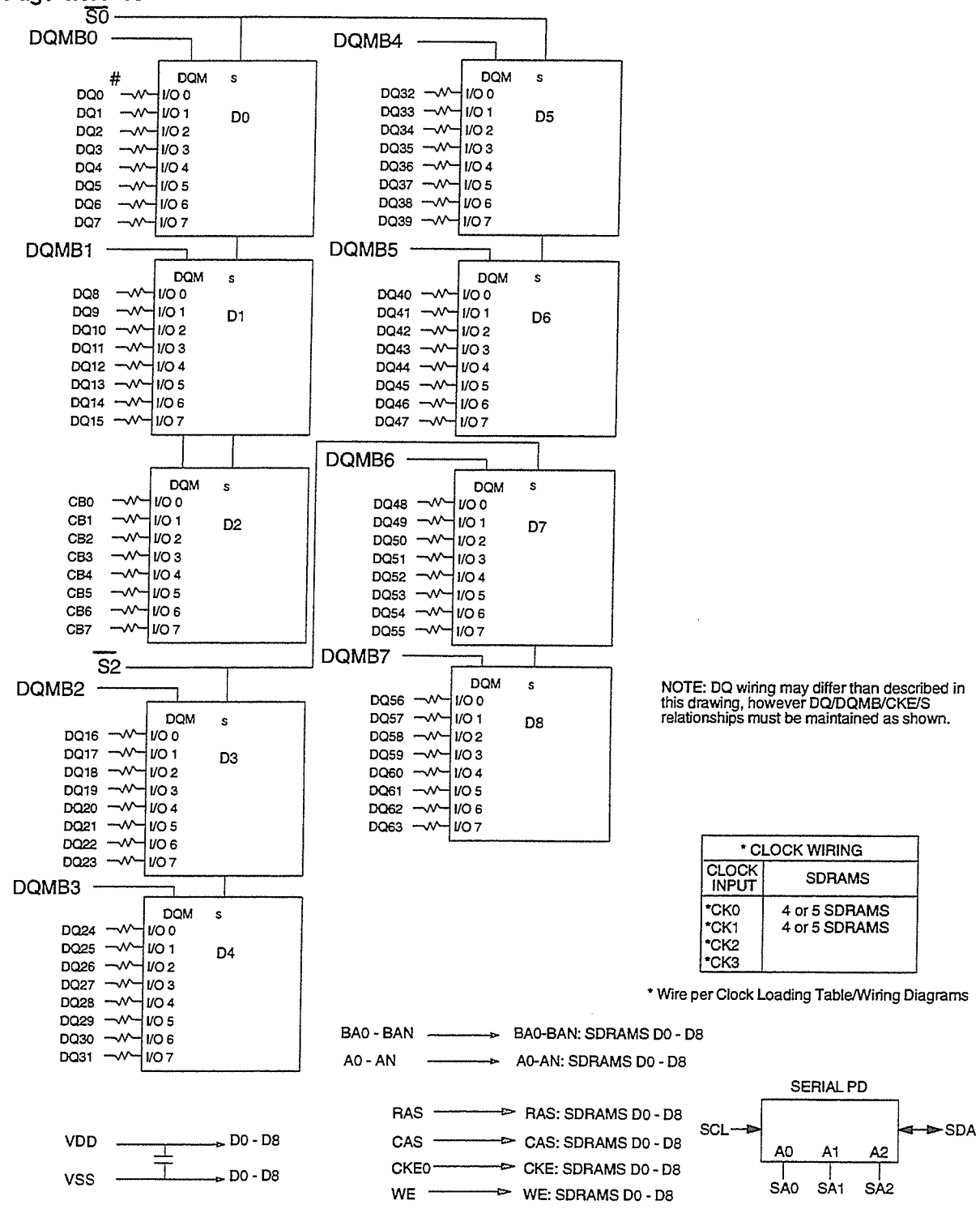


Figure 4.5.4–Q
X72 ECC SDRAM DIMM, 1 Banks with X8 SDRAMs

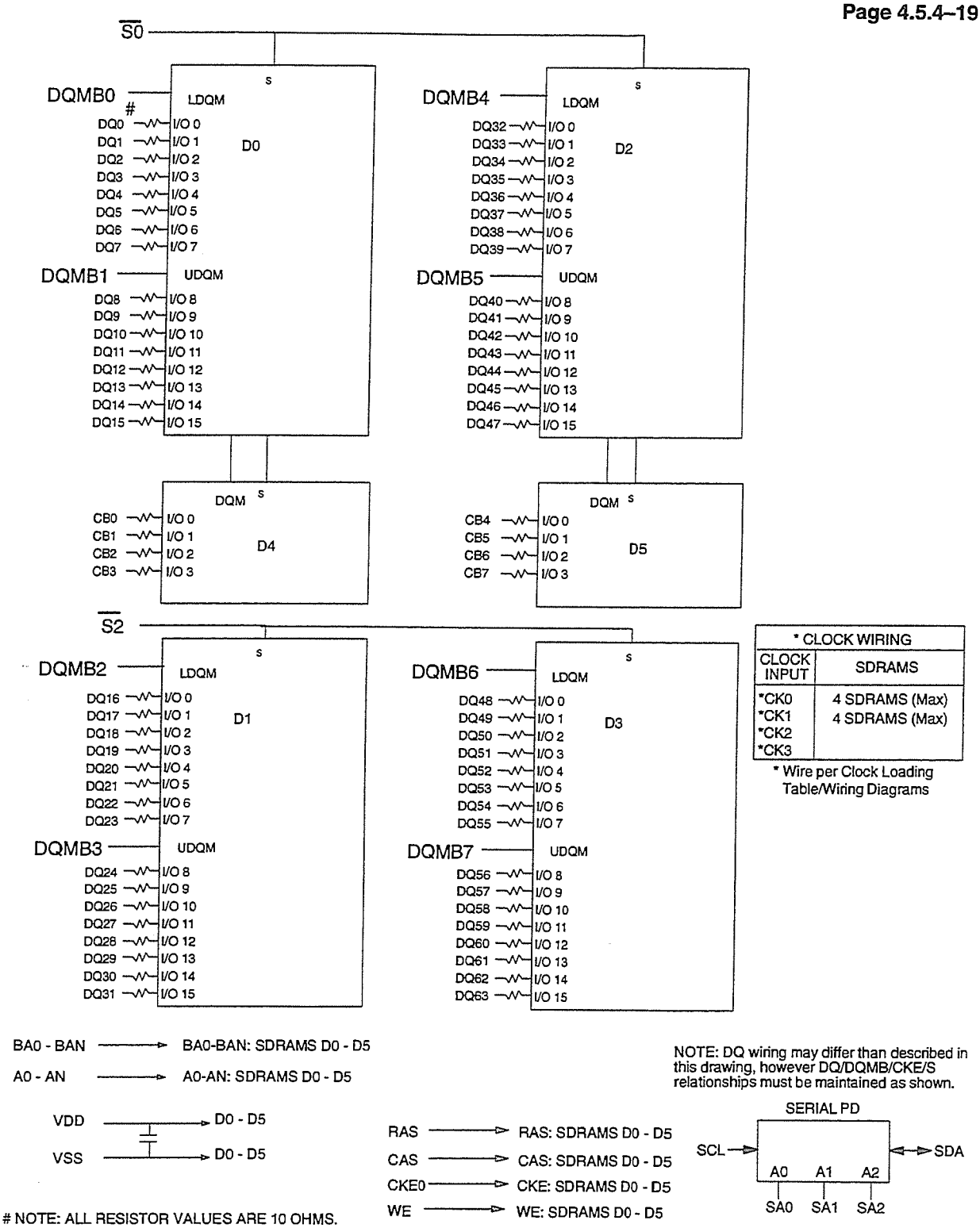


Figure 4.5.4–R
X72 ECC SDRAM DIMM, 1 Bank with X16 & X4 SDRAMs

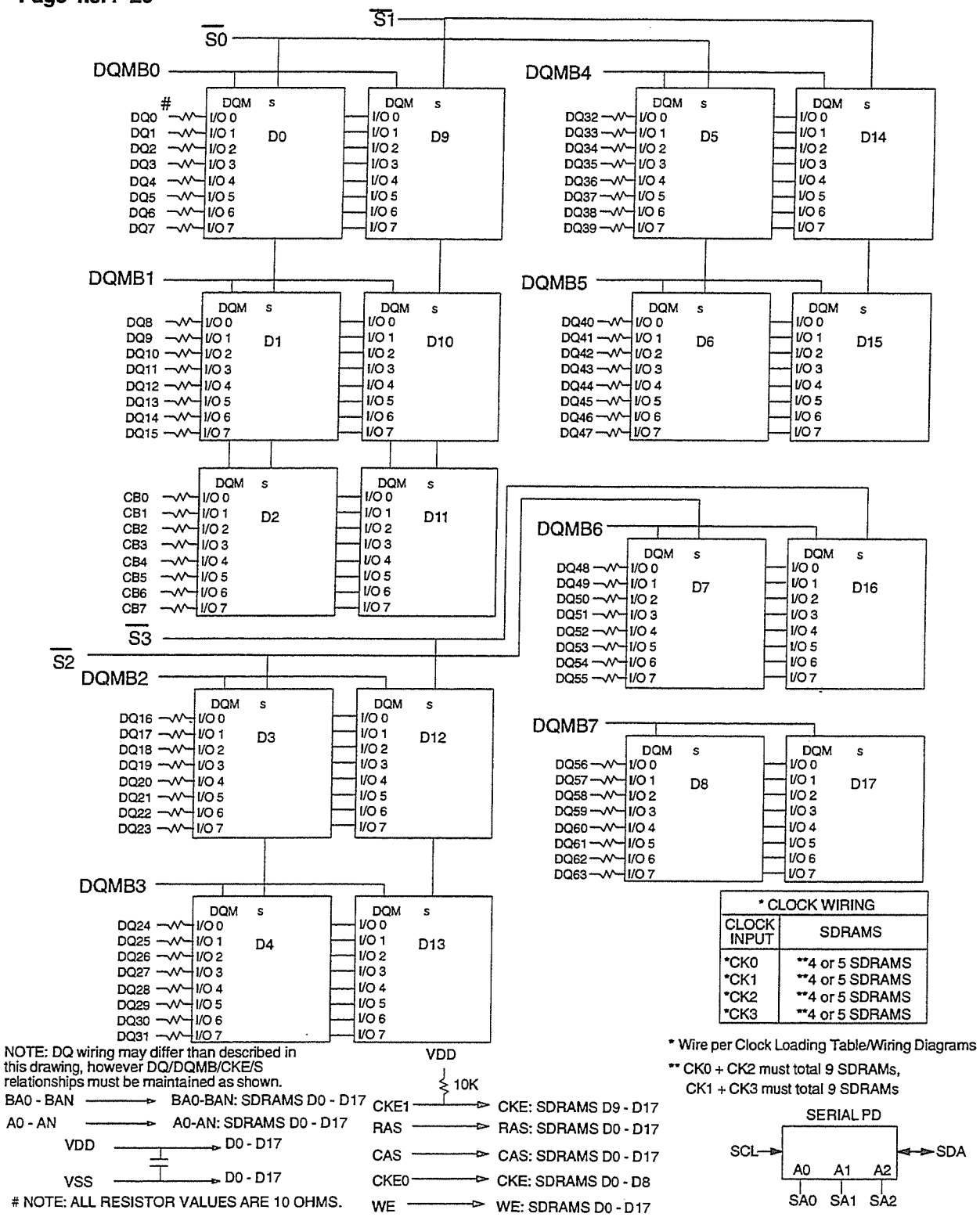


Figure 4.5.4–S
X72 ECC SDRAM DIMM, 2 Banks with X8 SDRAMs

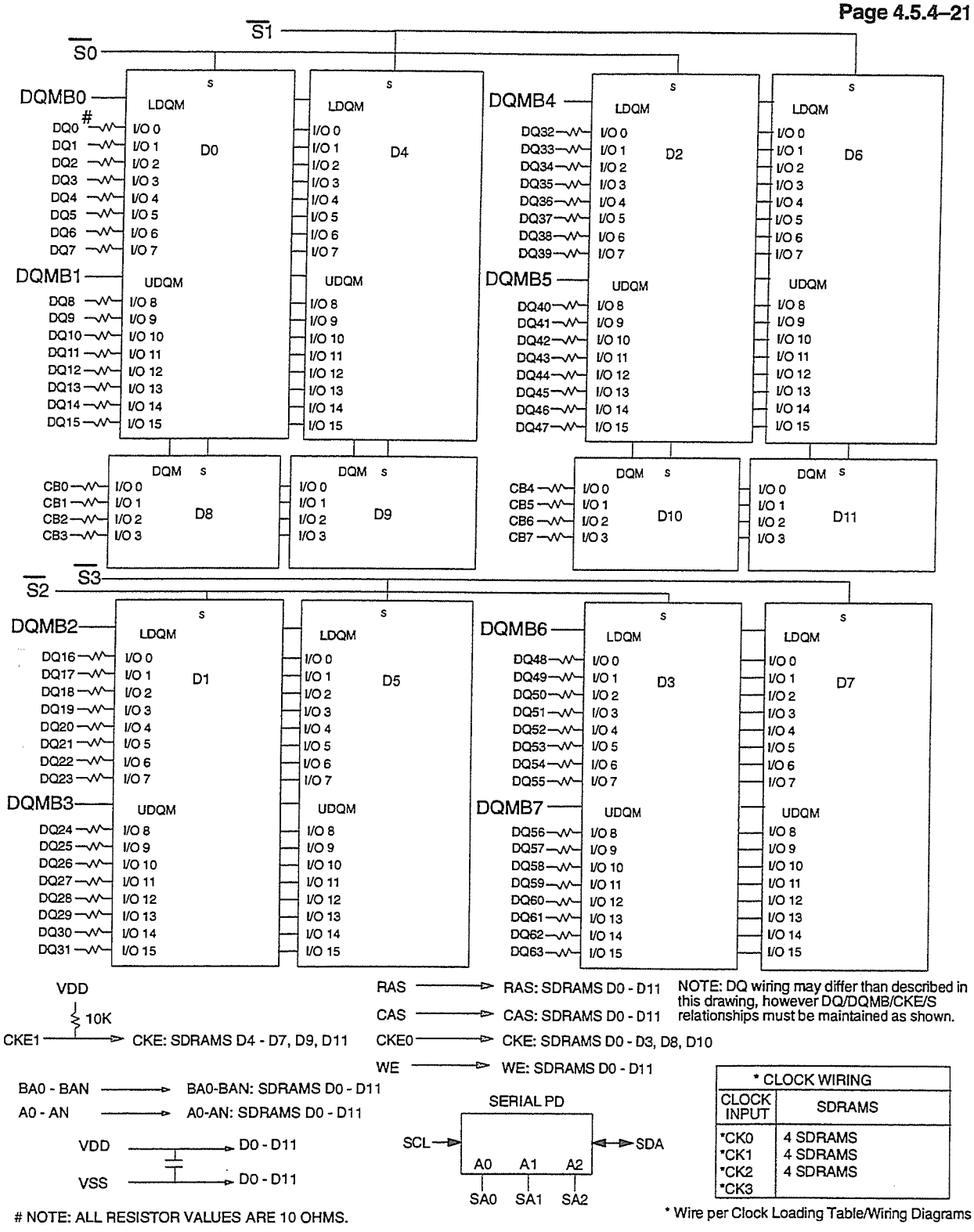


Figure 4.5.4–T
X72 ECC SDRAM DIMM, 2 Banks with X16 & X4 SDRAMs

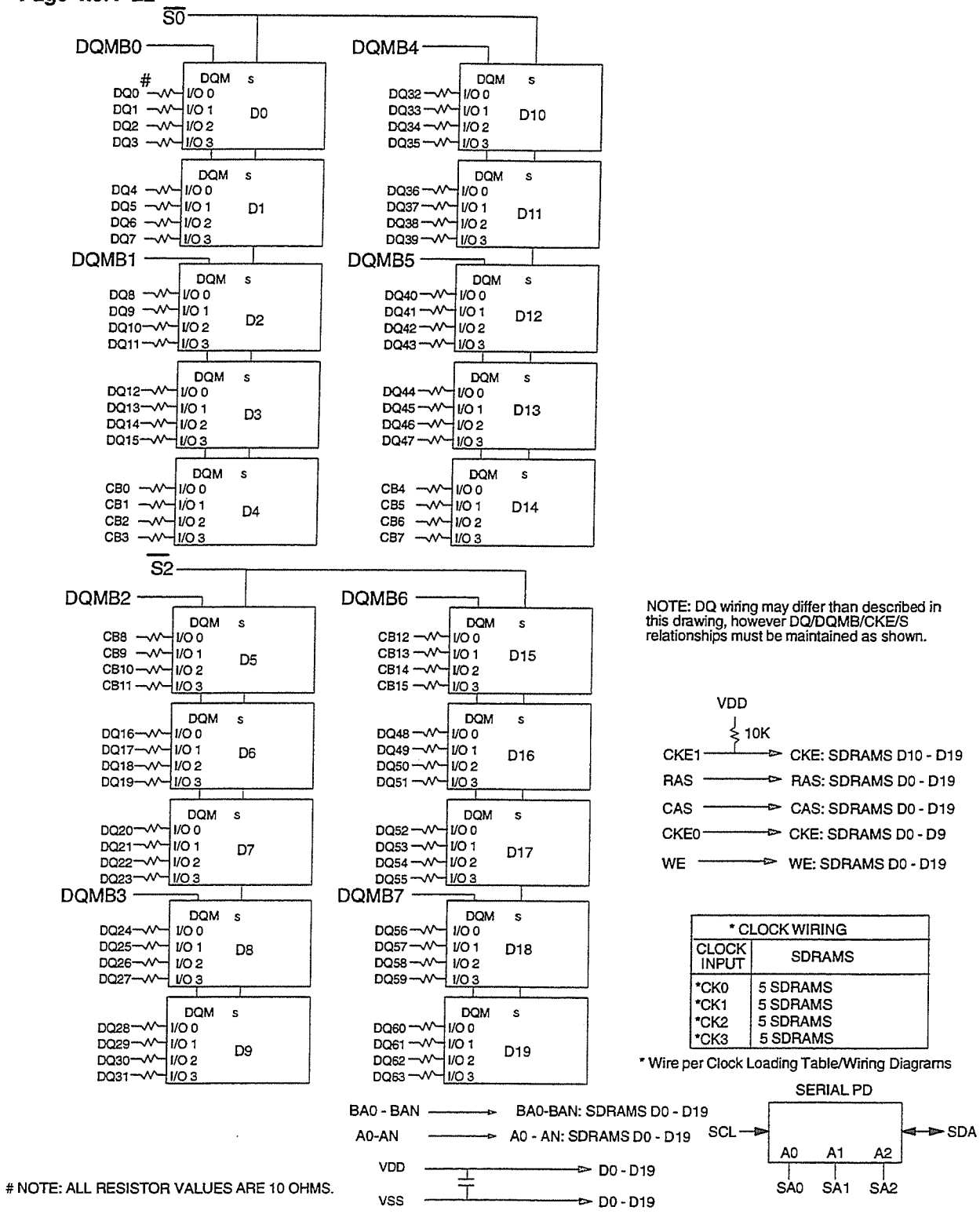


Figure 4.5.4-U
X80 SDRAM DIMM, 1 Bank with X4 SDRAMs

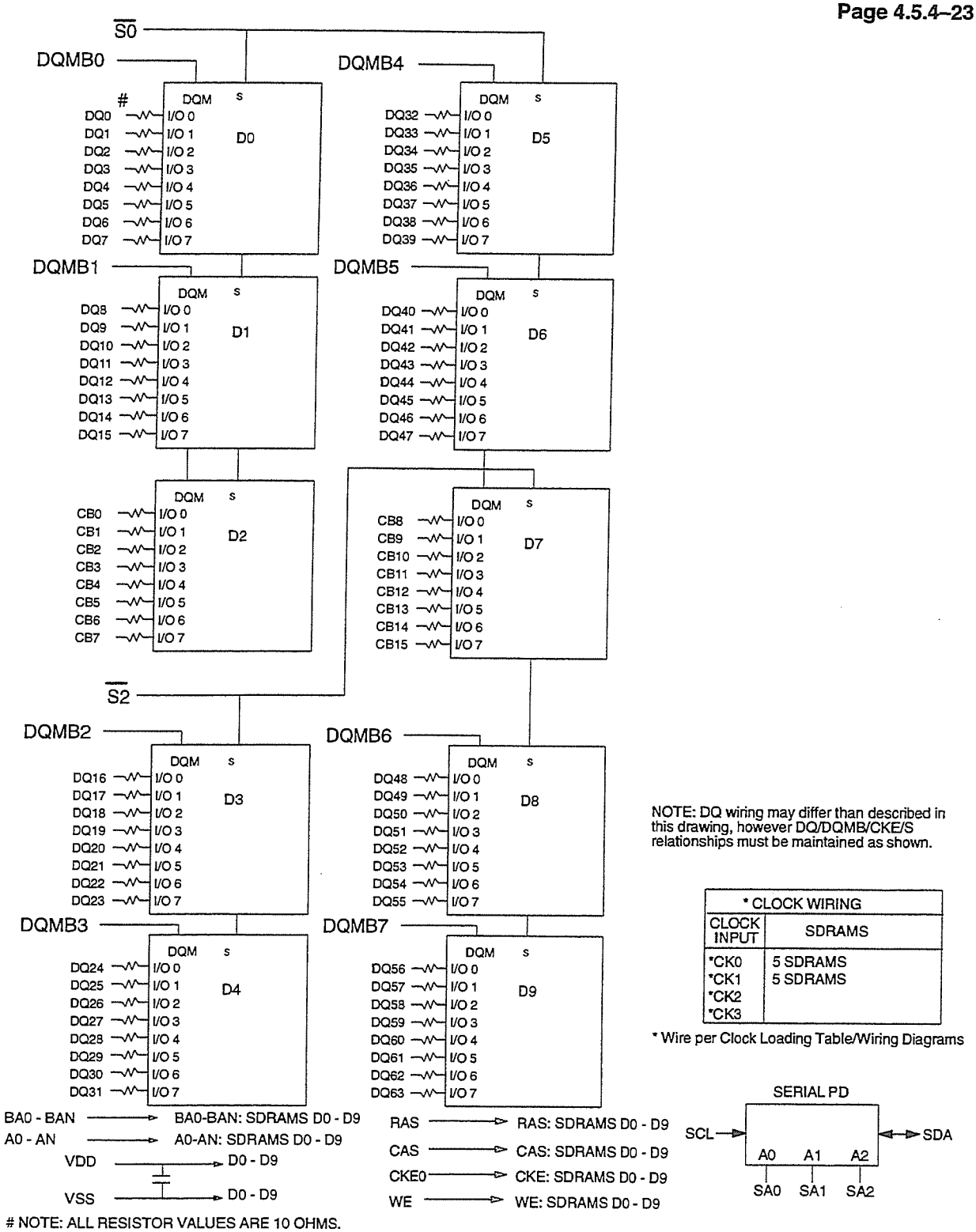


Figure 4.5.4–V
X80 ECC SDRAM DIMM, 1 Bank with X8 SDRAMs

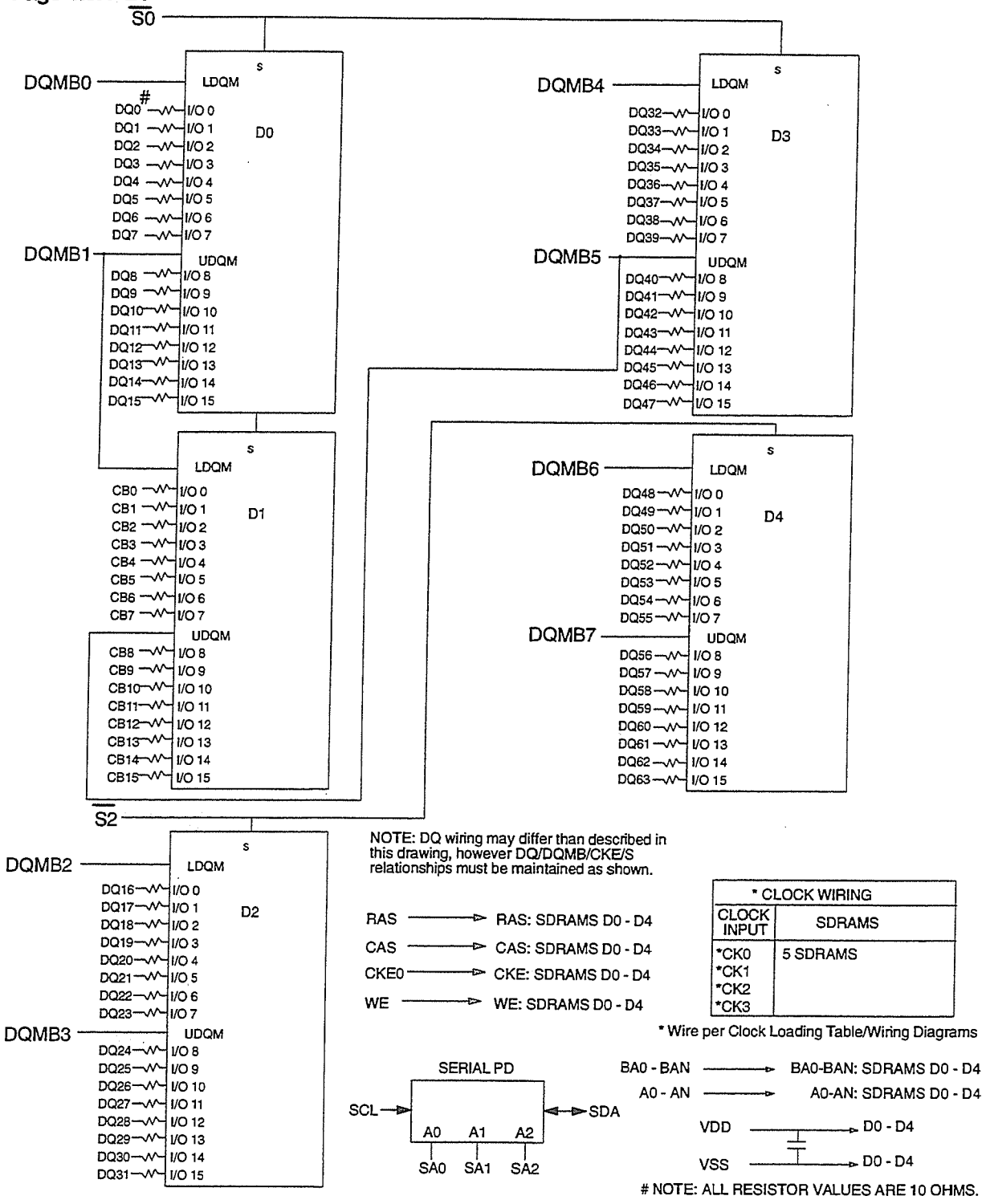


Figure 4.5.4–W
X80 ECC SDRAM DIMM, 1 Bank with X16 SDRAMs

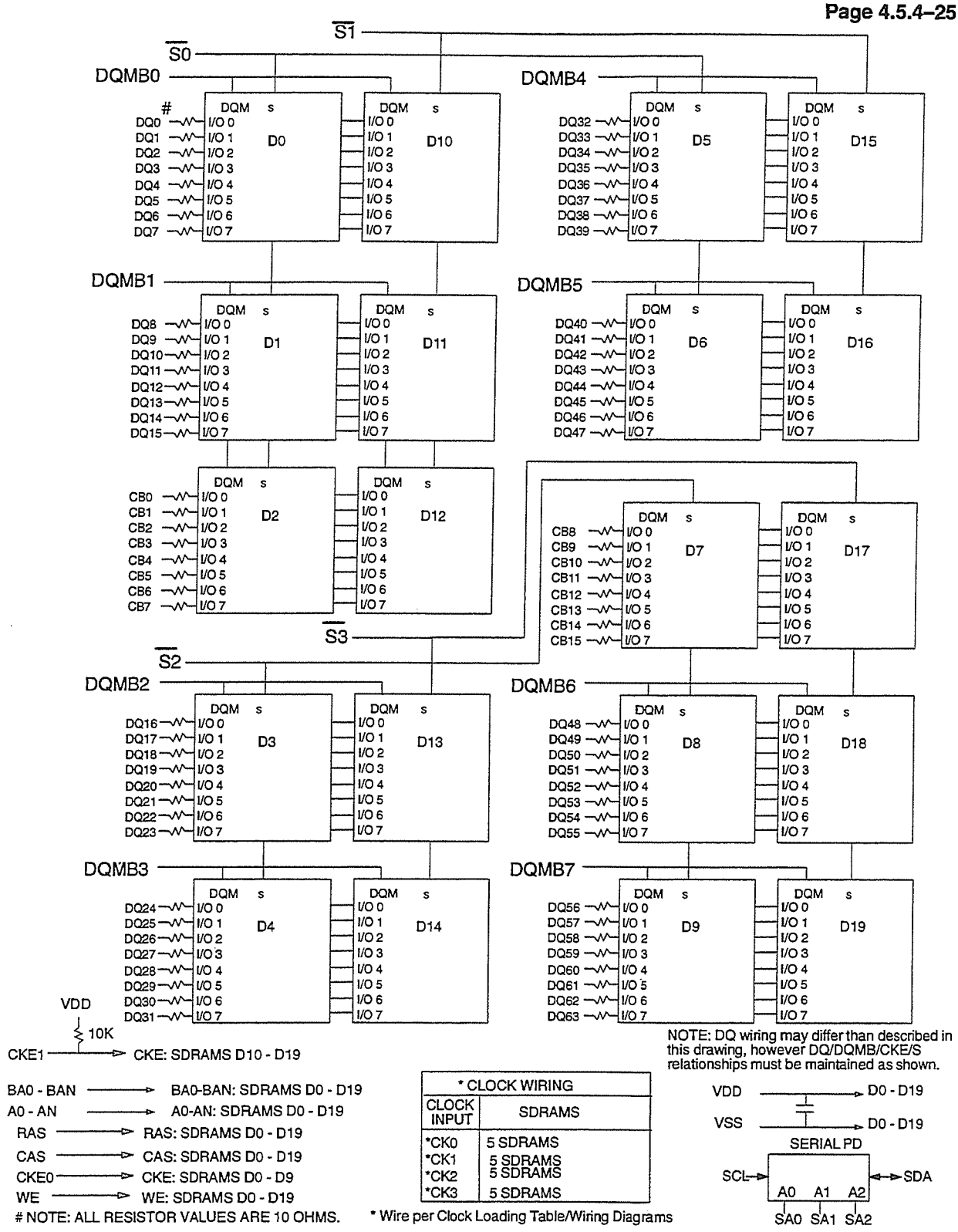


Figure 4.5.4–X
X80 ECC SDRAM DIMM, 2 Banks with X8 SDRAMs

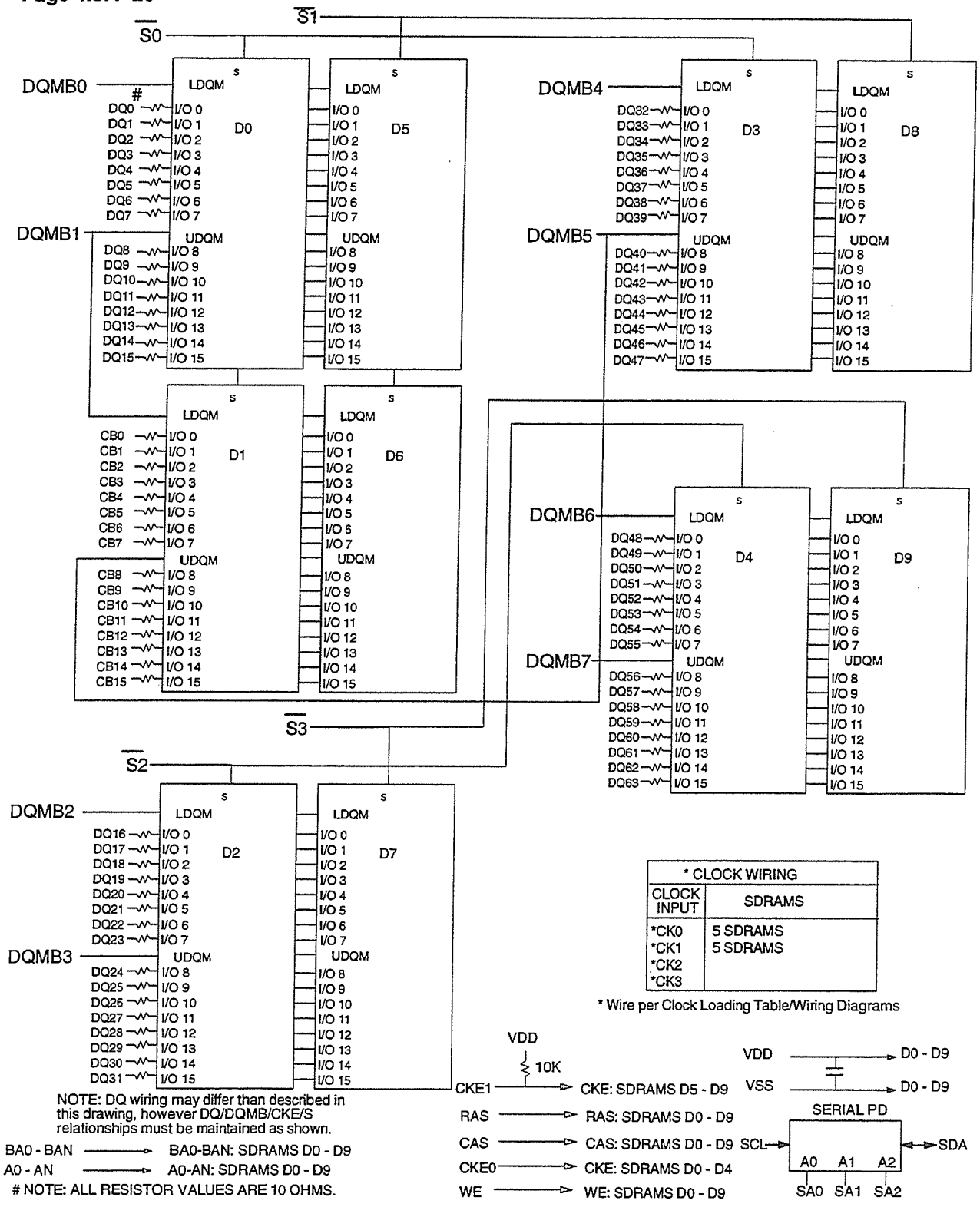


Figure 4.5.4–Y
X80 ECC SDRAM DIMM, 2 Banks with X16 SDRAMs

4.5.5 – 144 PIN DRAM SO–DIMM FAMILY

NOTE: It is recommended that this module be used primarily for main memory applications. At the time this standard was published, the Committee was working on a standard for a Graphics 144 Pin Module to be published in the near future.

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 32, 36, & 40 bits.

DATA CONFIGURATIONS—Two DATA Word configurations are defined:
—64 BIT DRAM without PARITY
—72 BIT DRAM for ECC CODES

CONFIGURATION—10 Different Configurations are defined using various combinationa of X4, X8, and X16 DRAM memories including 2 bank configurations, 5 for 64 bit and 5 for 72 bit.

LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that consist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

PACKAGE—144 PIN JEDEC SO–DIMM MEMORY MODULE

PIN ASSIGNMENTS —Figs. 4.5.5–A & 4.5.5–B

MODULE PIN NUMBERING AND KEYING METHODOLOGY — Fig. 4.5.5–C

TECHNOLOGY COMPARISON TABLE — Fig. 4.5.5–D

DRAM SPD INFORMATOION — Fig. 4.5.5–E

X64 DRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.5–F through 4.5.5–J

X72 DRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.5–K through 4.5.5–O

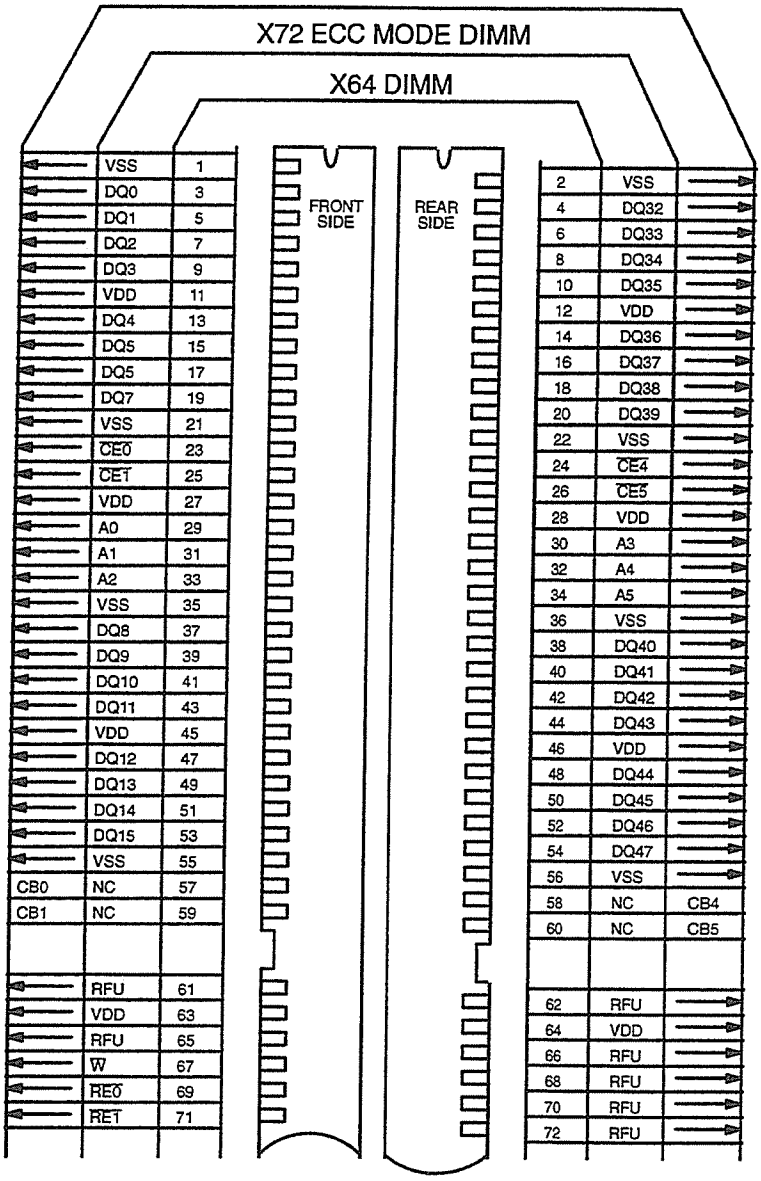


Figure 4.5.5–A
144 Pin X64 & X72 DRAM SO–DIMM, PIN ASSIGNMENTS
UPPER HALF

0

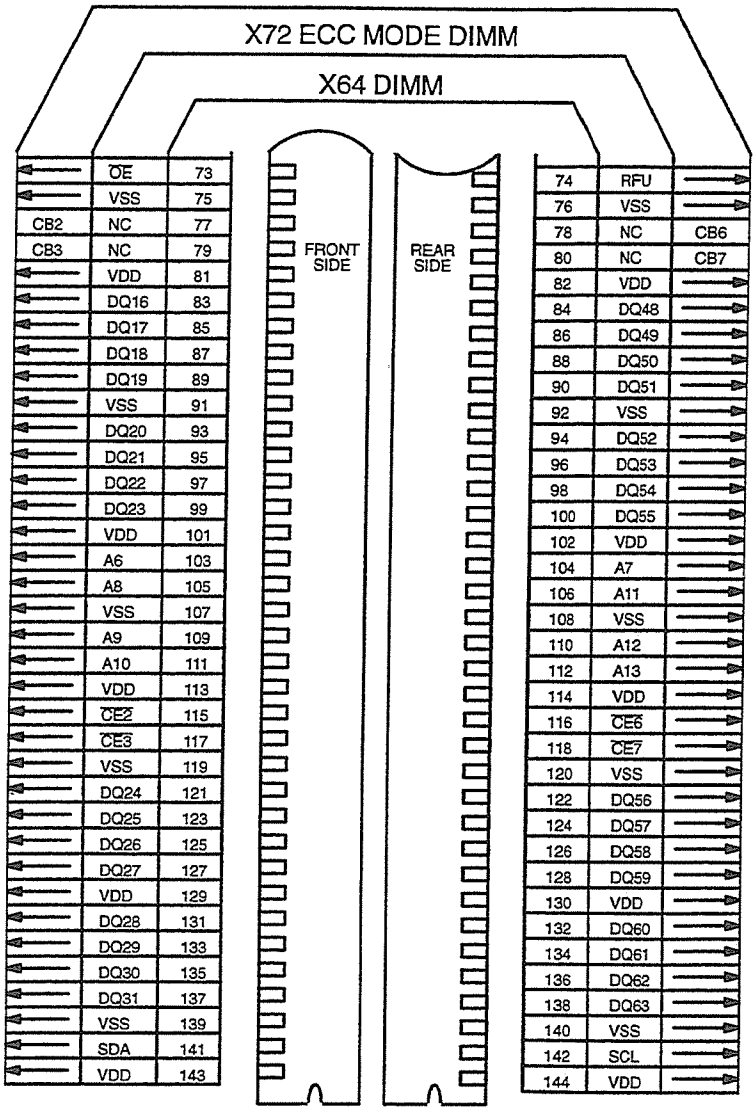


Figure 4.5.5–B
144 Pin X64 & X72 DRAM SO–DIMM, PIN ASSIGNMENTS
LOWER HALF

The diagram below shows the keying methodology employed on 8-byte SO DIMMs. The voltage key provides a positive interlock so that SO DIMMs can only be plugged into a system with the proper supply voltage, reducing potential damage to the module DRAM chips. Unless the designer chooses the appropriate connector, the system will not work.

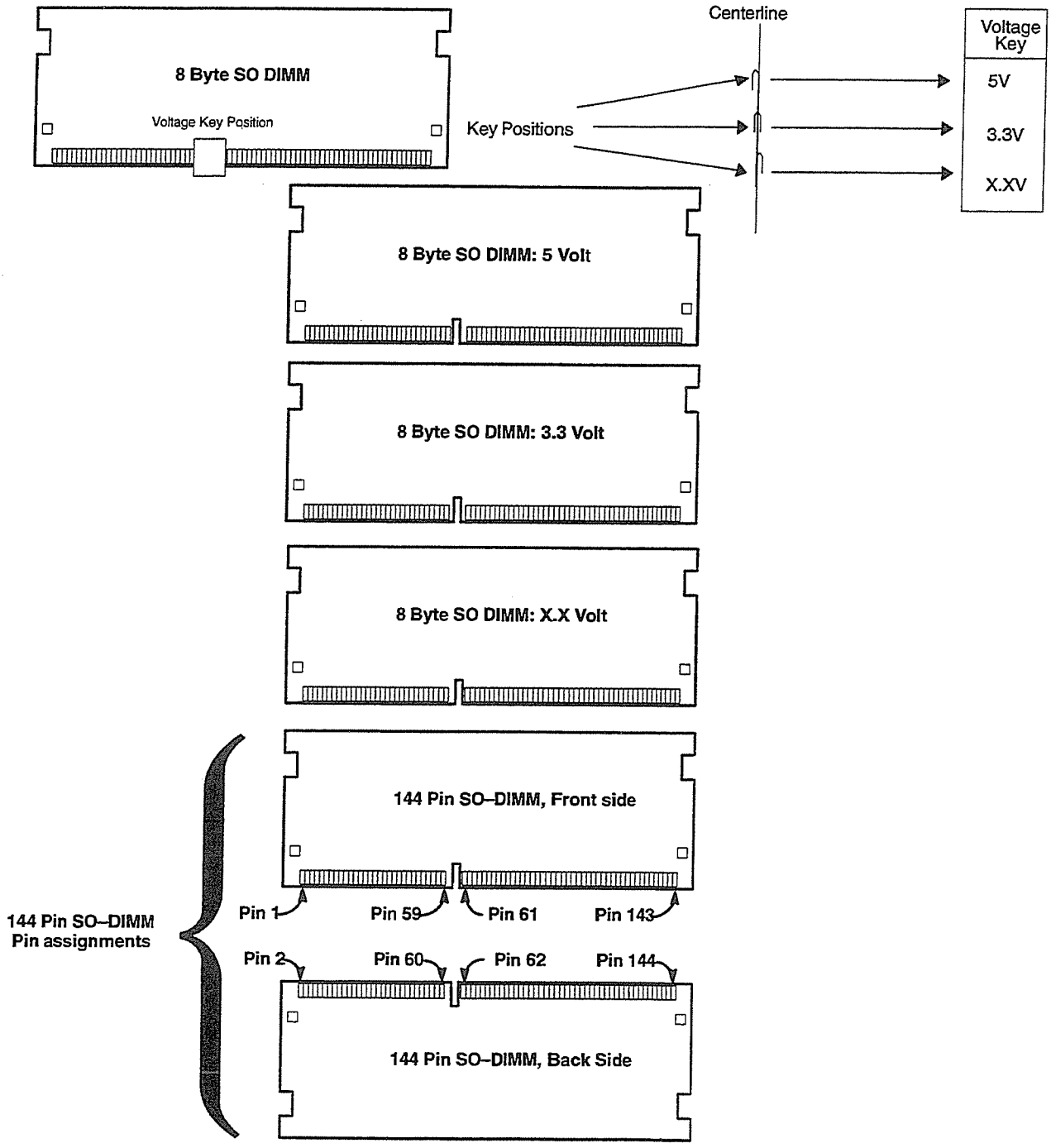


Figure 4.5.5–C
144 Pin SO–DRAM DIMM Keying Methodology

Pin #	DRAM SODIMM	SDRAM SODIMM
23	$\overline{CAS0}$	DQMB0
25	$\overline{CAS1}$	DQMB1
61	DU	CK0
65	DU	$\overline{RAS}$
69	$\overline{RAS0}$	$\overline{S0}$
71	$\overline{RAS1}$	$\overline{S1}$
73	$\overline{OE}$	DU
111	A10	A10/AP
115	$\overline{CAS2}$	DQMB2
117	$\overline{CAS3}$	DQMB3
24	$\overline{CAS4}$	DQMB4
26	$\overline{CAS5}$	DQMB5
62	DU	CKE0
66	DU	$\overline{CAS}$
68	NC	CKE1
70	NC	A12
72	NC	A13, DSF
74	NC	CK1
106	A11	BA0
110	A12	BA1
112	A13	A11
116	$\overline{CAS6}$	DQMB6
118	$\overline{CAS7}$	DQMB7

Figure 4.5.5–D
Pinout Comparison, 144 Pin DRAM & SDRAM SO–DIMM

8 Byte DRAM SO–DIMM PD Information

- Serial PD Interface Protocol: I^2C (Synchronous 2-Wire Bus)
- The following information is to be written into EEPROM device during module production:
  a. Module Configurations, Addressing: (Bytes 3-7)

Module Configuration	DRAM Organization	Option 1		Option 2		Option 3	
		$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.
512K x 64/72	512K x 8	10	9				
1M x 64/72	512K x 8	10	9				
1M x 64/72	1M x 4/16	10	10	12	8		
2M x 64/72	1M x 16	10	10	12	8		
2M x 64/72	2M x 8	11	10	12	9		
4M x 64/72	2M x 8	11	10	12	9		
4M x 64/72	4M x 4/16	11	11	12	10	*13	9
8M x 64/72	4M x 16	11	11	12	10	*13	9
8M x 64/72	8M x 8	12	11	13	10		
16M x 64/72	8M x 8	12	11	13	10		
16M x 64/72	16M x 4/16	12	12	13	11	*14	10
32M x 64/72	16M x 16	12	12	13	11	*14	10
32M x 64/72	32M x 8	13	12	14	11		
64M x 64/72	32M x 8	13	12	14	11		
64M x 64/72	64M x 4	13	13	14	12		
(Note: All options possible with DRAM standards are shown) * This addressing option applies to x16 DRAM configuration							

  b. Allowable configurations: (Byte 11)
     - x64 (Non-parity, Byte controls)
     - x72 (ECC-optimized, Byte controls)
  c. Functional Attributes:
     - Power Supply Voltage/Interface levels (Byte 8)
     - $\overline{RAS}$ access (Byte 9)
     - $\overline{CAS}$ access (Byte 10)
     - Refresh rate/type (Byte 12)

For Detailed Serial PD Byte data see section 4–?–?, DRAM Serial Presence Detect Definitions.

1. Serial PD interface is standard I^2C architecture
2. Pull-up resistors (4.7K typical value) are required on all open drain/open collector bus devices (SCL and SDA).
3. Current sink capability on SCL and SDA source (I_{OL} max) must be at least 3ma to maintain a valid "low level".
4. I^2C Bus specification:

Figure 4.5.5–E
144 Pin X64 DRAM SO–DIMM, SPD TABLE AND INFORMATION

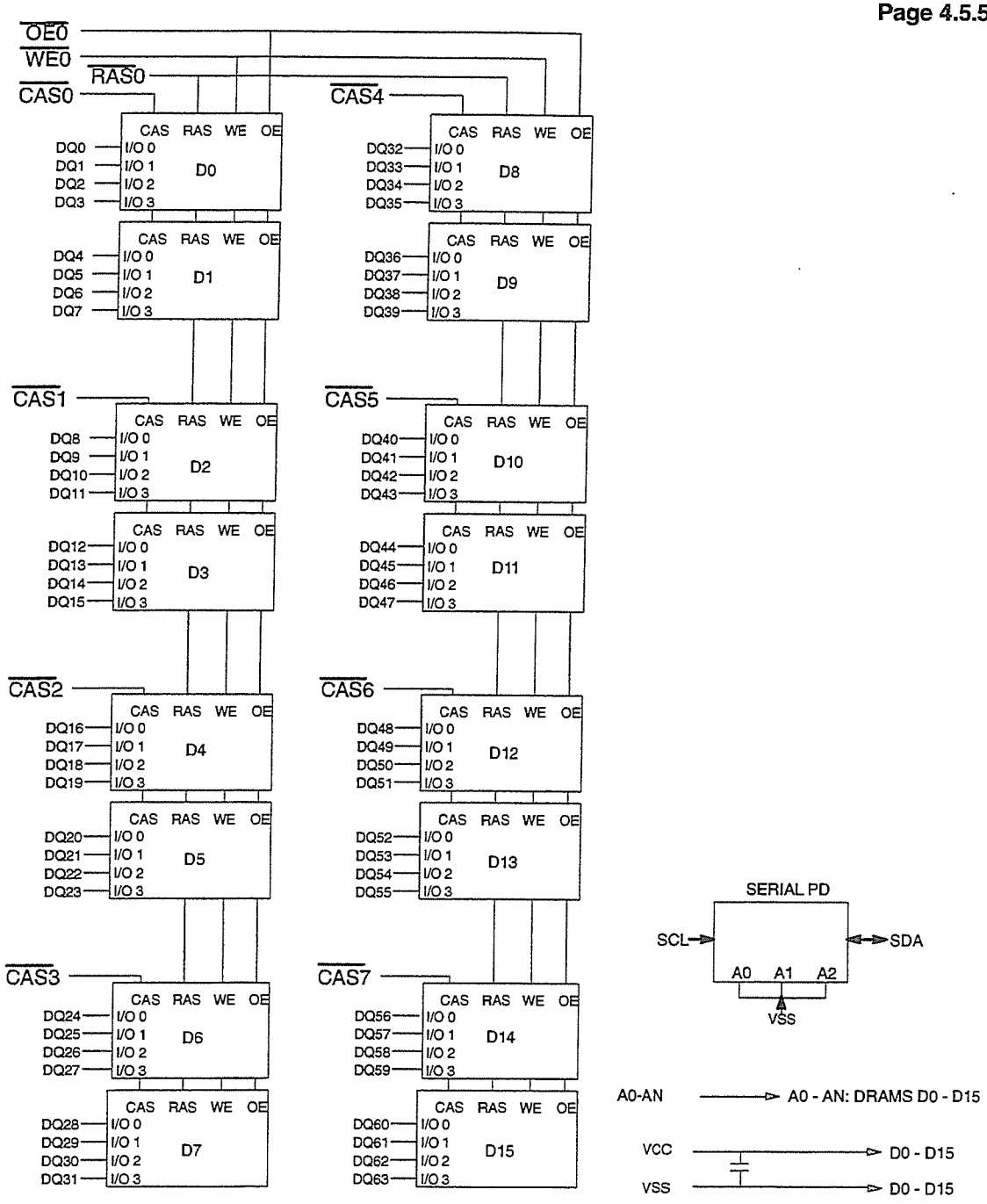


Figure 4.5.5–F
144 Pin X64 DRAM SO–DIMM, 1 Bank with X4 DRAMs

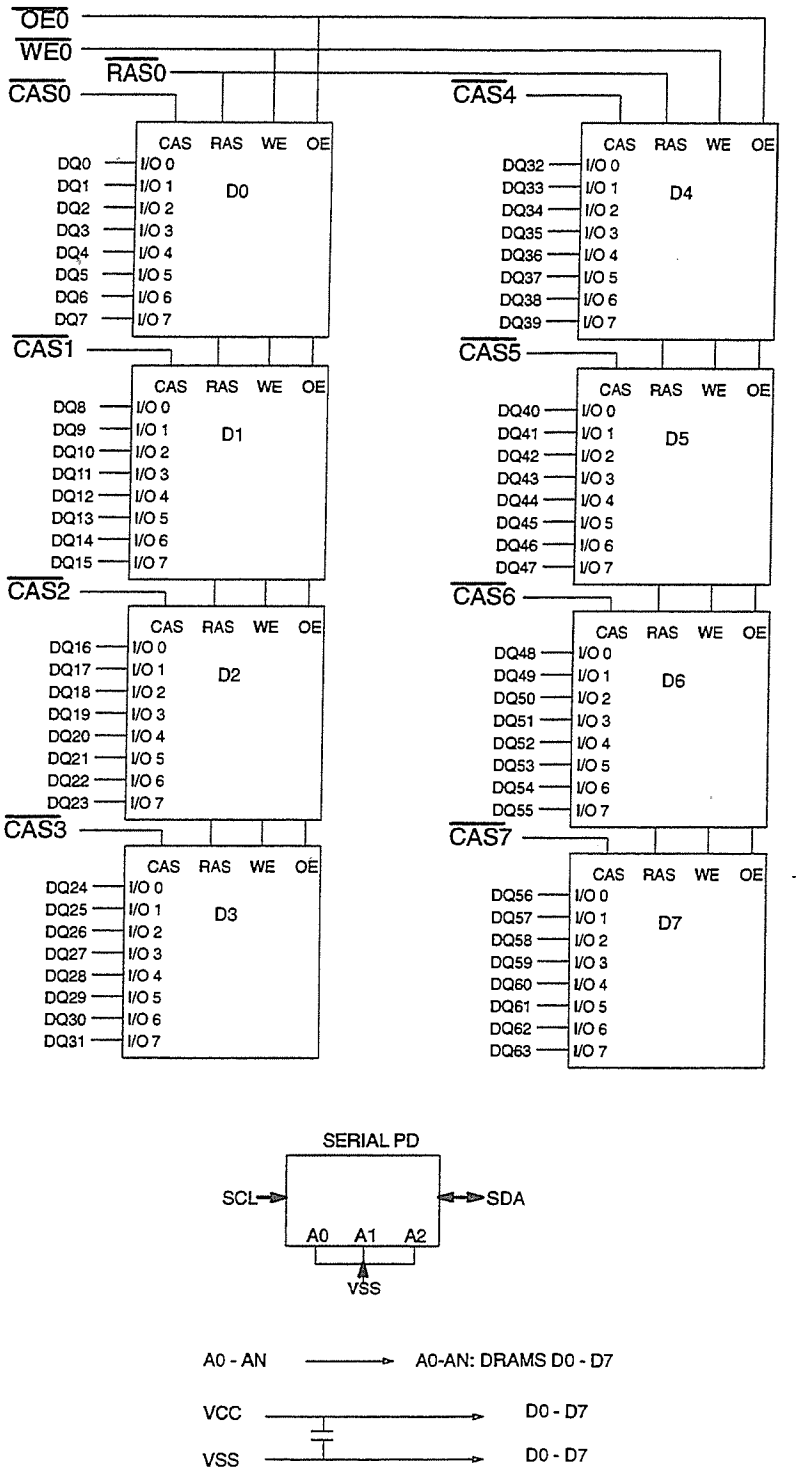


Figure 4.5.5–G
144 Pin X64 DRAM SO–DIMM, 1 Bank with X8 DRAMs

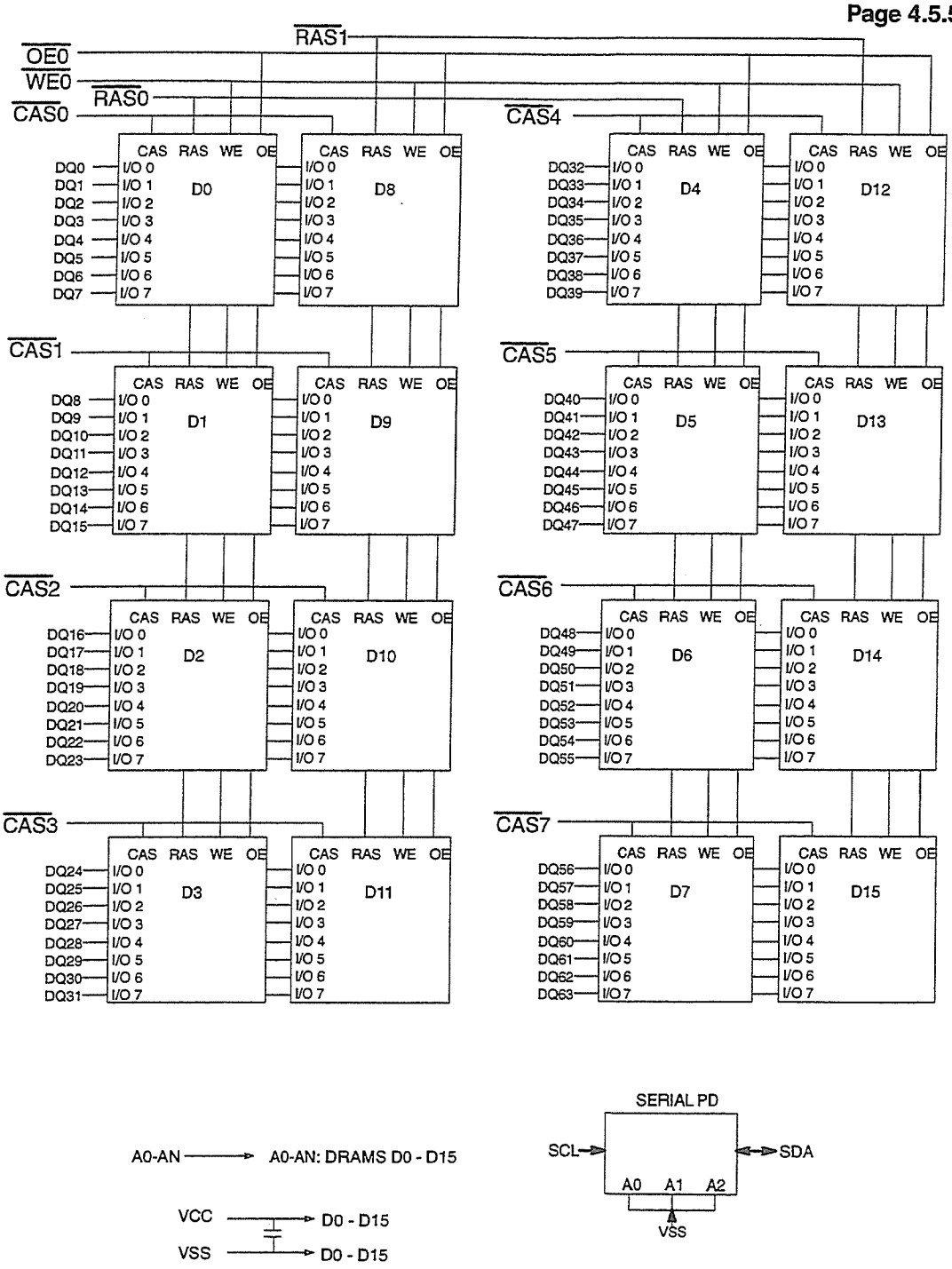


Figure 4.5.5–H
144 Pin X64 DRAM SO–DIMM, 2 Bank with X8 DRAMs

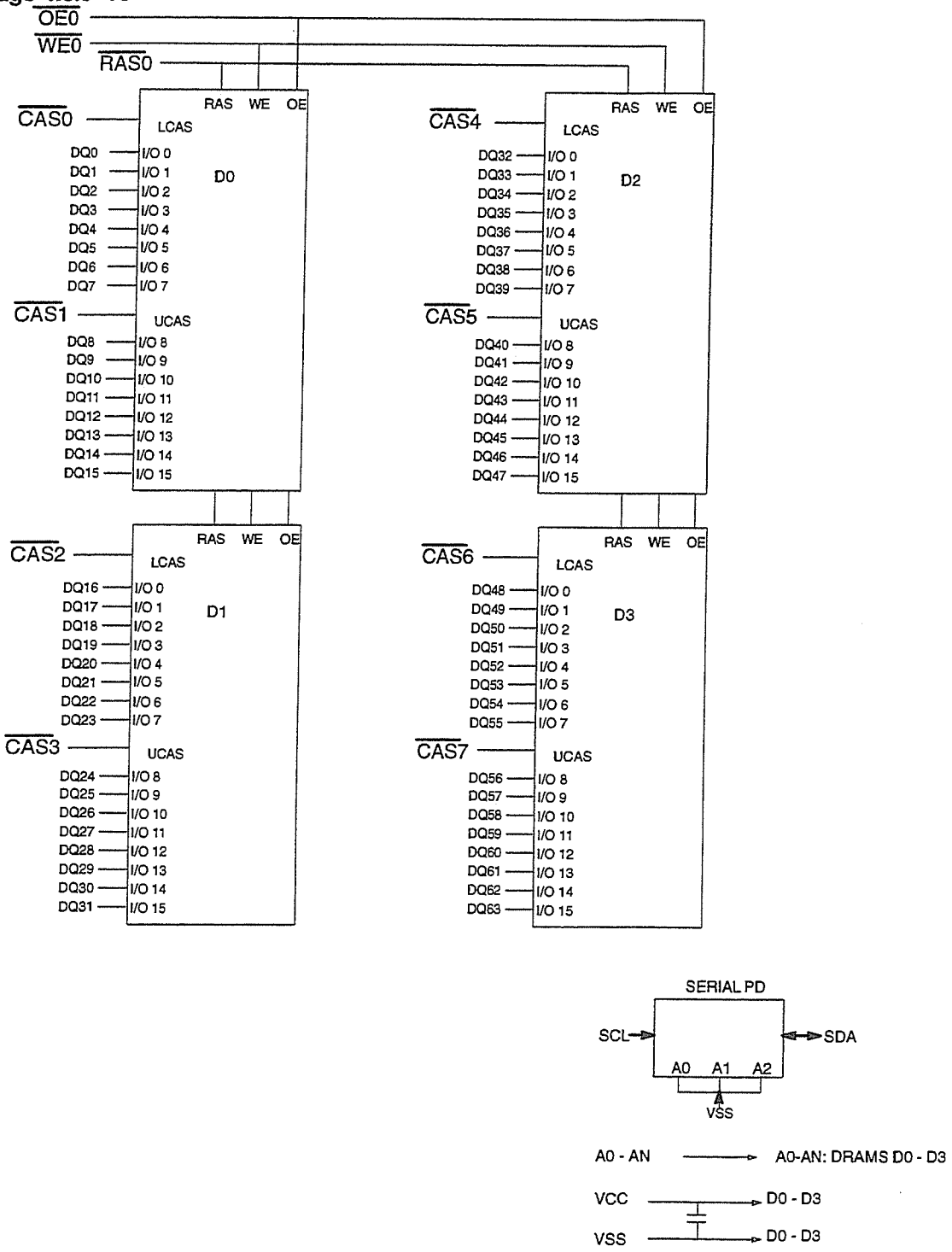


Figure 4.5.5–I
144 Pin X64 DRAM SO–DIMM, 1 Bank with X16 DRAMs

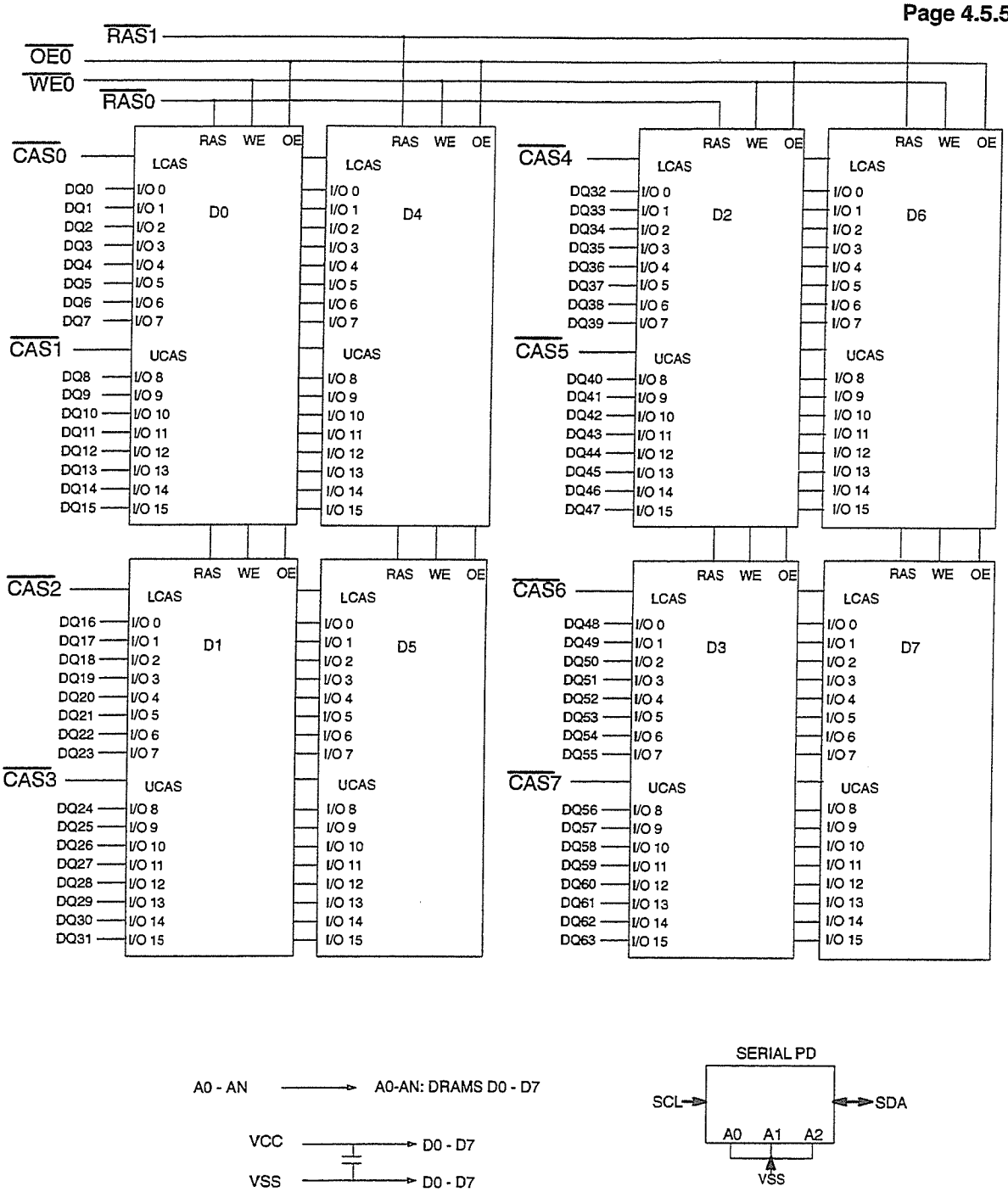


Figure 4.5.5–J
144 Pin X64 DRAM SO–DIMM, 2 Bank with X16 DRAMs

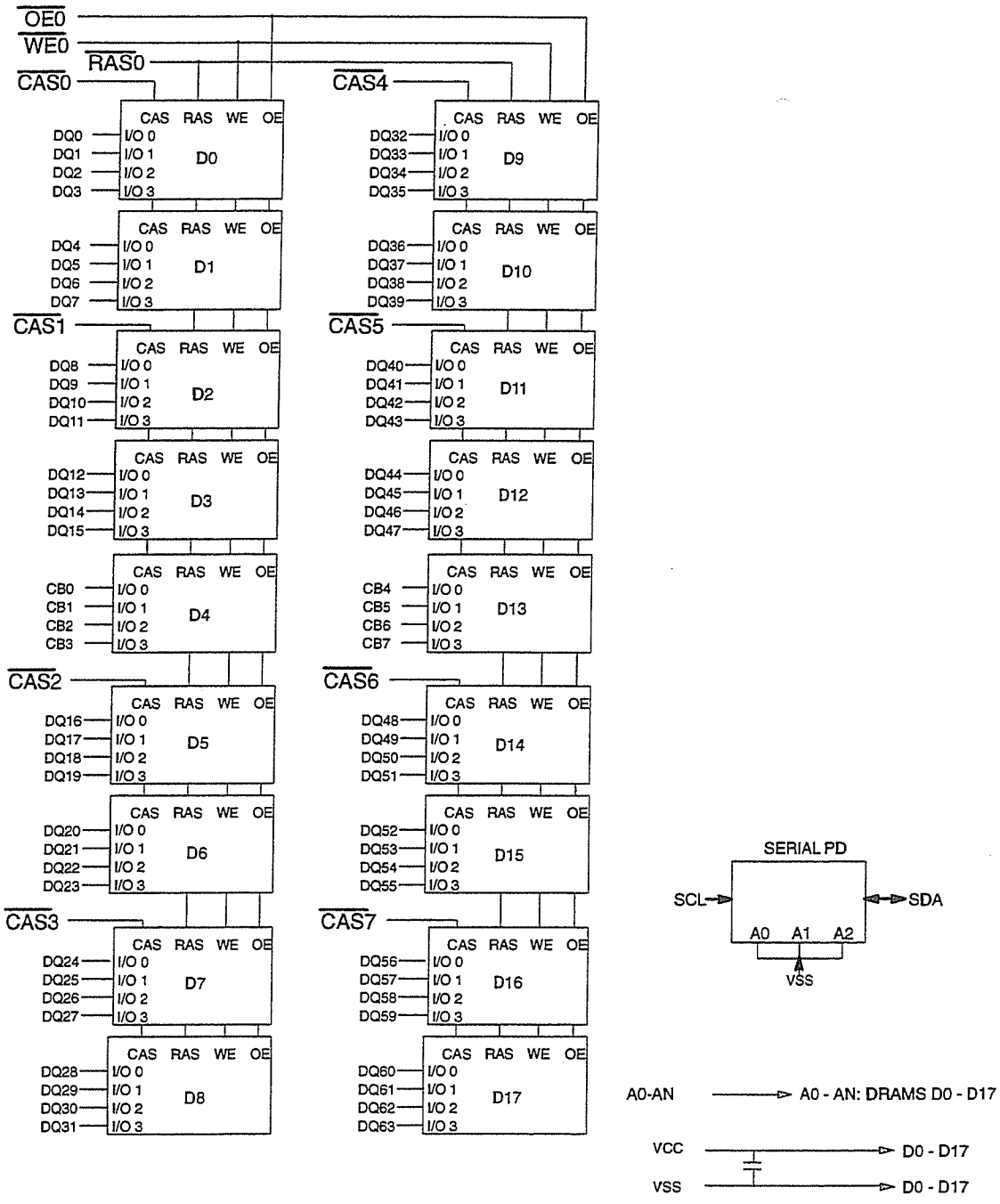


Figure 4.5.5–K
144 Pin X72 ECC DRAM SO–DIMM, 1 Bank with X4 DRAMs

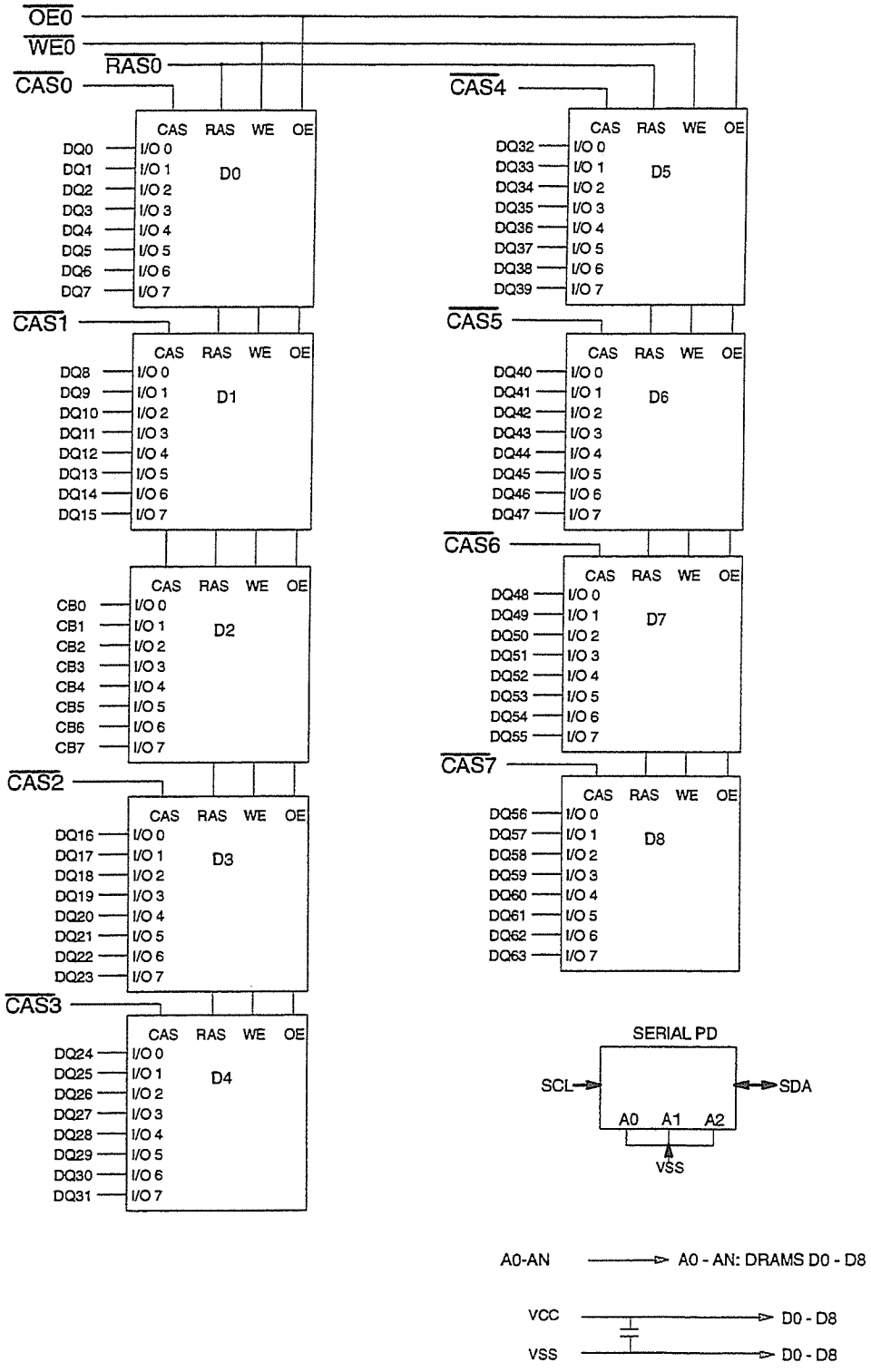


Figure 4.5.5–L
144 Pin X72 ECC DRAM SO–DIMM, 1 Bank with X8 DRAMs

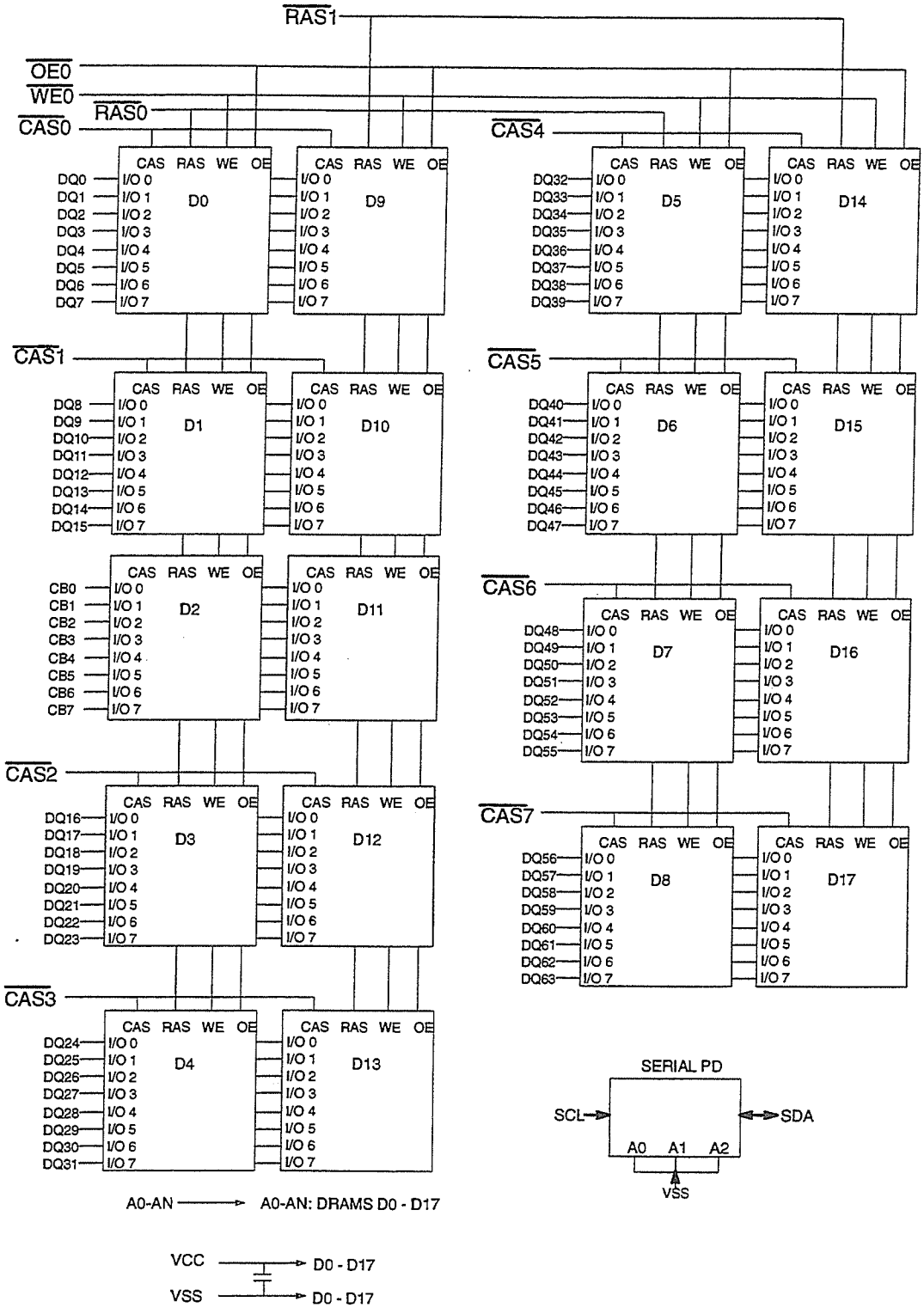


Figure 4.5.5–M
144 Pin X72 ECC DRAM SO–DIMM, 2 Bank with X8 DRAMs

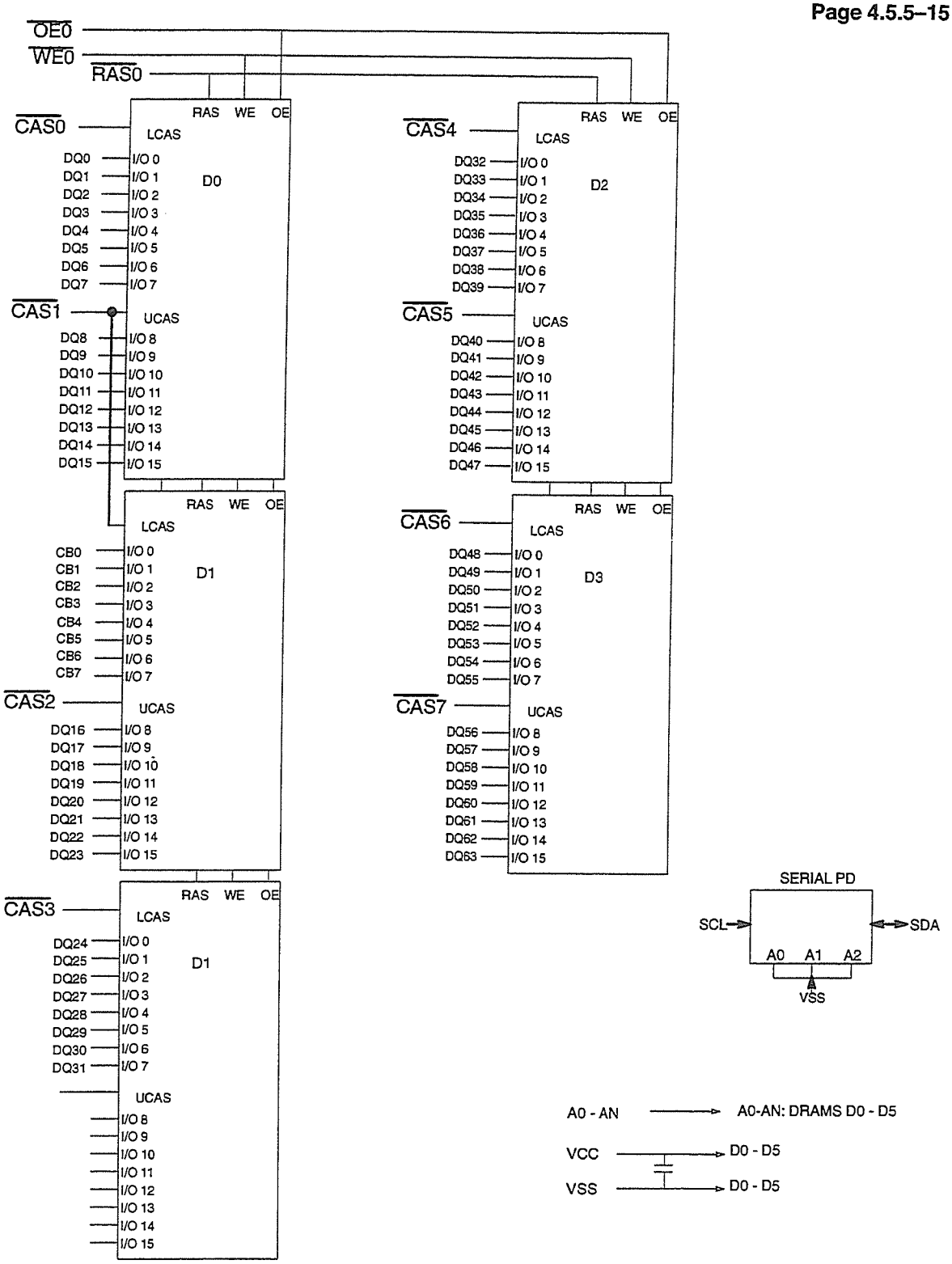


Figure 4.5.5–N
144 Pin X72 ECC DRAM SO–DIMM, 1 Bank with X16 DRAMs

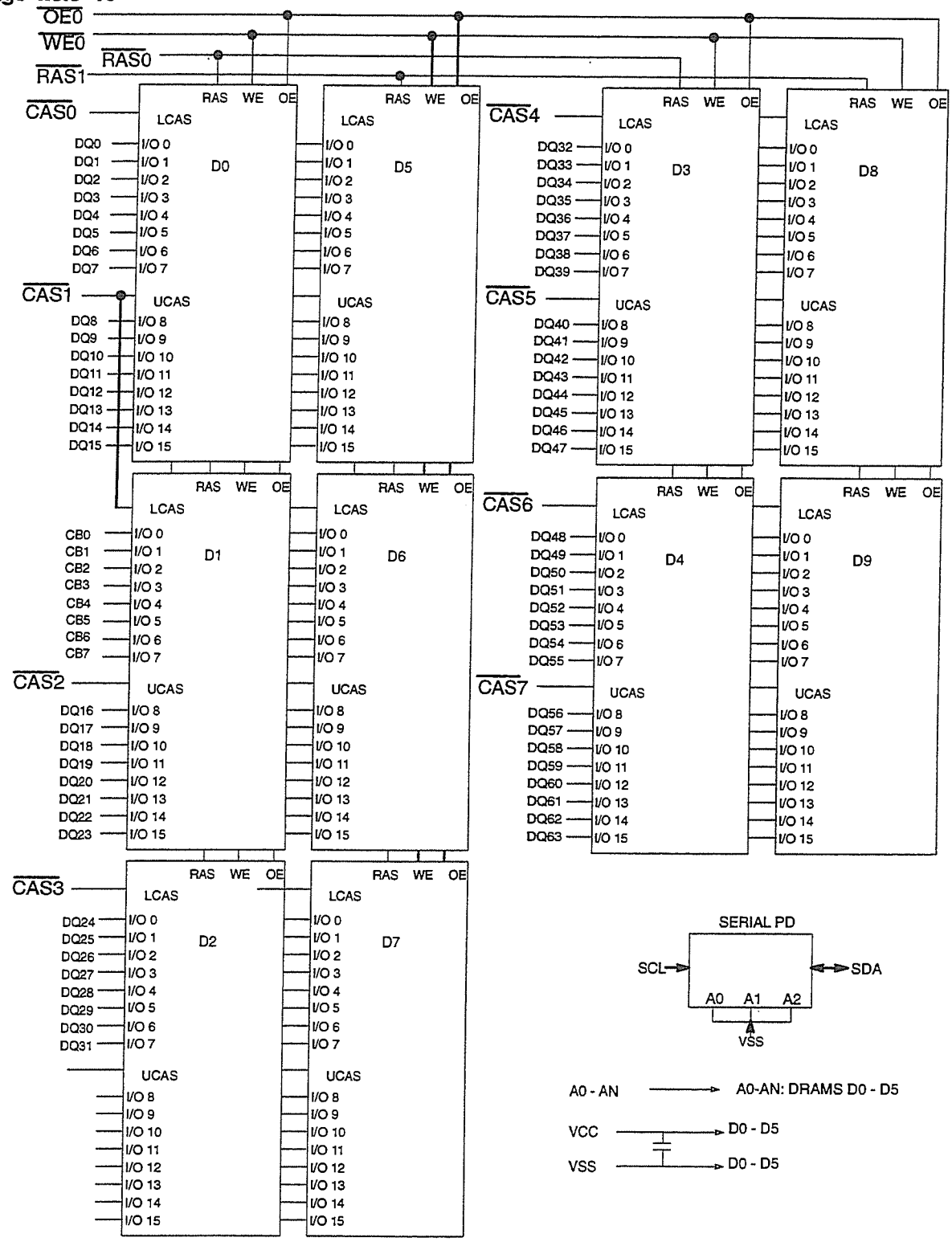


Figure 4.5.5–O
144 Pin X72 ECC DRAM SO–DIMM, 2 Bank with X16 DRAMs

4.5.6 – 144 PIN SDRAM SO-DIMM FAMILY

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 32, 36, & 40 bits.
DATA CONFIGURATIONS—Two DATA Word configurations are defined:
—64 BIT SDRAM without PARITY
—72 BIT SDRAM for ECC CODES
CONFIGURATION—10 Different Configurations are defined using various combinationa of X4, X8, and X16 SDRAM memories including 2 bank configurations, 5 for 64 bit and 5 for 72 bit.
LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that conist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—144 PIN JEDEC SO-DIMM MEMORY MODULE
PIN ASSIGNMENTS —Figs. 4.5.6-A & 4.5.6-B
SDRAM SPD INFORMATOION — Fig. 4.5.6-C
MODULE PIN NUMBERING AND KEYING METHODOLOGY — Fig. 4.5.6-D
TECHNOLOGY COMPARISON TABLE — Fig. 4.5.6-E
SDRAM CLOCK LOADING & WIRING—Figs. 4.5.6-F
X64 SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.6-G through 4.5.6-L
X72 SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.6-M through 4.5.6-P

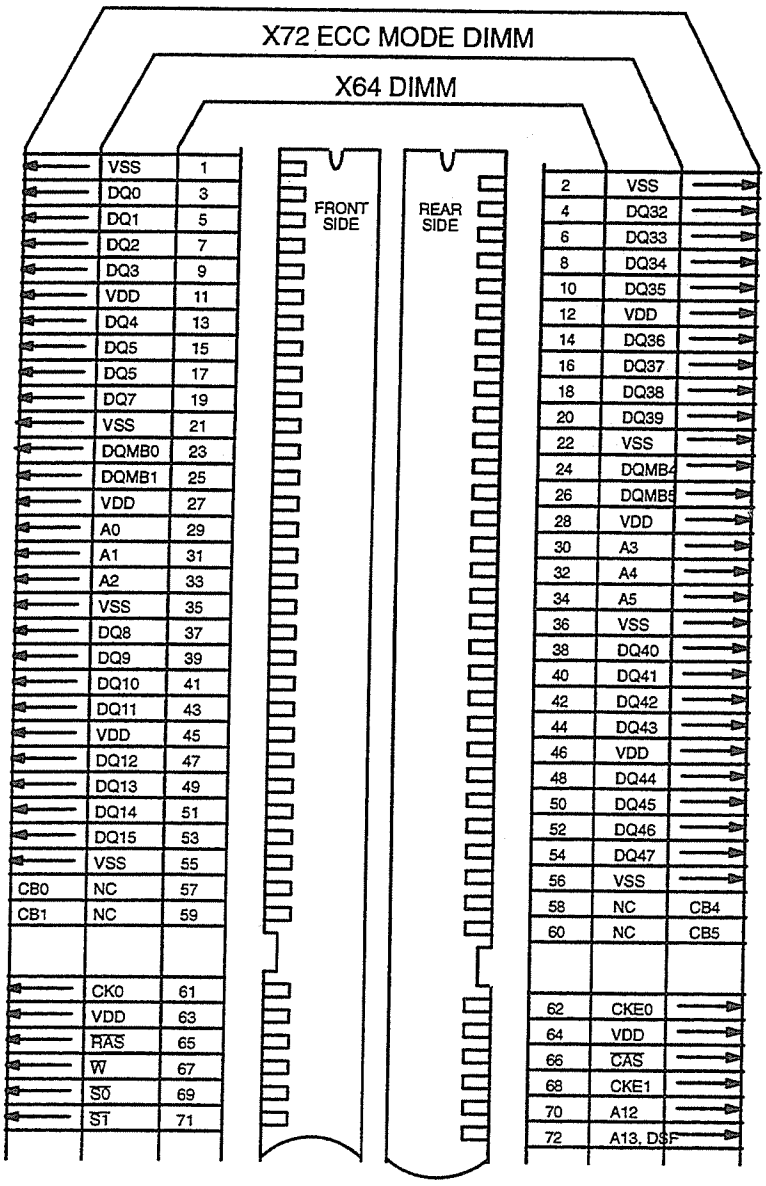


Figure 4.5.6–A
144 Pin X64 & X72 SDRAM SO–DIMM, PIN ASSIGNMENTS
UPPER HALF

0

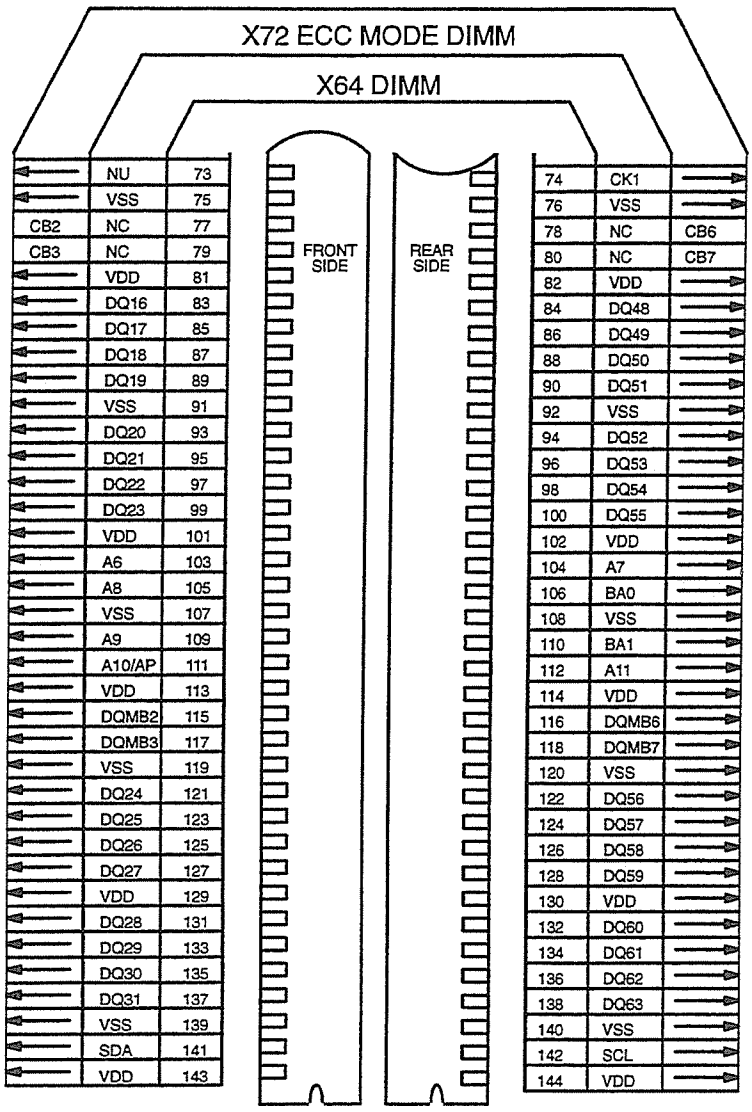


Figure 4.5.6–B
144 Pin X64 & X72 SDRAM SO–DIMM, PIN ASSIGNMENTS
LOWER HALF

Module Configuration	SDRAM Organization	Option 1			Option 2			Option 3		
		# Bank accr.	$\overline{RAS}$ accr.	$\overline{CAS}$ accr.	# Bank accr.	$\overline{RAS}$ accr.	$\overline{CAS}$ accr.	# Bank accr.	$\overline{RAS}$ accr.	$\overline{CAS}$ accr.
1M x 64/72	1M x 16	1	11	8						
2M x 64/72	1M x 16	1	11	8						
2M x 64	2M x 32	2	11	8						
2M x 64/72	2M x 8	1	11	9						
4M x 64/72	2M x 8	1	11	9						
4M x 64	2M x 32	2	11	8						
4M x 64/72	4M x 16	2	12	8	1	13	8			
8M x 64/72	4M x 16	2	12	8	1	13	8			
8M x 64	8M x 32	2	13	8	2	12	9			
8M x 64/72	8M x 8	2	12	9	1	13	9			
16M x 64/72	8M x 8	2	12	9	1	13	9			
16M x 64	8M x 32	2	13	8	2	12	9			
16M x 64/72	16M x 16	2	13	9						
32M x 64/72	16M x 16	2	13	9						
32M x 64/72	32M x 8	2	13	10						
64M x 64/72	32M x 8	2	13	10						
(Note: All options possible with SDRAM standards are shown)										

b. Allowable configurations: (Byte 11)
   - x64 (Non-parity, Byte controls)
   - x72 (ECC-optimized, Byte controls)

c. Functional Attributes:
   - Power Supply Voltage/Interface levels (Byte 8)
   - SDRAM cycle time (Byte 9)
   - SDRAM access from Clock (Byte 10)
   - Refresh rate/type (Byte 12)
   - SDRAM module attributes (Byte 13)
   - SDRAM device attributes (Bytes 14 - 20)
   - Primary/Secondary SDRAM (Bytes 21 - 22)

Figure 4.5.6–C
144 Pin SDRAM SO–DIMM, PD INFORMATION

The diagram below shows the keying methodology employed on 8-byte SO DIMMs. The voltage key provides a positive interlock so that SO DIMMs can only be plugged into a system with the proper supply voltage, reducing potential damage to the module DRAM chips. Unless the designer chooses the appropriate connector, the system will not work.

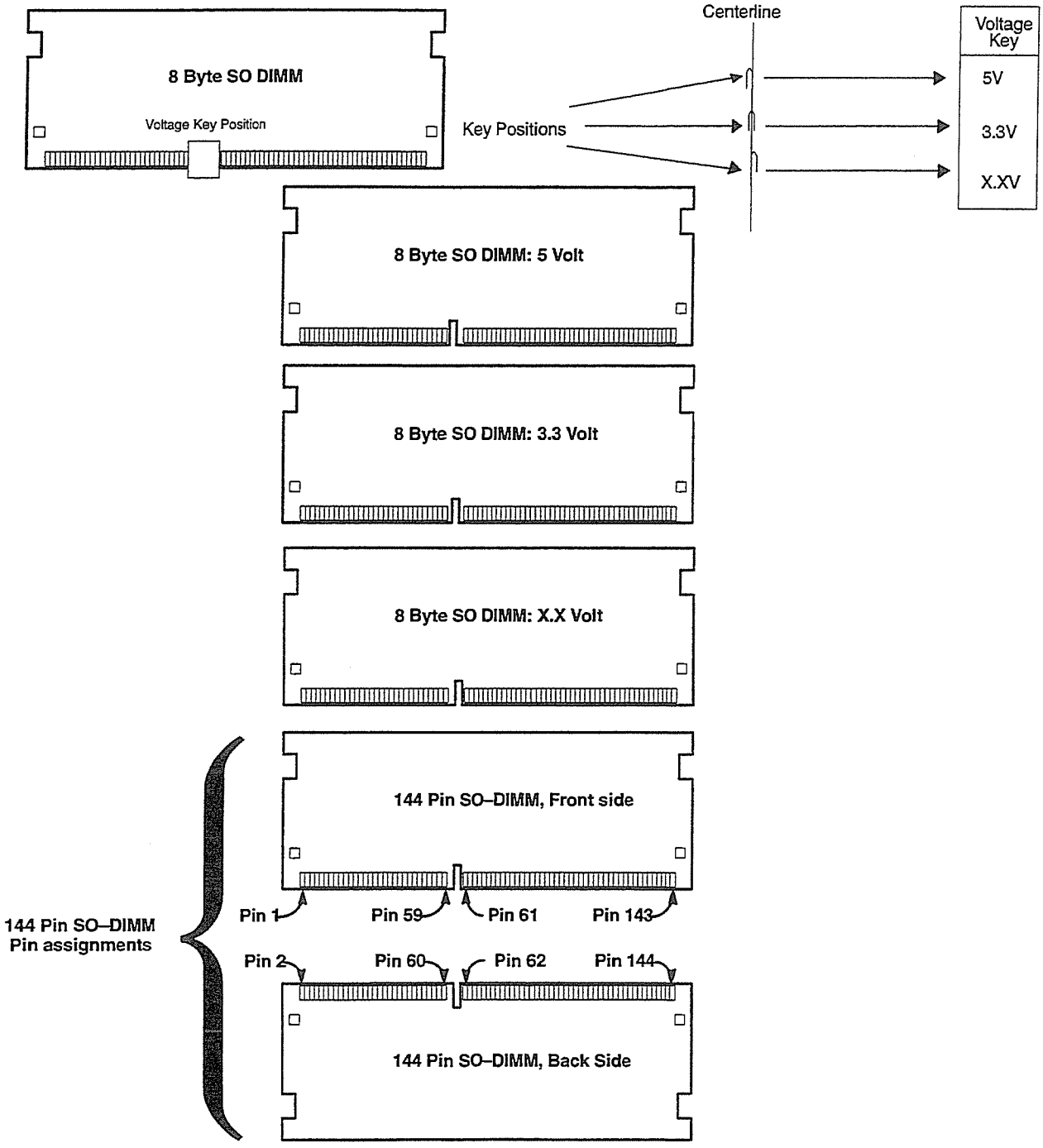


Figure 4.5.6–D
144 Pin SDRAM DIMM Keying Methodology

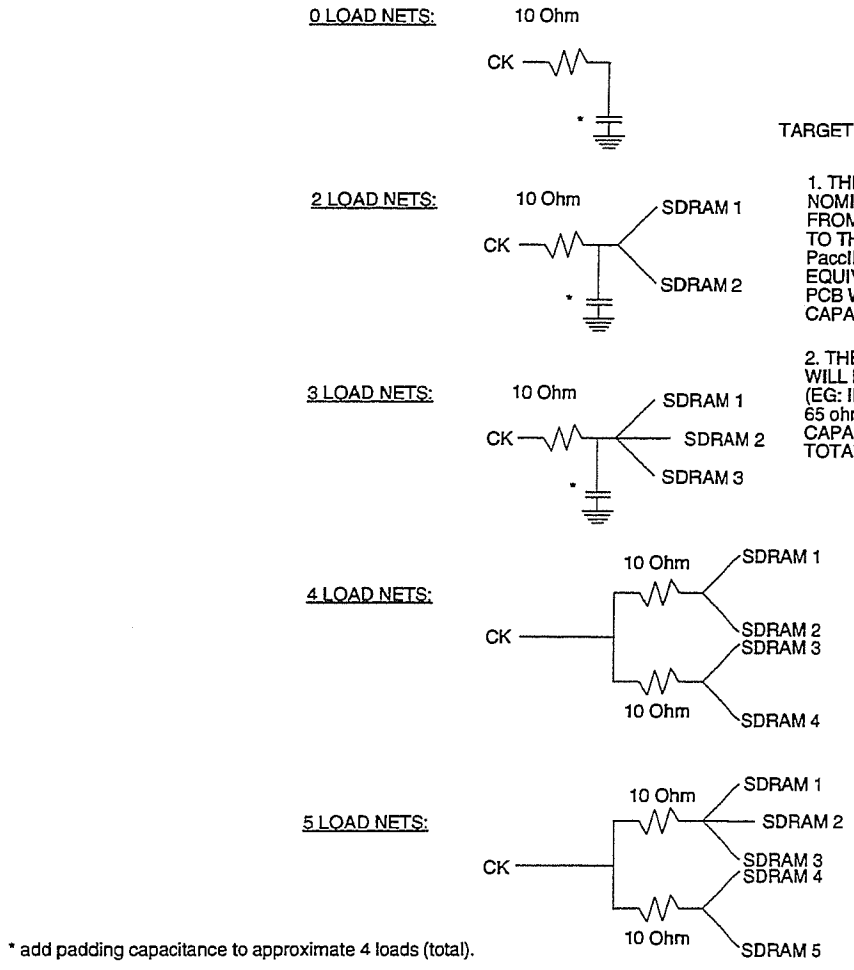
Pin #	DRAM SODIMM	SDRAM SODIMM
23	$\overline{CAS0}$	DQMB0
25	$\overline{CAS1}$	DQMB1
61	DU	CK0
65	DU	$\overline{RAS}$
69	$\overline{RAS0}$	$\overline{S0}$
71	$\overline{RAS1}$	$\overline{S1}$
73	$\overline{OE}$	DU
111	A10	A10/AP
115	$\overline{CAS2}$	DQMB2
117	$\overline{CAS3}$	DQMB3
24	$\overline{CAS4}$	DQMB4
26	$\overline{CAS5}$	DQMB5
62	DU	CKE0
66	DU	$\overline{CAS}$
68	NC	CKE1
70	NC	A12
72	NC	A13, DSF
74	NC	CK1
106	A11	BA0
110	A12	BA1
112	A13	A11
116	$\overline{CAS6}$	DQMB6
118	$\overline{CAS7}$	DQMB7

FIGURE 4.5.6–E
Pinout Comparison, 144 Pin DRAM & SDRAM SO–DIMM

Configuration	CK0	CK1
x8 (1 bank)	4	4
x16 (1 bank)	4	*
x8 (2 bank)	*1 (PLL)	*
x16 (2 bank)	4	4

Configuration	CK0	CK1
x8 (1 bank)	*4 OR 5	*4 OR 5
x16/x4 (1 bank)	*4 (MAX)	*4 (MAX)
x8 (2 bank)	*1 (PLL)	*
x16/x4 (2 bank)	*1 (PLL)	*

- add padding capacitance per clock wiring diagram.



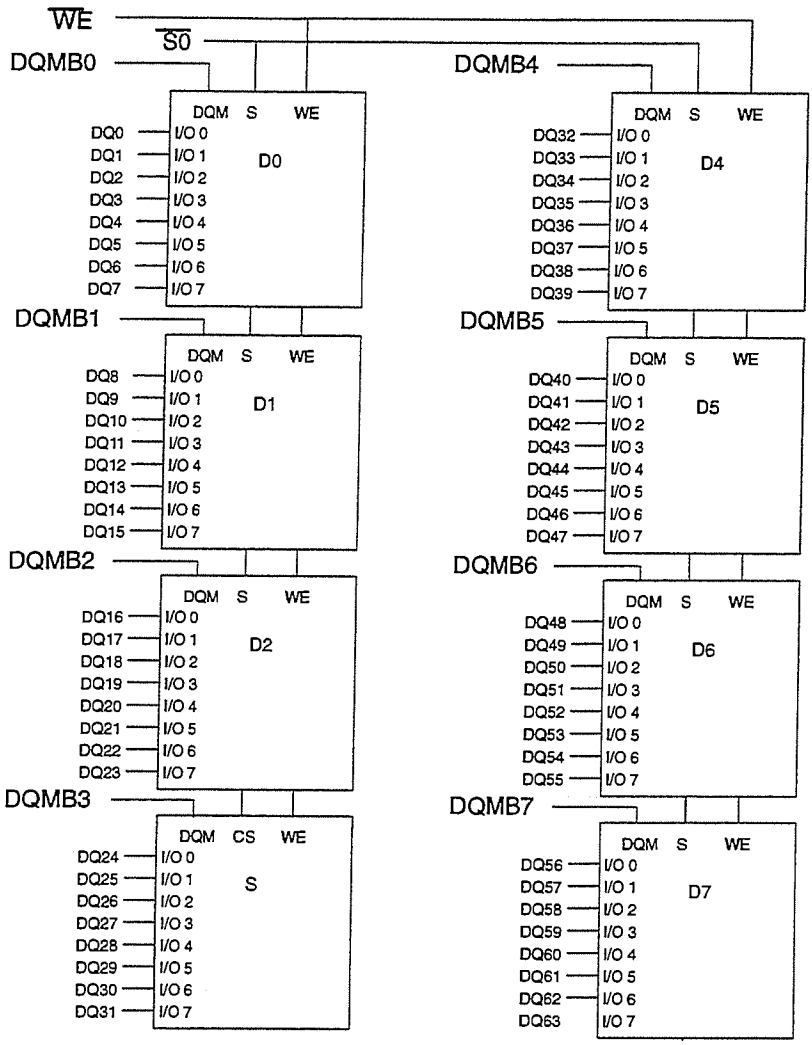
TARGET CLOCK (CK) SPECIFICATION:

1. THE CK INPUTS SHOULD HAVE A NOMINAL DELAY OF .4ns MEASURED FROM THE CK INPUT AT THE DIMM TAB TO THE CK INPUT OF THE SDRAM (OR PACCING CAPACITOR). (EG: THIS IS EQUIVALENT TO APPROXIMATELY 2" OF PCB WIRE AND 2.5pf OF INPUT CAPACITANCE).

2. THE VARIATION OF CK INPUT DELAY WILL BE +/- .1ns FOR BOTH CK INPUTS. (EG: IF THE WIRE IMPEDANCE IS APPROX 65 ohms, THIS CORRESPONDS TO A CAPACITANCE VARIATION OF +/- 3pf IN TOTAL CK INPUT CAPACITANCE).

* add padding capacitance to approximate 4 loads (total).

Figure 4.5.6–F
144 Pin SDRAM SO–DIMM, CLOCK LOADING AND WIRING



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

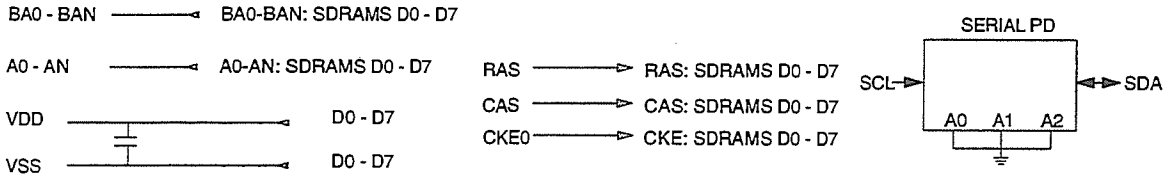
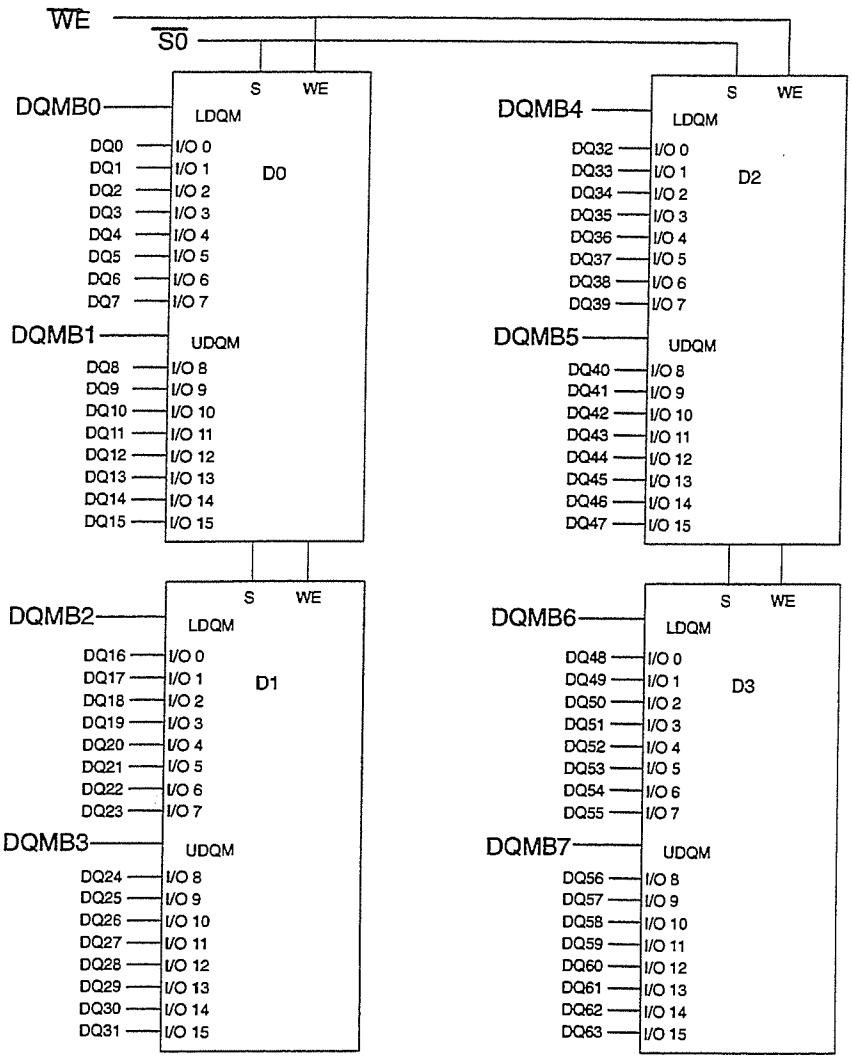


Figure 4.5.6–G
144 Pin X64 SDRAM SO–DIMM, 1 Bank with X8 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

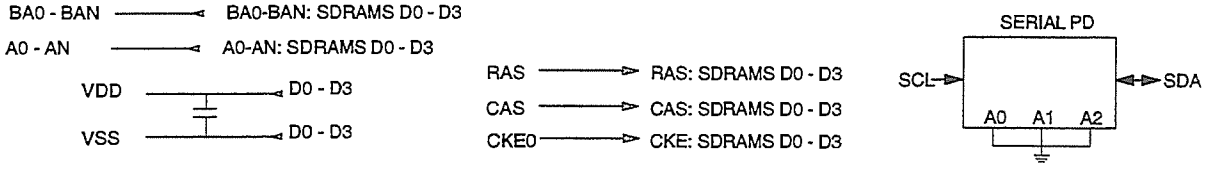


Figure 4.5.6–H
144 Pin X64 SDRAM SO–DIMM, 1 Bank with X16 SDRAMs

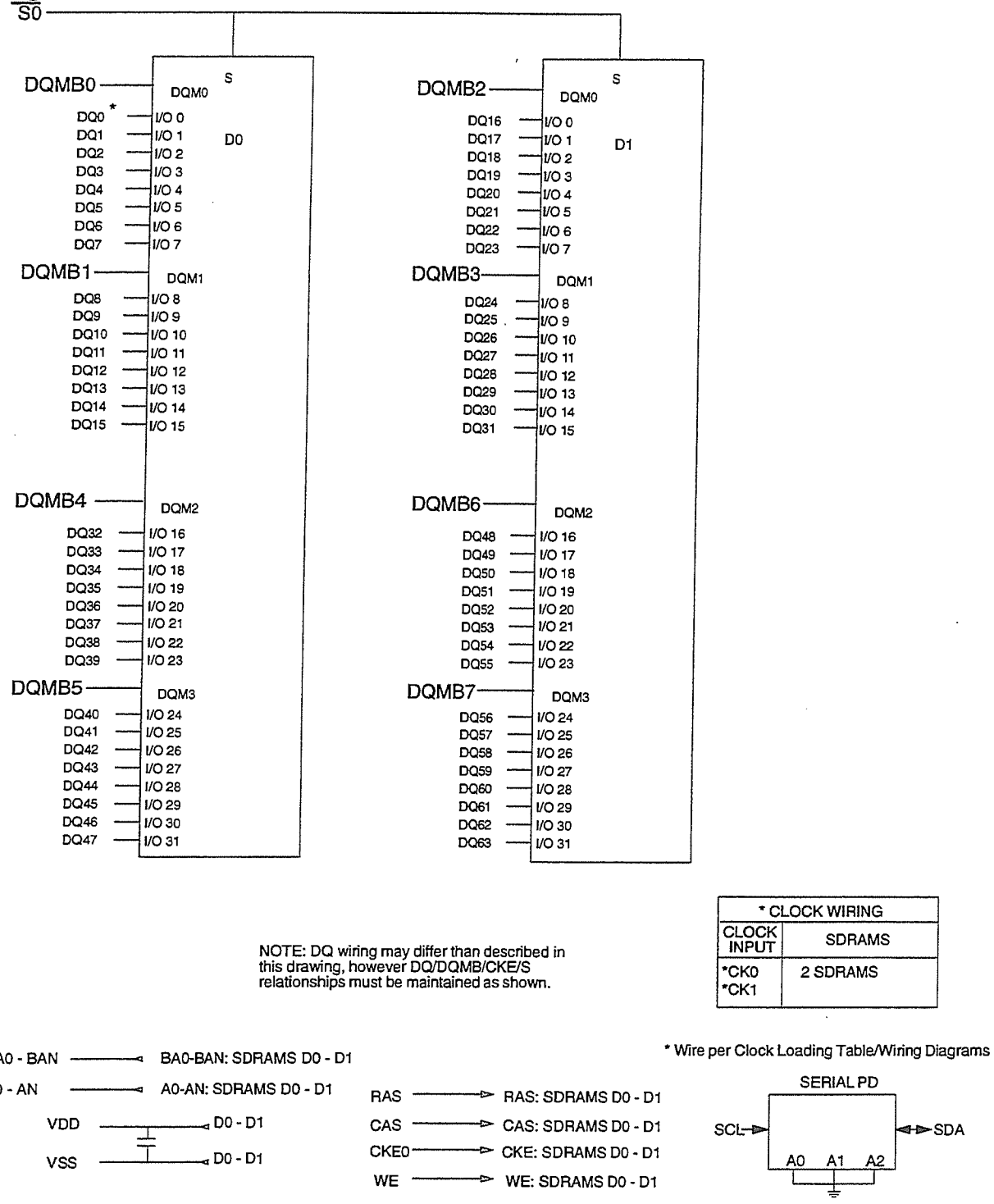
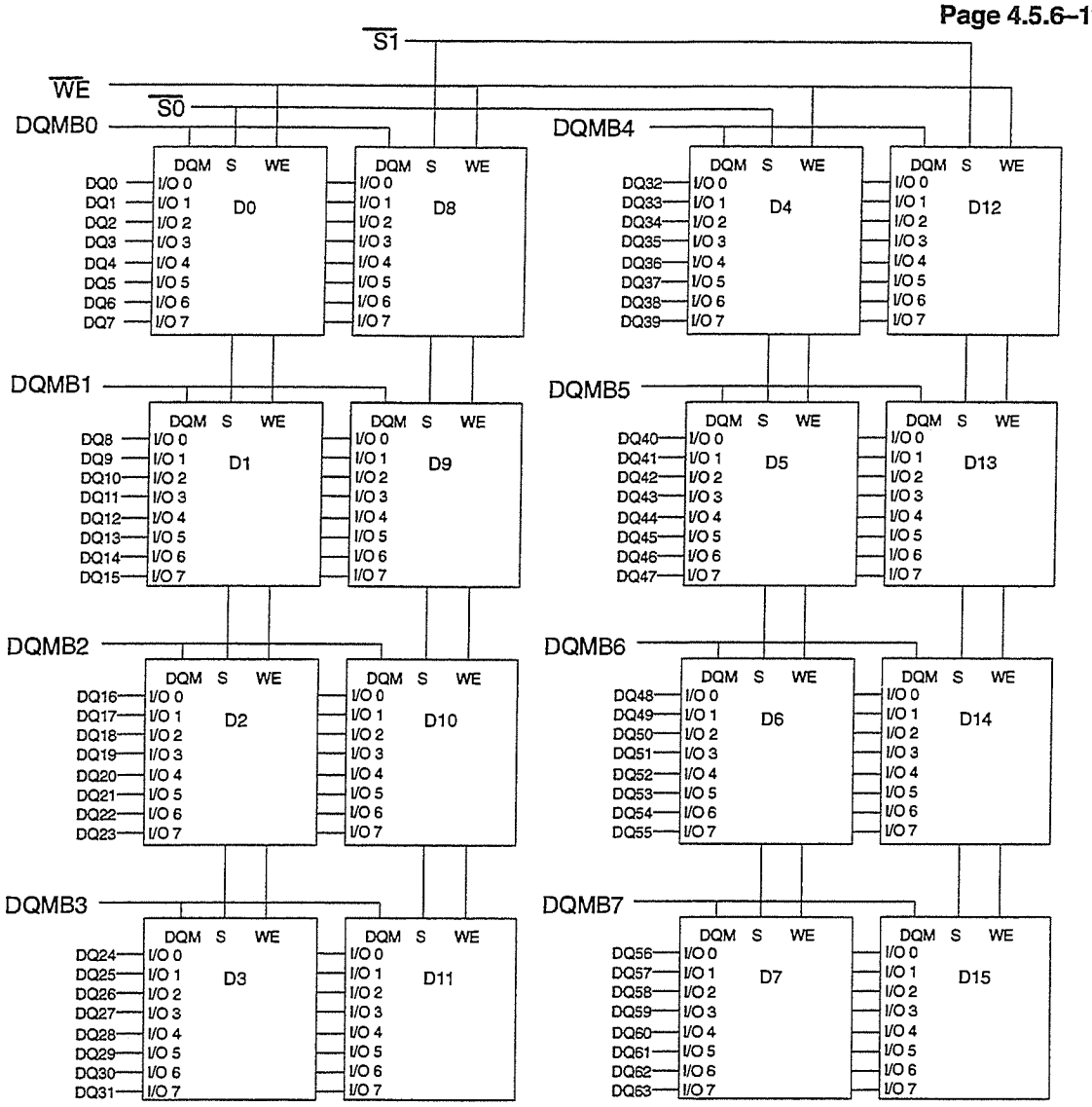


Figure 4.5.6-I
144 Pin X64 SDRAM SO-DIMM, 1 Bank with X32 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	VIA PLL TO ALL SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

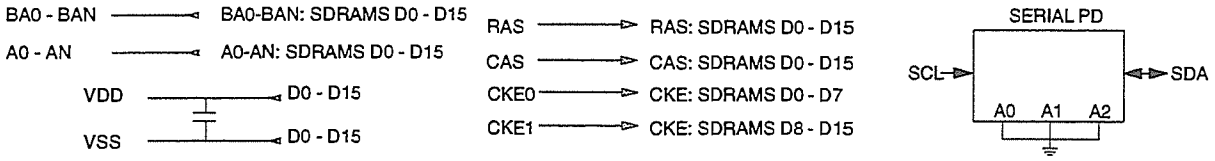
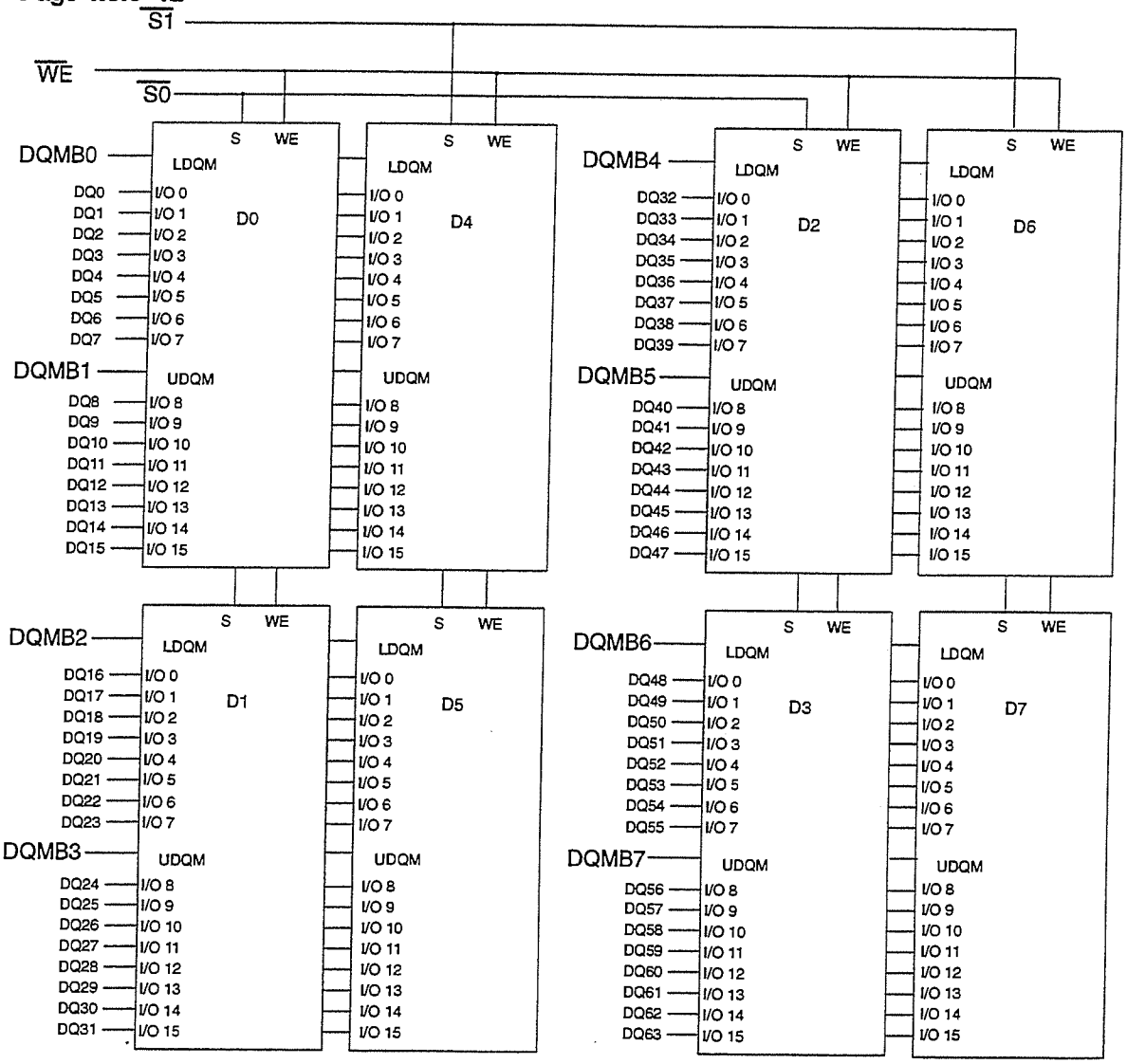


Figure 4.5.6–J
144 Pin X64 SDRAM SO–DIMM, 2 Bank with X8 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

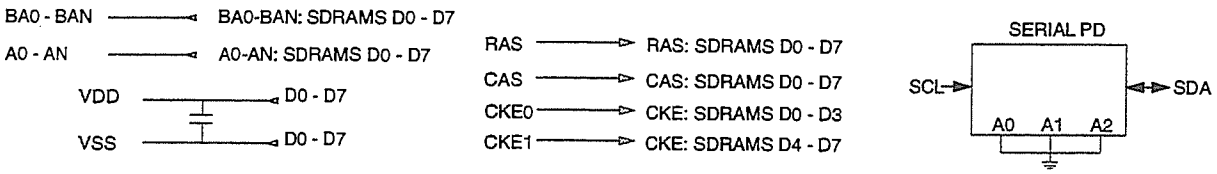
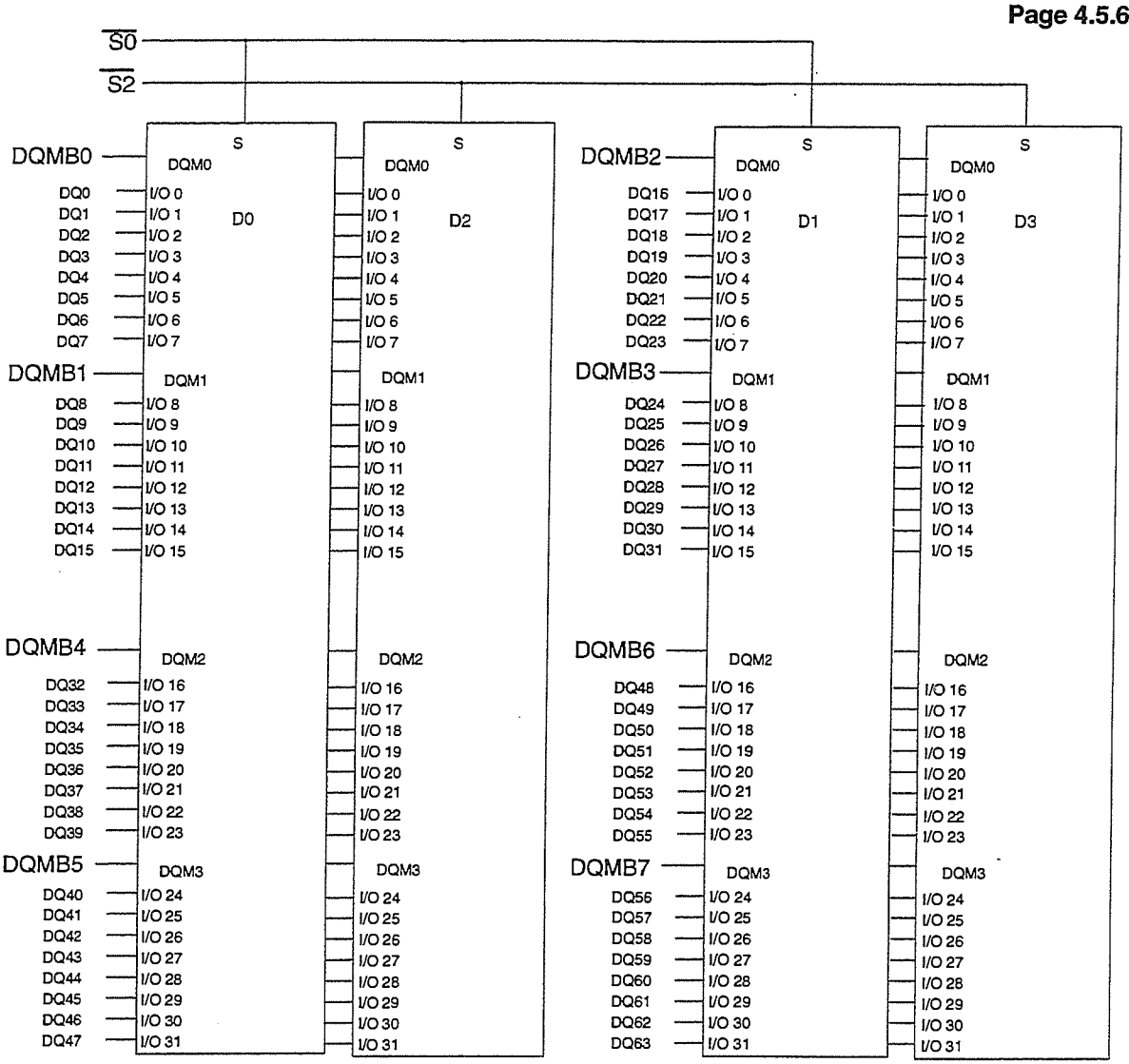


Figure 4.5.6–K
144 Pin X64 SDRAM SO–DIMM, 2 Bank with X16 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CK0 *CK1	4 SDRAMS

* Wire per Clock Loading Table/Wiring Diagrams

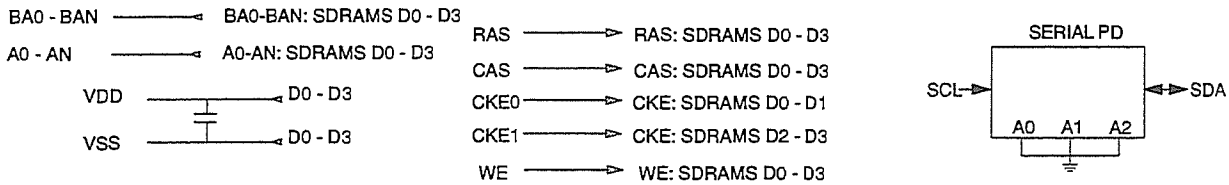


Figure 4.5.6–L
144 Pin X64 SDRAM SO–DIMM, 2 Bank with X32 SDRAMs

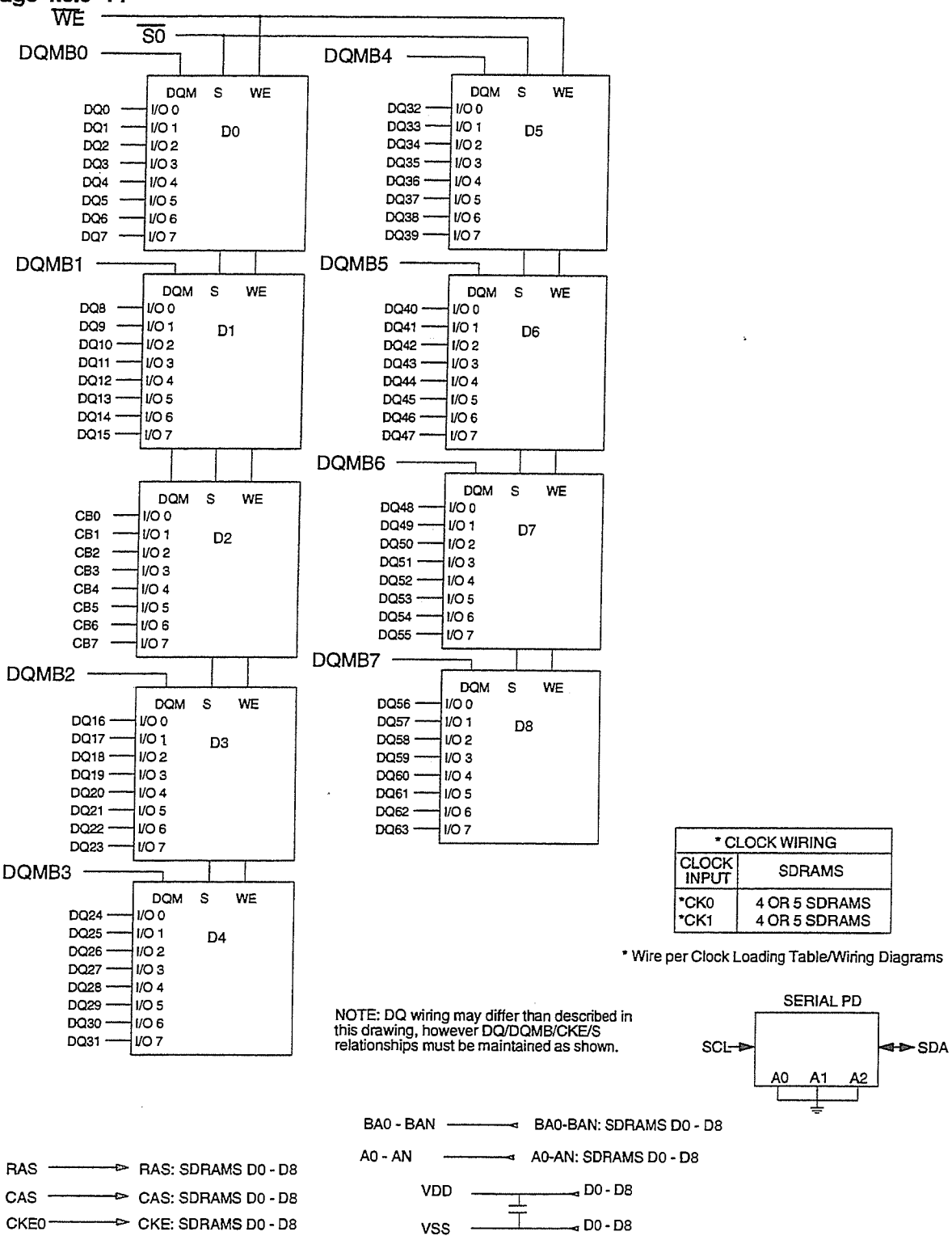


Figure 4.5.6–M
144 Pin X72 ECC SDRAM SO–DIMM, 1 Bank with X8 SDRAMs

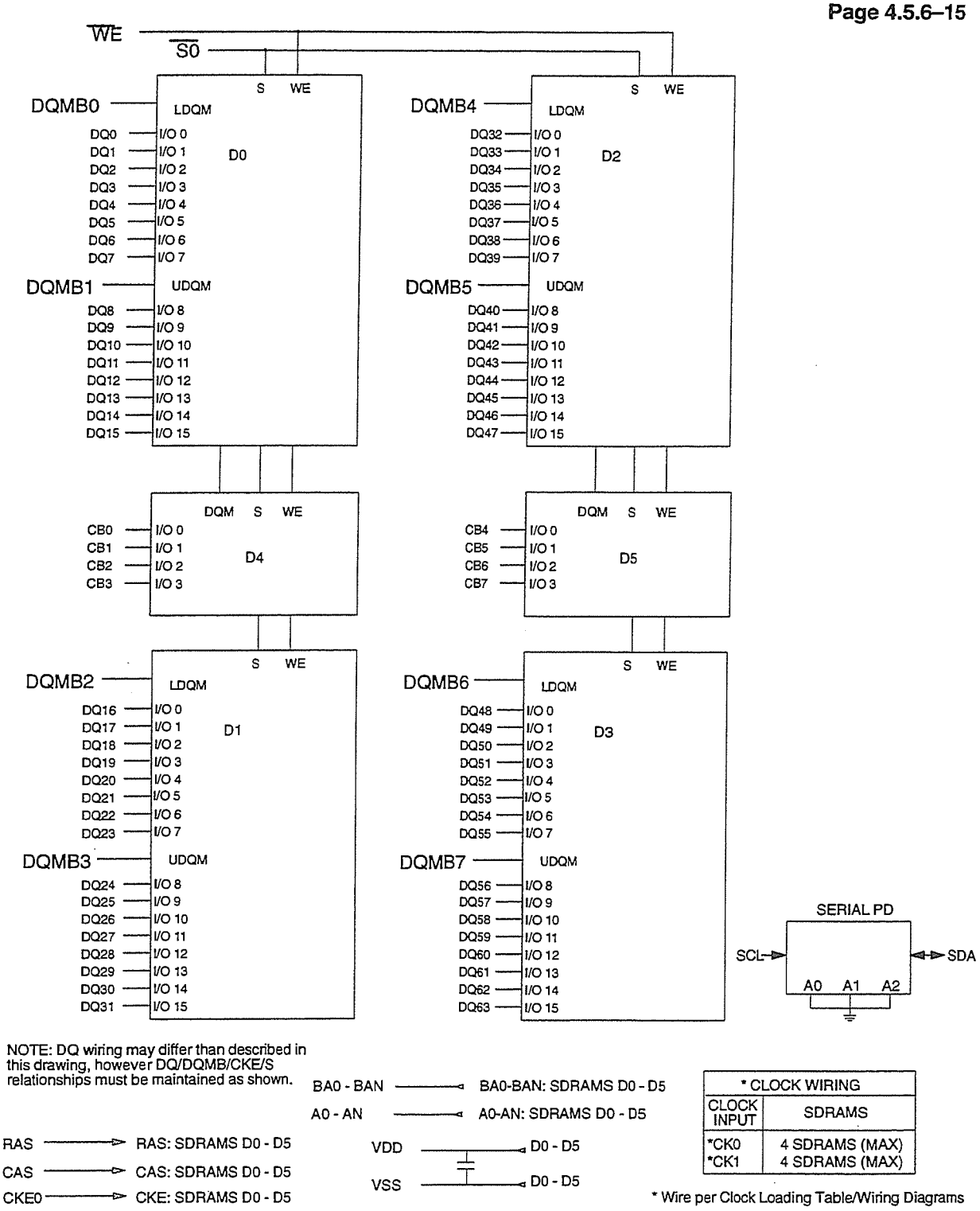


Figure 4.5.6–N
144 Pin X72 ECC SDRAM SO–DIMM, 1 Bank with X16 & X4 SDRAMs

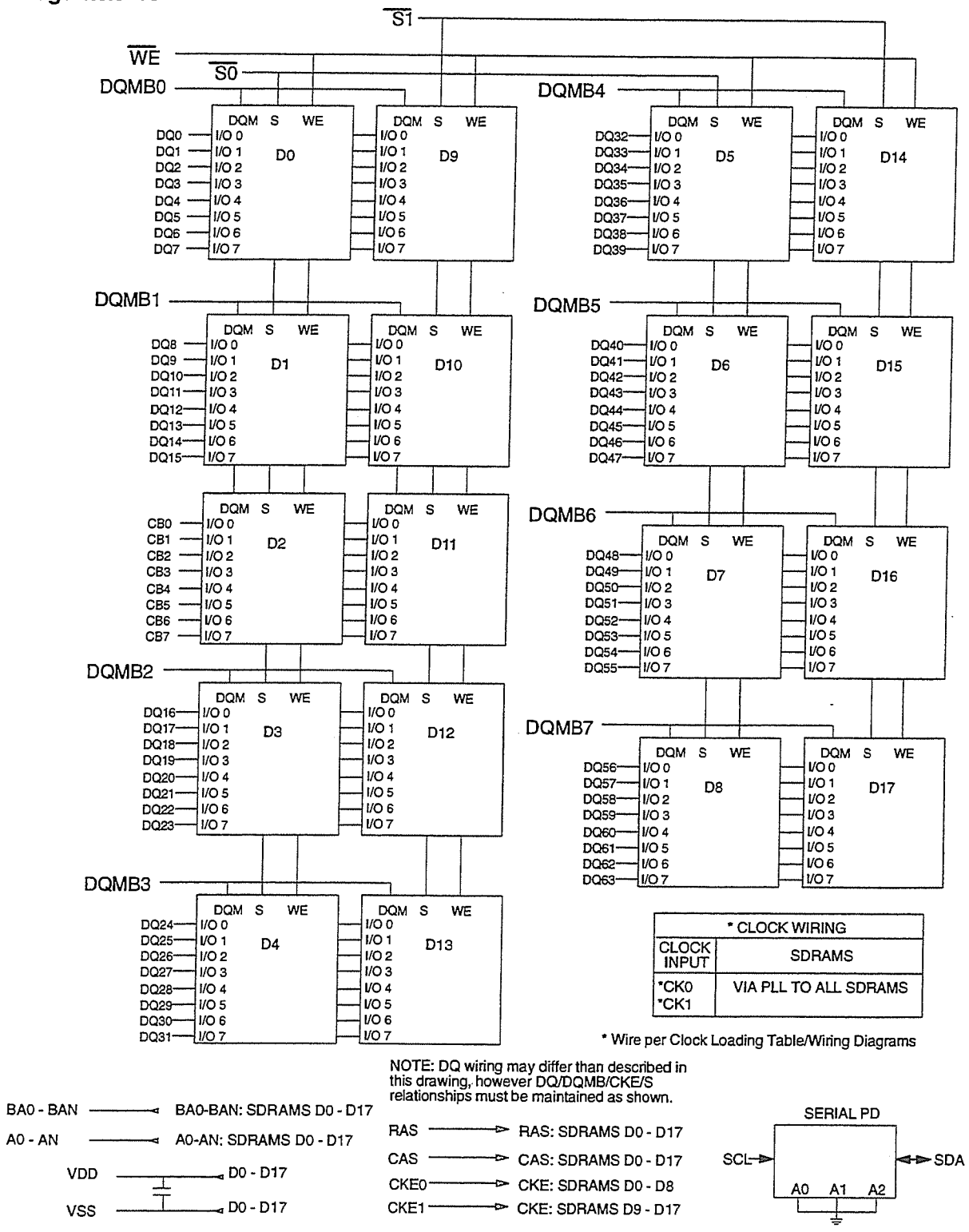


Figure 4.5.6–O
144 Pin X72 ECC SDRAM SO–DIMM, 2 Bank with X8 SDRAMs

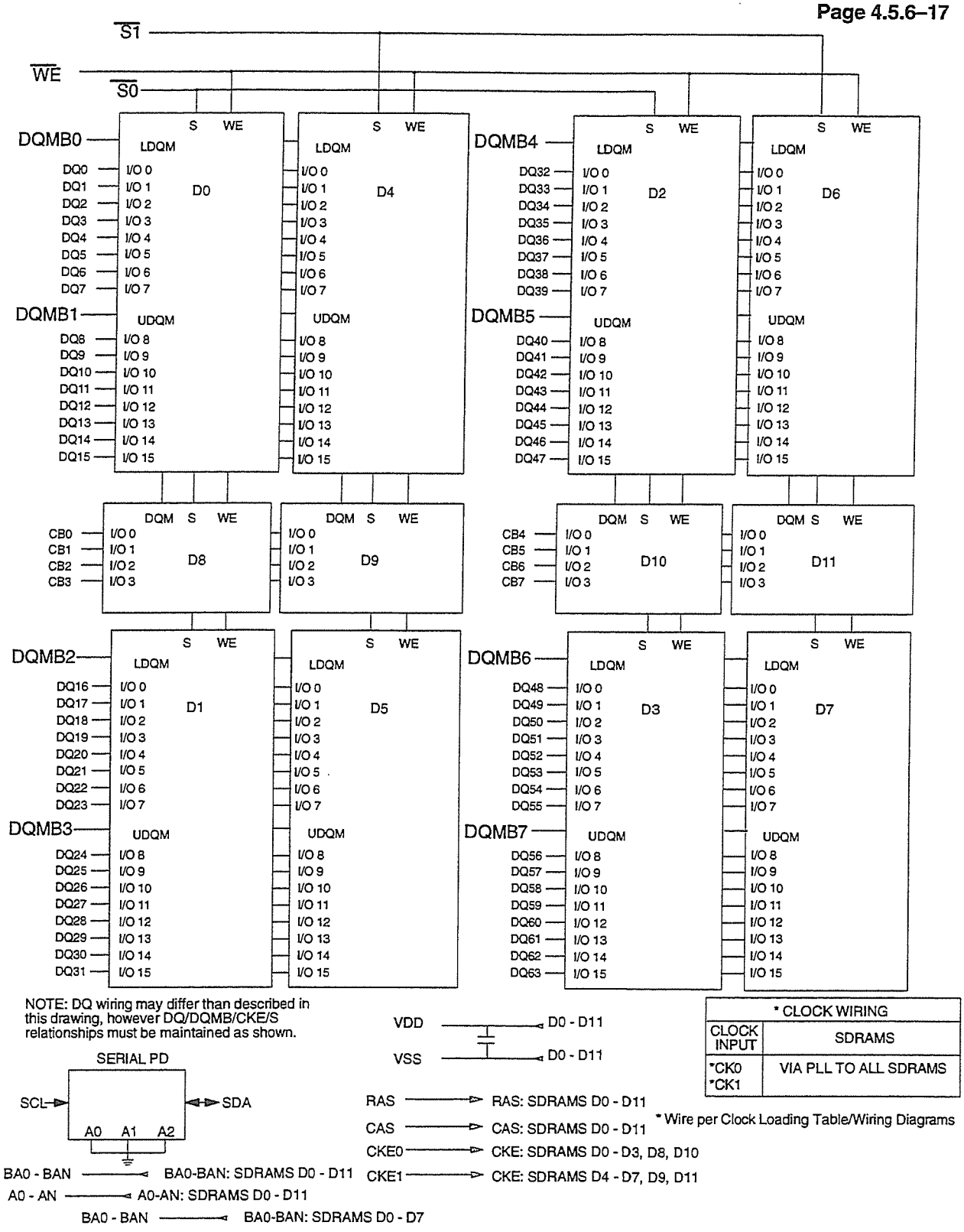


Figure 4.5.6–P
144 Pin X72 ECC SDRAM SO–DIMM, 2 Bank with X16 & X4 DRAMs

4.6 Sixteen Byte Memory Modules

4.6.1 – 278 PIN BUFFERED SDRAM DIMM FAMILY

4.6.1 – 278 PIN BUFFERED SDRAM DIMM FAMILY

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 16 bytes (144 bits).
DATA CONFIGURATIONS—Only one DATA Word configurations is defined in the initial release:
—144 BIT SDRAM with the location of CHECKBITS undefined
CONFIGURATION—2 Different Configurations are defined using X16 SDRAM memories with 1 and 2 banks
LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that conist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—278 PIN JEDEC DIMM MEMORY MODULE
PIN ASSIGNMENTS —Figs. 4.6.1–A, 4.6.1–B, & 4.6.1–C
DRAM SPD INFORMATOION — Fig. 4.6.1–D
MODULE KEYING DEFINITION — Fig. 4.6.1–E
MODULE PIN DEFINITIONS — Fig. 4.6.1–F
X144 SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.6.1–G and 4.6.1–H

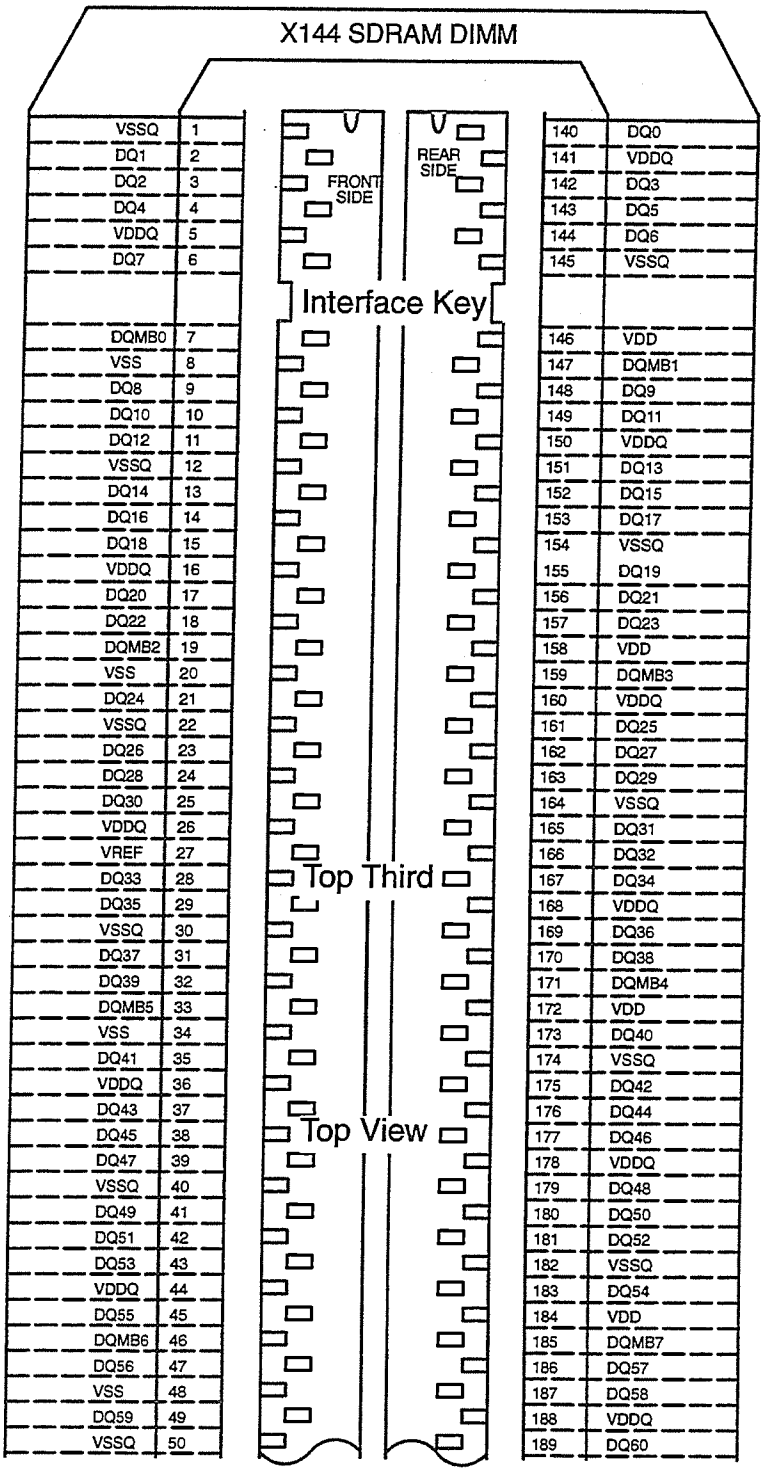


Figure 4.6.1–A
278 PIN X144 SDRAM DIMM PINOUT (TOP THIRD)

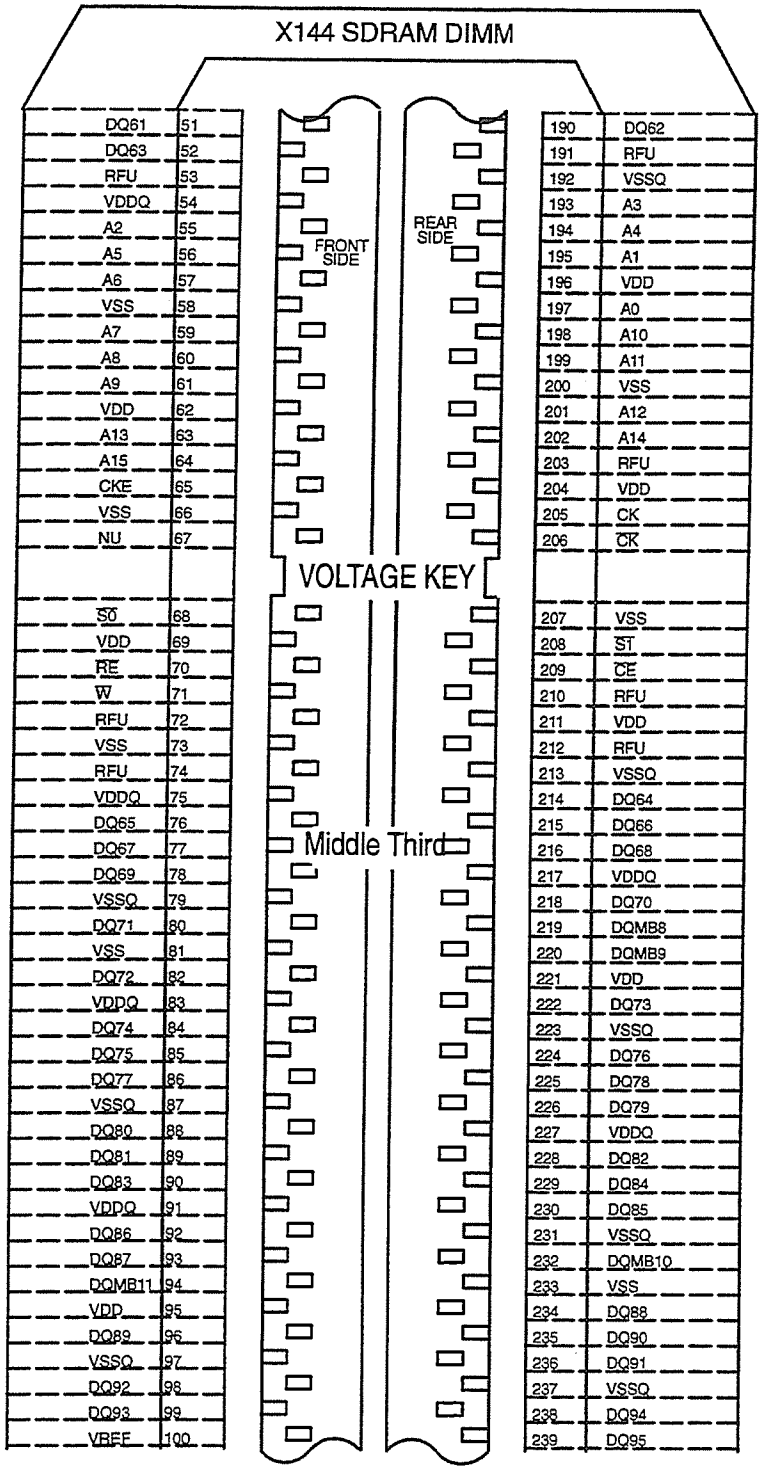


Figure 4.6.1–B
278 PIN X144 SDRAM DIMM PINOUT (MIDDLE THIRD)

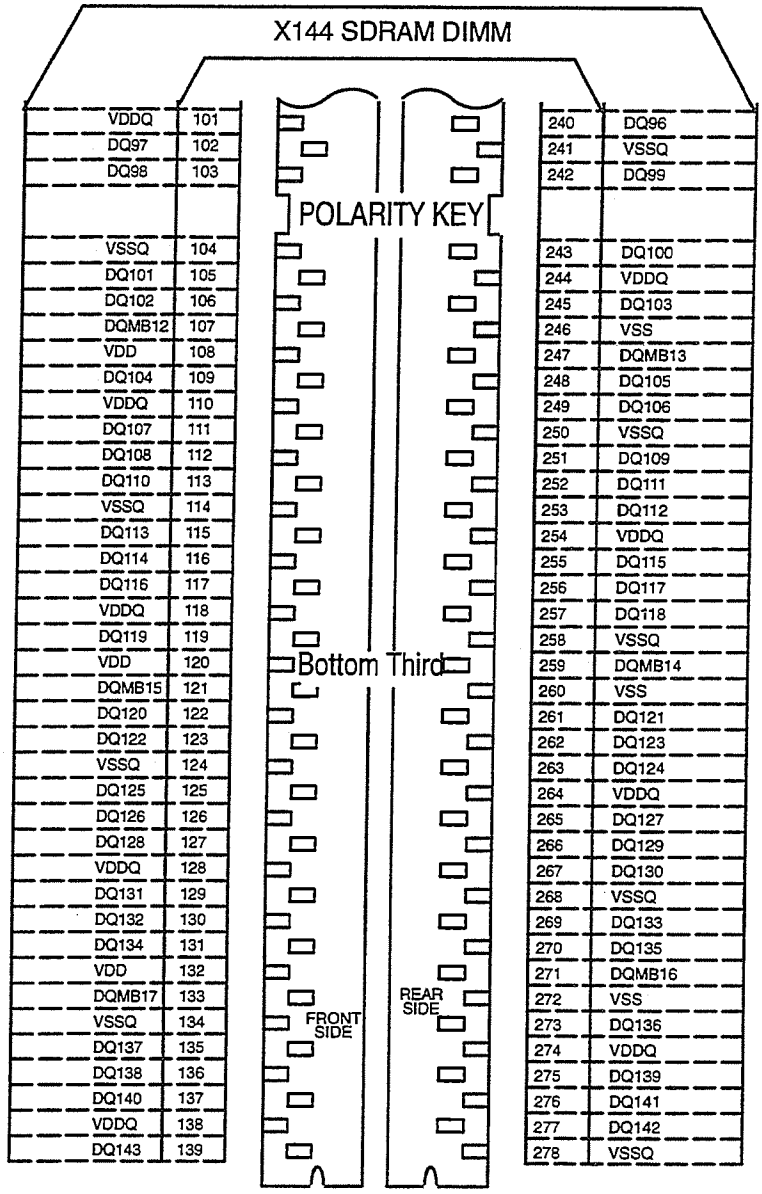


Figure 4.6.1–C
278 PIN X144 SDRAM DIMM PINOUT (BOTTOM THIRD)
Release 7

This page is reserved for the future addition of serial presence detect tables.

Figure 4.6.1–D
278 PIN X144 SDRAM DIMM PD AND CONFIGURATION TABLES
Release 7

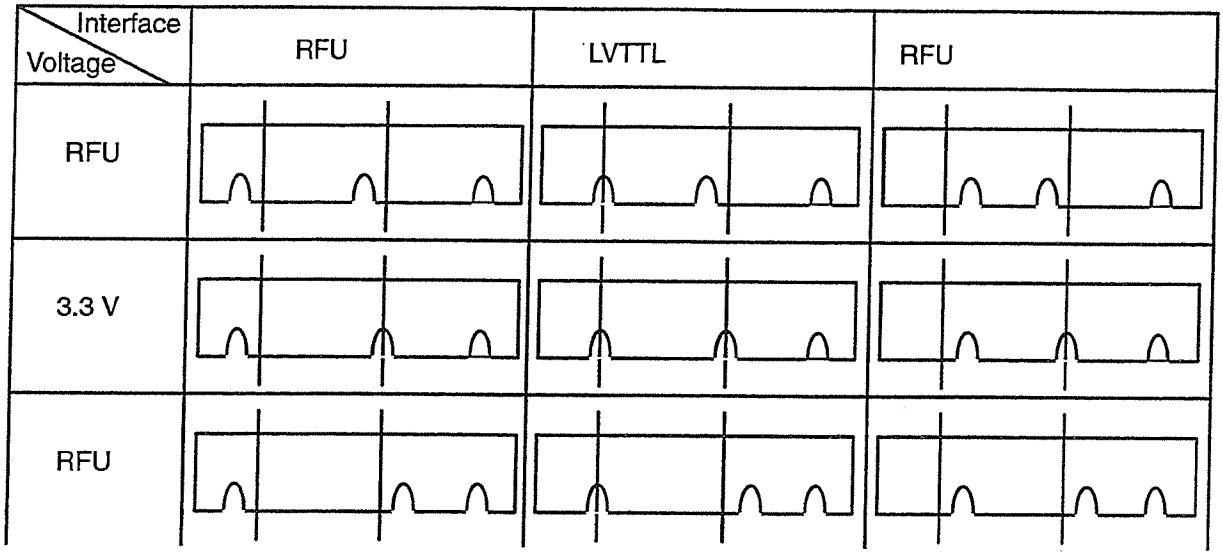
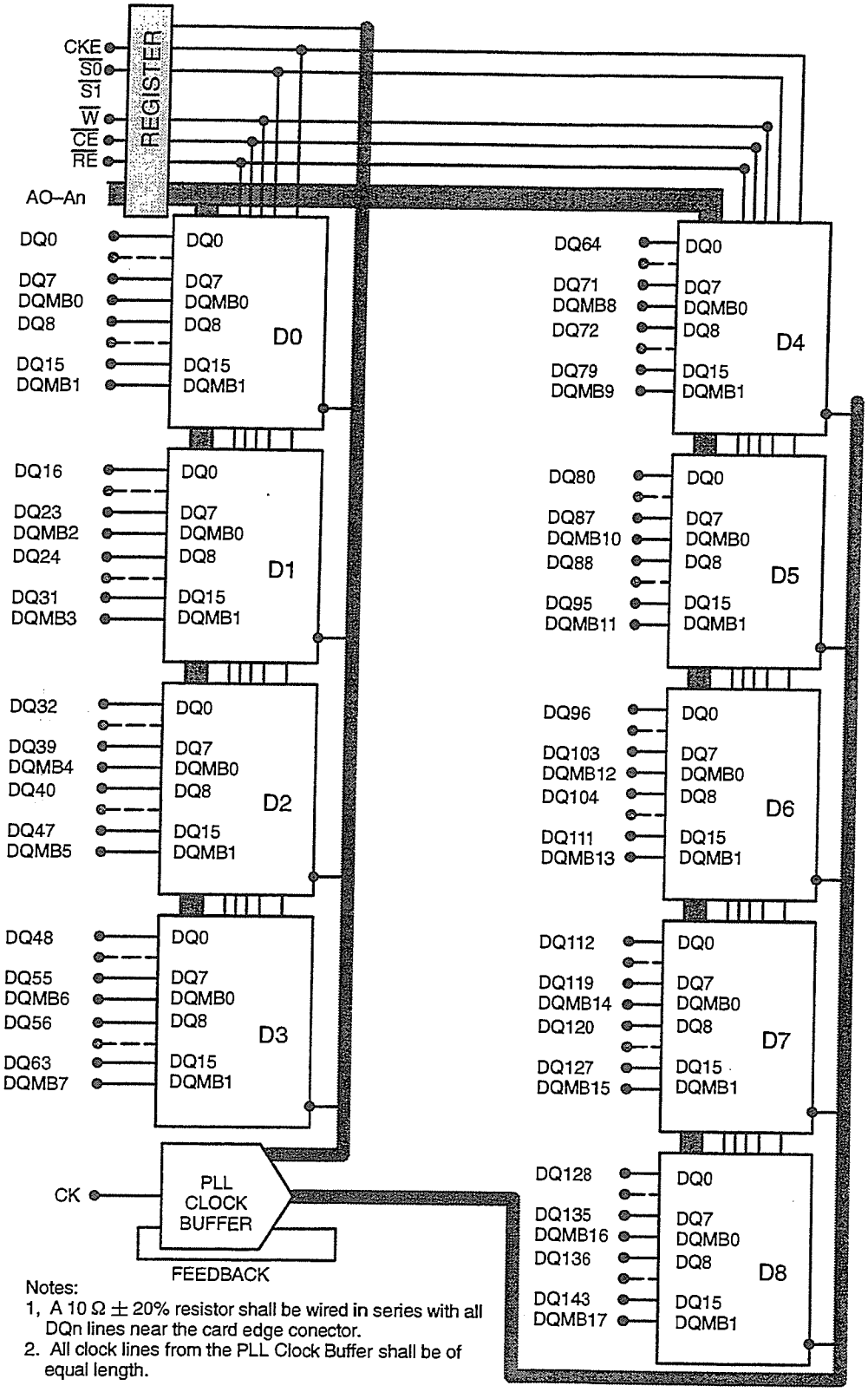


Figure 4.6.1-E
278 PIN 144 BIT SDRAM DIMM MECHANICAL KEY DEFINITION

Pin Name	Number	Function
A0....A15	16	Address Input (multiplexed)
DQ0....DQ143	144	Data Input/Output (common)
CK, $\overline{CK}$	2	Clock Input
CKE	1	Clock Enable Input
$\overline{S0}$, $\overline{S1}$	2	Chip Select Input
$\overline{RE}$	1	Row Enable (RAS) Input
$\overline{CE}$	1	Column Enable (CAS) Input
$\overline{W}$	1	Write Enable Input
DQM	1	Data Mask
DQMB0....DQMB17	18	Byte Data Mask input
VDD	14	Primary Positive Power Supply
VDDQ	27	Posivite Power for Input/Output
VREF	2	Reference Power Supply
VSS	14	Ground
VSSQ	27	Ground for data Input/Output
NU	1	Reserved for board test of PLL
RFU	7	Reserved for Future Use

Notes:
1. NU pin is reserved for board test control of PLL, Make no connection at system level.
2 RFU pins are available for future standardization of serial Presence Detect and VTT.

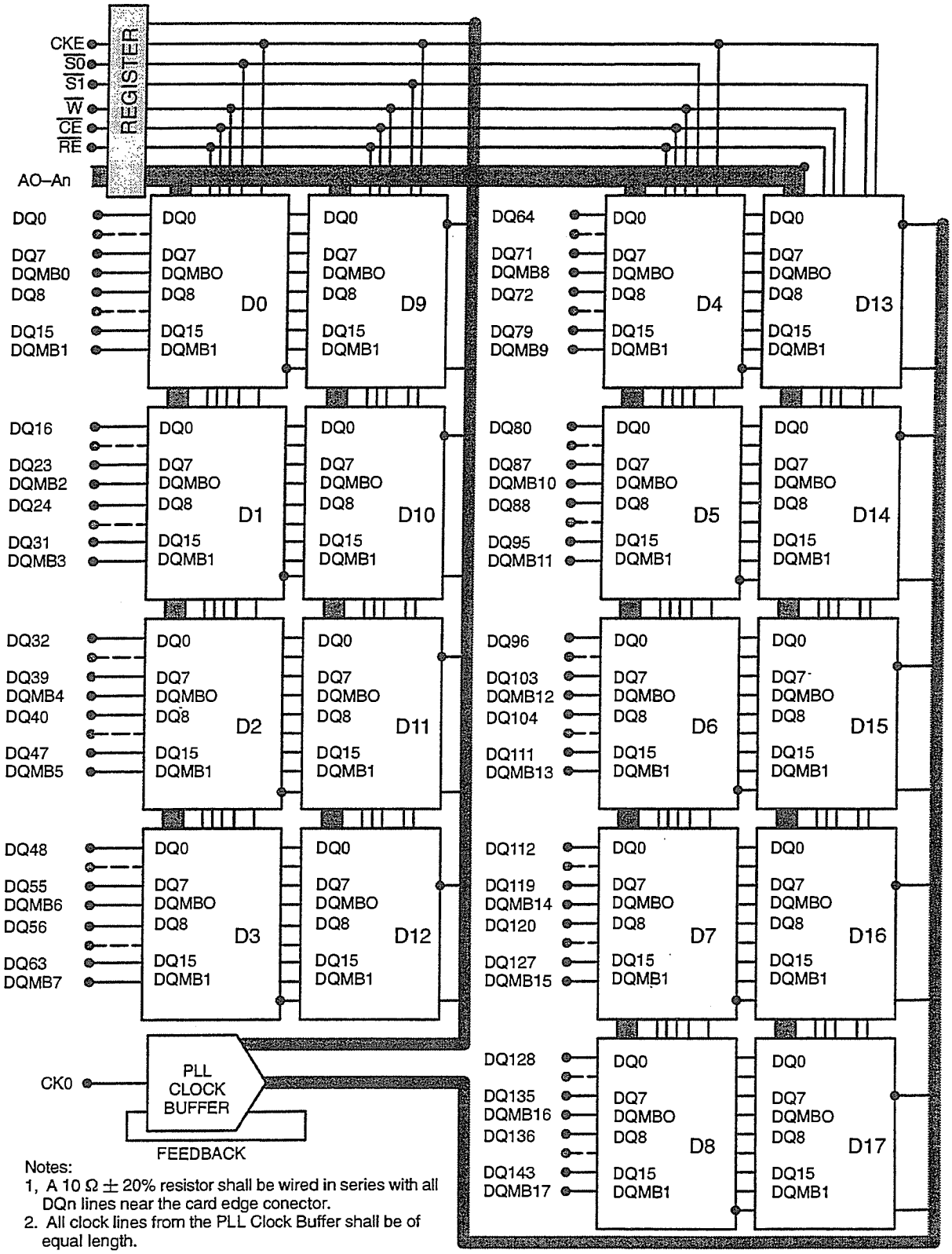
Figure 4.6.1-F
278 PIN 144 BIT SDRAM DIMM PIN DEFINITIONS



Notes:
1, A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.6.1–G
278 PIN X144 BUFFERED SDRAM DIMM 1 BANK with X16 SDRAM

Release 7



Notes:
1, A 10 Ω ± 20% resistor shall be wired in series with all DQn lines near the card edge conector.
2. All clock lines from the PLL Clock Buffer shall be of equal length.

Figure 4.6.1–H
278 PIN X144 BUFFERED SDRAM DIMM 2 BANKS with X16 SDRAM
Release 7

532

5 PROGRAMMABLE LOGIC AND ASIC DEVICES

The following standards define pinouts for Programmable Logic Devices (PLD) and Programmable Application Specific Devices (ASIC). These standards were all developed by the BIPOLAR Committee.

5.1 Pin Out Standards

5.1.1 PIN–OUT STANDARDS FOR PLD DIP TO SCC CONVERSION

This standard defines the pin–out conventions for converting a PLD in DIP to an SCC. Conversions are given for five different packages:

5.1.1.1 – 20 PIN DIP to 20 TERMINAL SCC, 0.350" BY 0.350", Fig. 5–1

5.1.1.2 – 24 PIN DIP to 28 TERMINAL SCC, 0.450" BY 0.450", Fig. 5–2

5.1.1.3 – 28 PIN DIP to 28 TERMINAL SCC, 0.450" BY 0.450", Fig. 5–2

5.1.1.4 – 24 PIN FUNCTIONS IN 28 PIN DIP & 28 TERMINAL SCC, Fig. 5–9

5.1.1.5 – 20 PIN FUNCTIONS IN 28 TERMINAL SCC AND 24 PIN DIP FOR HIGH SPEED OPERATION, Fig. 5–11

5.1.2 POWER PIN LOCATIONS FOR PLD and ASIC DEVICES

The following standards define the power pin locations for PLD and ASIC devices in a variety of packages.

5.1.2.1 – POWER PIN LOCATIONS FOR ECL PLD IN DIP

This standard defines the location of the power pins for ECL PLD devices in 24 PIN DIP. It is applicable to all currently available ECL families. The power pin locations are defined in Fig. 5–3.

5.1.2.2 – POWER PIN LOCATIONS FOR TTL PLD IN DIP and CC

This standard defines the location of the power pins for TTL PLD devices in 40 PIN DIP and 44 TERMINAL CC. It is applicable to all currently available TTL compatible families. The power pin locations are defined in Figures 5–4 & 5–5.

5.1.2.3 – POWER PIN LOCATIONS FOR TTL PROGRAMMABLE ASIC IN DIP and CC

This standard defines the location of the power pins for TTL compatible PROGRAMMABLE ASIC devices in 48 & 64 PIN DIP and 52, 64, & 84 TERMINAL CC. It is applicable to all currently available TTL compatible families. The power pin locations are defined in Figures 5–6 & 5–7.

5.1.2.4 – POWER PIN LOCATIONS FOR PLD IN 132 PIN QFP

This standard defines the POWER and GROUND connections for PLD devices in 132 Pin Quad Flat Pack packages. This standard is compatible with other standards for JEDEC Standards on packages with 40 through 84 pins. The power pin locations are defined in Figure 5–10.

5.1.3 Nomenclature for FPLD

This standard defines a compact nomenclature to be used to describe Field Programmable Logic Devices. The standard is applicable to all current and future devices, regardless of technology, density, and package. The details of the standard will be published as an addendum to EIA standard RS–428.

5.1.4 PLD Data Transfer Format

This standard defines a data transmission format to be used for transmitting data between a data preparation system and a device programmer that is used to program a PLD device.
The details of this standard are contained in JEDEC STANDARD #3–B published Nov. 1989.

5.1.5 PLD Standard OUTPUT LOADS

This standard defines a set of output loads providing various drive capabilities for PLD devices operating at either TTL, CMOS, and 3.3 V interface levels. A method is given whereby loads for other combinations of drive capabilities may be established. The details of this standard are shown in Figures 5–8A, B, C, & D.

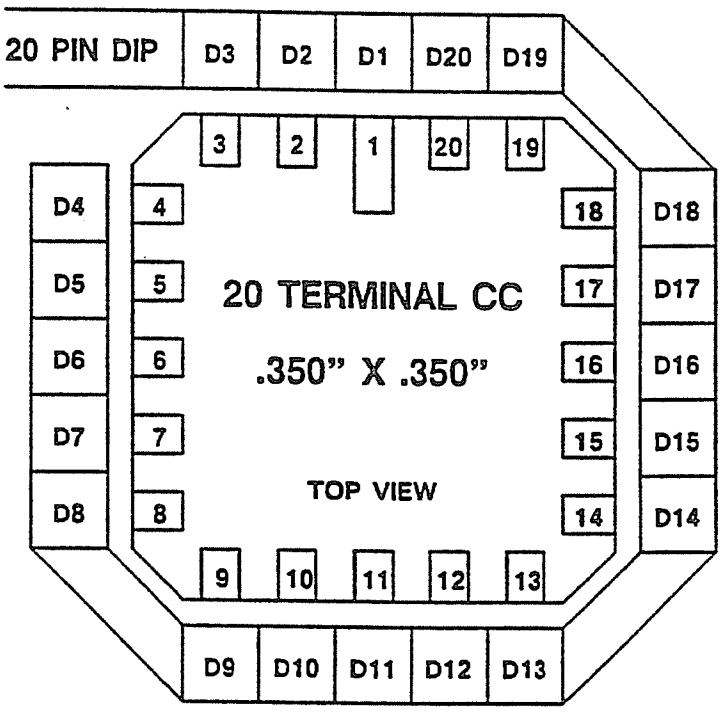
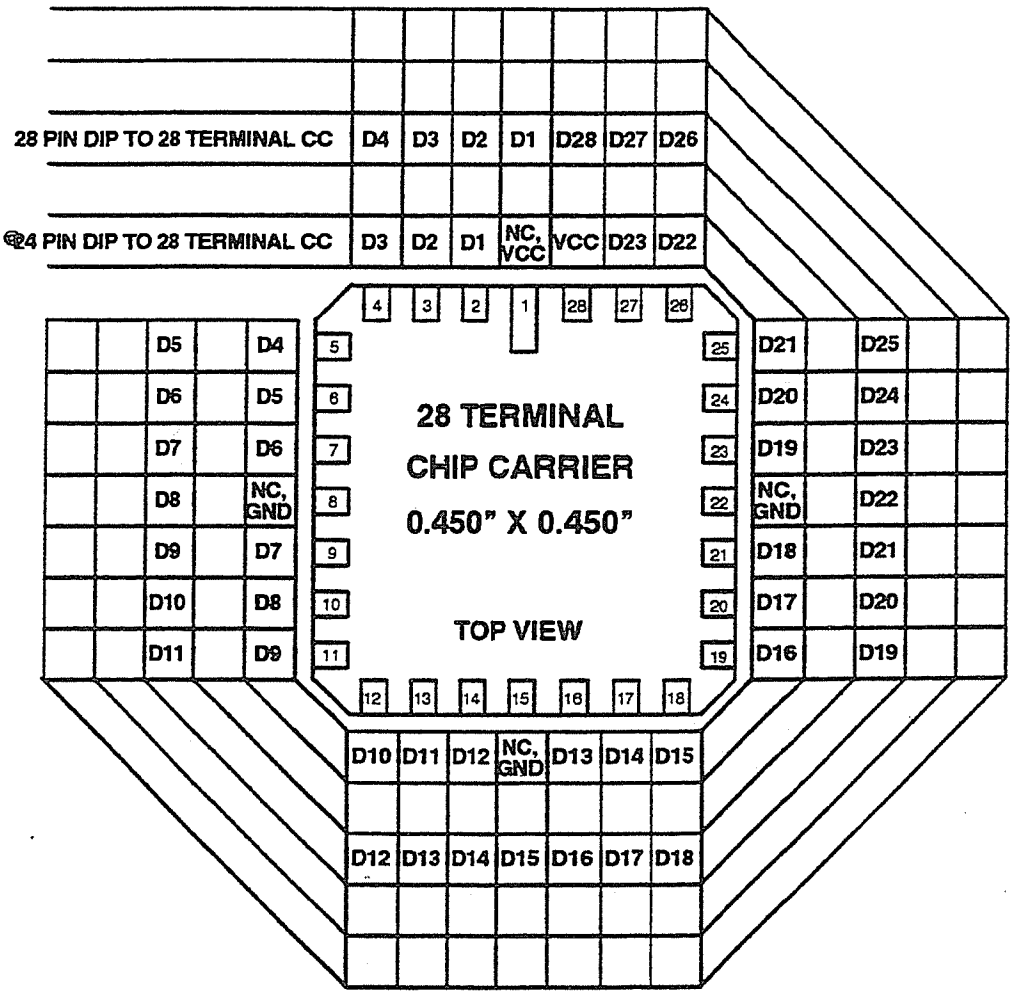


FIGURE 5-1
20 PIN DIP TO 20 TERMINAL CC PLD CONVERSION



Dnn = DIP PIN NUMBER

@ = THIS STANDARD IS APPLICABLE TO TTL DEVICES ONLY

FIGURE 5–2
24 & 28 PIN DIP TO 28 PAD CC CONVERSION

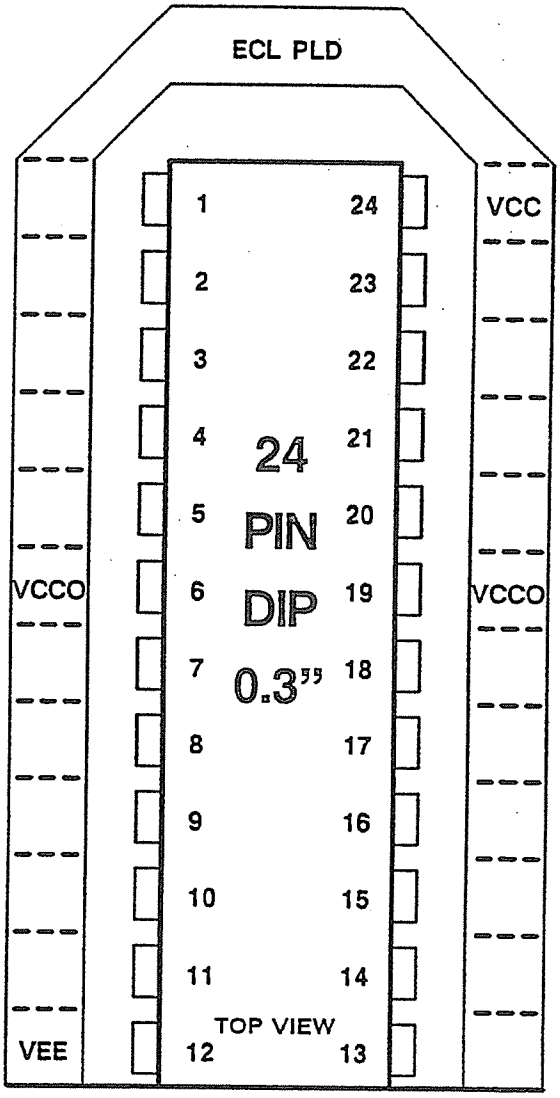
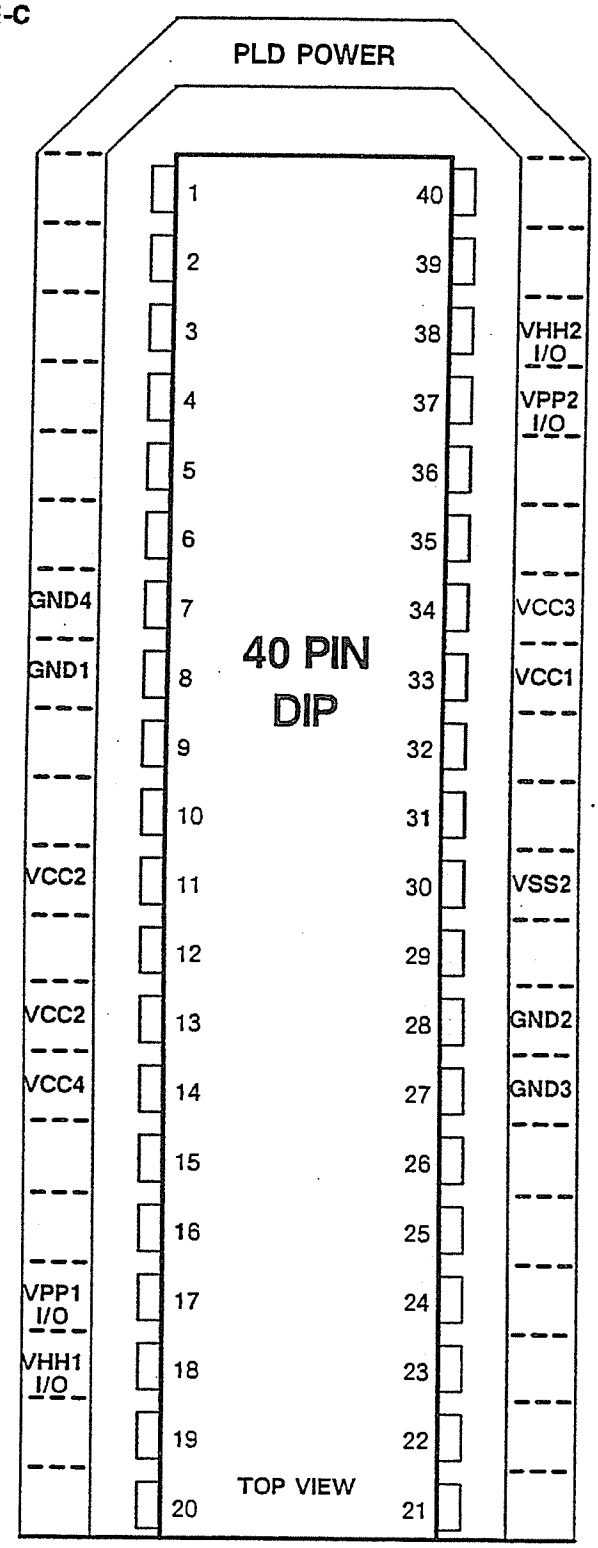


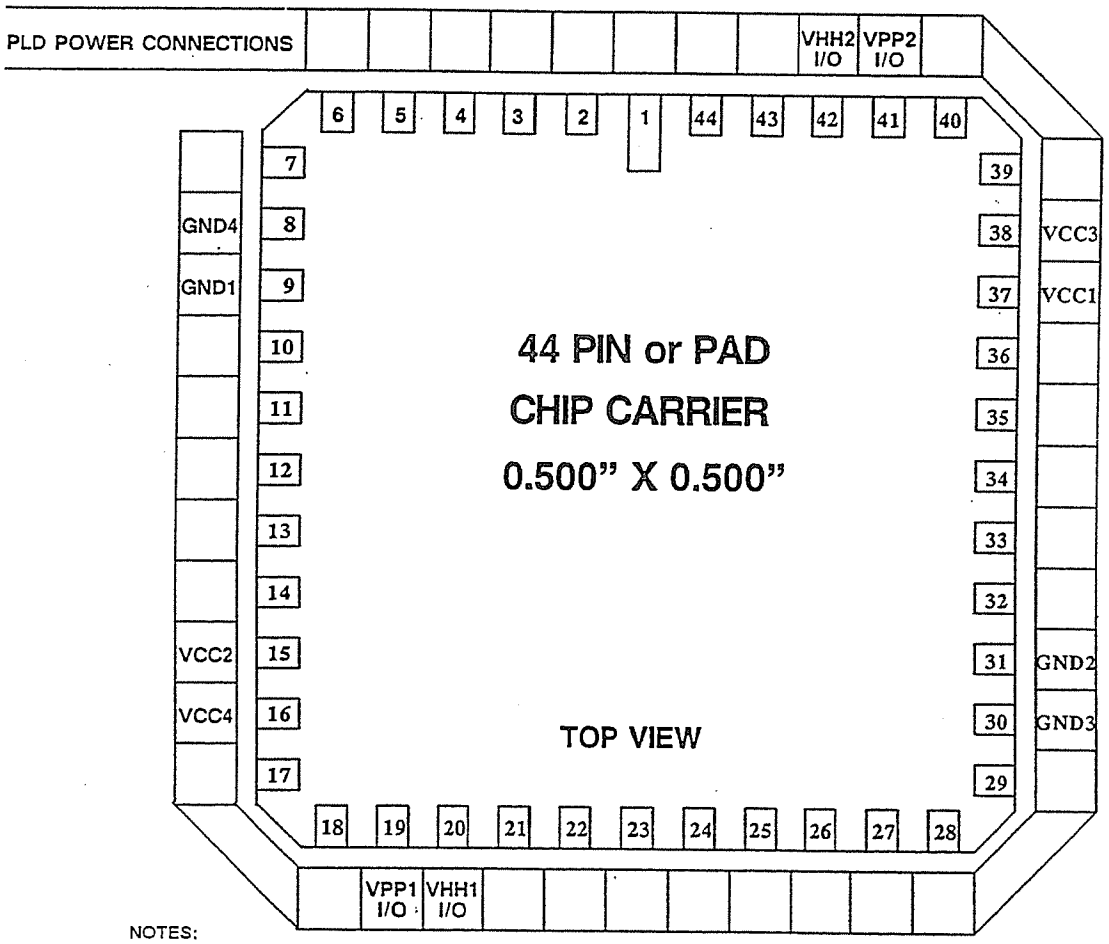
FIGURE 5-3
POWER PIN PLACEMENT FOR ECL PLD



NOTES:

1. VCC, VHH, VPP, and GND numbers are recommended sequence only and do not imply connectivity
2. Recommended order for adding power and ground is to maintain symmetry. However, other considerations (e.g. high drive output cluster) may dictate a difference sequence.
3. Unused VCC, VHH, VPP, and GND become I/O (for maximum compatibility, a manufacturer may restrict to input-only)

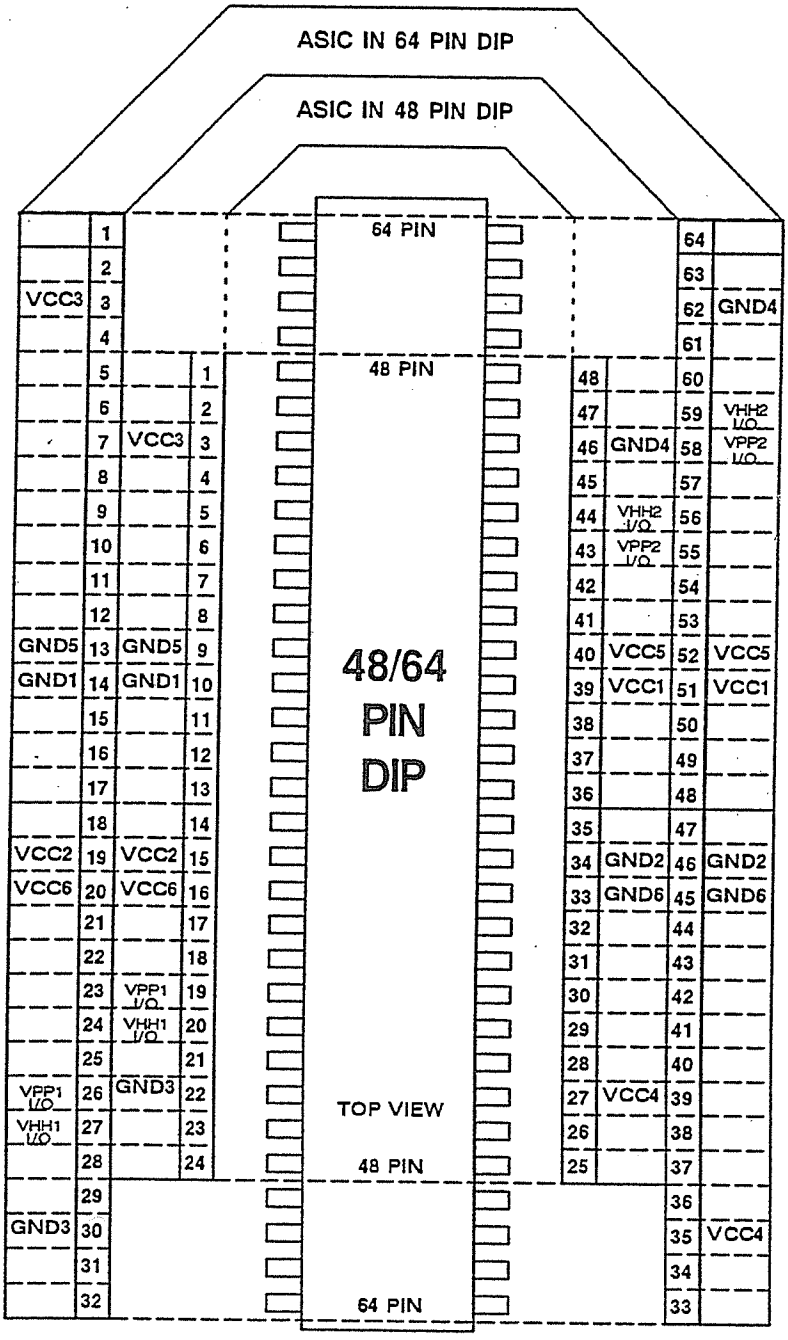
FIGURE 5-4
40 PIN DIP PLD POWER PIN PLACEMENT



NOTES:

1. VCC, VHH, VPP, and GND numbers are recommended sequence only and do not imply connectivity
2. Recommended order for adding power and ground is to maintain symmetry. However, other considerations (e.g. high drive output cluster) may dictate a difference sequence.
3. Unused VCC, VHH, VPP, and GND become I/O (for maximum compatibility, a manufacturer may restrict to input-only)

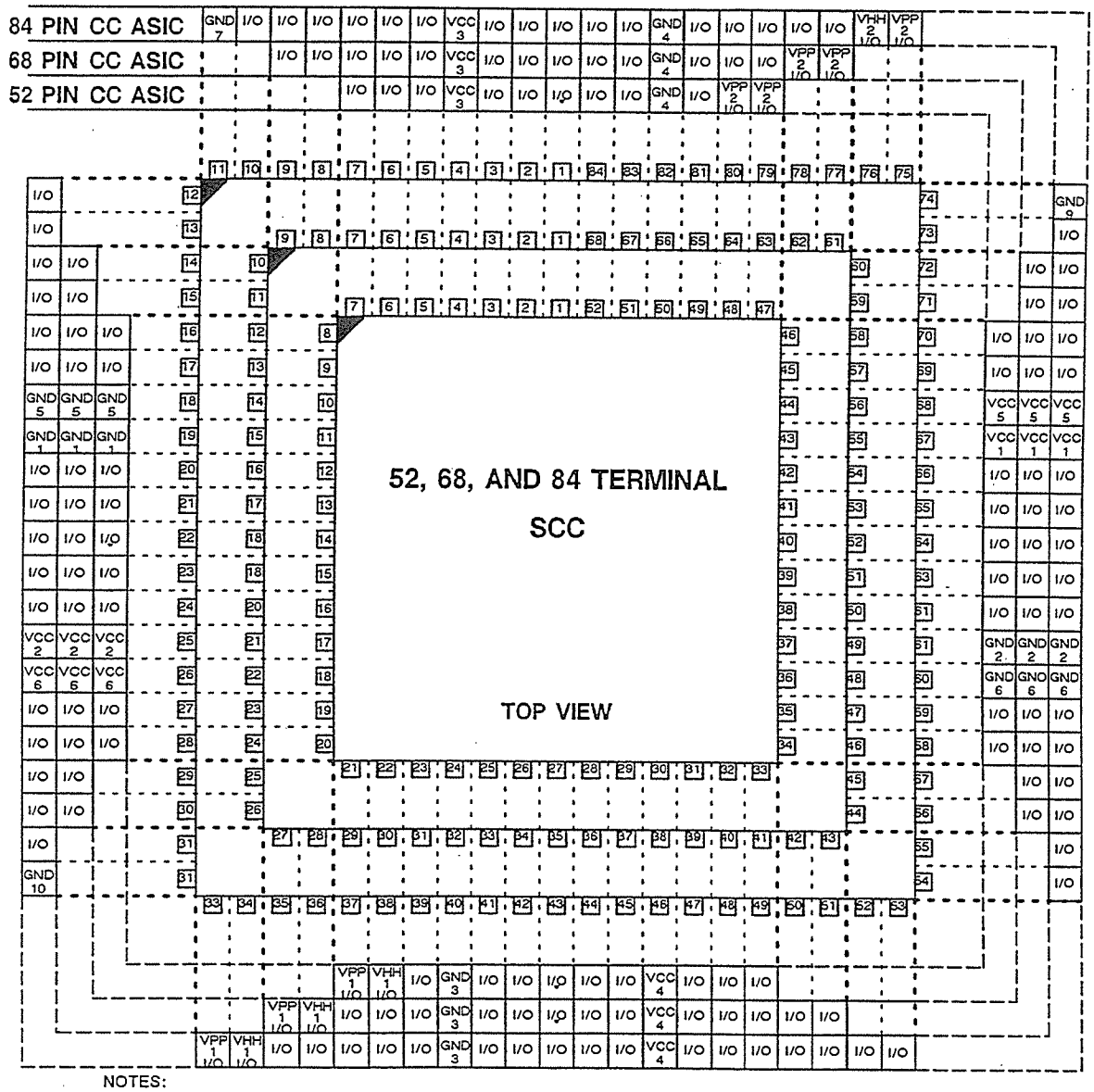
FIGURE 5-5
44 TERMINAL CC POWER PIN PLACEMENT



NOTES:

1. VCC, VHH, VPP, and GND numbers are recommended sequence only and do not imply connectivity
2. Recommended order for adding power and ground is to maintain symmetry. However, other considerations (e.g. high drive output cluster) may dictate a difference sequence.
3. Unused VCC, VHH, VPP, and GND become I/O (for maximum compatibility, a manufacturer may restrict to input-only)

FIGURE 5-6
48 & 64 PIN DIP ASIC POWER PIN PLACEMENT



NOTES:

1. VCC, VHH, VPP, and GND numbers are recommended sequence only and do not imply connectivity
2. Recommended order for adding power and ground is to maintain symmetry. However, other considerations (e.g. high drive output cluster) may dictate a difference sequence.
3. Unused VCC, VHH, VPP, and GND become I/O (for maximum compatibility, a manufacturer may restrict to input-only)
4. I/O can be any signal input and/or output.

* Recommended no-connect pins when going from DIP to larger CC.

FIGURE 5-7
52, 64, & 84 TERMINAL CC ASIC POWER PIN PLACEMENT

INTRODUCTION

This standard establishes a set of standardized output loads to be used for testing PLDs. It defines the loads to be used for some of the most commonly encountered output loads for TTL and CMOS devices. In addition, it gives a method for defining the load circuit for other values of output loading.

TTL INTERFACE LEVELS

Output logic levels which meet TTL logic levels defined in JEDEC Standard 17. They can typically be identified by VOH(min) specified at 2.4 Volts.

CMOS INTERFACE LEVELS

Output logic levels which meet CMOS logic levels defined in JEDEC Standard 17. They can typically be identified by VOH(min) at 3.8 Volts.

3.3 V INTERFACE LEVELS (WIDE AND NARROW RANGES)

Output logic levels which meet the 3.3 V logic levels defined in JEDEC Standard 8.

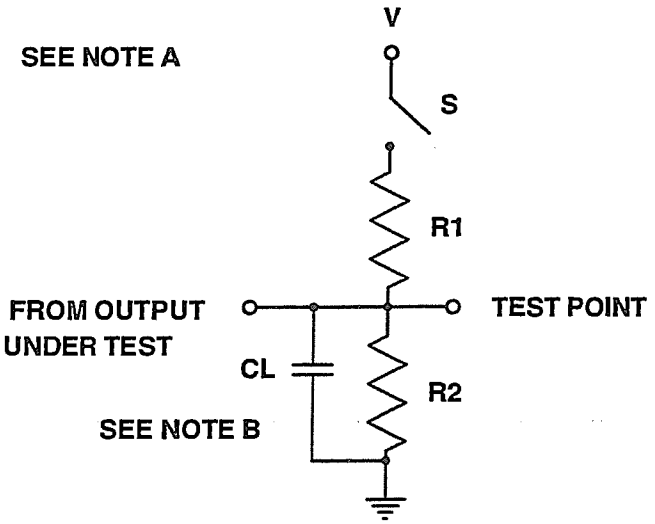
TEST CIRCUITS

Test conditions and loads are data sheet limits. While the limits are guaranteed under these specific conditions, this test circuit does not necessarily represent the way devices are physically tested.

FIGURE 5-8A
PLD STANDARD LOADS, DEFINITIONS

STANDARD LOAD CIRCUIT

The circuit configuration and tables of circuit component values define standard loads for commonly encountered output loads for TTL, CMOS, and 3.3 V devices. For load values that are different, the equations shown on the next page should be used.



NOTE A: S IS OPEN FOR HIGH IMPEDENCE TO "1" TEST AND CLOSED FOR HIGH IMPEDENCE TO "0" TEST.

NOTE B: CL INCLUDES PROBE AND JIG CAPACITANCE

IOL (mA)	R1 (ohms)	R2 (ohms)	V (volts)	CL* (pF)
24	200	200	5.0	50
16	300	300	5.0	50
8	620	620	5.0	50
4	1200	1200	5.0	50

* FOR TPHZ AND TPLZ, CL = 5 pF

TTL INTERFACE LEVELS

IOL (mA)	R1 (ohms)	R2 (ohms)	V (volts)	CL * (pF)
6	820	820	5.0	30
4	1300	1300	5.0	30
20 µA	250 k	250 k	5.0	30

* FOR TPHZ AND TPLZ, CL = 5 pF

CMOS INTERFACE LEVELS

IOL (mA)	R1 (ohms)	R2 (ohms)	V (volts)	CL * (pF)
2	1600	1600	3.3	30
4	800	800	3.3	30
8	400	400	3.3	30

* FOR TPHZ AND TPLZ, CL = 5 pF

3.3 V INTERFACE LEVELS

FIGURE 5–8B

PLD STANDARD LOAD CIRCUIT

OUTPUT LOAD CALCULATIONS

The following equations give the resistance values to be used for loads which differ from those given in the tables on the prrevious page.

TTL EQUATIONS (SEE NOTE A)

R1 = 5.0 V/IOL; R2 = (2.5/2.5) X R1 = R1
EXAMPLE FOR IOL = 24 ma; R1 = 5.0V/25 mA = 208 Ω = R2
ROUND TO STANDARD VALUE (200 Ω)

CMOS EQUATIONS (SEE NOTE A)

R1 = 5.0V/IOL; R2 = 2.5/2.5) X R1 = R1
EXAMPLE FOR IOL = 6 mA; R1 = 5.0V/6 mA = 833 Ω = R2
ROUND TO STANDARD VALUE (820 Ω).

3.3 V EQUATIONS (SEE NOTE A)

R1 = 3.3 V/IOL; R2 = 1.65/1.65) X R1 = R1
EXAMPLE FOR IOL = 2 mA; R1 = 3.3 V/2 mA = 1.65 kΩ = R2
ROUND TO STANDARD VALUE (1.6 kΩ).

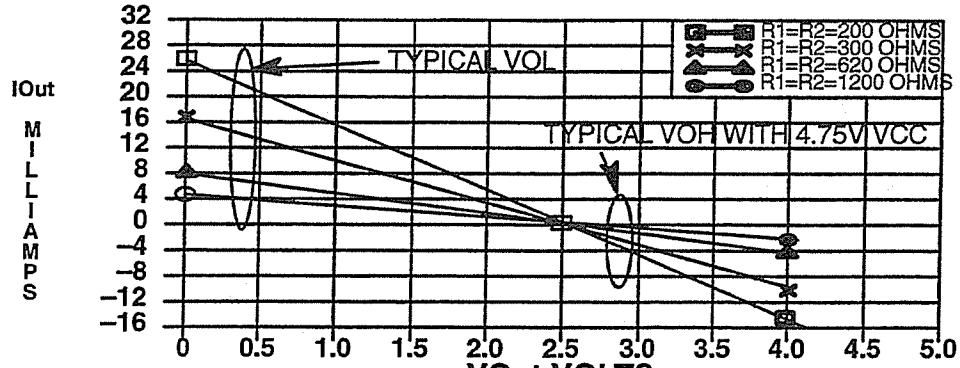
NOTE A: ROUND OFF RESISTOR TO THE NEAREST VALUE IN TABLE BELOW.

STANDARD RESISTOR VALUES
The resistors used shall be from the EIA approved 5% tolerance values and shall have a resistance between the value of 22 Ω to 680K Ω. The 5% values are as follows:

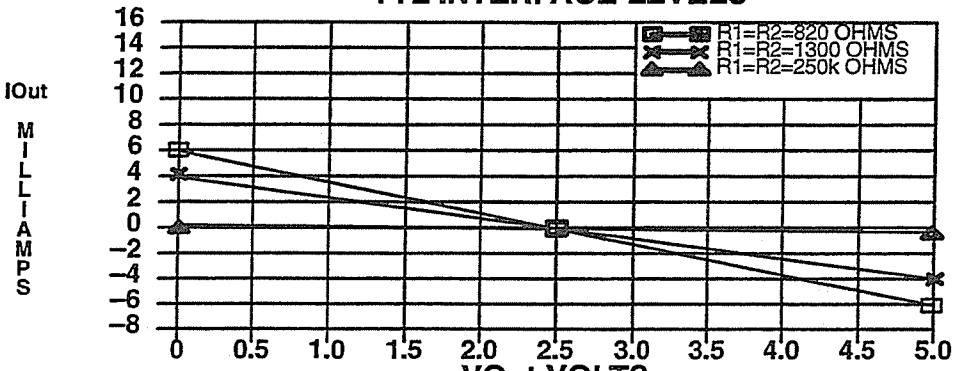
1.0	1.6	2.7	4.3	9.1
1.1	1.8	3.0	4.7	6.8
1.2	2.0	3.3	5.1	7.5
1.3	2.2	3.6	5.6	8.2
1.5	2.4	3.9	6.0	9.1

These values are multiplied by 10, 100, 1K, 10K, or 100K to achieve the resistance desired.

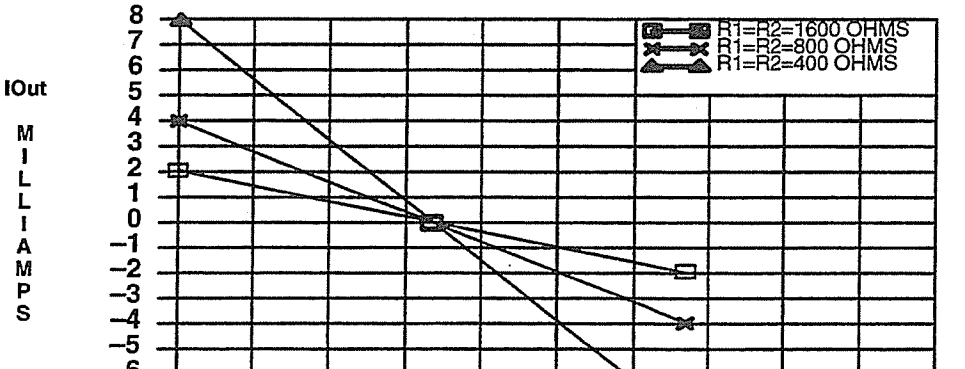
FIGURE 5-8C
PLD OUTPUT LOAD CALCULATIONS



TTL INTERFACE LEVELS



CMOS INTERFACE LEVELS



3.3 V INTERFACE LEVELS

FIGURE 5–8D
PLD AC LOAD LINES

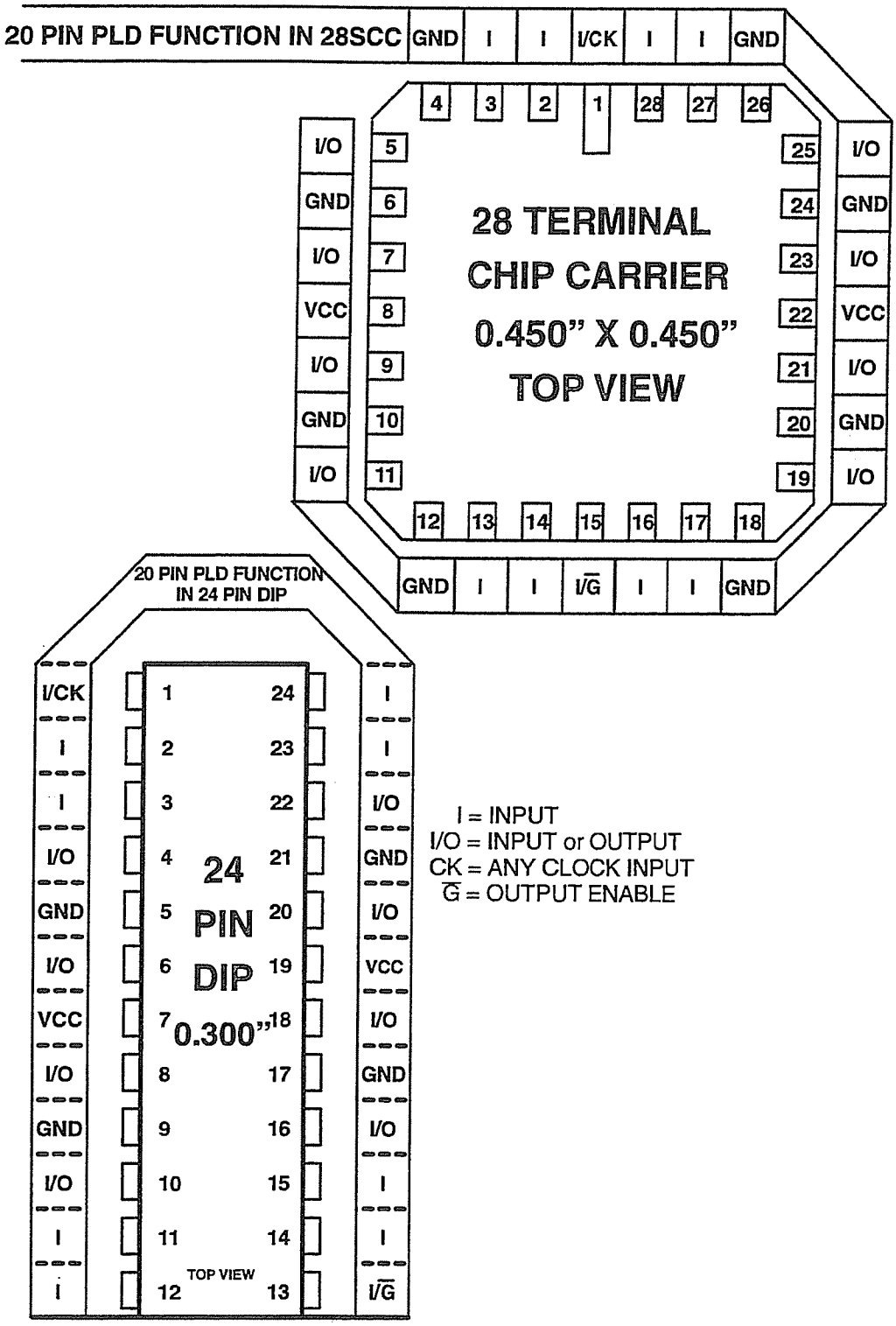
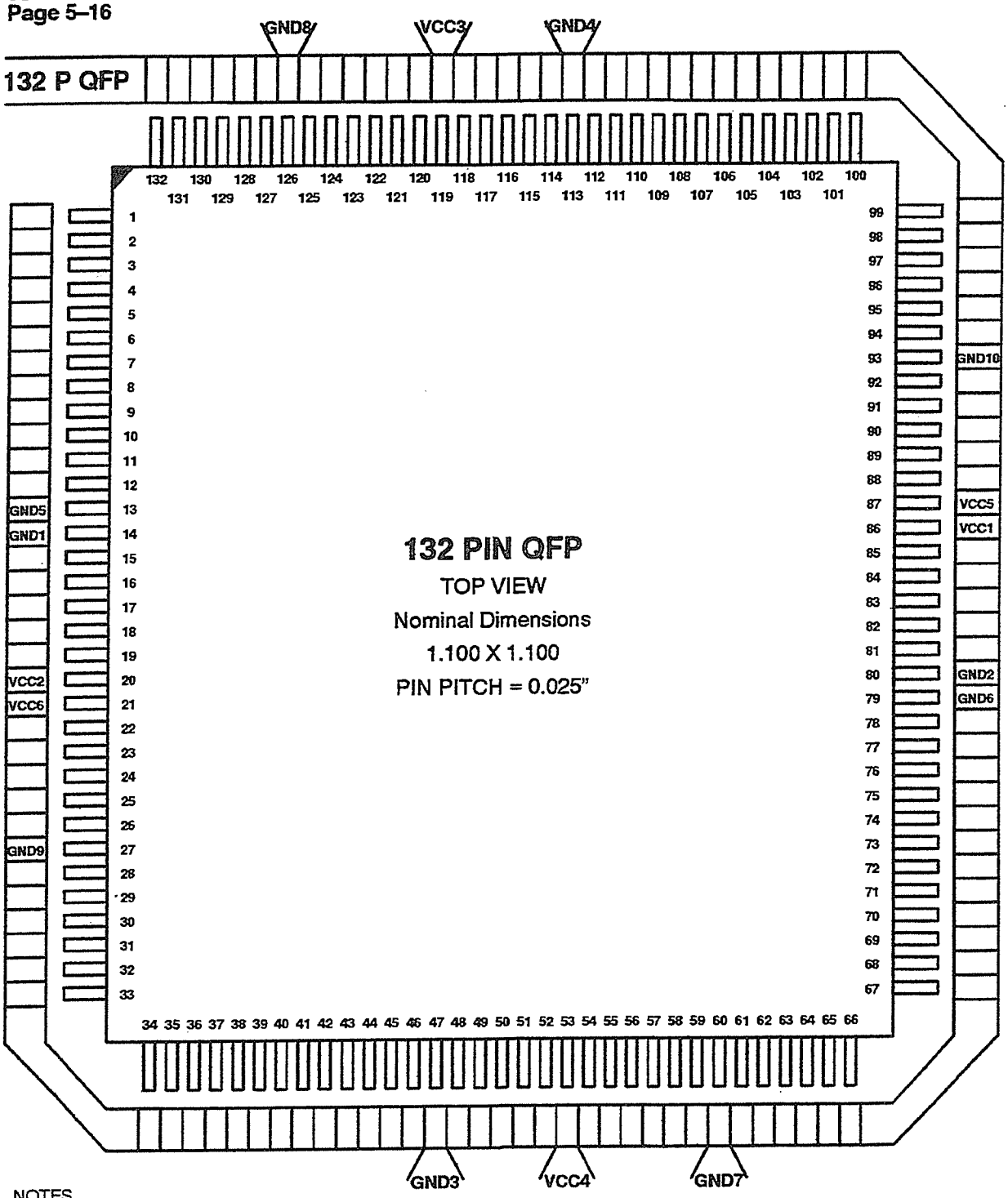


FIGURE 5–11
HIGH SPEED PINOUT FOR 20 PIN PLD FUNCTIONS



NOTES
1. VCC and GND numbers are recommended sequence only and do not imply connectivity.
2. Recommended order for adding power and ground to maintain symmetry. However other considerations (e.g. high driver output cluster) may dictate a different sequence.
3. Unused VCC and GND = I/O (for maximum compatibility, a manufacturer may restrict to input–only).
4. This Standard is compatible with other JEDEC standards for related packages..

FIGURE 5–10
POWER PIN PLACEMENT FOR PLD IN 132 PIN QFP

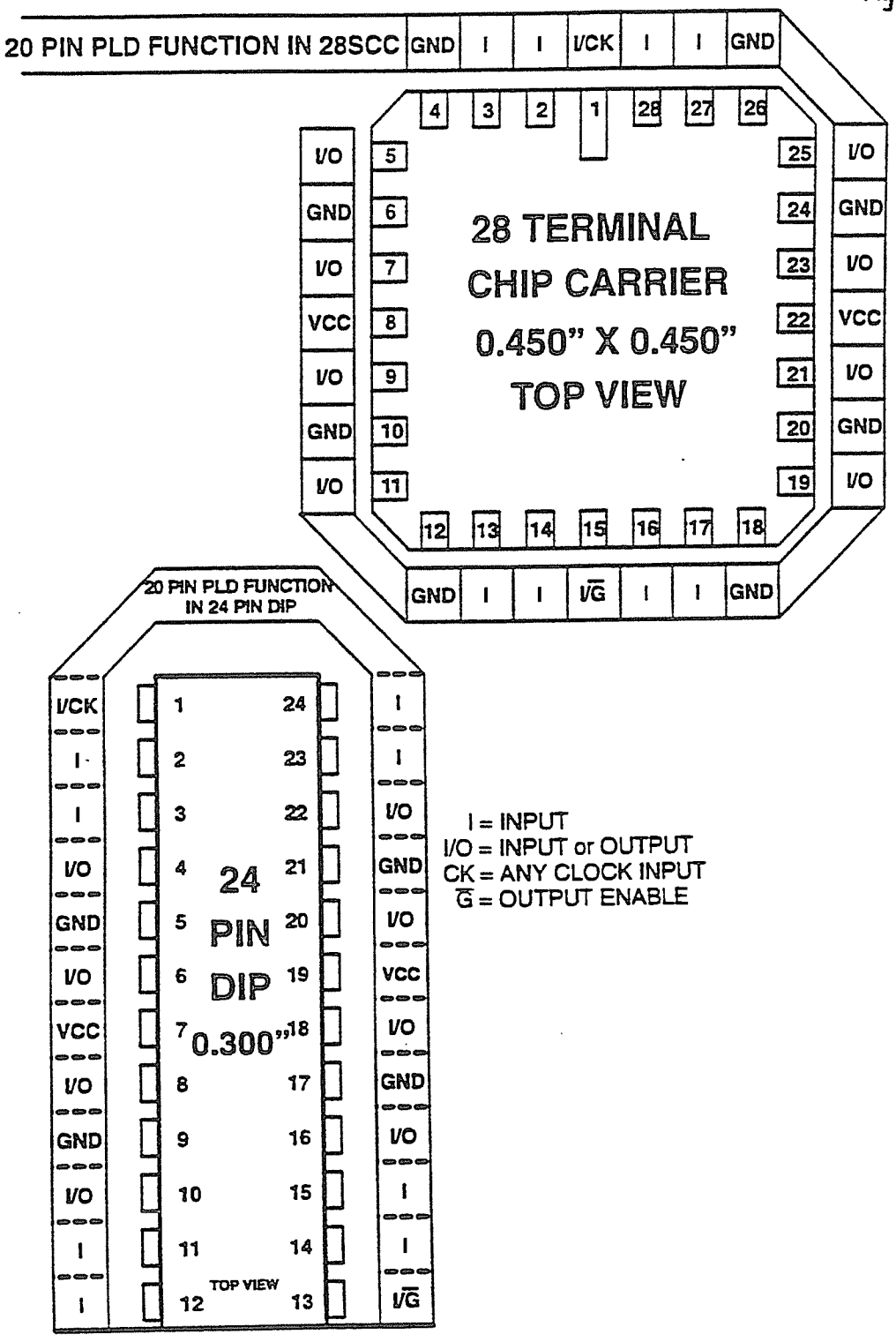


FIGURE 5–11
HIGH SPEED PINOUT FOR 20 PIN PLD FUNCTIONS

6 APPLICABLE OTHER DOCUMENTS

The following documents are publications which are related to the work of Committee JC-42 and may be obtained from the Electronic Industries Association, Standards Sales Department.

6.1 Standard Manufacturers Identification Code.

JEDEC Publication No. 106A

JEDEC Committee JC-42 maintains a Vendor identification code list for memory device manufacturers. This code number which can be used as a unique numerical identification for a Vendor in documentation, software, or encoded in ROM on a memory device. The list is updated periodically and published as JEDEC publication 106A.

6.2 Interface Standard for Low Voltage TTL-Compatible Devices (LVTTL)

JEDEC Standard No. 8 and Addendum No. 1

A series of standards have been developed which define the power supply and signal interface limits for devices which operate with a power voltage of three (3.0) volts nominal. It includes tolerances for both battery and regulated power supply operation. The input and output signal limits when operating with 5.0 V nominal TTL circuits are defined. These standards are intended to define the electrical environment for the device families which will utilize the 3.0 V power supply voltage which, it is expected, will replace the current 5.0 V standard. These standards have been published as JEDEC Standard 8 with Addendum 1.

6.3 Package Outlines, JEDEC Publication 95

This document contains dimensional drawings of all component packages which have been registered or approved as standards by JEDEC. It is issued in loose leaf binder form into which periodic updates may be added.

6.4 PLD Data Transfer Format, JEDEC Standard 3-B

This standard defines the format used to communicate the device programming information to a programmer for a field programmable memory device. In addition, it gives a simple transmission protocol to be used for the transmission..

6.5 Nomenclature for FPLD, EIA Standard RS-428

This standard defines a compact nomenclature to be used to describe Field Programmable Logic Devices. The standard is applicable to all current and future devices, regardless of technology, density, and package. The details of the standard will be published as an addendum to EIA Standard RS-428.