SYNCHRONOUS DRAM

4 MEG x 4 SDRAM

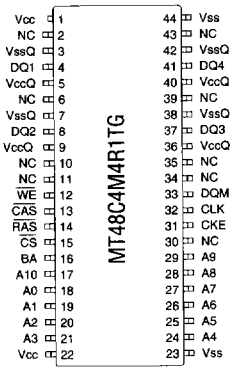
Pulsed $\overline{RAS}$, Dual Bank,
BURST Mode, 3.3V, SELF REFRESH

FEATURES

- Fully synchronous; all signals (excluding clock enable) registered to positive edge of system clock
- Meets all JEDEC functional specifications
- Dual internal banks: dual 2 Meg x 4 architecture
- Programmable burst-lengths: 2, 4, 8 cycles or full-page burst
- Programmable burst-sequence: sequential or interleave
- Burst termination
- Multiple burst READ, single WRITE capability
- Hidden precharge capability with optional automatic precharge command
- Programmable READ latency: 1, 2 or 3 clocks
- Industry-standard x8 pinouts, timing, functions and packages
- Refresh modes: AUTO and SELF
- Standard and extended AUTO REFRESH rates
- High-performance CMOS silicon-gate process
- Lead-over-chip assembly architecture
- Single +3.3V ±0.3V power supply
- Low power, 3mW standby; 200mW active, typical
- LVTTL-compatible
- CKE-controlled power-down and suspend operations
- Mode register programming
- JEDEC-standard command set (pulsed $\overline{RAS}$)

PIN ASSIGNMENT (Top View)

44-Pin TSOP
FORWARD
(DD-7)



OPTIONS — MARKING

- Timing

10ns access	(≤100 MHz)	-10
12ns access	(≤83 MHz)	-12
13.3ns access	(≤75 MHz)	-13

- Auto Refresh

4,096-cycle in 64ms	(15.6µs/row)	none
4,096-cycle in 128ms	(31.25µs/row)	S

- SELF REFRESH

Not allowed	none
Allowed	S

- Plastic Packages

44-pin TSOP (400 mil)—forward	TG

- Part Number Example: MT48LC4M4R1TG-10 S

GENERAL DESCRIPTION

The MT48LC4M4R1(S) is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x4 [illegible] with a synchronous interface. Each byte is uniquely addressed through a bank-select bit and 20 address bits. The bank select and address are entered first by $\overline{RAS}$ registering (row active command) 12 bits (A0-A10, BA) and then $\overline{CAS}$ registering 11 bits (A0-A9, BA). At $\overline{CAS}$ registration (READ or WRITE command), address bit A10 defines auto-precharge state (active HIGH). Bank selection is controlled by BA during both $\overline{RAS}$ and $\overline{CAS}$ registration.

The MT48LC4M4R1 is designed to operate in a synchronous, 3.3V memory system. All input and output signals, with the exception of clock enable (CKE) during POWER-DOWN and SELF REFRESH modes, are synchronized to the positive-going edge of the system clock (CLK).

The synchronous DRAM has several programmable features to allow maximum performance in each user's system. Additionally, bank switching between the two internal memory banks in conjunction with the programmable BURST mode provides very high-speed performance.

The synchronous DRAM allows both AUTO REFRESH (during normal operation) and SELF REFRESH (for low-[illegible]

SYNCHRONOUS DRAM

FUNCTIONAL BLOCK DIAGRAM