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[54] **CIRCUIT AND METHOD FOR RETAINING DRAM CONTENT**

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[30] **Foreign Application Priority Data**

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[51] **Int. Cl.**[6] **G11C 7/00**

[52] **U.S. Cl.** **365/222**; 365/226; 365/229

[58] **Field of Search** 365/229, 228, 365/226, 222

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Attorney, Agent, or Firm—Fay, Sharpe, Beall, Fagan, Minnich & McKee

[57] **ABSTRACT**

For a DRAM provided with a self-refreshing function, self-refresh starting operations and execution of the self-refresh mode are performed when the power supply voltage is cut off thereby achieving battery backup of the DRAM. This is achieved by detecting when the power supply voltage is at the lowest voltage at which normal data transfer can be performed. The operations carried out by the DRAM control circuit relate to stopping transfer of the following data after completing any transfer that was in the course of execution, executing refreshing, and establishing the self-refresh mode. All except for the last function are preceding processes for self-refreshing. Then, when the voltage of the power supply is determined to be in the proximity of the lowest voltage at which the DRAM drive circuit can perform normally, the drive circuit is disabled and the RAS and CAS signals of the drive circuit go low by means of pull-down resistors so that the self-refresh mode is established.

19 Claims, 3 Drawing Sheets

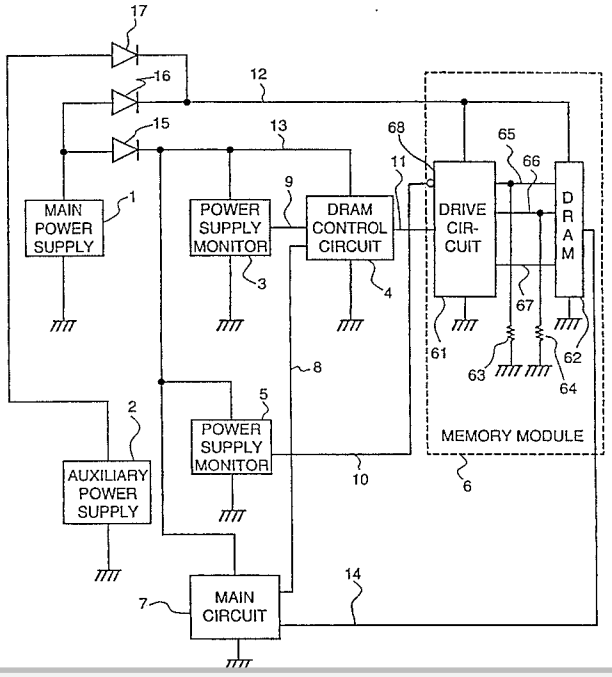


FIG. 1

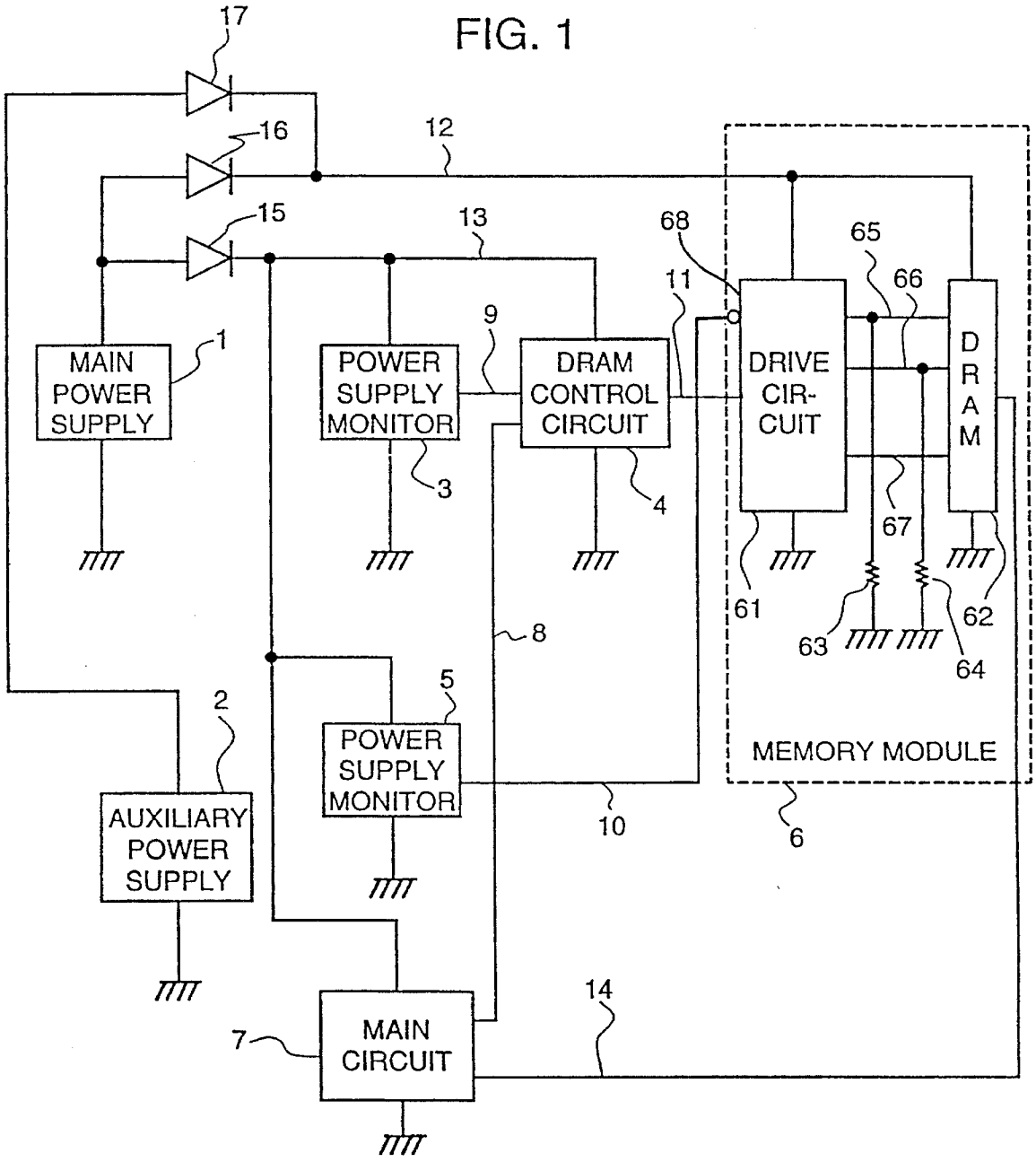


FIG. 2

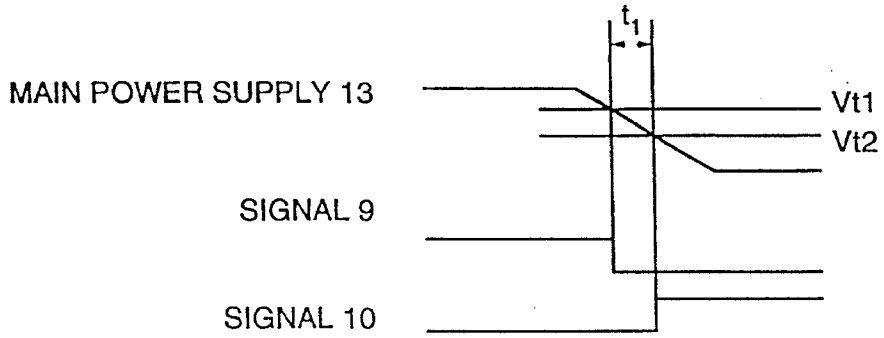


FIG. 3

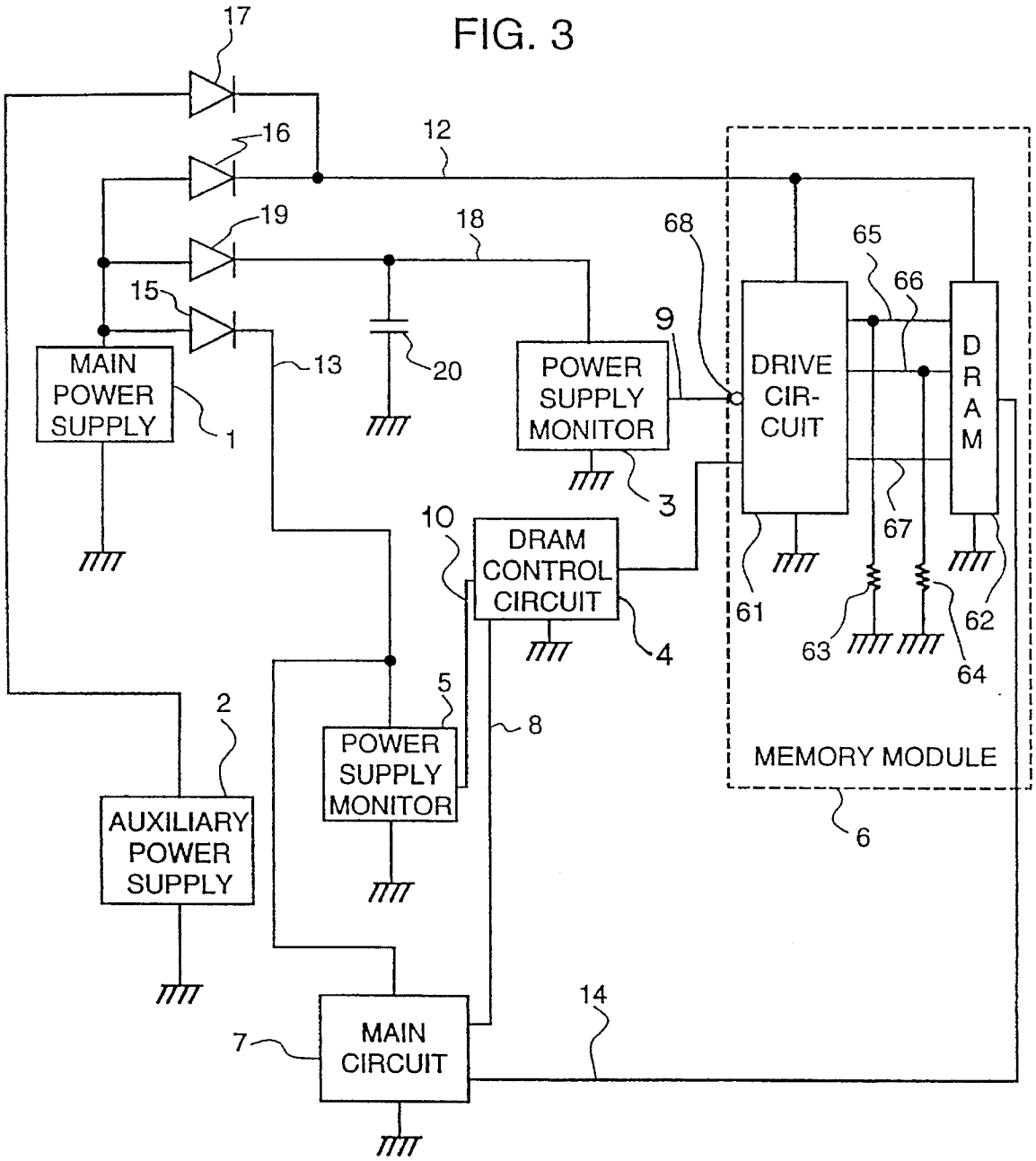


FIG. 4

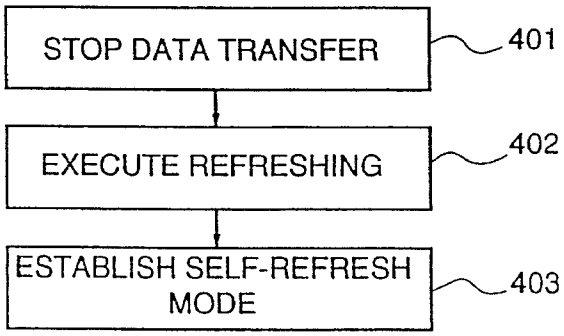
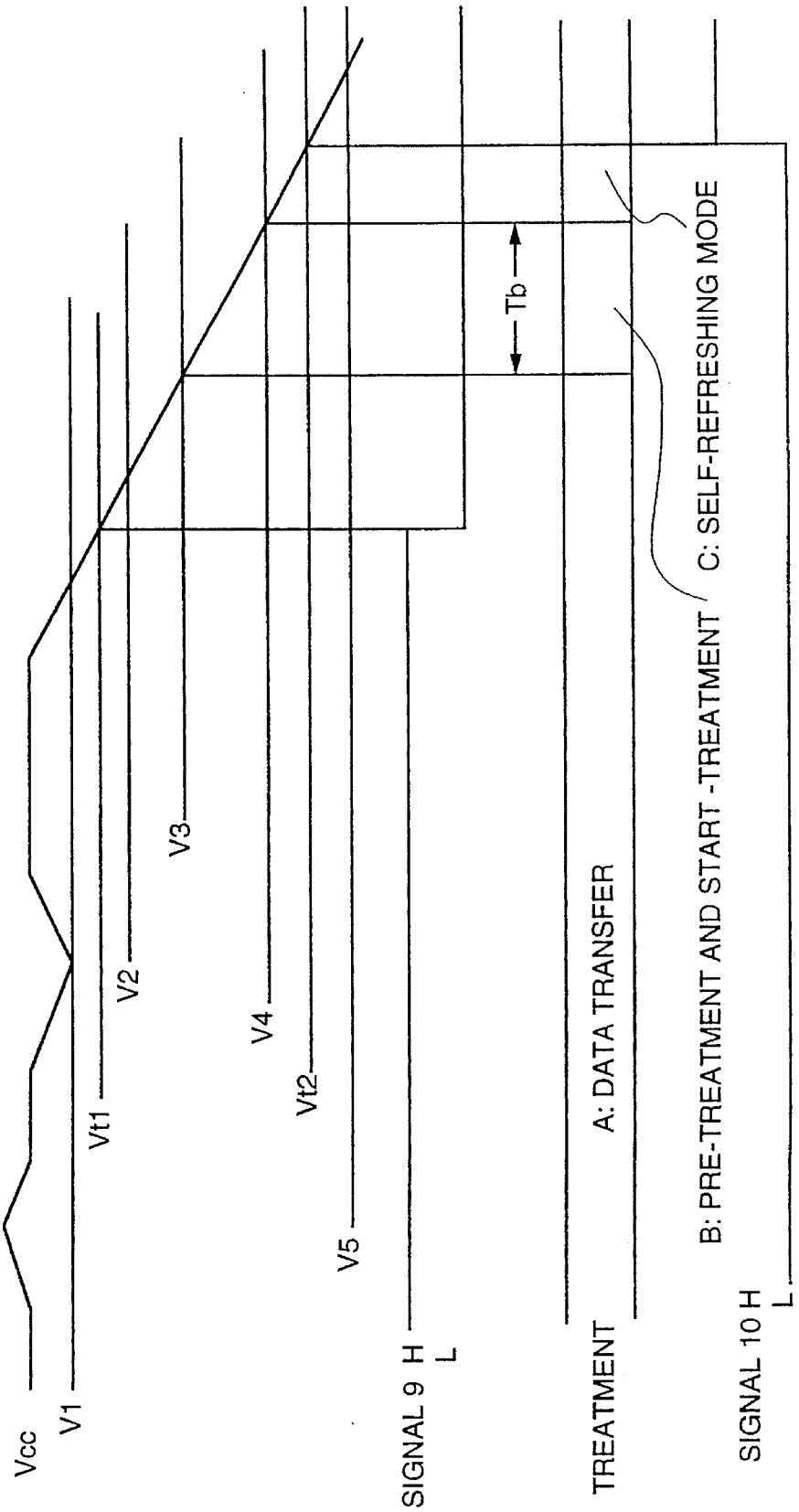


FIG. 5



CIRCUIT AND METHOD FOR RETAINING DRAM CONTENT

FIELD OF THE INVENTION

The present invention relates to a memory control circuit having a DRAM and, more particularly, to a control circuit retaining the content stored in a DRAM having a self-refreshing function with the use of an auxiliary power supply when the main power supply is cut off.

BACKGROUND OF THE INVENTION

As a control circuit for retaining the content stored in a CMOS memory or the like with the use of an auxiliary power supply, there is known a memory control circuit utilizing an output signal of a power supply monitor to protect the memory by means of a circuit causing the chip select signal of an SRAM to go high to thereby disable the memory when the power supply is cut off. As a known example of the described type, there is for example one disclosed in the gazette of Japanese Utility Model Laid-open No. Sho 62-23349.

SUMMARY OF THE INVENTION

In the above described prior art, the content stored in an SRAM is retained while consuming a small amount of power and, with such an SRAM, the disabling control can be achieved in a short period of time of tens of ns when the power supply voltage is lowered. However, the prior art method is directed to an SRAM and no disclosure is provided about how to retain the content stored in a DRAM with an auxiliary power supply when the power supply voltage is lowered by having the DRAM provided with a self-refreshing function or a method to carry out self-refresh starting operations taking several μs in a stabilized manner to retain the content of storage. Further, in the case where the content stored in a DRAM provided with a self-refreshing function is retained with the use of an auxiliary power supply, the RAS signal and the CAS signal as the outputs of the DRAM drive circuit must be held low while the stored content is retained with the auxiliary power supply. However, since an SRAM is disabled by a high-level signal according to the prior art, there is not known any method for bringing the RAS signal and the CAS signal of a DRAM drive circuit to low level with a small amount or number of circuit components.

An object of the present invention is to solve the above mentioned problems, i.e., to provide a memory control circuit capable of reliably carrying out self-refresh starting operations to establish a self-refresh mode for a DRAM when the power supply voltage is lowered and, further, to easily realize a self-refresh mode consuming small power at the time when the power supply voltage is lowered with the use of a simple circuit configuration formed of a small number of circuit components.

In order to achieve the above mentioned object, the present invention provides a memory control circuit having a DRAM, a drive circuit for driving the DRAM, a DRAM control circuit for controlling operation of the DRAM through the drive circuit, a power supply, a first detection circuit (first power supply monitor) for generating a first detection signal when the power supply voltage is lowered to a voltage higher than the lowest power supply voltage at which data transfer for the DRAM can be performed normally, and a second detection circuit (second power supply monitor) for generating a second detection signal when the power supply voltage is lowered to a voltage equal to or slightly higher than the lowest power supply voltage at which the DRAM control circuit can operate normally. When the first detection signal is detected, the DRAM control circuit starts self-refreshing and completes the relative preceding processes and then, when the second detection signal is detected, the drive circuit establishes a self-refresh mode for the DRAM.

According to the invention, when the power supply voltage is lowered to a voltage slightly higher than the lowest power supply voltage at which data transfer for the DRAM can be performed, the DRAM control circuit (adapted to be operative at a voltage lower than the power supply voltage at which data transfer can be performed normally) is caused to start the self-refreshing function by a first detection signal. As a result, necessary preceding processes (to completely finish the data transfer being executed and stop the following transfer as well as cause the refreshing function to be executed and the self-refresh mode to be established) can be performed well by the DRAM control circuit. Then, when the power supply voltage is further lowered and tends to drop below the voltage at which the DRAM control circuit can operate normally, the outputs (RAS signal and CAS signal) of the drive circuit are brought to a low level by a second detection signal. Thereby, the RAS signal and the CAS signal are held low while the content stored in the DRAM is retained by the auxiliary power supply and thus the self-refresh mode is maintained.

Since the drive circuit is made up of a general drive circuit having a normal output impedance that is high and having extra pull-down resistors, a logic circuit is not required and the number of component parts can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a first embodiment of the memory control circuit of the invention.

FIG. **2** is a timing chart when the main power supply is cut off in the first embodiment.

FIG. **3** is a block diagram of a second embodiment of the memory control circuit of the invention.

FIG. **4** is a sequence diagram of self-refresh starting operations in the invention.

FIG. **5** is a timing chart similar to FIG. **2** showing the correspondence between various voltage levels and the timing of the establishing of the self-refresh mode of a DRAM.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the invention will be described below in detail with reference to the accompanying drawings.

FIG. **1** is a block diagram of a memory control circuit of a first embodiment of the invention. Referring to the figure, the system comprises a main power supply **1** such as a commercial power supply, main battery power supply or the like, an auxiliary power supply **2** such as a battery or the like, a main circuit **7**, a DRAM control circuit **4**, a memory module **6**, a first power supply monitor **3** and a second power supply monitor **5**. Memory module **6** is made up of a drive circuit **61**, a DRAM **62**, and pull-down resistors **63** and **64**. A power supply line **12** supplies power to the memory module **6** and a power supply line **13** supplies power to the main circuit **7** (CPU). A data bus **14** is connected between main circuit **7** and DRAM **62**. Output lines of the drive

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