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(12) **United States Patent**
Goodman

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(45) **Date of Patent:** **Jun. 5, 2001**

(54) **COMPUTER MEMORY SYSTEM WITH A LOW POWER DOWN MODE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(57) **ABSTRACT**

(21) Appl. No.: **09/477,920**

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(51) **Int. Cl.**⁷ **G11C 7/00**

(52) **U.S. Cl.** **365/222; 365/230.03; 365/229; 365/52**

(58) **Field of Search** **365/222, 51, 63, 365/52, 230.03, 229**

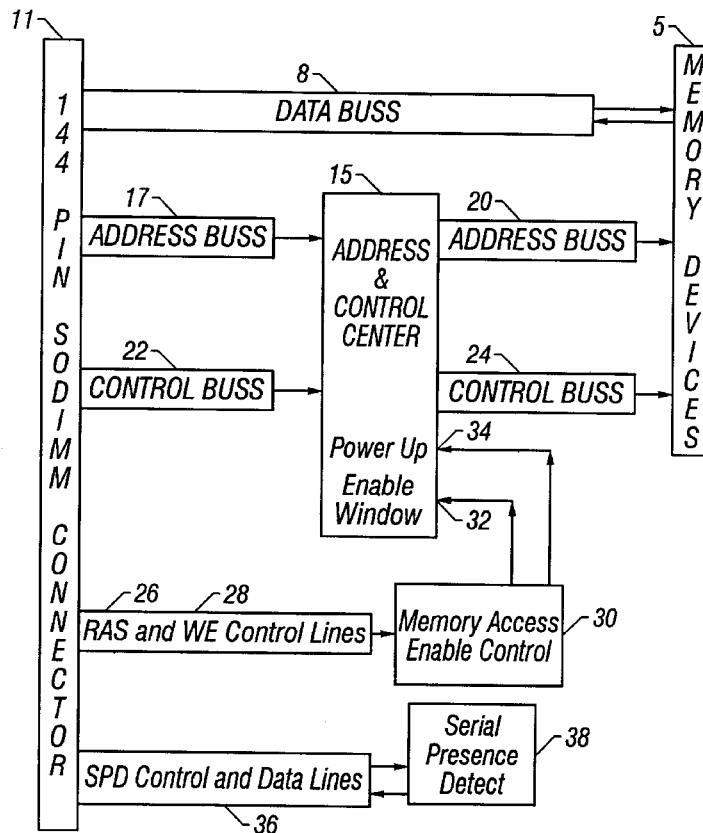
A memory system for use in a computer system, includes a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to the memory devices within a predetermined voltage range, and are capable of being placed in a self refresh mode. The memory devices have respective address and control lines, and a control device for selectively electrically isolating the memory devices from respective address lines and respective control lines so that when the memory devices are electrically isolated, any signals received on the respective address lines and respective control lines do not reach the memory devices. The memory system includes a memory access enable control device coupled to the control device and to the control lines for determining when the memory system is not being accessed, and for initiating a low power mode for the memory system wherein the control device electrically isolates the memory devices and places the memory devices in the self refresh mode.

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20 Claims, 59 Drawing Sheets



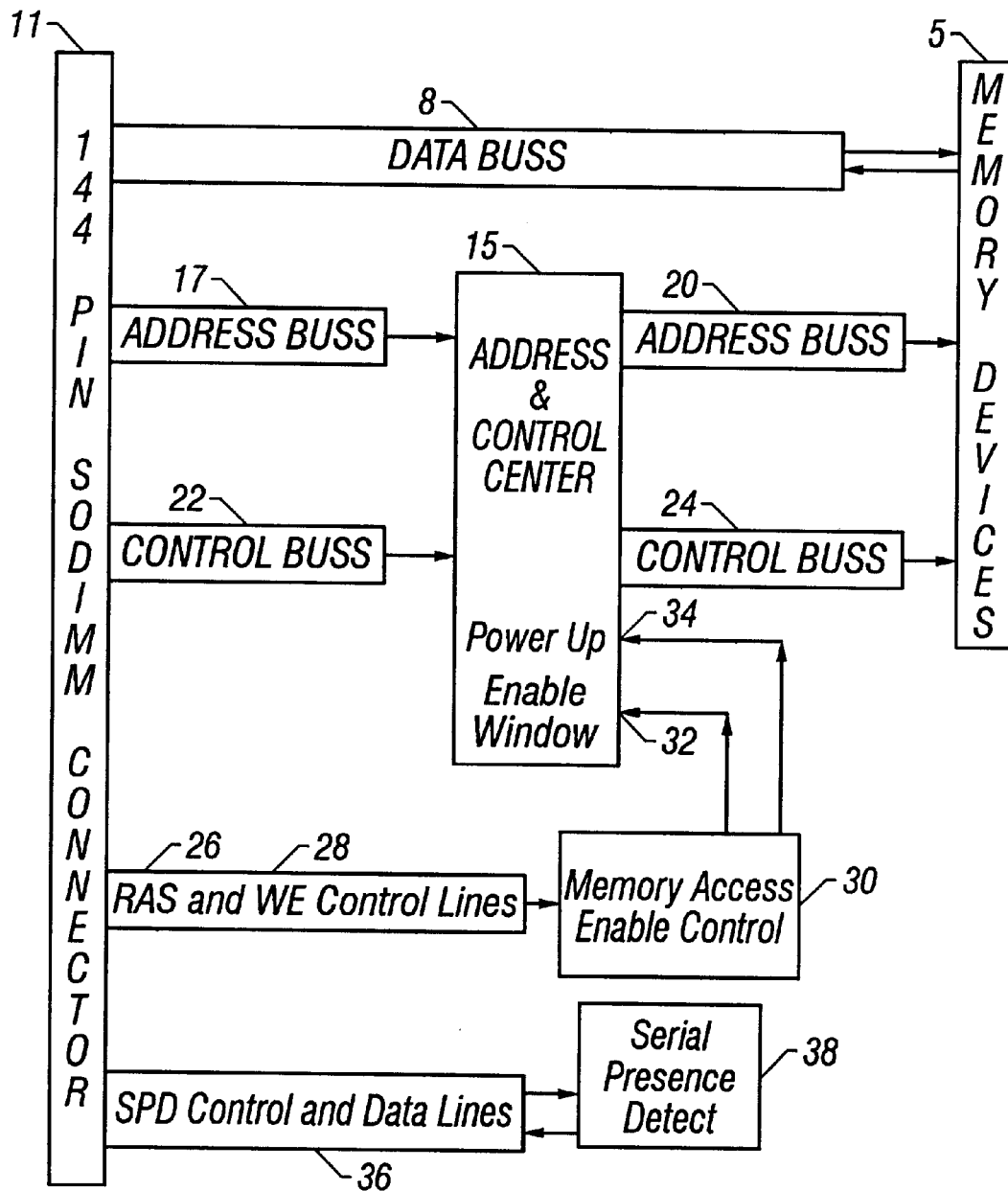


FIG. 1

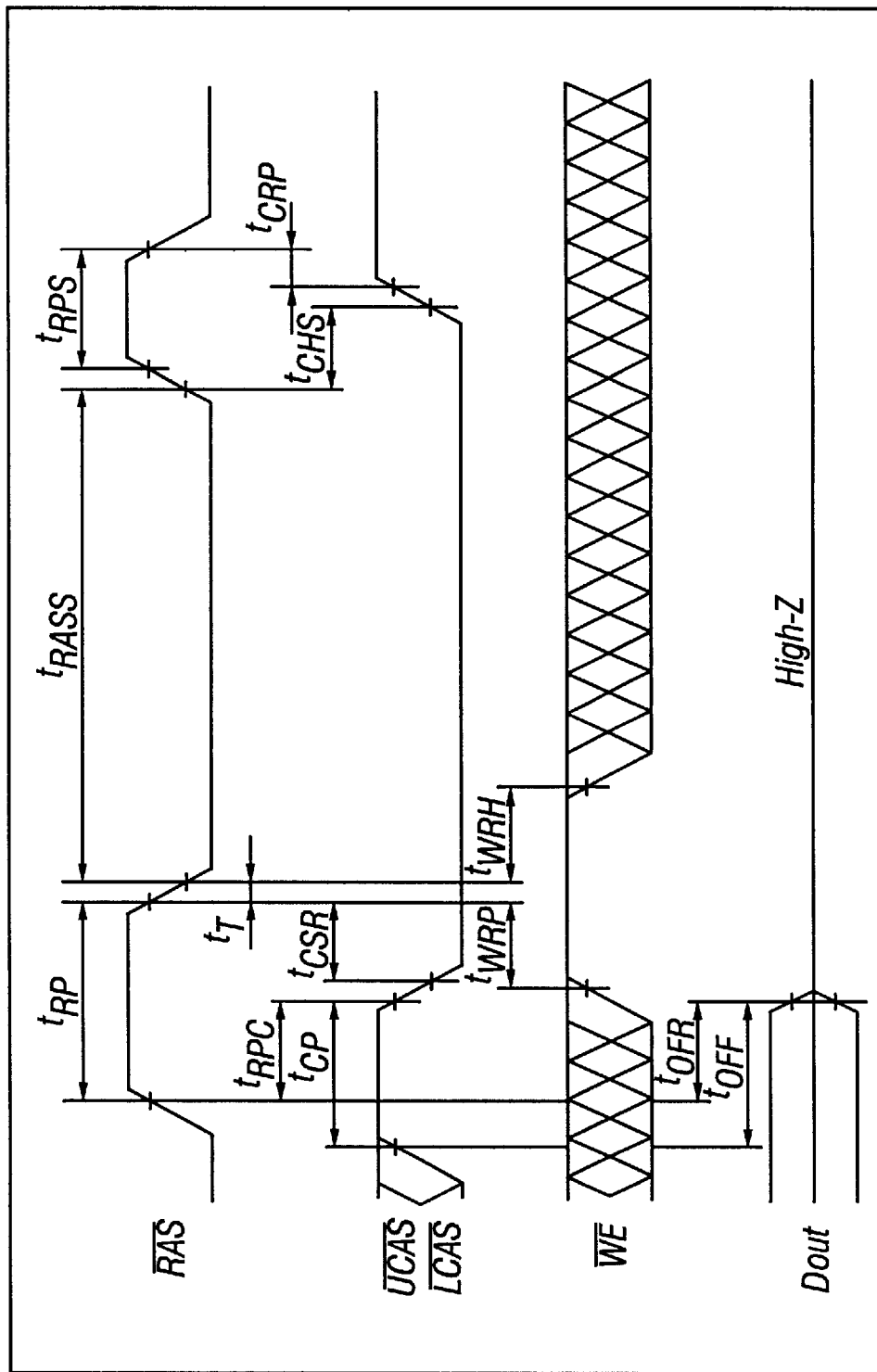


FIG. 2

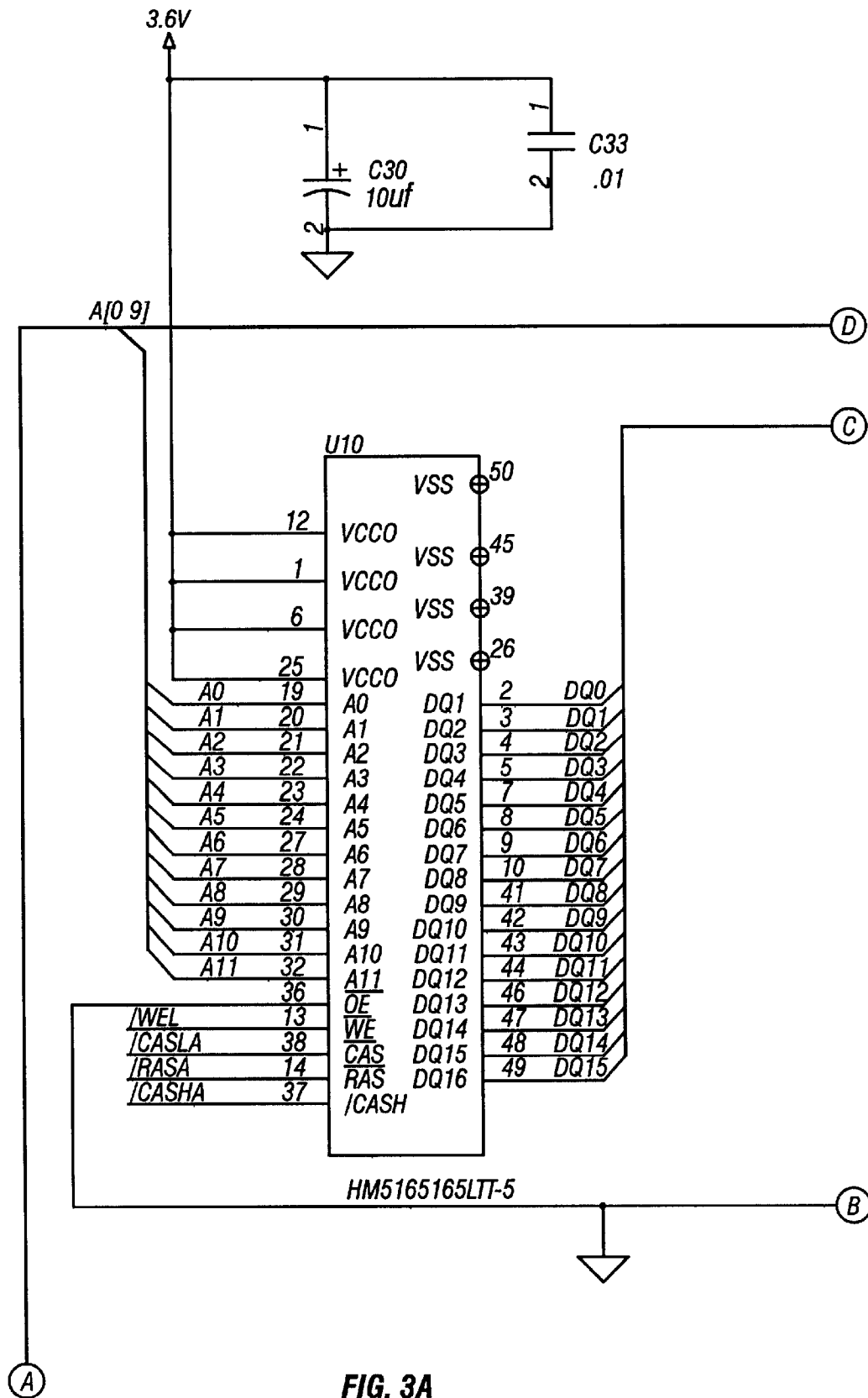


FIG. 3A

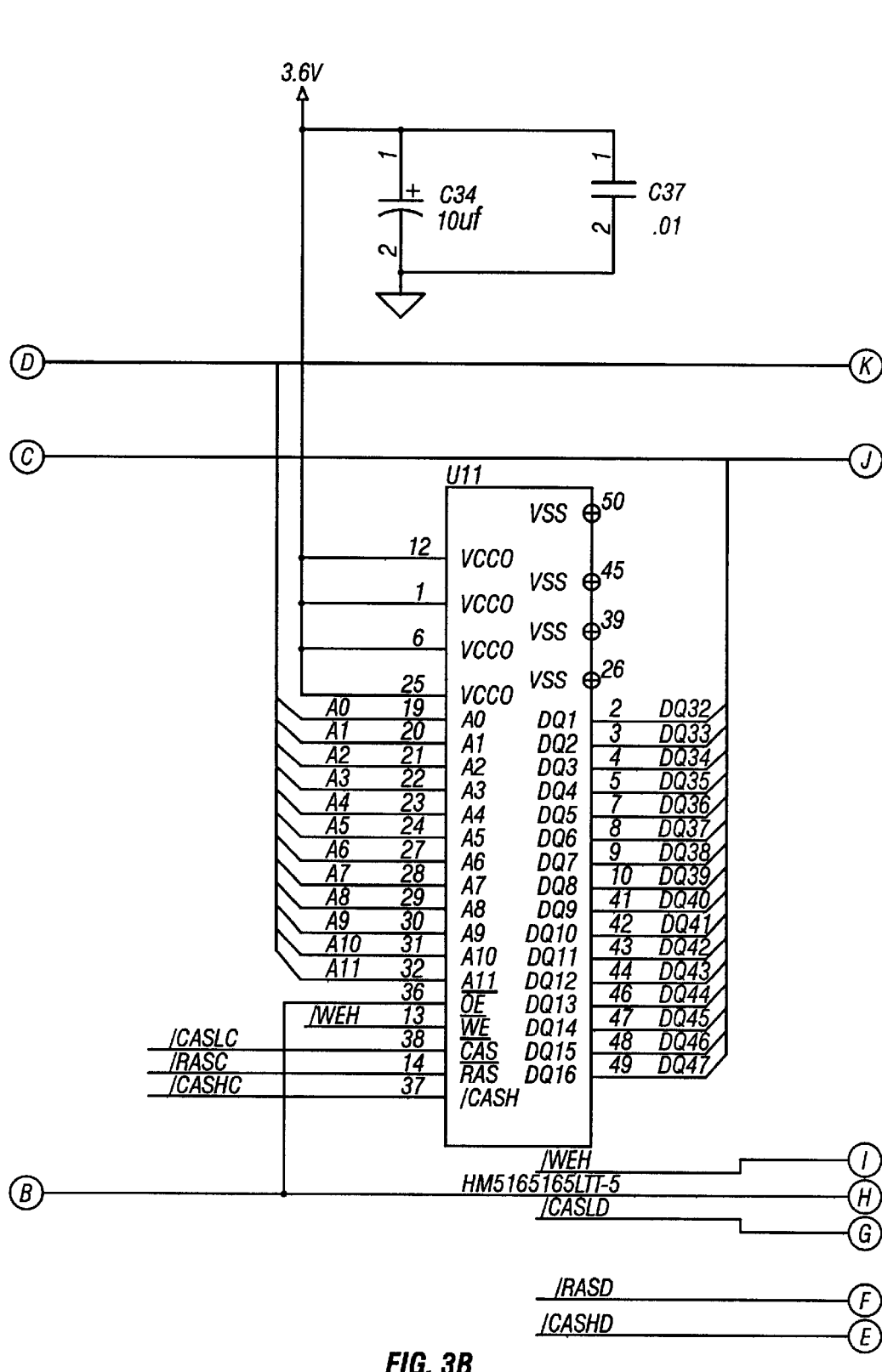


FIG. 3B

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