UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS AMERICA, INC. and ASUS COMPUTER INTERNATIONAL, INC.

Petitioner,

V.

JAMES B. GOODMAN,

Patent Owner,

Case IPR2017-02021[1]
Patent No. 6,243,315

Before BRIAN J. McNAMARA, PATRICK M. BOUCHER, and KIMBERLY McGRAW, *Administrative Patent Judges.*

PATENT OWNER'S RESPONSE TO THE DECISION ON THE PETITION

By James B. Goodman
Patent Owner

[1] Case IPR2018-00047, filed by ASUS Computer International, Inc. has been joined with this proceedings.

I. RELATED CASES

A final decision in this proceeding could affect the following cases pending in the U.S. District Courts in which the '315 Patent is asserted: *Goodman v. Hewlett-Packard Co.*, C.A. No. 16-CV-03195 (S.D. Tex.) ("HP Case"); *Goodman v. ASUS Computer International*, C.A. 17-CV-05542 (N.D. Cal. 05542) (Transferred from the S.D. Texas.); *Goodman v. Samsung Electronics America, Inc.*, C.A. No. 17-CV-05539 (S.D. N.Y.); and *Goodman v. Lenovo (United States) Inc.*, C.A. 17-CV-06782.

In addition, an IPR has been instituted against the present patent, U.S. Patent No. 6,423,315, by HP Inc. (Case IPR2017-01994).

II. THE CLAIMED INVENTIONS OF THE '315 PATENT

Fig. 1 of the '315 Patent is shown below. As stated in the '315 Patent at 5:41-42, "Fig. 1 is a block diagram of a preferred embodiment of the low power down memory system."

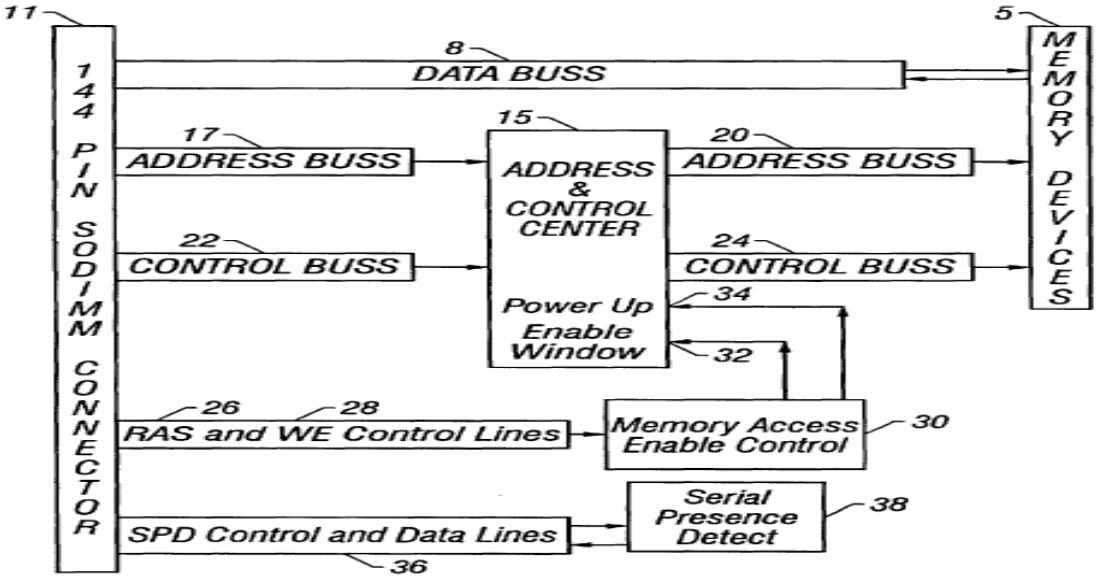

FIG. 1

The following is independent claim 1:

> 1. A memory system for use in a computer system, said memory system comprising:
>
> a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and capable of being placed in a self refresh mode; said memory devices having address lines and control lines;
>
> a **control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices**; and
>
> a **memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode**, thereby reducing the amount of electrical energy being drawn from an electrical power supply for said computer system. (Emphasis added)

The phrase "a control device … " has been highlighted to draw attention to this important aspect of the claimed invention. Electrically isolating the memory devices from the respective address lines and the respective control lines so that any signals on those lines do not reach the memory devices is critical for avoiding any corruptions of the data in the memory devices from unwanted signals during the self refresh mode.

The phrase "a memory access enable control device …" has been highlighted to point to the important issue of when the low power down mode for the memory system starts: It starts when the memory system is not being accessed.

Claims 2-9 depend on claim 1.

Fig. 4 of the ‘315 Patent is shown below. The embodiment shown in Fig. 4 features a memory system with a backup battery to avoid a loss of data when the initial battery fails. In addition, data in the memory devices are protected against corruption when the initial battery is less than the minimum voltage to maintain the data in the memory devices. Claims 10-20 are directed to a system with battery backup.

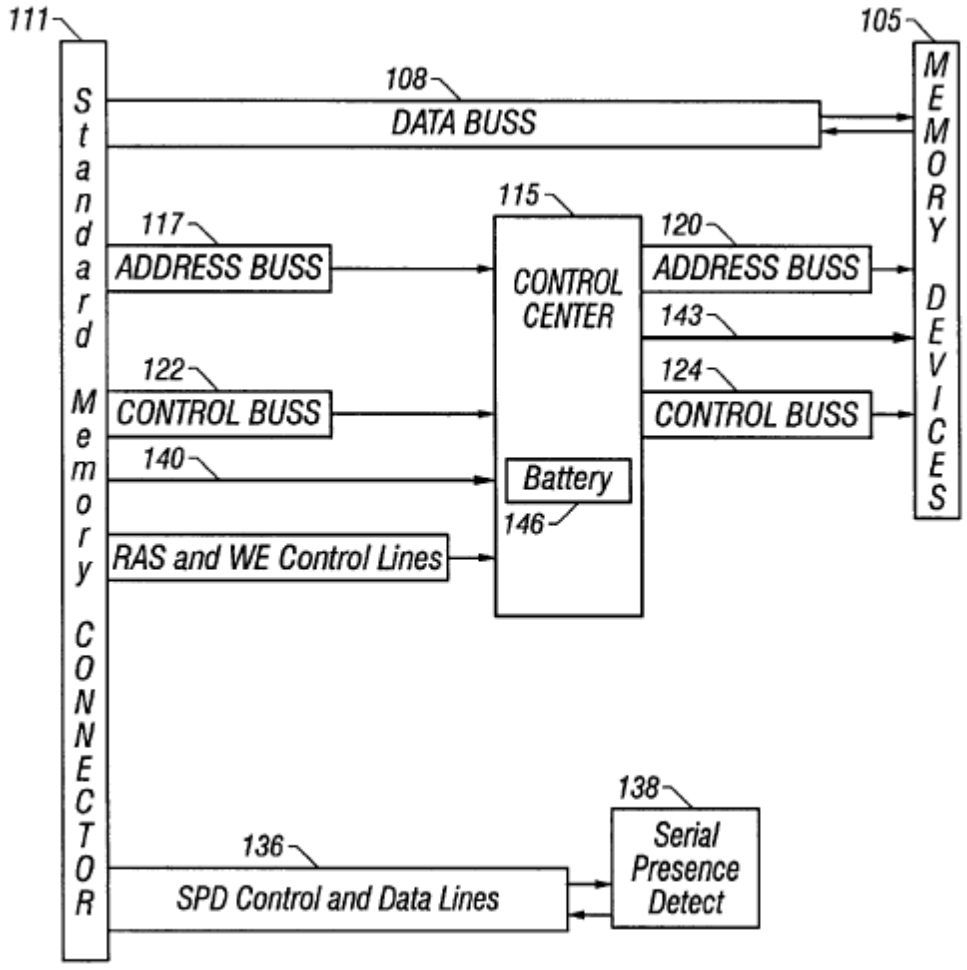

FIG. 4

The following is independent claim 10:

> 10. A memory system for use in a computer system, said memory system comprising:
>
> a plurality of volatile solid state memory devices that retain information when an electrical power source having a voltage greater than a predetermined voltage is applied to said devices; said memory devices having address lines and control lines;
>
> said computer system including a first electrical power source for operating said computer and being capable of producing a first voltage applied to said memory devices;
>
> a **control device for monitoring said first voltage to determine when said first voltage is less than said predetermined voltage and for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices;** and
>
> a second electrical power source operable for supplying a second voltage to said memory devices greater than said predetermined voltage;
>
> said control device being operable for disconnecting said first electrical power source from said memory devices and connecting said second electrical power source to said memory devices when said first voltage is less than said predetermined voltage;
>
> whereby, data in said memory devices is preserved by said second electrical power source when said first electrical power source fails to maintain at least said predetermined voltage on said memory devices, and said memory devices are isolated from errant signals. (Emphasis added)

The subsystem starting with "control device" has been made bold to draw attention to this particular feature. It is known in the prior art to use backup batteries and the like as an electrical power source in the event of a failure of the power source being used initially. The "control source" protects data in the memory devices when the first electrical power source is less than the minimum required for the memory devices by electrically isolating address and control lines from the memory devices so that errant signals cannot reach the memory devices and potentially

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