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Paper 6
Entered February 11, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SMART MODULAR TECHNOLOGIES, INC.,
Petitioner,

v.

JAMES B. GOODMAN,
Patent Owner.

Case IPR2015-01675
Patent 6,243,315 B1

Before BRIAN J. MCNAMARA, PATRICK M. BOUCHER, and GARTH D. BAER, *Administrative Patent Judges*.

BAER, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

Smart Modular Technologies, Inc. ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting *inter partes* review of claims 1, 5, 10, and 16 ("the challenged claims") of U.S. Patent No. 6,243,315 B1 (Ex. 1001, "the '315 patent"). James B. Goodman ("Patent Owner") did not file a Preliminary Response.

Pursuant to 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." As set forth below, we conclude that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of the challenged claims. Therefore, we institute *inter partes* review of the challenged claims.

I. BACKGROUND

A. RELATED PROCEEDINGS

The parties identify Case No. 4:14-cv-01380 pending in the Southern District of Texas as a related matter involving the same parties and the '315 patent. Paper 1, 1–2; Paper 5, 2.

B. THE '315 PATENT

The '315 patent is directed to volatile memory devices. Ex. 1001, Abstract. Volatile memory devices "retain the contents of their memory states when electrical power is provided and maintained on the devices," but "[w]henever electrical power is removed from the devices, the memory contents of the device [are] lost and irretrievable." *Id*. at 2:54–58.

The '315 patent's Fig. 4 is reproduced below:

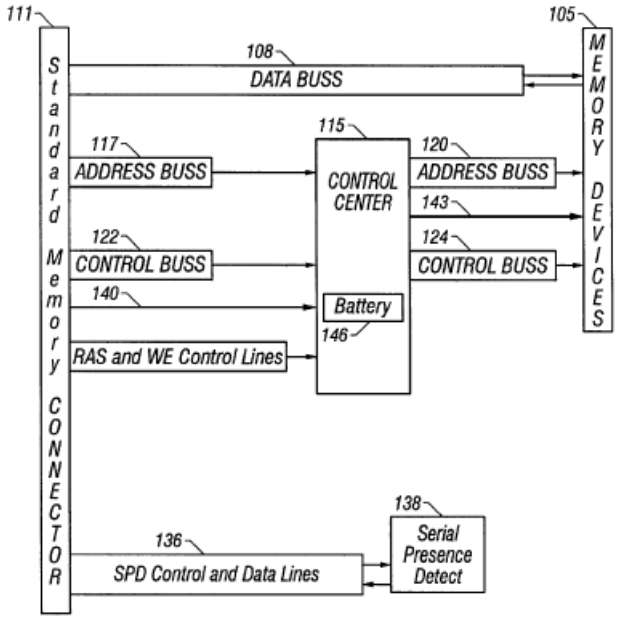

FIG. 4

"FIG. 4 is a block diagram of a non-volatile memory system according to the invention." Ex. 1001, 4:41–42.

According to the '315 patent:

> The invention prevents the loss of data due to unexpected power outages and also prevents errant control and address signals to the memory devices by monitoring the input electrical power source to the memory devices for acceptable conditions, and electrically isolating the memory devices from signals received on the control lines and address lines and switching to an alternate internal electrical power source, typically a battery, whenever the input power source is unacceptable.

Ex. 1001, 3:15–24. The '315 patent explains further that the system "maintains the integrity of the data retained by the memory devices by isolating the devices from the external power source, control lines and address lines and placing the memory devices into a power down self-refresh mode which will maintain the data using a minimum of electrical power." *Id*. at 3:25–30.

C. ILLUSTRATIVE CLAIMS

Claims 1 and 10 (reproduced below) are illustrative of the claimed subject matter.

> 1. A memory system for use in a computer system, said memory system comprising:
>
> a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and capable of being placed in a self refresh mode; said memory devices having address lines and control lines;
>
> a control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and
>
> a memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode, thereby reducing the amount of electrical energy being drawn from an electrical power supply for said computer system.

Ex. 1001, 13:18–40.

> 10. A memory system for use in a computer system, said memory system comprising:
>
> a plurality of volatile solid state memory devices that retain information when an electrical power source having a voltage greater than a predetermined voltage is applied to said devices; said memory devices having address lines and control lines;
>
> said computer system including a first electrical power source for operating said computer and being capable of producing a first voltage applied to said memory devices;

> a control device for monitoring said first voltage to determine when said first voltage is less than said predetermined voltage and for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and
>
> a second electrical power source operable for supplying a second voltage to said memory devices greater than said predetermined voltage;
>
> said control device being operable for disconnecting said first electrical power source from said memory devices and connecting said second electrical power source to said memory devices when said first voltage is less than said predetermined voltage;
>
> whereby, data in said memory devices is preserved by said second electrical power source when said first electrical power source fails to maintain at least said predetermined voltage on said memory devices, and said memory devices are isolated from errant signals.

Ex. 1001, 13:65–14:32.

D. Asserted Prior Art

The Petition relies on a supporting Declaration from Dr. Nader Bagherzadeh (Ex. 1002), as well as the following prior art references:

U.S. Patent No. 5,600,605 (issued Feb. 4, 1997) (Ex. 1004, "Schaefer");
U.S. Patent No. 5,793,776 (issued Aug. 11, 1998) (Ex. 1005, "Qureshi");
U.S. Patent No. 5,204,840 (issued Apr. 20, 1993) (Ex. 1006, "Mazur").

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability. Pet. 5.

References	Basis	Challenged Claims
Schaefer and Qureshi	§ 103(a)	1 and 5
Schaefer, Qureshi, and Mazur	§ 103(a)	10 and 16

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