

# United States Patent [19]

[11] Patent Number: **5,600,605**

Schaefer

[45] Date of Patent: **Feb. 4, 1997**

[54] **AUTO-ACTIVATE ON SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY**

Kazuyuki Nakamura, et al., "A 220-MHz Pipelined 16-Mb BiCMOS SRAM with PLL Proportional Self-Timing Generator", *IEEE Journal of Solid-State Circuits*, No. 11, pp. 1317-1321, (Nov. 1994).

[75] Inventor: **Scott Schaefer**, Boise, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **481,920**

*Primary Examiner*—Viet Q. Nguyen

*Assistant Examiner*—Son Mai

[22] Filed: **Jun. 7, 1995**

*Attorney, Agent, or Firm*—Schwegman, Lundberg, Woessner & Kluth, P.A.

[51] Int. Cl.<sup>6</sup> ..... **G11C 7/00**

[52] U.S. Cl. .... **365/233; 365/230.03**

[58] Field of Search ..... 365/233, 203, 365/222, 230.03

[57] **ABSTRACT**

A synchronous dynamic random access memory (SDRAM) includes a memory array and is responsive to command signals and address bits. A command decoder/controller times, at different times, a precharge command, an active command, and a transfer command. The command decoder/controller initiates the active command during the precharge command. Indicating circuitry responds to the precharge command to provide a precharge complete signal indicating the completion of a precharge command operation. A row address latch responds to the active command to receive and hold a value representing a row address of the memory array as indicated by the address bits provided at the time the active command is initiated, and responds to the precharge complete signal to release the row address.

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

5,208,779	5/1993	Walther et al.	365/222
5,229,969	7/1993	Lee et al.	365/222
5,229,970	7/1993	Lee et al.	365/222
5,257,233	10/1993	Schaefer	365/227
5,335,201	8/1994	Walther et al.	365/222
5,444,667	8/1995	Obara	365/233
5,463,581	10/1995	Koshikawa	365/189.01
5,471,430	11/1995	Sawada	365/222

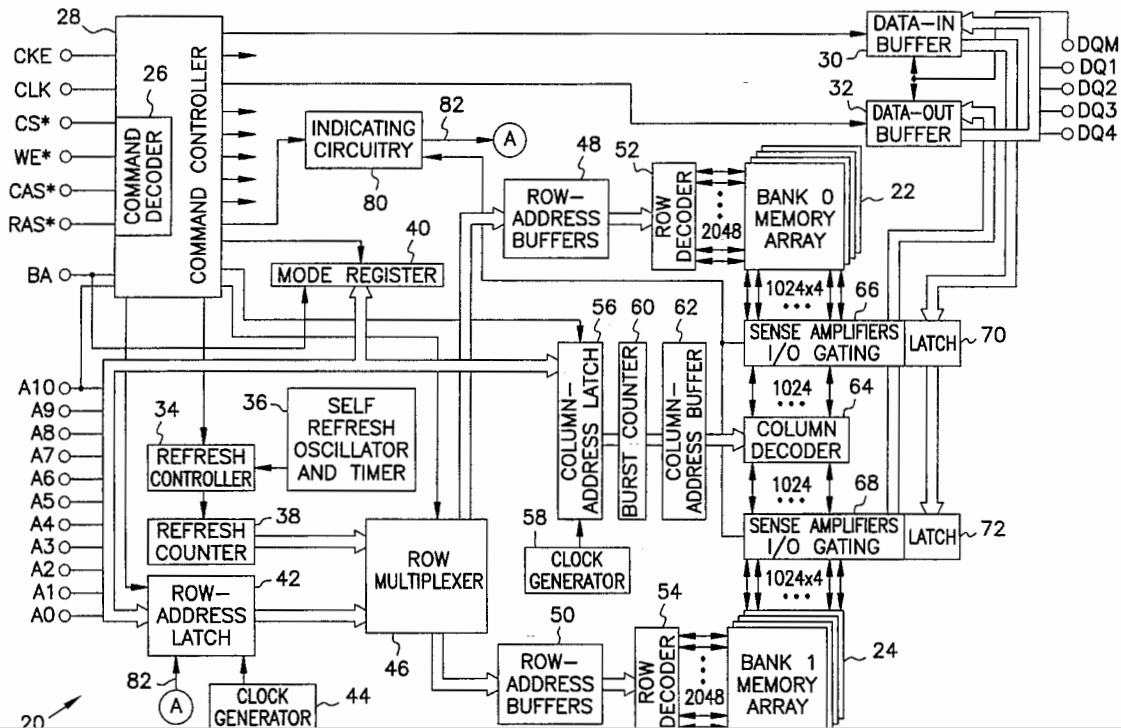
**FOREIGN PATENT DOCUMENTS**

0561306 9/1993 European Pat. Off. .

**OTHER PUBLICATIONS**

Yasuhiro Takai, et al., "250 Mbyte/s Synchronous DRAM Using a 3-Stage pipelined Architecture", *IEEE Journal of Solid-State Circuits*, No. 4, pp. 426-430, (Apr. 1994).

**24 Claims, 4 Drawing Sheets**



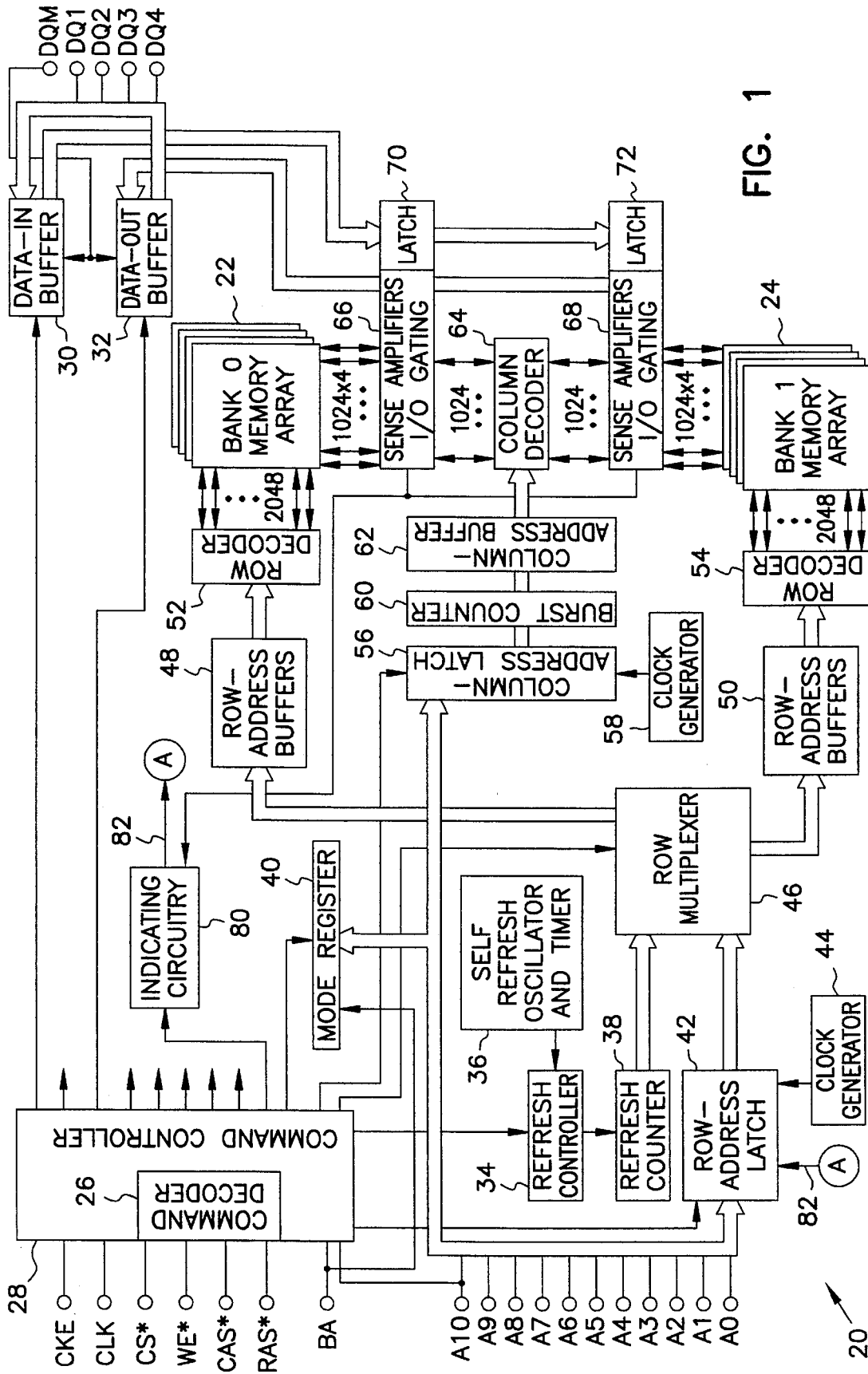


FIG. 1

20

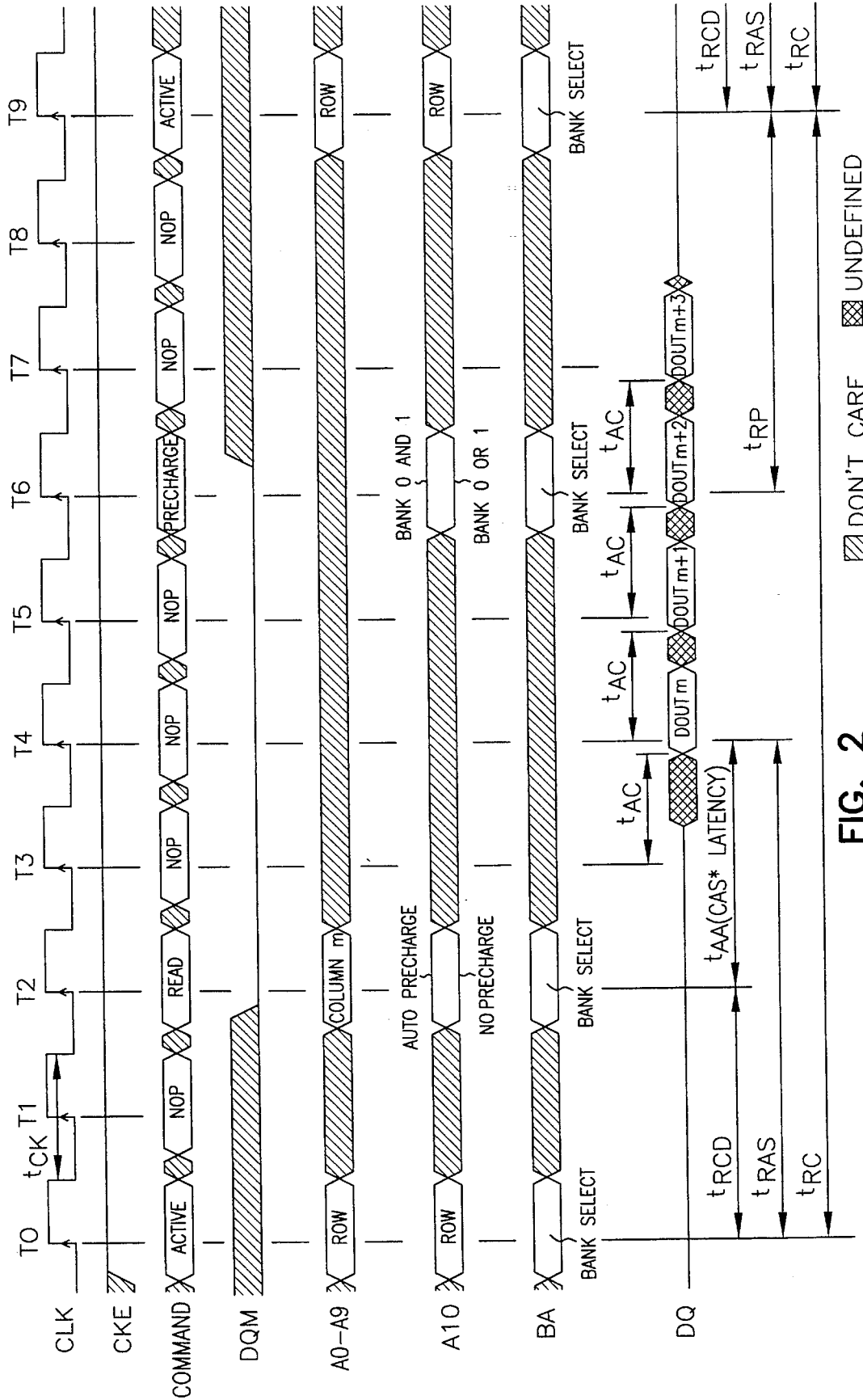


FIG. 2

☐ DON'T CARE

▨ UNDEFINED

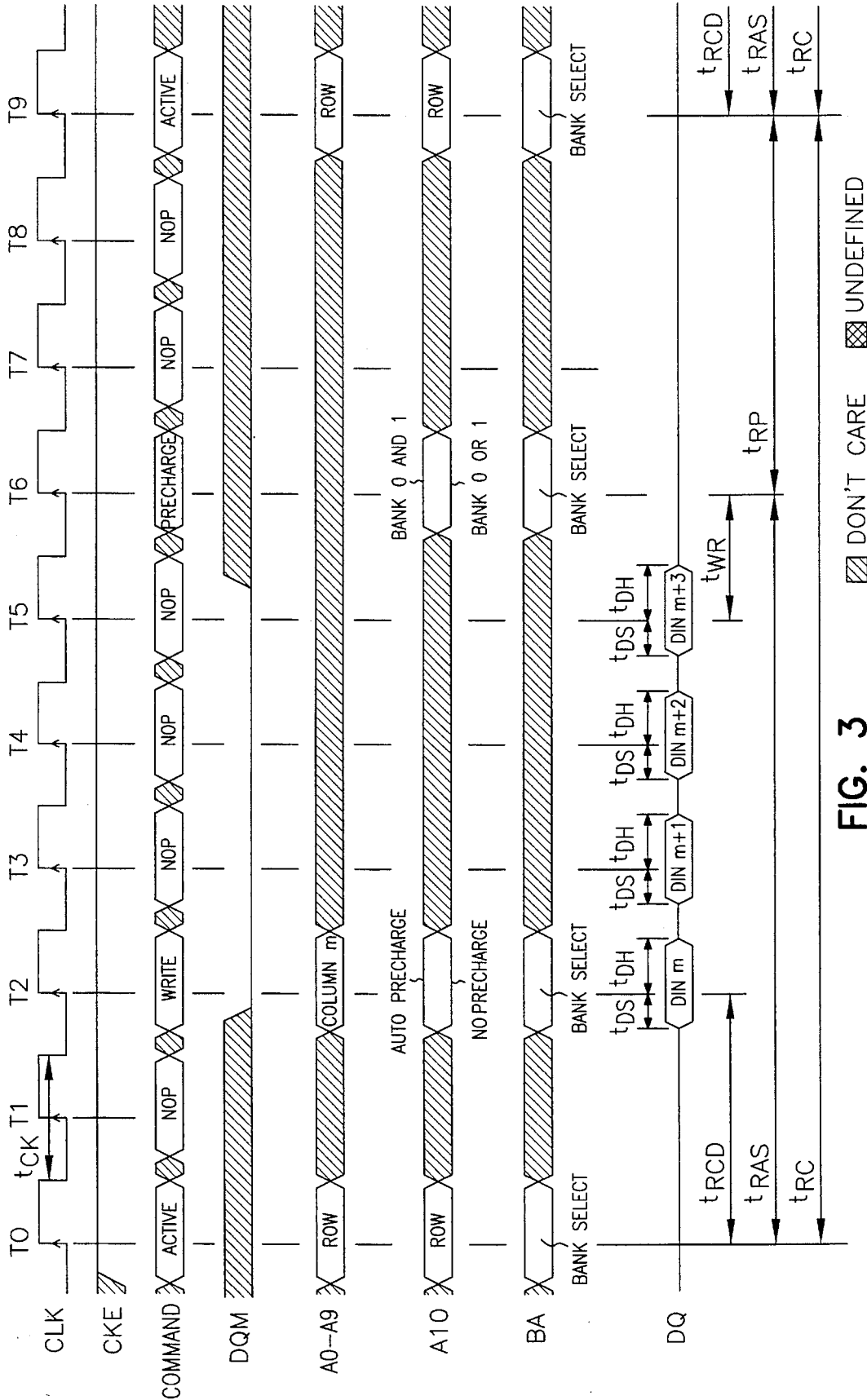


FIG. 3

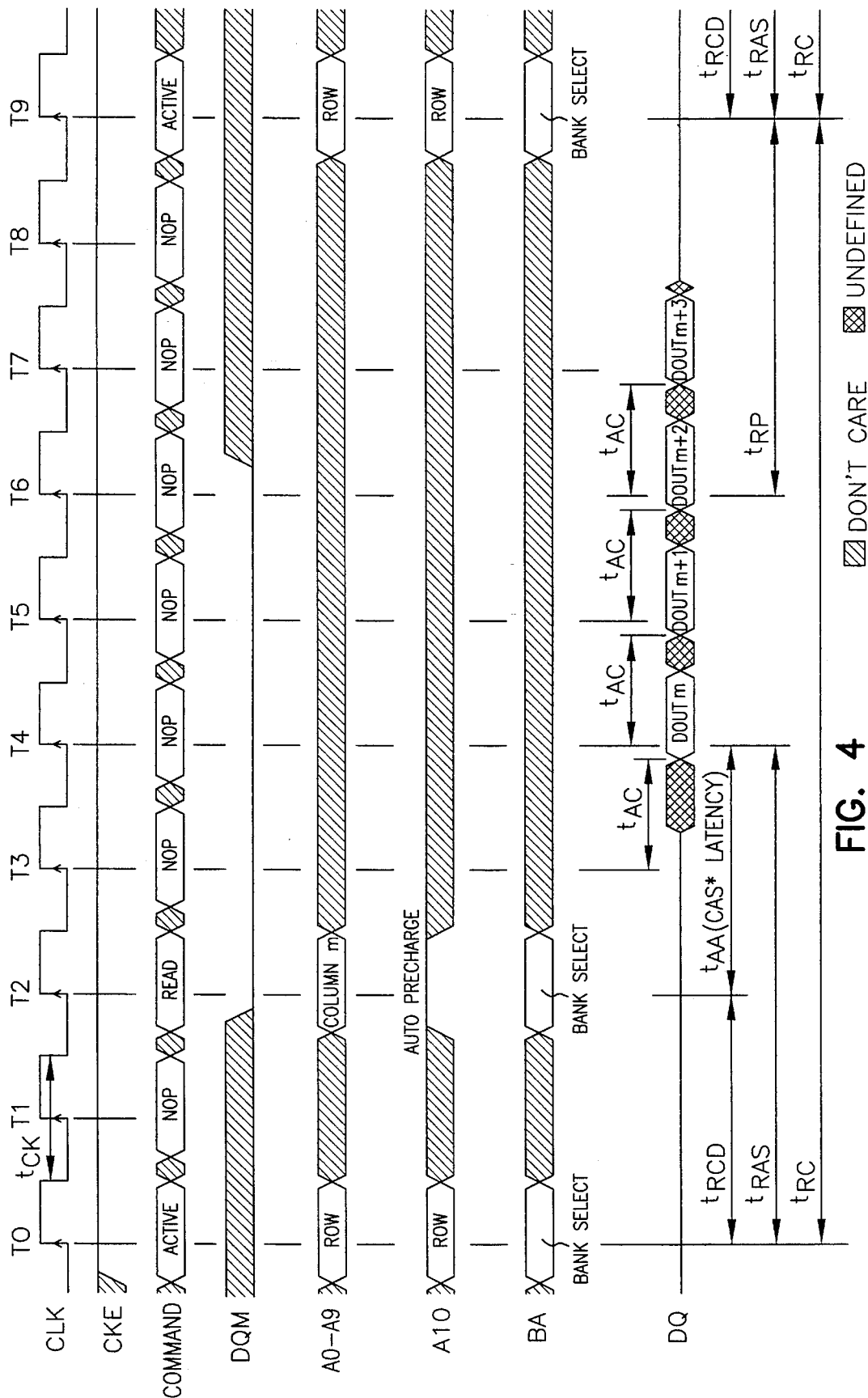


FIG. 4

# Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

## Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

## Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

## Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

## API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

## LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

## FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

## E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.