

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

**HP INC.**

**Petitioner**

**v.**

**JAMES B. GOODMAN**

**Patent Owner**

**Case No. IPR2017-01994**

**U.S. Patent No. 6,243,315**

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**DECLARATION OF DR. NADER BAGHERZADEH**

**UNDER 37 C.F.R. § 1.68**

I, Nader Bagherzadeh, declare as follows:

1. I am making this declaration at the request of HP Inc. (“HP”) in support of HP’s petition for *Inter Partes* review of U.S. Patent No. 6,243,315.

This declaration includes Appendices A and B.

2. I am being compensated for my services in this matter at the rate of \$525/hour plus expenses. My compensation is not contingent upon the outcome of this proceeding.

3. In preparing this declaration, I considered the following materials:

4. the ’315 patent, attached as Exhibit 1001;

5. the ’315 patent file history;

6. U.S. Patent No. 5,600,605 to Schaefer (“Schaefer”), attached as Exhibit 1003;

7. U.S. Patent No. 5,793,776 to Qureshi et al. (“Qureshi”), attached as Exhibit 1004;

8. U.S. Patent No. 5,204,840 to Mazur (“Mazur”), attached as Exhibit 1005;

9. U.S. Patent No. 4,005,395 to Fosler, Jr. et. al. (“Fosler”), attached as Exhibit 1006;

10. Reengineering the Curriculum: Design and Analysis of a New Undergraduate Electrical and Computer Engineering Degree at Carnegie Mellon University, Director et al., IEEE 1995, attached as Exhibit 1007;

11. Micron Technology, Inc. Functional Specification for MT48LC4M4R1(S) SDRAM, attached as Exhibit 1008;

12. Micron Technology, Inc. Data Sheet for MT48LC4M4A1/A2 SDRAM, attached as Exhibit 1009; and

13. Decision Instituting *Inter Partes* Review, Paper 6, IPR2015-01675 (PTAB February 11, 2016), attached as Exhibit 1010.

## **I. PROFESSIONAL BACKGROUND**

14. My *Curriculum Vitae* is attached hereto as Appendix A. I earned a bachelor's degree in electrical engineering in 1977 from the University of Texas at Austin. In 1979 and 1987, respectively, I earned a master of science in electrical engineering and a doctorate degree in computer engineering from the University of Texas at Austin.

15. I am currently a professor in the department of Electrical Engineering and Computer Science at the University of California, Irvine – a position I have held since 2003. Previously, from 1987 to 1992, I was an assistant professor in the Department of Electrical & Computer Engineering at the University of California, Irvine. Thereafter, from 1993 to 1997, I was an associate professor in the

Department of Electrical & Computer Engineering at the University of California, Irvine. In 1998, I was promoted to Professor and Chair of the Department of Electrical Engineering at the University of California, Irvine. I held that position until 2003, when I assumed my current role with the Department. I was elected as an IEEE Fellow in 2014.

16. I have been involved in design and development of digital systems for more than 30 years. While at AT&T Bell Labs in the early 1980's, I worked on an interface card for T1 lines as part of a support R&D team for the design of the first #5ESS digital switches. I was responsible for design of the hardware and software of this board which included memory devices (EEPROM, DRAM, and SRAM).

17. Since joining University of California, Irvine in 1987, I have been teaching, researching, and consulting regarding almost all aspects of memory design for high performance computer systems, including but not limited to DRAMs and SRAMs. In 2000, I became a cofounder of a high-tech company called Morpho Technologies, which was focused on the design and development of low power and high performance digital signal processors for mobile applications. As part of my duties as the chief technologist for the company, I evaluated patents, technical reports and presentations related to memory chip designs, DSPs, and parallel processing algorithms for mobile platforms.

18. For the Morpho project, I designed, developed and tested the key memory block responsible for exchanging data between the host processor and the slave processor (array processor). This subcomponent was designed to meet the power and performance requirements of the architecture for mobile embedded applications. I also designed the main data storage of the microcontroller (Tiny RISC) that was used for storing temporary data, as is the case for synchronous random-access memory (SRAM), which is a type of volatile memory. I was a primary contributor for the prototype board design for the Morpho device, which was integrated with DRAMs, FPGA, and other prototype board components.

19. As part of my teaching and research experience, I was responsible for developing circuits, electronic modules, and related architectures for memory systems. For the multithreaded superscalar DSP that was developed at UCI, I designed the memory block responsible for managing out-of-order execution of data registers corresponding to different threads. I also designed the original temporary data storage subcomponents for the VLIW processor, ViPER, and for the original Tiny RISC processor. I have done extensive work on the design of efficient data correction schemes for NAND flash memory circuits.

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