EXHIBIT A

TERM/PHRASE	CONSTRUCTION	COURT'S CONSTRUCTION
'memory system"	'a system capable of retaining data"	**[AGREED]**
'memory device"	"integrated circuit or chip"	**[AGREED]**
'a plurality of volatile solid state memory device"	"two or more memory devices in the memory system into which data may be written or from which data may be retrieved that retain information while an electrical power source, having a predetermined voltage range, is applied to the memory devices and when the voltage reaches a predetermined threshold outside of that range, the memory devices will no longer retain their current state of information"	**[AGREED]**
"selectively electrically isolating said memory devices from respective address lines and respective control lines"	"inhibiting signals on the respective address and respective control lines from the memory devices such that signals on those lines do not arrive at the memory devices"	**[AGREED]**
'any signals received on said respective address lines and respective control lines do not reach said memory devices"	any signals received on the respective address lines and respective control lines do not arrive at the memory devices"	**[AGREED]**
'address lines"	"lines that carry signals specifying a memory location to be accessed"	**[AGREED]**
'control signals"	"signals that control the sequence of addressing and the memory mode"	**[AGREED]**
'control lines"	"lines that carry control signals"	**[AGREED]**
"determining when said memory system is not being accessed"	"determining when there are no pending requests to retrieve information from or save information to a memory device of the memory system"	**[AGREED]**

"for initiating a low power mode for said memory system"	"when it is determined that said memory system is not being accessed, initiating a low power mode for said memory system"	**[AGREED]**
"low power mode"	"the memory device is in a state whereby it is in self refresh mode and is unable to respond to memory requests including read and write requests"	**[AGREED]**
"said control device electrically isolates said memory devices and places said memory devices in said self refresh mode"	"the control device isolates the respective address and respective control lines from the memory devices such that any signals received on the respective address lines and respective control lines do not arrive at the memory devices and the control device places the memory devices in the self refresh mode"	**[AGREED]**
"self refresh mode"	"mode in which the volatile solid state memory device is capable of maintaining the state of the data retained by it by generating signals that refresh the data within its memory array"	**[AGREED]**