Trials@uspto.gov
571.272.7822

Paper No. 6
Filed: March 9, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HP INC.,
Petitioner,

v.

JAMES B. GOODMAN,
Patent Owner.

Case IPR2017-01994
Patent 6,243,315 B1

Before BRIAN J. McNAMARA, PATRICK M. BOUCHER, and KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

HP Inc. ("Petitioner") filed a Petition requesting an *inter partes* review of claims 1, 5, 10, and 16 ("the challenged claims") of U.S. Patent No. 6,243,315 B1 (Ex. 1001, "the '315 patent"). Paper 2 ("Pet."). James B. Goodman ("Patent Owner") filed a Preliminary Response. Paper 5 ("Prelim. Resp.").

We have jurisdiction under 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition shows "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." Upon consideration of the Petition, the Preliminary Response, and the evidence therein, we conclude the information presented shows there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claims 1, 5, 10, and 16 of the '315 patent.

Our factual findings and conclusions at this stage of the proceeding, including claim construction, are preliminary and are based on the evidentiary record developed thus far. This is not a final decision as to patentability of claims for which *inter partes* review is instituted. Our final decision will be based on the record as developed fully during trial.

A. Related Proceedings

The parties identify the following litigations as related proceedings: *Goodman v. Hewlett-Packard Co.*, C.A. No. 16-CV-03195 (S.D. Tex.); *Goodman v. ASUS Computer International*, C.A. 17-CV-05542 (N.D. Cal. 05542) (Transferred from the S.D. Texas.); *Goodman v. Samsung Electronics America, Inc.*, C.A. No. 17-CV-05539 (S.D. N.Y.); and

Goodman v. Lenovo (United States) Inc., C.A. 17-CV-06782. Pet. 2; Prelim. Resp. 2.

We also note that the '315 patent is also the subject of current petitions for *inter partes* review by Petitioner Samsung (Case IPR2017-02021) and by Petitioner ASUS Computer International Inc. (IPR2018-00047).

B. The '315 patent

The '315 patent is directed to volatile memory devices. Ex. 1001, Abstract. Volatile memory devices "retain the contents of their memory states when electrical power is provided and maintained on the devices," but "[w]henever electrical power is removed from the devices, the memory contents of the device [are] lost and irretrievable." *Id.* at 2:54–58. Figure 4 of the '315 patent is reproduced below:

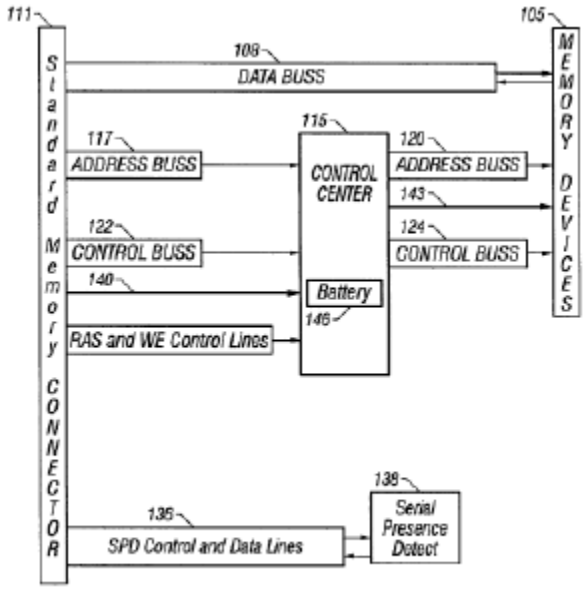

FIG. 4

Figure 4, shown above, illustrates a block diagram of a non-volatile memory system according to the invention. Ex. 1001, 4:41–42.

According to the '315 patent:

> The invention prevents the loss of data due to unexpected power outages and also prevents errant control and address signals to the memory devices by monitoring the input electrical power source to the memory devices for acceptable conditions, and electrically isolating the memory devices from signals received on the control lines and address lines and switching to an alternate internal electrical power source, typically a battery, whenever the input power source is unacceptable.

Id. at 3:15–24. The '315 patent explains further that the system "maintains the integrity of the data retained by the memory devices by isolating the devices from the external power source, control lines and address lines and placing the memory devices into a power down self-refresh mode which will maintain the data using a minimum of electrical power." *Id.* at 3:25–30.

C. Illustrative Claims

Independent claims 1 and 10 are illustrative of the claims at issue and are reproduced below.[1]

> 1. [a] A memory system for use in a computer system, said memory system comprising:
>
> [b-d] a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and capable of being placed in a self refresh

[1] Paragraph breaks and bracketed letters have been added for ease of reference and for consistency with nomenclature utilized by Petitioner.

mode; said memory devices having address lines and control lines;

[e] a control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and

[f] a memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode, thereby reducing the amount of electrical energy being drawn from an electrical power supply for said computer system.

Id. at 13:18–40.

10. [a] A memory system for use in a computer system, said memory system comprising:

[b] a plurality of volatile solid state memory devices that retain information when an electrical power source having a voltage greater than a predetermined voltage is applied to said devices;

[c] said memory devices having address lines and control lines;

[d] said computer system including a first electrical power source for operating said computer and being capable of producing a first voltage applied to said memory devices;

[e] a control device for monitoring said first voltage to determine when said first voltage is less than said predetermined voltage and for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals

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