

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HP INC.,
Petitioner,

v.

JAMES B. GOODMAN,
Patent Owner.

Case IPR2017-01994
Patent 6,243,315 B1

Before BRIAN J. McNAMARA, PATRICK M. BOUCHER, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, HP Inc. (“Petitioner”) challenges the patentability of claims 1, 5, 10, and 16 (“the challenged claims”) of U.S. Patent No. 6,243,315 B1 (Ex. 1001, “the ’315 patent”), owned by James B. Goodman (“Patent Owner”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, addresses issues and arguments raised during trial. For the reasons discussed below, we determine that Petitioner has shown by a preponderance of the evidence that claims 10 and 16 of the ’315 patent are unpatentable, but has not shown by a preponderance of the evidence that claims 1 and 5 of the ’315 patent are unpatentable.

A. Procedural History

On August 24, 2017, Petitioner filed a Petition requesting an *inter partes* review of claims 1, 5, 10, and 16 of the ’315 patent (Paper 2, “Pet.”), supported by the declaration testimony of Dr. Nader Bagherzadeh (Ex. 1002). Patent Owner filed a Preliminary Response. Paper 5 (“Prelim. Resp.”). On March 8, 2018, we instituted an *inter partes* review of the challenged claims. Paper 6 (“Decision on Institution” or “Dec. on Inst.”). On June 1, 2018, Patent Owner filed a Patent Owner Response (Paper 8) and later in the day, filed a second Patent Owner Response (Paper 9, “PO Resp.”). We refer herein to the second filed Patent Owner Response (Paper 9).¹ On August 24, 2018, Petitioner filed a Reply (Paper 10, “Reply”).

¹ Petitioner has not objected to our consideration of the second-filed Response.

A hearing was held on November 16, 2018. A transcript of the hearing has been entered into the record. Paper 15 (“Tr.”).

B. Related Proceedings

The parties identify the following litigations as related proceedings: *Goodman v. Hewlett-Packard Co.*, C.A. No. 16-CV-03195 (S.D. Tex.); *Goodman v. ASUS Computer International*, C.A. No. 17-CV-05542 (N.D. Cal.) (transferred from the S.D. Tex.); *Goodman v. Samsung Electronics America, Inc.*, C.A. No. 17-CV-05539 (S.D.N.Y.); and *Goodman v. Lenovo (United States) Inc.*, C.A. 17-CV-06782 (N.D. Cal.). Pet. 2; Paper 4 ¶ 2; Paper 4, 1.

In addition, we note that the ’315 patent is also the subject of current petitions for *inter partes* review by Samsung Electronics America, Inc. (IPR2017-02021) and by ASUS Computer International Inc. (IPR2018-00047²).

C. The ’315 patent

The ’315 patent is directed to memory systems having volatile solid state memory devices that retain information when an electrical power source is applied but lose their memory contents when power is removed. Ex. 1001, 2:54–58, 3:46–52. To reduce energy consumption and preserve memory contents, volatile memory devices are placed in low power “self-refresh mode” when the memory system is not receiving requests for access. *See id.* at 3:46–54 (stating the “low power mode utilizes

² Case IPR2018-00047 has been joined with IPR2017-02021.

significantly less electrical current than when the memory device is in the operating mode or powered up mode”), *id.* at 3:25–30 (stating “placing the memory devices into a power down self-refresh mode . . . will maintain the data using a minimum of electrical power”). The memory system of the ’315 patent has a control device interposed electrically between the memory devices and a central processing unit (“CPU”). *Id.* at 3:54–56. The control device senses CPU access of the memory devices and conditions the memory devices to an operating mode condition prior to allowing access to the information contained therein. *Id.* at 3:56–59. The control device also places the solid state memory devices into a low power standby mode when it “senses the termination of a memory cycle.” *Id.* at 3:59–62.

Figure 1 of the ’315 patent, reproduced below, illustrates a preferred embodiment in which address and control busses are electrically isolated from the memory devices when the memory devices are in a power down self-refresh mode. *Id.* at 5:60–63.

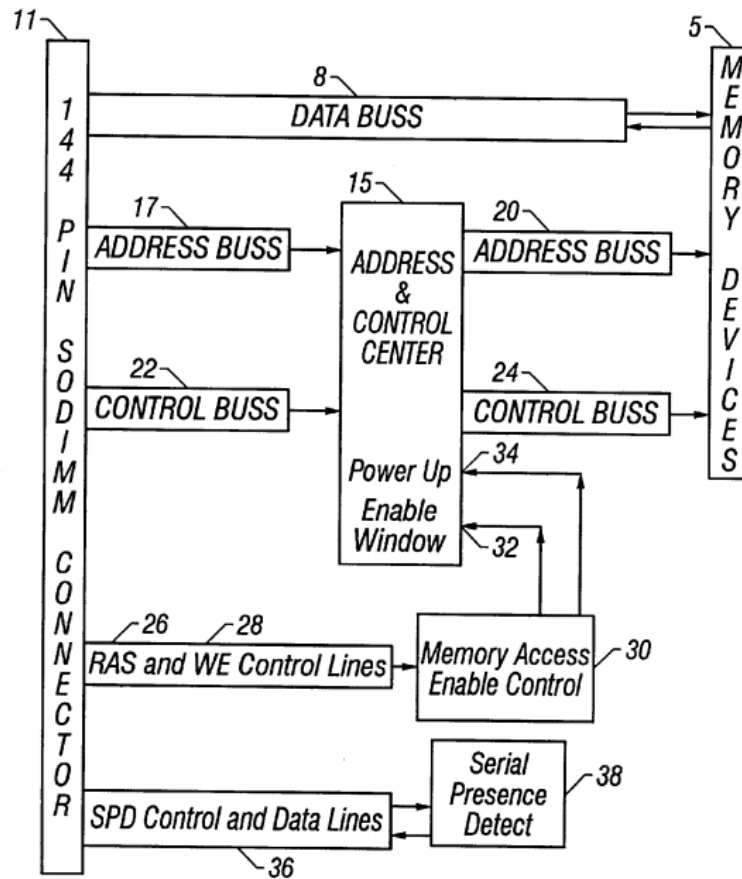


FIG. 1

As shown in Figure 1 of the '315 patent above, control device 15 is interdisposed between address bus³ 17 and address bus 20 (*id.* at 5:50–52) as well as between control bus 22 and control bus 24 (*id.* at 5:54–56). Control device 15 isolates address bus 17 and control bus 22 from memory devices 5 when the memory devices are in a power down self-refresh mode. *Id.* at 5:60–63. By isolating the memory devices from control bus 22 and address bus 17, control device 15 prevents errant signals from erroneously changing

³ The Decision uses the conventional spelling “bus” as opposed to “buss” as used in the '315 patent.

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