

ADVANCE



MT48LC4M4R1(S)  
4 MEG x 4 SDRAM

# SYNCHRONOUS DRAM

# 4 MEG x 4 SDRAM

Pulsed  $\overline{RAS}$ , Dual Bank,  
BURST Mode, 3.3V, SELF REFRESH

SYNCHRONOUS DRAM

## FEATURES

- Fully synchronous; all signals (excluding clock enable) registered to positive edge of system clock
- Meets all JEDEC functional specifications
- Dual internal banks: dual 2 Meg x 4 architecture
- Programmable burst-lengths: 2, 4, 8 cycles or full-page burst
- Programmable burst-sequence: sequential or interleave
- Burst termination
- Multiple burst READ, single WRITE capability
- Hidden precharge capability with optional automatic precharge command
- Programmable READ latency: 1, 2 or 3 clocks
- Industry-standard x8 pinouts, timing, functions and packages
- Refresh modes: AUTO and SELF
- Standard and extended AUTO REFRESH rates
- High-performance CMOS silicon-gate process
- Lead-over-chip assembly architecture
- Single +3.3V  $\pm 0.3V$  power supply
- Low power, 3mW standby; 200mW active, typical
- LVTTTL-compatible
- CKE-controlled power-down and suspend operations
- Mode register programming
- JEDEC-standard command set (pulsed  $\overline{RAS}$ )

## PIN ASSIGNMENT (Top View)

### 44-Pin TSOP FORWARD (DD-7)

Vcc	1	44	Vss
NC	2	43	NC
VssQ	3	42	VssQ
DQ1	4	41	DQ4
VccQ	5	40	VccQ
NC	6	39	NC
VssQ	7	38	VssQ
DQ2	8	37	DQ3
VccQ	9	36	VccQ
NC	10	35	NC
NC	11	34	NC
WE	12	33	DCM
CAS	13	32	CLK
$\overline{RAS}$	14	31	CKE
$\overline{CS}$	15	30	NC
BA	16	29	A9
A10	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
Vcc	22	23	Vss

## OPTIONS

## MARKING

- Timing
 

10ns access ( $\leq 100$ MHz)	-10
12ns access ( $\leq 83$ MHz)	-12
13.3ns access ( $\leq 75$ MHz)	-13
- Auto Refresh
 

4,096-cycle in 64ms (15.6 $\mu$ s/row)	none
4,096-cycle in 128ms (31.25 $\mu$ s/row)	S
- SELF REFRESH
 

Not allowed	none
Allowed	S
- Plastic Packages
 

44-pin TSOP (400 mil)—forward	TG
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- Part Number Example: MT48LC4M4R1TG-10 S

with a synchronous interface. Each byte is uniquely addressed through a bank-select bit and 20 address bits. The bank select and address are entered first by  $\overline{RAS}$  registering (row active command) 12 bits (A0-A10, BA) and then  $\overline{CAS}$  registering 11 bits (A0-A9, BA). At  $\overline{CAS}$  registration (READ or WRITE command), address bit A10 defines auto-precharge state (active HIGH). Bank selection is controlled by BA during both  $\overline{RAS}$  and  $\overline{CAS}$  registration.

The MT48LC4M4R1 is designed to operate in a synchronous, 3.3V memory system. All input and output signals, with the exception of clock enable (CKE) during POWER-DOWN and SELF REFRESH modes, are synchronized to the positive-going edge of the system clock (CLK).

The synchronous DRAM has several programmable features to allow maximum performance in each user's system. Additionally, bank switching between the two internal memory banks in conjunction with the programmable BURST mode provides very high-speed performance.

The synchronous DRAM allows both AUTO REFRESH (during normal operation) and SELF REFRESH (for low-

## GENERAL DESCRIPTION

The MT48LC4M4R1(S) is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x4



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MICRON

MT48LC4M4R1(S)  
4 MEG x 4 SDRAM

FUNCTIONAL BLOCK DIAGRAM

SYNCHRONOUS DRAM

