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Qureshi et al.

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- [54] **STRUCTURE AND METHOD FOR SDRAM DYNAMIC SELF REFRESH ENTRY AND EXIT USING JTAG**
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- [21] Appl. No.: **733,817**
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- [51] Int. Cl.⁶ **G01R 31/28**
- [52] U.S. Cl. **371/22.1; 395/183.18**
- [58] Field of Search **371/22.1, 21.1, 371/22.31, 22.32, 22.5, 42; 365/201, 222, 189.01, 233; 395/881, 285, 183.06, 183.18; 324/765**

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Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel, LLP; David T. Millers

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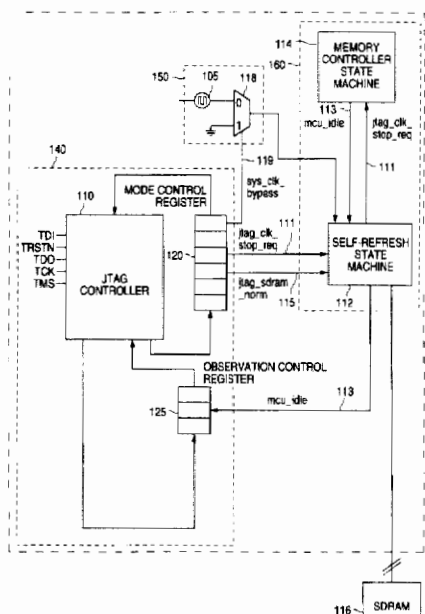
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[57] ABSTRACT

JTAG test logic and a memory controller place an SDRAM in a self refresh mode prior to beginning JTAG testing. The memory controller can complete a current memory access and otherwise prepare for the JTAG test. During the JTAG test, self refresh mode operation of the SDRAM retains data without the need for a clock signal or refresh signals which are suspended for the JTAG test. Accordingly, after the JTAG test, circuit operation can continue without reinitializing data in the SDRAM.

16 Claims, 6 Drawing Sheets



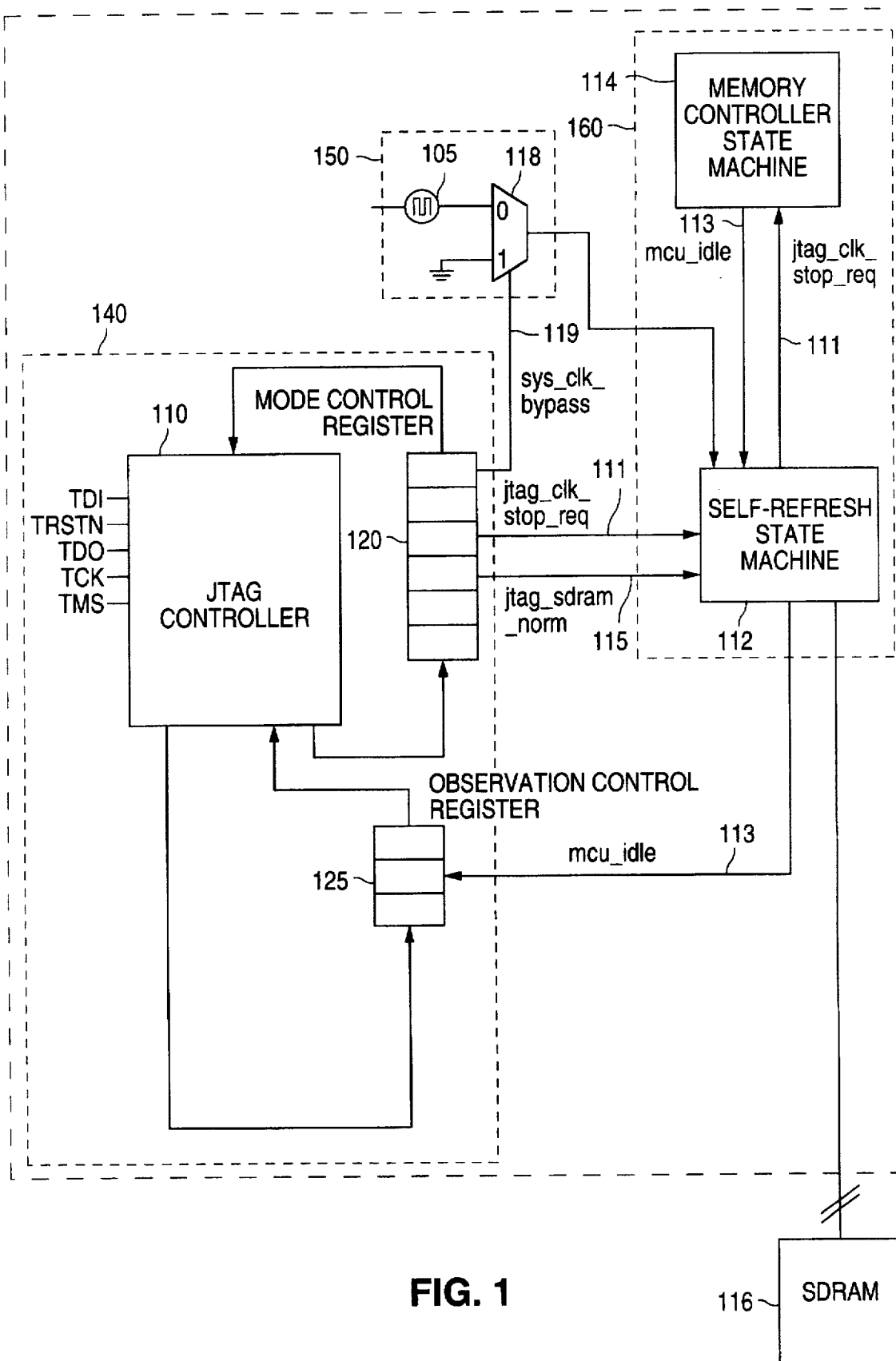


FIG. 1

116 SDRAM

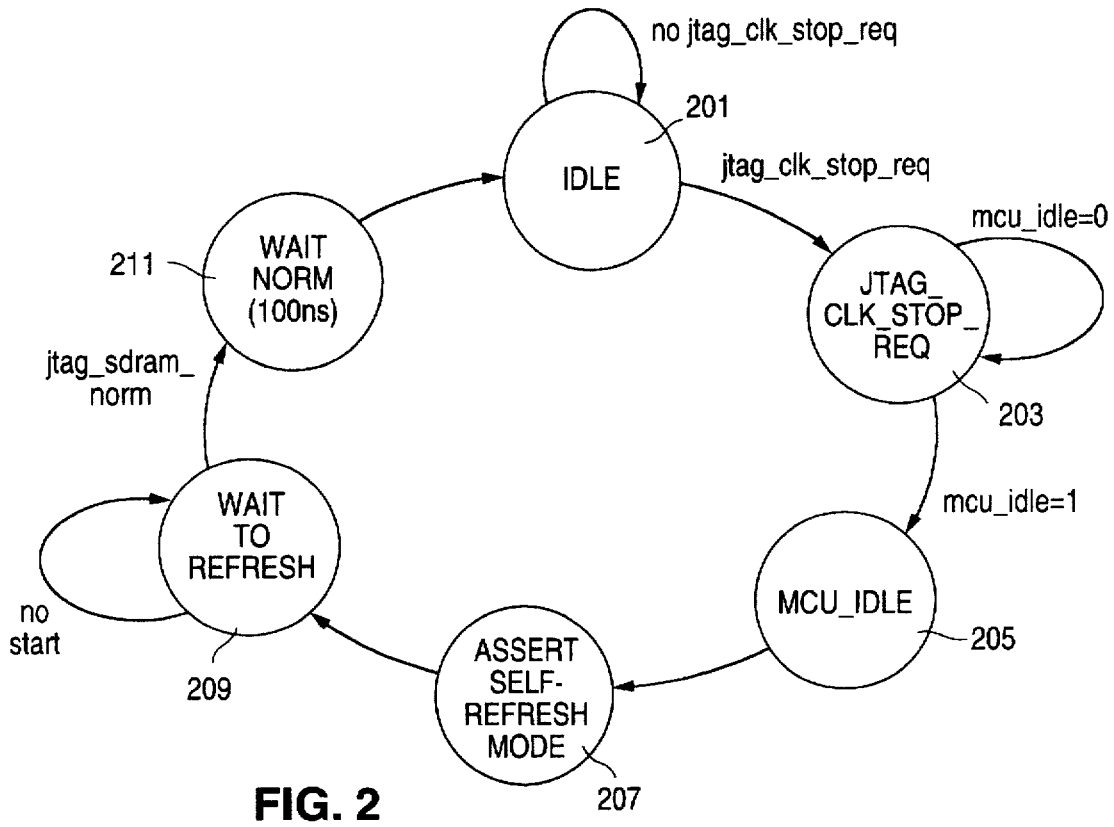


FIG. 2

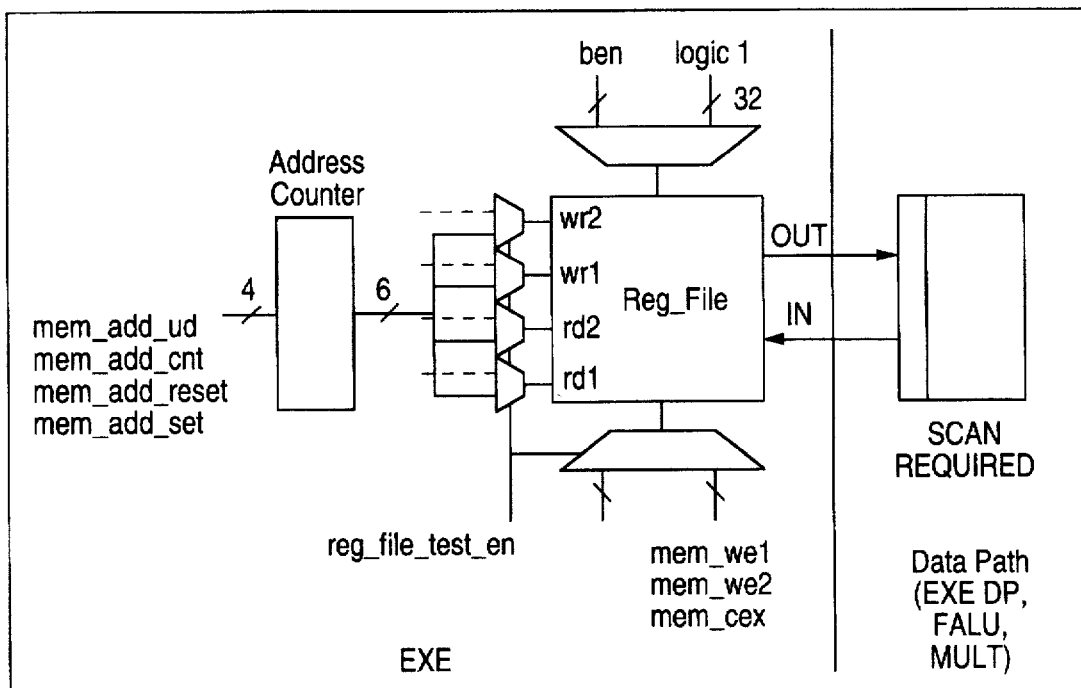
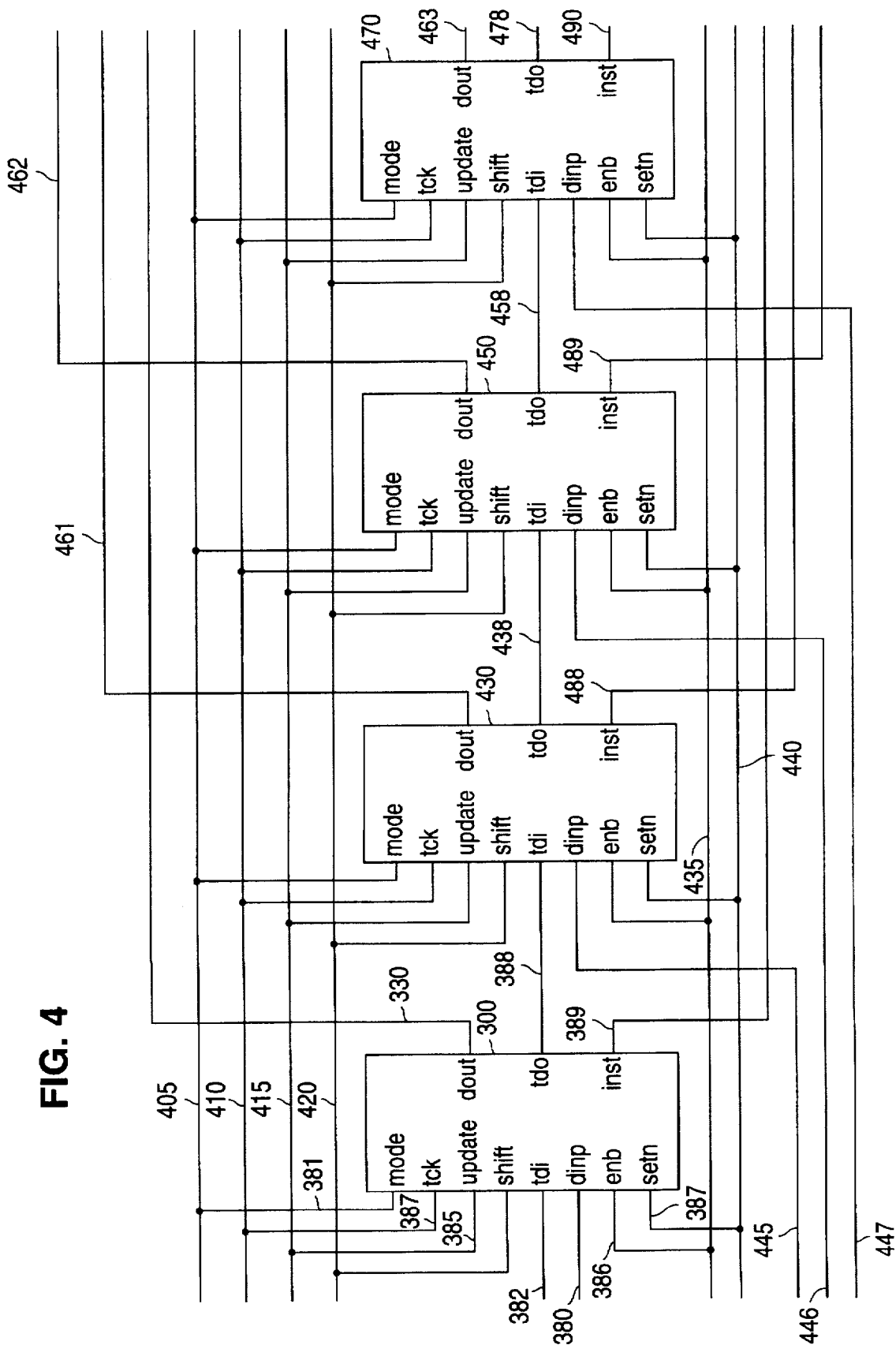


FIG. 7

FIG. 4



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