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United States Patent [19]

Schaefer

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[54] **AUTO-ACTIVATE ON SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY**

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[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **481,920**

[22] Filed: **Jun. 7, 1995**

[51] **Int. Cl.**[6] **G11C 7/00**

[52] **U.S. Cl.** **365/233**; 365/230.03

[58] **Field of Search** 365/233, 203, 365/222, 230.03

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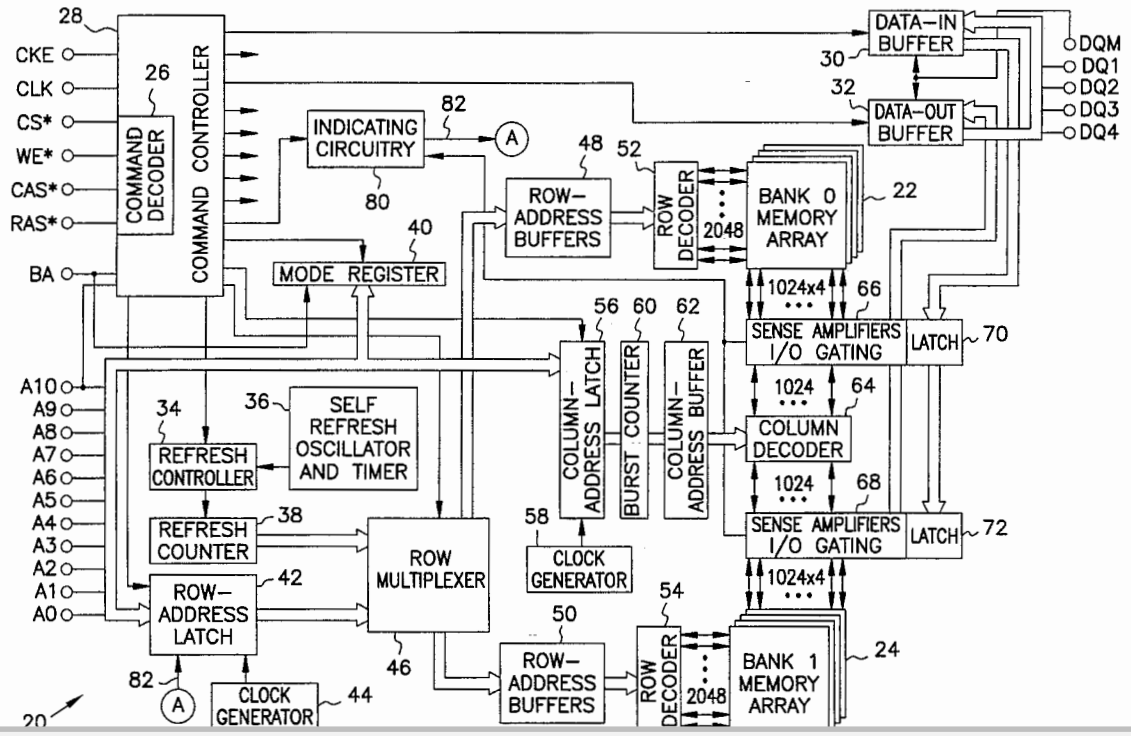
[57] **ABSTRACT**

A synchronous dynamic random access memory (SDRAM) includes a memory array and is responsive to command signals and address bits. A command decoder/controller responds to selected command signals to initiate, at different times, a precharge command, an active command, and a transfer command. The command decoder/controller initiates the active command during the precharge command. Indicating circuitry responds to the precharge command to provide a precharge complete signal indicating the completion of a precharge command operation. A row address latch responds to the active command to receive and hold a value representing a row address of the memory array as indicated by the address bits provided at the time the active command is initiated, and responds to the precharge complete signal to release the row address.

24 Claims, 4 Drawing Sheets



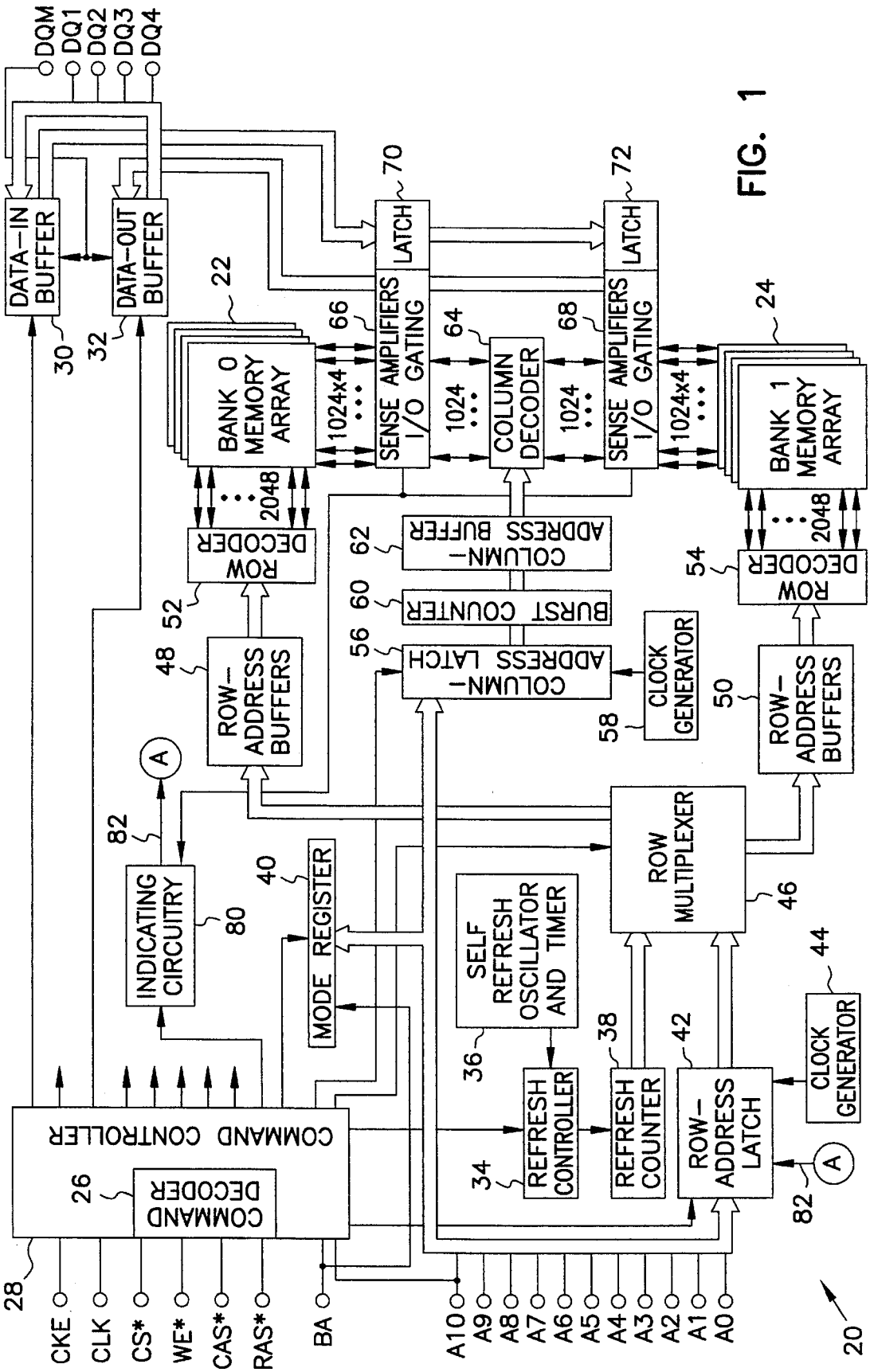


FIG. 1

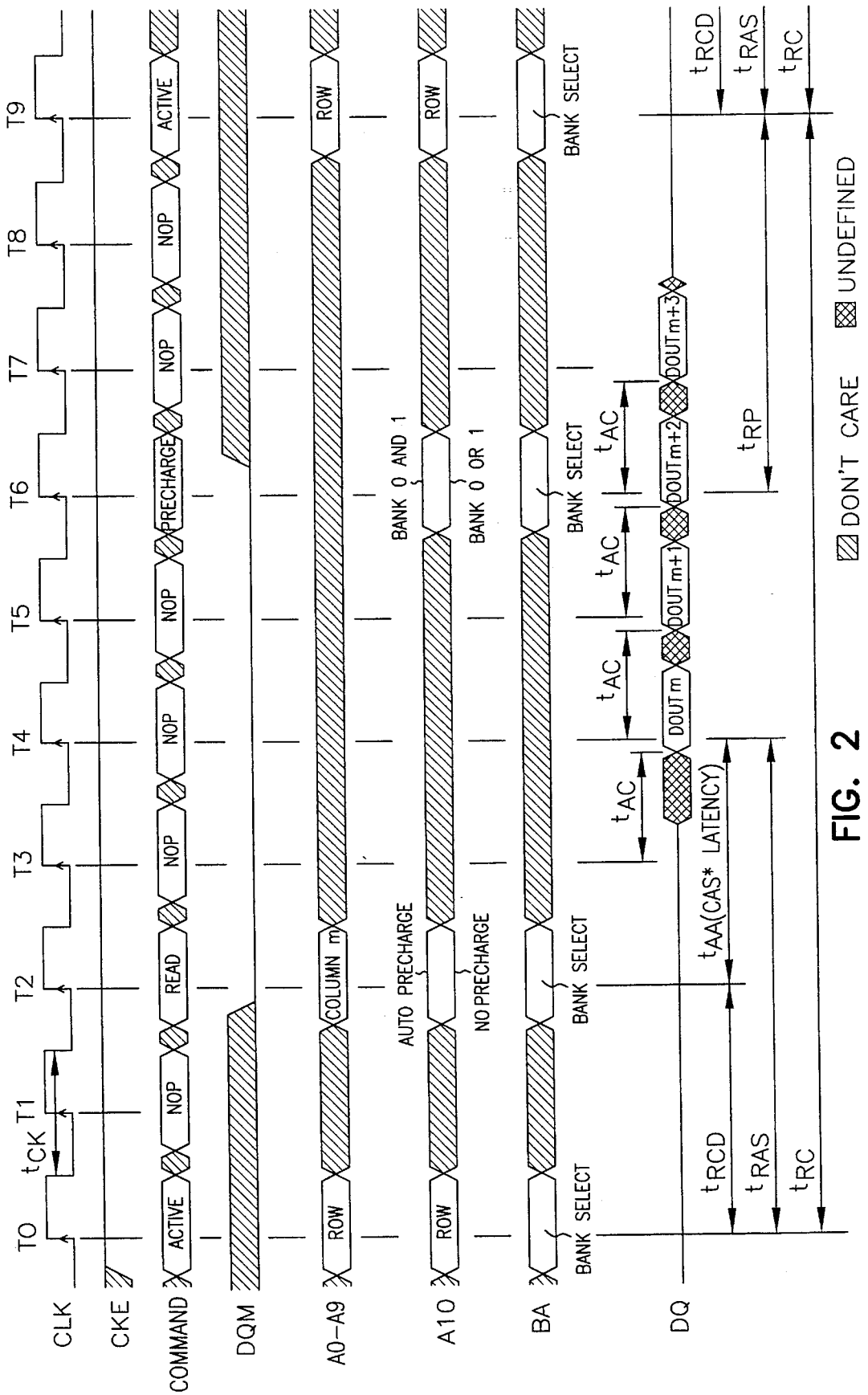


FIG. 2

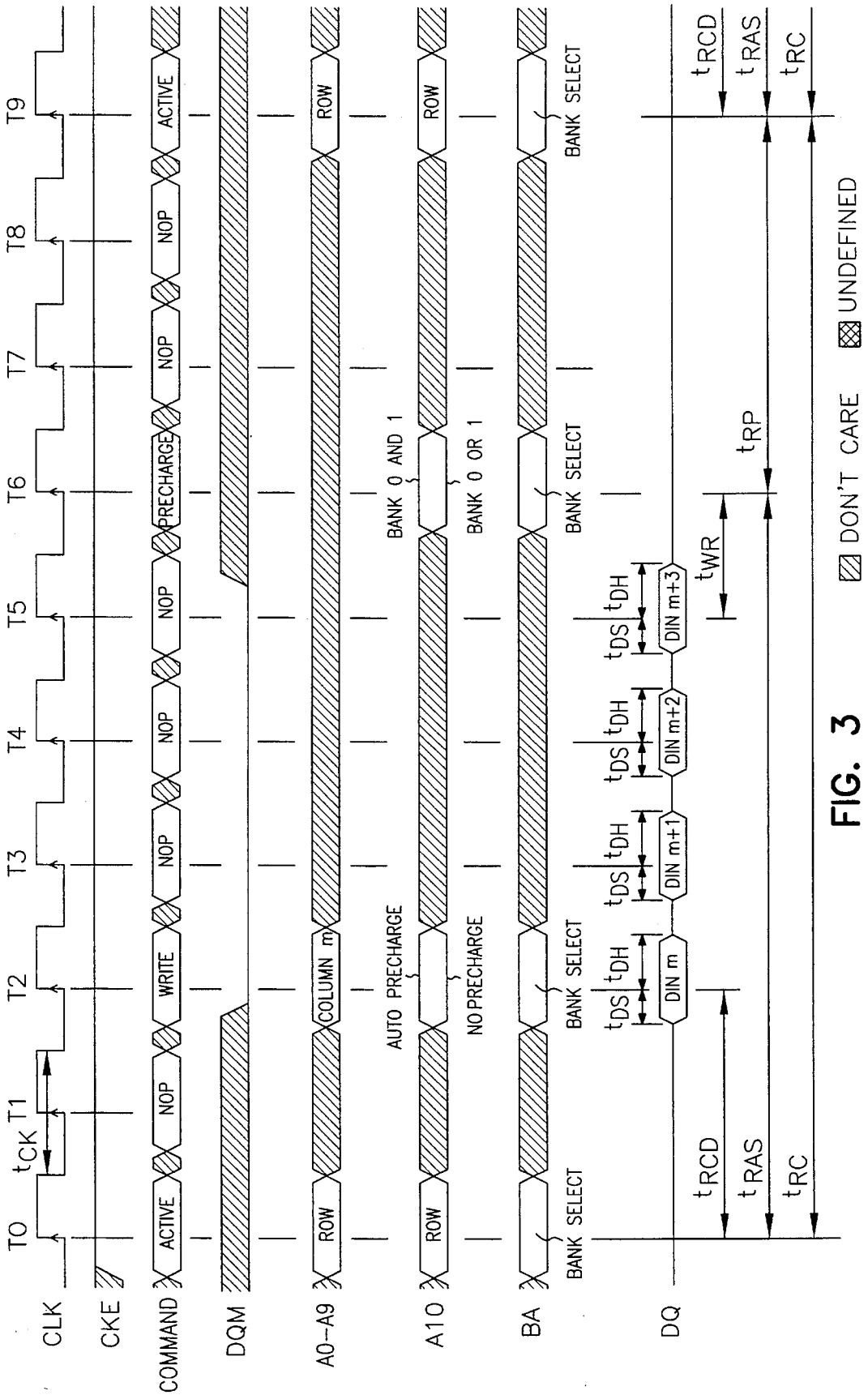


FIG. 3

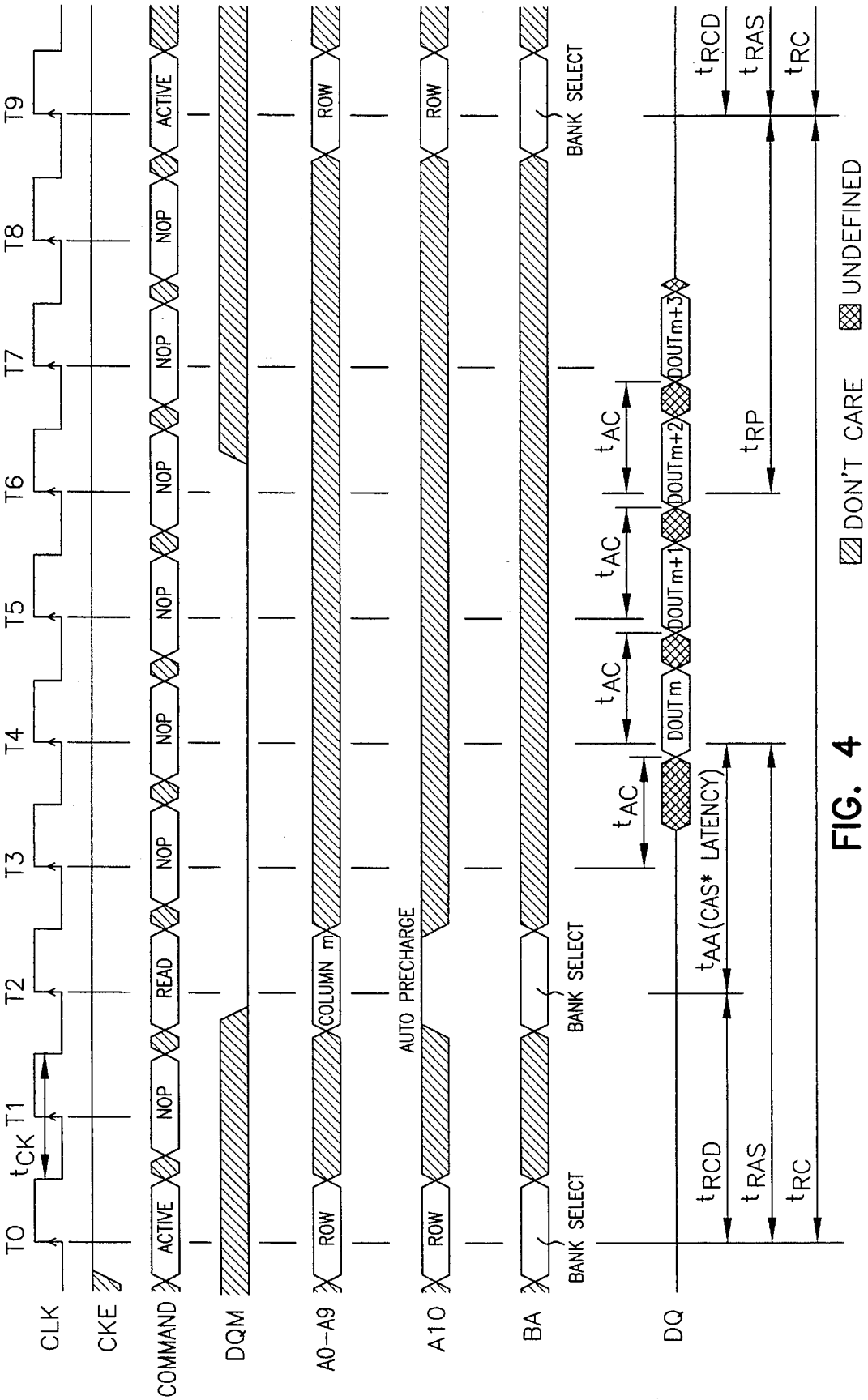


FIG. 4

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