# Travis N. Blalock

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**Education:**

> Auburn University, Ph.D., July 1991.  Major emphasis on CMOS analog and digital IC design.  Dissertation - *Design of Very High Speed Sense Amplifiers for CMOS Random Access Memory*.

> University of Tennessee, M.S.E.E., December 1988. Major emphasis on analog and digital circuit design.  Thesis - *Development of a Radiation Hardened 600 Watt Switchmode Power Converter*.

> University of Tennessee, B.S.E.E. with High Honors, January 1985. Senior year specialization in analog circuit design.

**Work Experience:**

Skills:     Successful entrepreneur (built and sold medical device company), strategic leadership for product creation and development, software and hardware technical team leadership, mixed-signal integrated circuit design, low-noise analog design, memory design, system level architecture and design, VHDL/Verilog, application software, assembly and high-level firmware, kernel driver software, network control software, university teaching and research, mentoring, invention.

8/98 -     Associate Professor, University of Virginia.  Research in mixed-signal CMOS integrated circuit design.  Principle focus areas are integrated imaging and signal processing, smart sensors, low-voltage low-power design, and analog design techniques in 'digital' processes.  Developing and teaching courses in analog and mixed-signal integrated circuit design.

9/13 - 7/17   Fellow, Analogic Inc., Joined Analogic via acquisition of PocketSonics startup.  Chief architect for handheld medical ultrasound imaging system.  This included leading a team and directing system architecture, custom integrated circuit design, software architecture and interface design.  Other activities include software development at all levels of the system.

1/04 – 9/13   Co-Founder, CEO, and CTO, PocketSonics, Inc., Built medical device startup based on unique ultrasound imaging architecture.  Led the technical development of a handheld 3D volume capable ultrasound imaging system.  Sold Enterprise to Analogic, Inc.

8/96 - 8/98   Principal Scientist, Hewlett-Packard Laboratories.  Technical lead on multiple mixed-signal optoelectronic image capture, processing, and display IC designs.  Exploration of new technologies and mentoring of other engineers.  Development of modeling software and custom CAD tools for circuit analysis and design.

7/91 - 8/96  <u>Member Technical Staff</u>, Hewlett-Packard Laboratories.  Designed CMOS analog signal processing integrated circuits for mass storage products.  Principal architect and designer of new integrated optoelectronic image acquisition and processing IC.  This chip is the principal enabler of several new HP products.  Also deployed numerous design tools and infrastructure improvements, including smart routing software for fiber optic access.

3/88 - 7/91  <u>Graduate Research Assistant</u>, Auburn University.  Developed high speed CMOS sense amplifier topologies for memory circuits.  Also developed memory circuits optimized for quasi-static low temperature operation.  Test circuits were fabricated and experimental results published.

3/88 - 7/91  <u>Graduate Teaching Assistant</u>, Auburn University.  Served as instructor teaching junior and senior level electronics courses.  Student teaching effectiveness average rating of 4.5/5.0 for last recent four quarters.  Total teaching experience of 11 quarters.

9/86 - 3/88  <u>Graduate Research Assistant</u>, University of Tennessee.  Designed and implemented radiation hardened switchmode power supply.  Addressed key stability issues with extensive computer simulation techniques.

2/85 - 8/86  <u>Development Engineer</u>, NASA Langley Research Center, Hampton, VA.  Developed measurement techniques and instrumentation for the characterization of composite materials.

9/84 - 1/85  <u>Assistant Engineer</u>, Control Technology Inc., Knoxville, TN, part-time while attending school, 25-30 hrs/week.  Developed firmware and hardware for industrial controller peripherals.

9/82 - 12/83  <u>Assistant Engineer</u>, Technology for Energy Corporation, Knoxville, TN, part-time while attending school, 25 - 30 hrs/week

**Consulting & Other Work:**

12/14 - 2/16  <u>Expert Consultant</u>, Samsung Inc., Patents and documents analysis, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

7/14 – 8/14  <u>Expert Consultant</u>, Intel Inc., Patents and documents analysis, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

11/12 - 5/13  <u>Expert Witness</u>, Sound Design Technologies, Sound Design v. Oticon, Inc., Perkins Coie Brown & Bain, LLP, mixed-signal CMOS circuits.

2/09 – 6/11  <u>Expert Witness</u>, Samsung, Spansion v. Samsung, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

8/09 – 6/10  <u>Expert Witness</u>, IBM, MOSAID v. IBM, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

10/09 - 2/10  <u>Expert Witness</u>, Cisco, Cisco Systems v. MOSAID, Kirkland & Ellis, LLP, mixed-signal electronics.

4/09 – 6/09  <u>Expert Witness</u>, Apple Computer, Wong, Cabello, Rutherford & Brucculeri, LLP, mixed-signal electronics, USB protocol.

8/08 –12/10  <u>Expert Witness</u>, Samsung, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

3/08 – 3/09   <u>Expert Witness</u>,  AMIS, AMIS v. PowerDsine, Perkins Coie Brown & Bain, pre-trial deposition, POE integrated circuits, protocols, POE product evals, reports.

10/07 – 2/08  <u>Expert Witness</u>, Analog Devices, Analog Devices v. Silicon Laboratories, Proskauer Rose LLP, pre-trial deposition, mixed-signal CMOS isolation circuits.

7/07 - 1/09   <u>Expert Witness</u>,  Micron, MOSAID v. Micron, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

3/07 – 7/07   <u>Expert Witness</u>, Samsung, Samsung v. Matsushita, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

9/06 – 5/07   <u>Expert Witness</u>, Samsung, Samsung v. Ericson, Kirkland & Ellis, LLP, mixed-signal CMOS circuits.

3/05 – 11/05  <u>Expert Witness</u>, Sigmatel, Sigmatel v. Actions Semiconductor, Kirkland & Ellis, LLP, mixed-signal CMOS circuits, firmware evaluation.

12/03 – 9/04  <u>Expert Witness</u>, Agere, Agere v. Broadcom, Kirkland & Ellis, LLP. Testimony at Markman, pre-Markman and pre-trial depositions, mixed-signal CMOS circuits, VCOs, interface, biasing.

8/98 - 6/03   <u>Consultant</u>, Agilent Technologies.  Exploratory design and simulation of next-generation circuit technologies.

2/01 - 3/01   <u>Consultant</u>, Displaytech. Analysis of circuit issues in silicon-backplane microdisplays.

**Awards:**

Best Paper of Conf. Award, Hewlett-Packard Design Technology Conference, May 1997.

Best Paper of Session Award, Hewlett-Packard Design Technology Conference, May 1994.

Auburn University Outstanding Graduate Student Award, March 1991.

Sigma Xi Carolyn Carr Outstanding Research Award, February 1991.

Tech Brief Award, NASA Langley Research Center, June 7, 1990.

Invention Disclosure Award, NASA Langley Research Center, December 1, 1989.

Outstanding Performance Award, NASA Langley Research Center, December 1985.

Invited Guest, National Security Forum, Air War College, May 23-27, 2002

**Affiliations/Service:**

Program Committee, VLSI Circuits Symposium, 2002 – 2007

Program Committee, Great Lakes Symposium on VLSI Circuits, 2003 - 2008

Associate Editor, IEEE/OSA Journal of Display Technology, 2004 - present

Associate Editor, IEEE Transactions on Very Large Scale Integration Systems, 2003 - 2005

Reviewer, IEEE Journal of Solid State Circuits, 1999 - present

Associate Director, Rodman Scholars Program, School of Engineering, UVa, 2000 – 2004

Mentor, NIH Biotech Training Grant, 2000-2005

Chairman, UVa ECE Graduate Committee, 2000-2002

Chairman, UVa SEAS Rules and Courses Committee, 2002- 2004

Board of Directors, University of Virginia Institute for Microelectronics, 1999 – present

Boy Scout Adult Leader, Troop 17, Charlottesville, VA

Institute of Electrical and Electronics Engineers

Phi Eta Sigma and Sigma Xi, National Honor Societies

Tau Beta Pi, National Engineering Honor Society

Eta Kappa Nu, National Electrical Engineering Honor Society

**Books and Book Chapters:**

R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design, Fifth Edition*, McGraw Hill, New York, February 2015.

R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design, Fourth Edition*, McGraw Hill, New York, April 2010.

R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design, Third Edition*, McGraw Hill, New York, January 2007.

J. Theil, M. Boehm, D. S. Gardner, and T. Blalock, editors, *Materials, Integration and Technology for Monolithic Instruments,* vol. 869, Materials Research Society, 2005.

R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design, Second Edition,* McGraw Hill, New York, July 2003.

R. W. Johnson, R. C. Jaeger, and T. N. Blalock, "Wafer-scale multichip packaging technology," *Wafer Scale Integration*, Chapter 10, Kluwer Publishing Company, 1989.

**Refereed Journals:**

J. F. Bolus, B. H. Calhoun, and T. N. Blalock, "39 fJ/bit On-Chip Identification of Wireless Sensors Based on Manufacturing Variation," *IEEE Journal of Low Power Electronics*, 2014.

S. N. Wooters, A. C. Cabe, Z. Qi. J. Wang, R. W. Mann, B. H. Calhoun, M. R. Stan, and T. N. Blalock. "Tracking on-chip age using distributed, embedded sensors," Tran. On VLSI Systems, vol. 20, pp.1974-1985, Nov. 2012.

S. N. Wooters, B. H. Calhoun, and T. N. Blalock, "An energy-efficient subthreshold level converter in 130-nm CMOS," Circuits and Systems II: Express Briefs, IEEE Transactions on, vol. 57, no. 4, pp. 290 –294, April 2010.

J. Hossack, Y. Li, W. F. Walker, T. N. Blalock, "Synthetic Axial Acquisition: Full Resolution Low-Cost C-Scan Ultrasonic Imaging," IEEE Trans. Ultrason. Ferroelec. Freq. Contr, vol. 55, no. 1, pp. 236-239, Jan. 2008.

Fuller, M. I., K. Ranganathan, S. Zhou, E. V. Brush, T.N. Blalock, J.A. Hossack, and W.F. Walker, "Experimental System Prototype of a Portable, Low-Cost, C-scan Ultrasound Imaging Device," IEEE Trans. Biomedical Engr., vol. 55, no. 2, pp. 519-530, Feb. 2008.

M. Fuller, T. N. Blalock, J. A. Hossack, and W. F. Walker, "Novel Transmit Protection Scheme for Ultrasound Systems," *IEEE Trans. Ultrasonics, Ferroelectrics and Frequency Control,* vol. 54, no. 1, pp. 79-86, Jan. 2007.

K. Ranganathan, M. K. Santy, T. N. Blalock, J. A. Hossack, and W. F. Walker, "Direct Sampled I/Q Beamforming for Compact and Very Low Cost Ultrasound Imaging," *IEEE Trans. Ultrasonics, Ferroelectrics and Frequency Control*, vol. 51, no. 9, pp. 1082-1094, Sep. 2004.

G. B. Ratanpal, R. D. Williams, and T. N. Blalock, "An on-chip signal suppression countermeasure to power analysis attacks," IEEE Transactions on Dependable and Secure Computing, vol. 1, no. 3, pp. 179-189, July-Sep. 2004.

T. N. Blalock, N. B. Gaddis, K. A. Nishimura, and T. A. Knotts, "True Color 1024x768 Microdisplay with Analog In-Pixel Pulse Width Modulation and Retinal Averaging Offset Correction," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 5, pp. 838-845, May 2001.

T. N. Blalock and R. C. Jaeger, "A high speed sensing scheme for 1T dynamic RAMs utilizing the clamped-bit-line sense amplifier," *IEEE Journal of Solid-State Circuits*, vol. SC-27, no. 4, pp. 618-625, April 1992.

T. N. Blalock and R. C. Jaeger, "A high speed clamped-bit-line current-mode sense amplifier," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 4, pp. 542-548, April 1991.

R. C. Jaeger and T. N. Blalock, "Quasi-static RAM design for high performance operation at liquid nitrogen temperature," *Cryogenics*, vol. 30, no. 12, pp. 1030-1035, Dec. 1990.

T. N. Blalock and W. T. Yost, "Detection of fiber damage in a graphite epoxy composite using current injection and magnetic field mapping," *1985 Review of Progress in Quantitative NDE*, June 23-28, 1985, pp. 1207-1213.

**Refereed Conference Proceedings:**

Z.Qi, J.Wang, A.Cabe, S.Wooters, T.Blalock, B.Calhoun,and M.Stan, "Sram-based NBTI/PBTI sensor system design," in Design Automation Conference, 2010. DAC '10. 47th ACM/IEEE, June 2010.

M. I. Fuller, K. Owen, T. N. Blalock, J. A. Hossack, W. F. Walker, "Real time imaging with the Sonic Window: A pocket-sized, C-scan, medical ultrasound device," *Ultrasonics Symposium (IUS), 2009 IEEE International Ultrasonics Symposium* , vol., no., pp.196-199, Sept. 2009.

S. C. Jocke, J. F. Bolus, S. N. Wooters, A. D. Jurik, A. C. Weaver, T. N. Blalock and B. H. Calhoun, "A 2.6-µW Sub-Threshold Mixed-Signal ECG SoC," Proc. of the 2009 VLSI Circuits Sym., June 2009, pp. 60-61.

A. Cabe, Z. Qi, S. Wooters, T. Blalock, and M. Stan, "Small embeddable NBTI sensors (sens) for tracking on-chip performance decay," in Quality of Electronic Design, 2009. ISQED 2009. Quality of Electronic Design, March 2009, pp. 1–6.

A. D. Jurik, J. F. Bolus, A. C. Weaver, B. H. Calhoun, and T. N. Blalock, "Mobile Health Monitoring Through Biotelemetry," International Conference on Body Area Networks (BodyNets), April 2009.

B. H. Calhoun, J. Bolus, S. Khanna, A. D. Jurik, A. F. Weaver, and T. N. Blalock, "Sub-threshold Operation and Cross-Hierarchy Design for Ultra Low Power Wearable Sensors," International Symposium on Circuits and Systems, pp. 1437-1440, May 2009.

B. L. Dell, J. F. Bolus, and T. N. Blalock, "An automated unique tagging system using CMOS process variation," Proceedings of the 17th Great Lakes Symposium on VLSI, March 11-13, 2007.

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