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(12) **United States Patent**  
**Xiang et al.**

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(45) **Date of Patent:** **Aug. 20, 2002**

(54) **SEMICONDUCTOR-ON-INSULATOR  
TRANSISTOR WITH RECESSED SOURCE  
AND DRAIN**

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(\*) **Notice:** Subject to any disclaimer, the term of this  
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U.S.C. 154(b) by 0 days.

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(22) **Filed:** **Aug. 10, 2000**

(51) **Int. Cl.<sup>7</sup>** ..... **H01L 27/01**; H01L 27/12;  
H01L 31/0392

(52) **U.S. Cl.** ..... **257/347**; 257/349; 257/382

(58) **Field of Search** ..... 257/347, 349,  
257/375, 382, 408; 438/149, 479, 517

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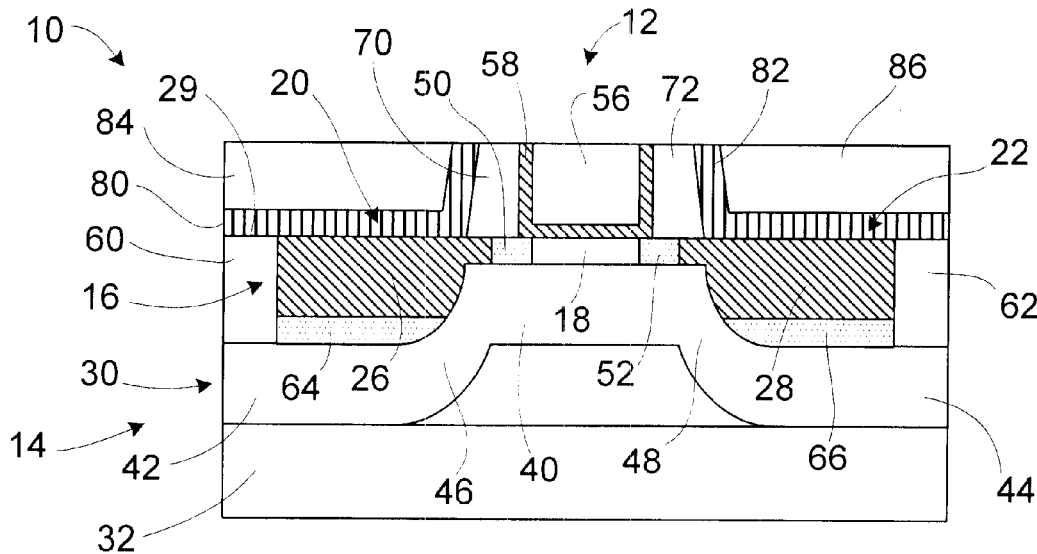
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(57) **ABSTRACT**

A fully-depleted semiconductor-on-insulator (SOI) transistor device has an SOI substrate with a buried insulator layer having a nonuniform depth relative to a top surface of the substrate, the buried insulator layer having a shallow portion closer to the top surface than deep portions of the layer. A gate is formed on a thin semiconductor layer between the top surface and the shallow portion of the insulator layer. Source and drain regions are formed on either side of the gate, the source and drain regions each being atop one of the deep portions of the buried insulator layer. The source and drain regions thereby have a greater thickness than the thin semiconductor layer. Thick silicide regions formed in the source and drain regions have low parasitic resistance. A method of making the transistor device includes forming a dummy gate structure on an SOI substrate, and using the dummy gate structure to control the depth of an implantation to form the nonuniform depth buried insulator layer.

**28 Claims, 5 Drawing Sheets**



**IP Bridge Exhibit 2302**  
**TSMC v. Godo Kaisha IP Bridge 1**

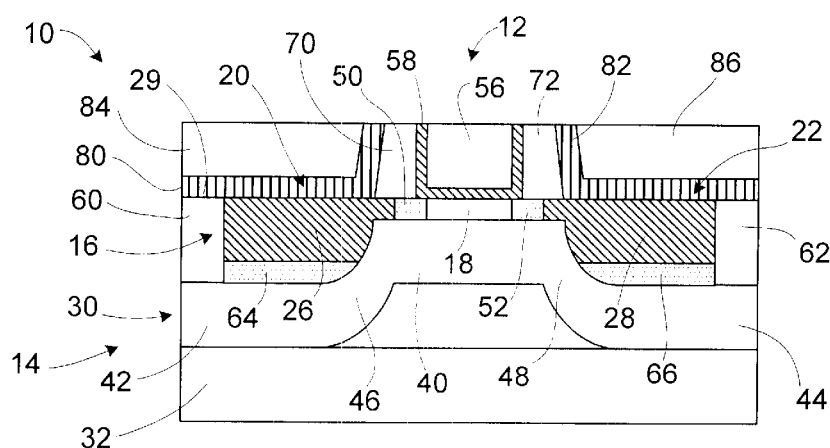


FIG. 1

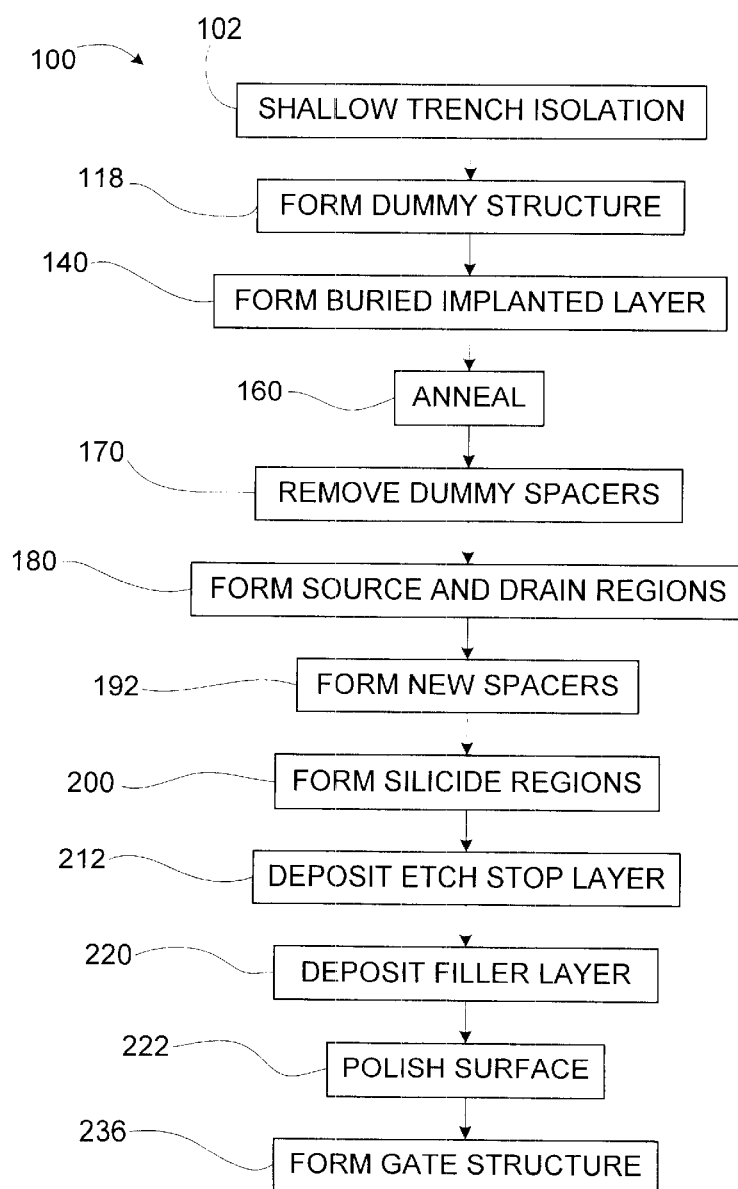


FIG. 2

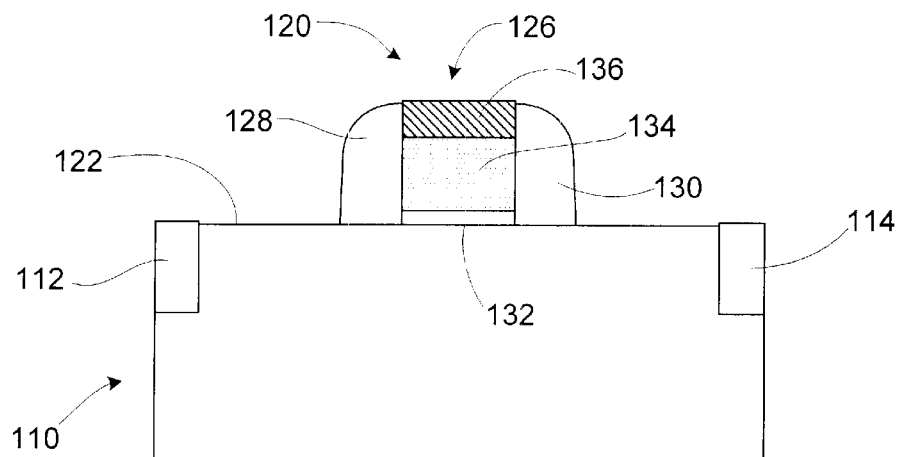


FIG. 3

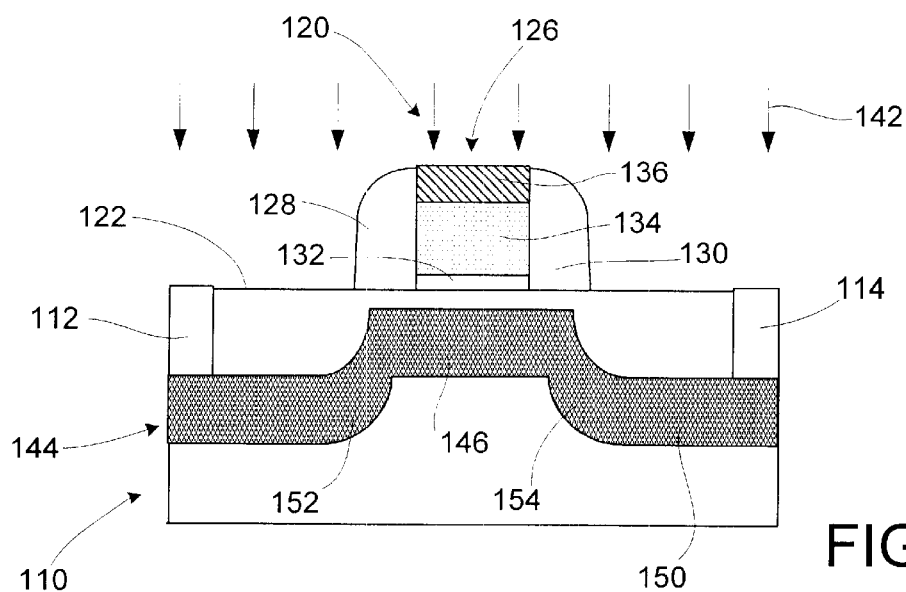


FIG. 4

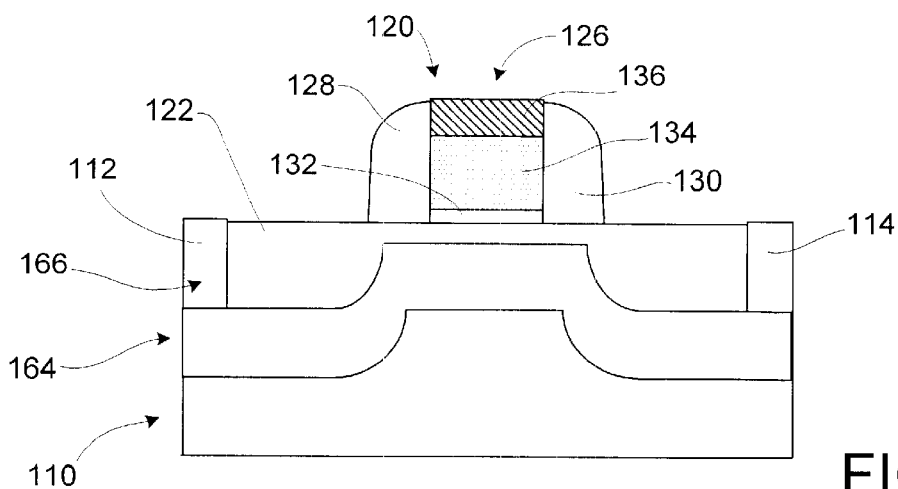


FIG. 5

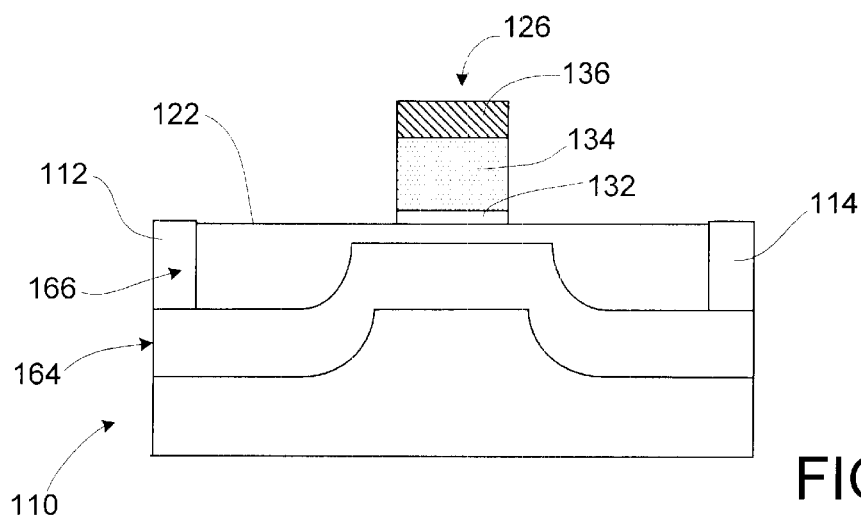


FIG. 6

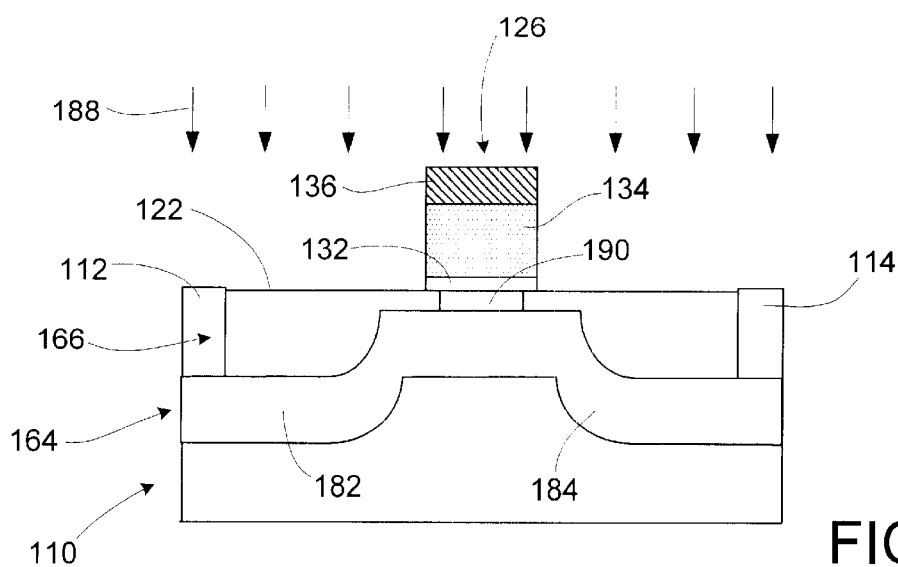


FIG. 7

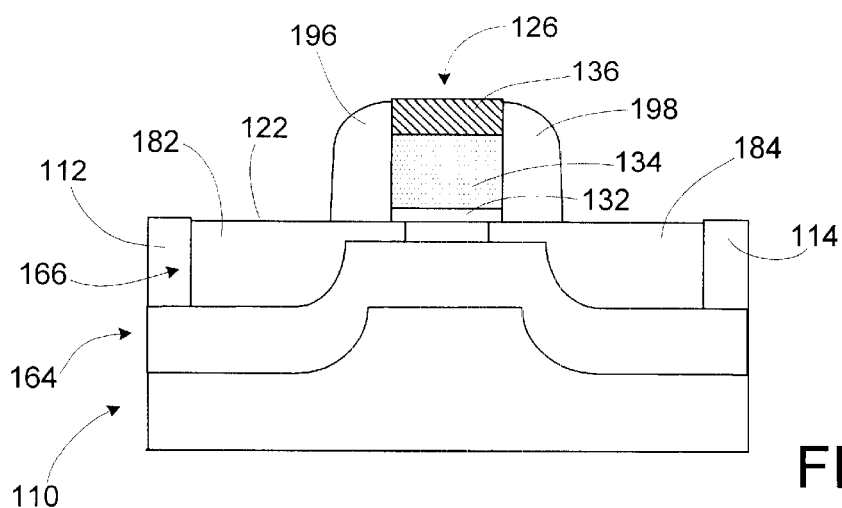


FIG. 8

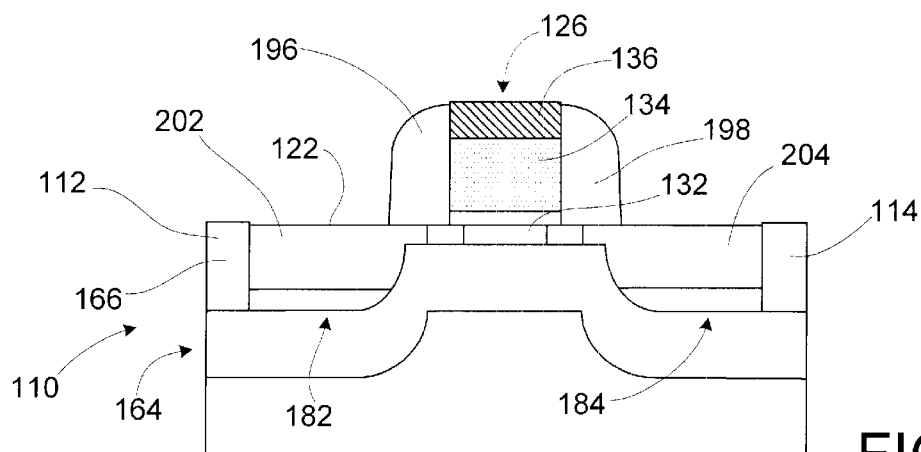


FIG. 9

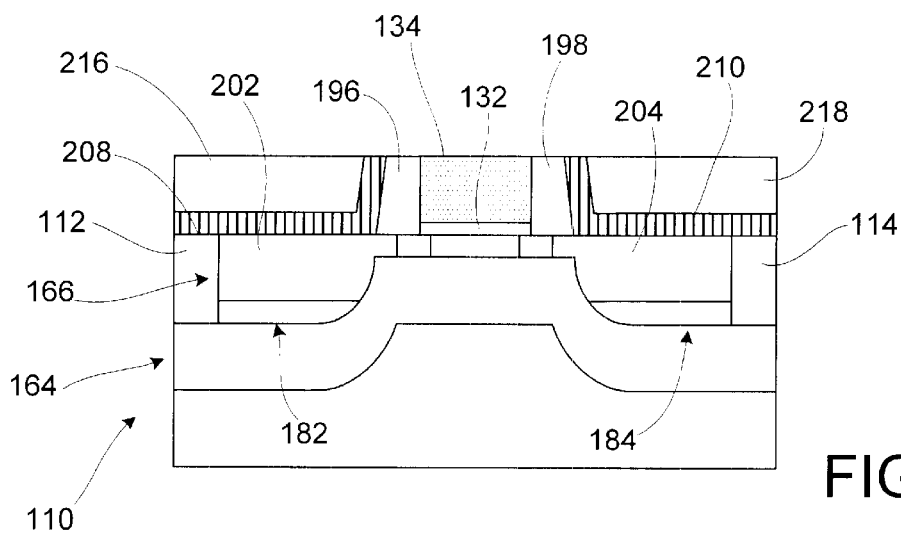


FIG. 10

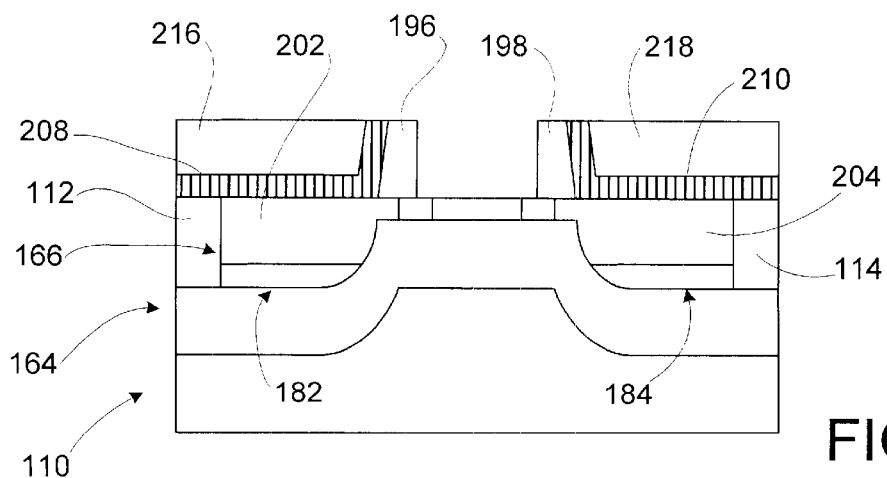


FIG. 11

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