APPLIED PHYSICS REVIEWS

Ultrathin (<4 nm) SiO_2 and Si–O–N gate dielectric layers for silicon microelectronics: Understanding the processing, structure, and physical and electrical limits

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The outstanding properties of SiO_2, which include high resistivity, excellent dielectric strength, a large band gap, a high melting point, and a native, low defect density interface with Si, are in large part responsible for enabling the microelectronics revolution. The Si/SiO_2 interface, which forms the heart of the modern metal–oxide–semiconductor field effect transistor, the building block of the integrated circuit, is arguably the worlds most economically and technologically important materials interface. This article summarizes recent progress and current scientific understanding of ultrathin (<4 nm) SiO_2 and Si–O–N (silicon oxynitride) gate dielectrics on Si based devices. We will emphasize an understanding of the limits of these gate dielectrics, i.e., how their continuously shrinking thickness, dictated by integrated circuit device scaling, results in physical and electrical property changes that impose limits on their usefulness. We observe, in conclusion, that although Si microelectronic devices will be manufactured with SiO_2 and Si–O–N for the foreseeable future, continued scaling of integrated circuit devices, essentially the continued adherence to Moore's law, will necessitate the introduction of an alternate gate dielectric once the SiO_2 gate dielectric thickness approaches ~1.2 nm. It is hoped that this article will prove useful to members of the silicon microelectronics community, newcomers to the gate dielectrics field, practitioners in allied fields, and graduate students. Parts of this article have been adapted from earlier articles by the authors [L. Feldman, E. P. Gusev, and E. Garfunkel, in *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices*, edited by E. Garfunkel, E. P. Gusev, and A. Y. Vul' (Kluwer, Dordrecht, 1998), p. 1 [Ref. 1]; E. P. Gusev, H. C. Lu, E. Garfunkel, T. Gustafsson, and M. Green, IBM J. Res. Dev. **43**, 265 (1999) [Ref. 2]; R. Degraeve, B. Kaczer, and G. Groeseneken, Microelectron. Reliab. **39**, 1445 (1999) [Ref. 3]. [DOI: 10.1063/1.1385803]

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TABLE I. Selected properties of SiO_2 gate dielectric layers.

Native to silicon (SiO_2 is the only stable oxide phase on Si)
Low interfacial (Si/SiO_2) defect density ($\sim 10^{10}\ eV^{-1}\ cm^{-2}$, after H_2 passivation)
Melting point=1713 °C
Energy gap=9 eV
Resistivity $\sim 10^{15}\ \Omega$ cm
Dielectric strength $\sim 1\times 10^7$ V/cm
Dielectric constant=3.9

I. INTRODUCTION AND OVERVIEW

A. SiO_2 enabled the microelectronics revolution

Nature has endowed the silicon microelectronics industry with a wonderful material, SiO_2, as is shown in Table I. SiO_2 is native to Si, and with it forms a low defect density interface. It also has high resistivity, excellent dielectric strength, a large band gap, and a high melting point. These properties of SiO_2 are in large part responsible for enabling the microelectronics revolution. Indeed, other semiconductors such as Ge or GaAs were not selected as the semiconducting material of choice, mainly due to their lack of a stable native oxide and a low defect density interface. The metal–oxide–semiconductor field effect transistor (MOSFET), Fig. 1, is the building block of the integrated circuit. The Si/SiO_2 interface, which forms the heart of the MOSFET gate structure, is arguably the worlds most economically and technologically important materials interface. The ease of fabrication of SiO_2 gate dielectrics and the well passivated Si/SiO_2 interface that results have made this possible. SiO_2 has been and continues to be the gate dielectric par excellence for the MOSFET. Figure 2 is a transmission electron photomicrograph of an actual submicron MOSFET, showing the SiO_2 gate dielectric as well as the Si/SiO_2 interface.

In spite of its many attributes, however, SiO_2 suffers from a relatively low dielectric constant (κ=dielectric constant, or permittivity, relative to air=3.9). Since high gate dielectric capacitance is necessary to produce the required drive currents for submicron devices,[1,4] and further since capacitance is inversely proportional to gate dielectric thickness, the SiO_2 layers have of necessity been scaled to ever thinner dimensions, as is shown in Fig. 3. This gives rise to a number of problems, including impurity penetration through the SiO_2, enhanced scattering of carriers in the

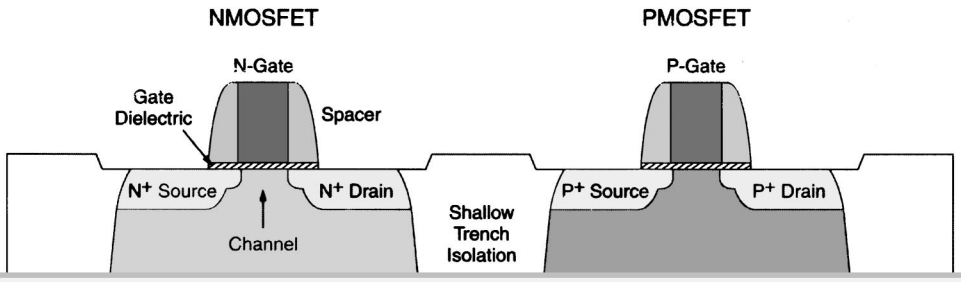


FIG. 1. Schematic illustration of a submicron (channel length) CMOSFET (complementary metal–oxide–semiconductor field effect transistor) (courtesy of C. P. Chang, Agere Systems).

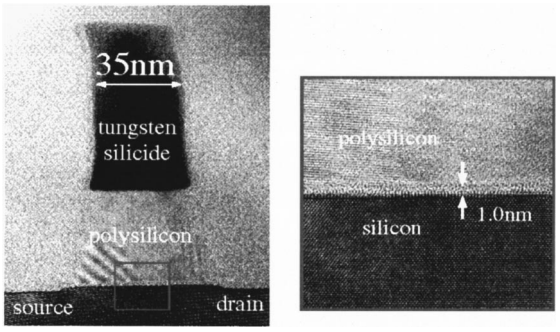
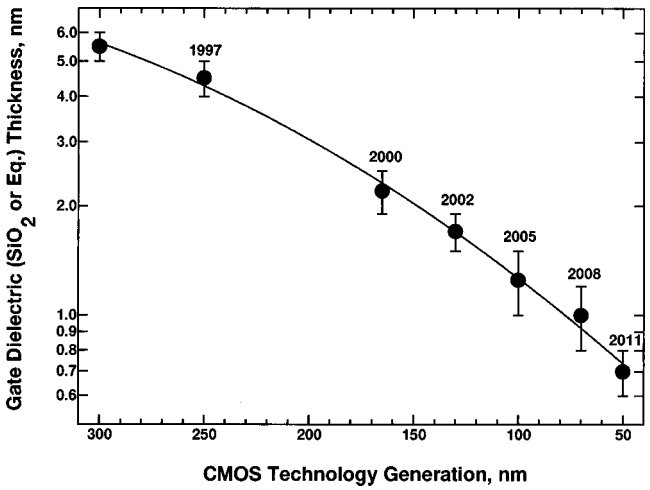


FIG. 2. Cross-section transmission electron photomicrographs of a 35 nm (channel length) transistor, and a detailed view of its 1.0 nm SiO_2 gate dielectric and Si/SiO_2 interface [from Timp *et al.* (Ref. 15)].

channel, possible reliability degradation, high gate leakage current, and the need to grow ultrathin and uniform SiO_2 layers.

This article summarizes recent progress and current scientific understanding of ultrathin (<4 nm) SiO_2 and Si–O–N gate dielectrics on silicon based devices. (Si–O–N will refer to oxynitride dielectrics for which $N/(N+O) \leqslant 0.5$, and most often much less than that.) We will emphasize an understanding of the limits of these gate dielectrics, i.e., how their continuously shrinking thickness, dictated by integrated circuit device scaling, results in physical and electrical property changes that impose limits on their usefulness. We will also discuss the near-future need for alternate gate dielectric materials such as Si_3N_4 and other metal oxides and nitrides, known as "high κ" materials.

In a continuous drive to increase integrated circuit performance through shrinkage of the circuit elements, the dimensions of MOSFETs and other devices have been scaled since the advent of integrated circuits about 40 years ago, according to a trend known as Moore's law.[5–8] Moore's law describes the exponential growth of chip complexity due to decreasing minimum feature size, accompanied by concurrent improvements in circuit speed, memory capacity, and cost per bit. SiO_2 gate dielectrics have decreased in thickness



from hundreds of nanometers (nm) 40 years ago to less than 2 nm today, to maintain the high drive current and gate capacitance required of scaled MOSFETs. Further, as can be seen in Fig. 3, SiO_2 thickness continues to shrink. Many ultrasmall transistors have been reported, with SiO_2 layers as thin as 0.8 nm.[9–15] The International Technology Roadmap for Semiconductors,[16] excerpted in Table II, shows that SiO_2 gate dielectrics of 1 nm or less will be required within 10 years. [It will become obvious while reading this article that SiO_2 layers thinner than ~1.2 nm may not have the insulating properties required of a gate dielectric. Therefore alternate gate dielectric materials, having "equivalent oxide thickness" less than 1.2 nm (for example), may be used. Equivalent oxide thickness, $t_{ox}(\text{eq})$, is the thickness of the SiO_2 layer ($\kappa=3.9$) having the same capacitance as a given thickness of an alternate dielectric layer, t_{diel} ($\kappa=\kappa_{diel}$). Equivalent oxide thickness is given by the relationship: $t_{ox}(\text{eq})=t_{diel}(3.9/\kappa_{diel})$.] At these thicknesses, the Si/SiO_2 interface becomes a more critical, as well as limiting, part of the gate dielectric. A 1 nm SiO_2 layer is mostly interface, with little if any bulk character. It contains about five layers of Si atoms, at least two of which reside at the interface.[17] Given its prominence, much of this article will focus on the physical and electrical properties of the Si/SiO_2 interface.

Due to its commercial relevance, the Si/SiO_2 system has received an enormous amount of scientific attention. It is daunting to count the number of scientific papers: using an INSPEC Database we found 36 708 references (since 1969) devoted to this system. [We intersected the set "silicon" with the set "(SiO or SiO_2 or SiO_x)" and then subtracted the set "quartz."] Only 2% of these references are cited in this article. Several excellent books[18–23] and review papers on dielectric selection,[24] atomic scale interactions between Si and O,[25–27] oxidation of Si,[28–30] SiO_2 structure,[31] interface structure and defects,[32–34] reliability,[35] metrology,[36] Si–O–N,[2,37,38] and general growth, structure and properties[39,40] have been published. However, some basic scientific issues at the forefront of the field remain unresolved. Among these issues are an understanding of the exact diffusion mechanisms and incorporation reactions of oxidizing and nitriding species in SiO_2, an atomistic understanding of the initial stages of oxidation, the role of postoxidation processing on physical and electrical properties, the bonding structure at and near the Si/SiO_2 interface, the relationship between local bonding/chemistry and electrical defects, and the failure mechanisms in ultrathin dielectrics. All of these topics will be addressed in this article.

It is amusing and instructive to learn that not only is SiO_2 enabling to microelectronics, but also to some forms of life itself. Many forms of animal and plant life have cell membranes and exoskeletons composed of pure, crystalline (opaline) SiO_2.[41] This should not be too surprising, since Si and O are the two most abundant elements in the earth's crust. In particular, one celled animals called diatoms fashion their cell membrane via self-assembly (molecule by molecule), from SiO_2 dissolved in H_2O, at ambient temperature.[42] They exist in thousands of symmetric mor-

TABLE II. MOSFET technology timetable, adapted from the International Technology Roadmap for Semiconductors (ITRS) (Ref. 16).

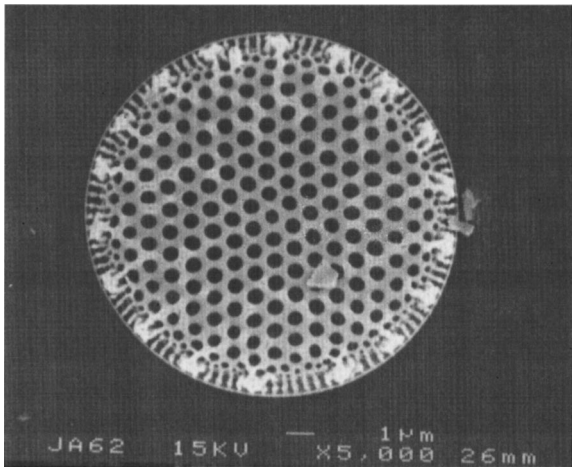
First year of production	1999	2001	2002	2005	2008	2011	2014
DRAM generation	1G	1G	4G	16G	64G	256G	1T
Minimum feature size, nm	180	160	130	100	70	50	35
Equivalent oxide thickness, nm	1.9–2.5	1.5–1.9	1.5–1.9	1.0–1.5	0.8–1.2	0.6–0.8	0.5–0.6

serve SiO_2 features as small as 100 nm. It is humbling to discover that diatoms evolved with such "scaled dimensions" 400 million years ago, and suggests that in the future, SiO_2, as well as other electronic materials structures, might be self-assembled by biomimetic processes. In fact, such structures have already been achieved.[43,44]

B. Fundamental limits of SiO_2: Is the end in sight?

The use of ultrathin SiO_2 gate dielectrics gives rise to a number of problems, including high gate leakage current, reduced drive current, reliability degradation, B penetration, and the need to grow ultrathin and uniform SiO_2 layers. We may ask when any of these effects will fundamentally limit the usefulness of SiO_2 as a gate dielectric.[45]

Due to the large band gap of SiO_2, ~9 eV, and the low density of traps and defects in the bulk of the material, the carrier current passing through the dielectric layer is normally very low. For ultrathin films this is no longer the case. When the physical thickness between the gate electrode and doped Si substrate becomes thinner than ~3 nm, direct tunneling through the dielectric barrier dominates leakage current.[11,40,46–48] According to fundamental quantum-mechanical laws, the tunneling current increases exponentially with decreasing oxide thickness. Gate leakage currents measured on 35 nm transistors fabricated using advanced wafer preparation, cleaning, and oxidation procedures[14] are shown in Fig. 5. The leakage current is seen to increase by one order of magnitude for each 0.2 nm thickness decrease.



Assuming a maximum allowable gate current density of 1 A/cm^2 for desktop computer applications, and 10^{-3} A/cm^2 for portable applications, minimum acceptable SiO_2 thicknesses (physical) would be approximately 1.3 and 1.9 nm, respectively.

Recent electron energy loss spectroscopy (EELS) experiments on ultrathin Si/SiO_2 interfaces, in a scanning transmission electron microscope (STEM), support these findings.[17] Oxygen profiles across the interface were obtained and are shown in Fig. 6 for SiO_2 films 1.0 and 1.8 nm thick. The profiles consist of bulk-like regions and interfacial regions, and the interfacial regions are thought to be due to interfacial states. Based on this analysis, it has been calculated that the minimum oxide thickness, before leakage current becomes overwhelming, is 1.2 nm. This comes from the fact that a satisfactory SiO_2 tunnel barrier is formed when it is equal in thickness to six times the decay length of the interfacial states, about 6×0.12 nm$\cong$0.7 nm, plus a 0.5 nm contribution from interfacial roughness.

Reduced drive (drain) current has been reported in small transistors with ultrathin gate dielectrics.[10] Figure 7 shows that drain current increases with decreasing SiO_2 thickness, but then falls off; gate leakage current continuously increases, as expected, with decreasing SiO_2 thickness. Thus for SiO_2 layers thinner than about 1.3 nm there is no advan-

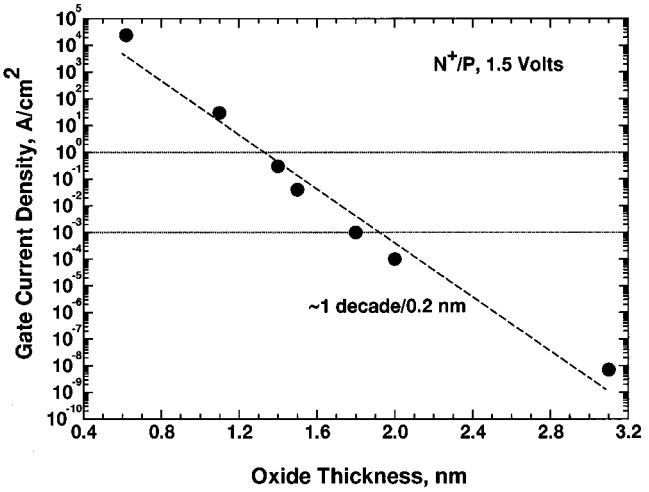


FIG. 5. Gate leakage current measured at 1.5 V as a function of oxide thickness (measured by TEM) for 35 nm NMOSFETs. Leakage current increases one order of magnitude for every 0.2 nm decrease in SiO_2 thickness.

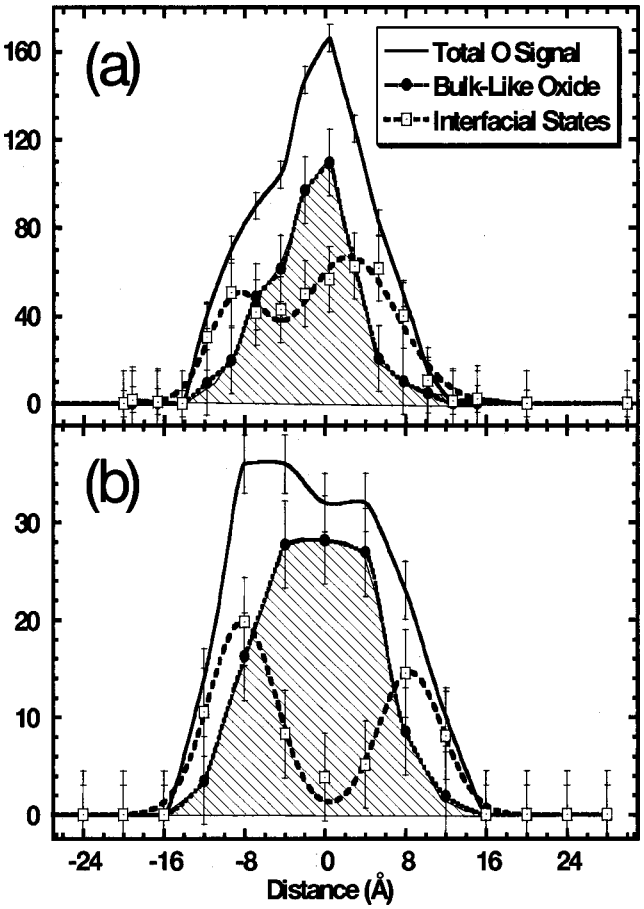


FIG. 6. Oxygen bonding profiles measured by STEM-EELS. The Si substrate is on the left and the gate polycrystalline Si is on the right. (a) 1.0 nm (ellipsometric) oxide, annealed at 1050 °C/10 s. The bulk-like O signal (y axis, arbitrary scale) yields a FWHM of 0.85 nm, whereas the total O signal yields a FWHM of 1.3 nm. The overlap of the two interfacial regions has been correlated with the observation of a very high gate leakage current, 10^2 A/cm^2. (b) a thicker (1.8 nm ellipsometric) oxide, also annealed. The interfacial regions no longer overlap and the gate leakage current is 10^{-5} A/cm^2 [from Muller *et al.* (Ref. 17)].

tage in performance (drive current) for incurring the burden of an ever-increasing gate leakage current. This would suggest that SiO_2 layers thinner than 1.3 nm no longer deliver any performance advantage. The cause of the decreased

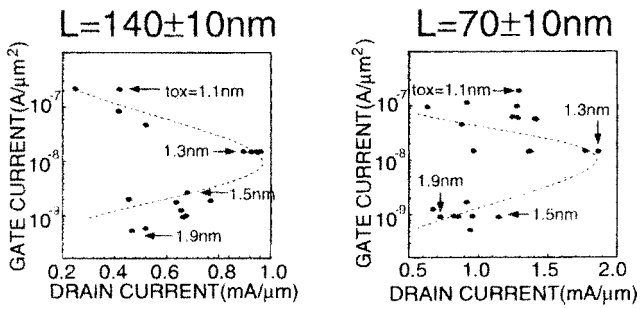


FIG. 7. Drive current vs leakage current for two ultrasmall (gate lengths of 70 and 140 nm) NMOSFETs. In both cases it can be seen that gate current increases, as is expected, with decreasing SiO_2 thickness. However, drain

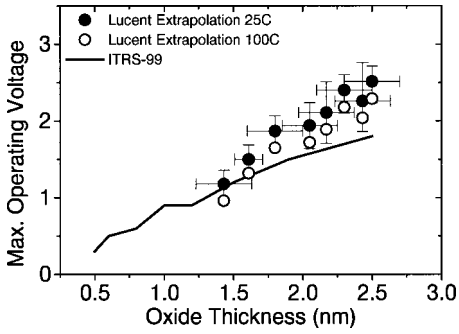


FIG. 8. Predicted maximum allowable operating voltage as a function of oxide thickness (Ref. 16) (solid line), modeled so that requirements of power dissipation and circuit speed for successive technology generations are met. The Lucent data, at either 25 or 100 °C, estimates the safe operating voltages (for 10 year lifetime reliability) for sub-2.5 nm oxides, based on measured results and extrapolation principles (Ref. 62). The Lucent data clearly show that the 10 year reliability of sub-2.5 nm oxides meets the ITRS specifications for SiO_2 layers as thin as 1.4 nm.

drive current is not fully understood. One possibility is an additional scattering component from the upper (SiO_2/polycrystalline Si gate) interface. Some experimental evidence exists for this case[49] but the observed effect is not enough to explain the data in Fig. 7. Another cause could be a universal mobility curve effect, i.e., lowered mobility due to enhanced scattering because of extreme carrier confinement in the inversion layer of the ultrathin oxide. The issue of long-range electrostatic interactions between charges in very heavily doped gate, source, and drain regions, and electrons traveling in the channel, was recently theoretically studied[50] using both semiclassical two-dimensional self-consistent Monte Carlo–Poisson simulations and a quantum mechanical model based on electron scattering from gate–oxide interface phonons. It was shown that excitation and absorption of plasma modes in the gate region may result in a net momentum loss of carriers in the channel, thus decreasing their velocity, and leading to reduced drain current.

Reliability (lifetime to breakdown) of ultrathin SiO_2 is a major concern for oxide scaling into the sub-2 nm range and currently a contentious issue.[35,40,51–62] Electrons traveling through the SiO_2 layer may create defects such as electron traps and interface states[63–65] that in turn, upon accumulation to some critical density, degrade the insulating properties of the oxide. The accumulated charge the film can withstand before its breakdown (Q_{bd}) decreases with oxide thickness.[54] Recently, it was predicted that oxide films thinner than about 2.2 nm would not have the reliability required by the industry roadmap.[54] Data from another research group,[62] shown in Fig. 8, indicates that acceptable reliability will be achievable for SiO_2 thicknesses as low as 1.4 nm. At about 1.0 nm thickness, the statistical probability of a percolation path may reduce reliability to an unacceptable level.[66] One should mention that all reliability data is model dependent. Unlike directly measured parameters such as the gate leakage and drive currents, reliability studies always involve extrapolations from relatively high (~2.5–4 V) stress voltages to real device operating voltages (~1.0–1.2 V). The extrapolations

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