PROCEEDINGS OF THE SYMPOSIUM ON

SILICON NITRIDE AND SILICON DIOXIDE THIN INSULATING FILMS

Editors

M. Jamal Deen
Simon Fraser University
Burnaby, BC, Canada

William D. Brown
University of Arkansas
Fayetteville, Arkansas, USA

Kalpathy B. Sundaram
University of Central Florida
Orlando, Florida, USA

Stanley I. Raider
IBM T. J. Watson Research Center
Yorktown Heights, New York, USA

DIELECTRIC SCIENCE AND TECHNOLOGY AND ELECTRONICS DIVISIONS

Proceedings Volume 97-10

THE ELECTROCHEMICAL SOCIETY, INC.,
10 South Main St., Pennington, NJ 08534-2896

TSMC 1325

Find authenticated court documents without watermarks at docketalarm.com.

TK7872
.T55S95
1997

Copyright 1997 by The Electrochemical Society, Inc.
All rights reserved.

This book has been registered with Copyright Clearance Center, Inc.
For further information, please contact the Copyright Clearance Center,
Salem, Massachusetts.

Published by:

The Electrochemical Society, Inc.
10 South Main Street
Pennington, New Jersey 08534-2896, USA

Telephone (609) 737-1902
Fax (609) 737-2743
e-mail: ecs@electrochem.org
Web site: http://www.electrochem.org

ISBN 1-56677-137-4

Printed in the United States of America

Find authenticated court documents without watermarks at docketalarm.com.

This material may be protected by Copyright law (Title 17 U.S. Code)

FABRICATION OF METAL INSULATOR FIELD EFFECT TRANSISTORS USING SILICON NITRIDE AND SILICON-OXYNITRIDE AS GATE INSULATORS

K. B. Sundaram and S. S. Seshan
Department of Electrical and Computer Engineering
University of Central Florida
Orlando, FL 32816-2450

Silicon nitride and silicon-oxynitride films were used as the gate dielectrics for the fabrication of metal insulator semiconductor field effect transistors. The dielectric films were deposited by an r. f. magnetron sputtering techniques using silicon nitride target. The fabrication process of an enhancement type n-channel device is discussed in detail. The electrical measurement done for the devices indicated low threshold voltages

INTRODUCTION

There is significant interest in high dielectric constant gate insulators for ultra scale integrated circuits. The gate dielectric materials used in MOSFET devices determine the threshold voltage (V_T) and the mode of operation of the device. Certain applications require not only low value of V_T, but also a precisely controlled value to match other devices in the circuit. New gate insulating materials for MOSFET devices are looked into get low V_T, better transconductance (g_m), and high break down voltages. Higher dielectric constant of the gate insulator yields higher gate capacitance (C_{ox}) which may affect the speed of the device. Even though higher C_{ox} affects the speed of the MOS device, it is advantageous A higher dielectric constant yields high gate dielectric capacitance (C_{ox}) which affects the speed of the device. Even though higher C_{ox} affects the speed of the MOS device, it is advantageous for applications like storage capacitors in the dynamic random access memory devices.[1] Potential high dielectric constant insulators for MOSFET devices are tantalum pentoxide (Ta_2O_5)[2], silicon nitride and silicon-oxynitride [3-7], cerium dioxide (CeO_2) [8], and zirconium oxide (ZrO_2) [9]. Silicon nitride films are used in non-volatile memory devices which utilizes the phenomenon of charge storage in the trap centers in the nitride films.[10] Threshold voltage control by the variation of the dielectrics and thickness of the dielectric, play an important role in the write and read cycle of the memory cell.[10]

In most cases, the stacked layers of silicon nitride and oxy-nitride were deposited by chemical vapor deposition (CVD) and plasma enhanced chemical vapor deposition (PECVD). The CVD deposited films have high hydrogen concentration coming from the source gas SiH_4. High hydrogen content (in the rage of 20-30 atomic per cent) has been reported to be responsible for degrading MOSFET device lifetimes, particularly with

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

shorter channel lengths.[11] Hydrogen contamination also induces some problems, such as the electrical passivation of the dopants of silicon and shifting V_T of MOSFETs, due to hot-electron trappings in the gate oxide.[12] The electron heating effects in silicon nitride and silicon oxy-nitride films were studied by DiMaria and Abernathey.[7] According to them, the average electron energy as a function of electric field is very similar to that of SiO_2, and the total number of electrons which can be heated to energies greater than 2 eV is greatly reduced owing to the increased trap centers in the nitride films compared with SiO_2. The reduction of hot electrons die to increased trapping is correlated to increasing N_2 content through the oxy-nitride phase of SiO_2. The traps keep the carriers near the bottom of the conduction band. This makes silicon nitride and oxy-nitride very attractive for gate dielectrics in the case of short and narrow channels that are adversely affected by hot carrier generation due to high electric fields. Hence in order to eliminate the hydrogen contamination in the films, in this present work, sputter deposited silicon nitride and oxy-nitride films were used as the gate insulators. The fabrication process of n-channel metal-insulator field effect transistors is discussed and device characteristics are studied.

EXPERIMENTAL

Two types of mask patterns, as shown in Fig. 1, were used for the fabrication of metal insulator field effect transistors. The minimum feature size was 5μm. The mask contained patterns of gate lengths of 5, 10, and 20 μm. The process steps involved in the fabrication of the devices are shown in Fig. 2. The substrates were p-Si with resistivity 8 Ω-cm of (100) orientation. The wafers were cleaned with boiling in tricholroethane, acetone, methanol, deionized water (DI) and then dipped in boiling 1:1 H_2SO_4: H_2O_2 for 3 minutes. Subsequently the wafers were etched with buffered oxide etch (BOE) (13 NH_4F: 2 HF) 9:1 diluted with water for 1 min. Finally, the wafers were washed with DI water and blown dry with nitrogen.

Field oxide of 450 nm was grown by a wet oxidation process. This thick oxide served as a mask for subsequent phosphorus diffusion. Waycoat HNR 120 negative photoresist (PR) was used for the first level clear field mask-1 to form the source and drain windows (Fig. 2a and 2b). Phosphorus diffusion was completed by 5 min. predeposition followed by 20 min. drive-in diffusions (Fig. 2c) The wafers were coated with Shipley 1400 positive PR. Clear field mask-2 was used to define SiN gate regions (Fig. 2d). Silicon nitride was sputter deposited in an r. f. sputtering system using a Si_3N_4 powder pressed target of 99.95% purity (Angstrom Sciences) (Fig. 2e). The sputtering conditions are given in the Table I. Oxygen was added during sputtering to deposit silicon oxynitride films. Using a negative photoresist and mask-3 the contact windows for source and drain windows were opened (Fig. 2f). Diluted buffered oxide etch (BOE) was used to etch silicon nitride and oxy-nitride films (Fig. 2g). Aluminum film was evaporated in a vacuum system (Fig. 2h). Using Shipley 1400 positive PR and clear field mask-4, metal patterning was completed (Fig. 2i). Finally, Al was etched using diluted

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

phosphoric acid at 60 °C and metal contacts were made to source, drain and gate regions Fig. 2j)

The device measurements were initially made on unannealed wafers and later measurements were made on the annealed wafers. The post annealing was performed to anneal out the interface charges and traps in the dielectric. It was carried out in an argon ambient at 350 °C for one hour. The SiN film thickness was measured using an optical interferometer. The C-V measurements of the MIS capacitors were performed using the Hewlett Packard impedance analyzer (Model HP 4192A LF). The MOS device characteristics were measured using Hewlett Packard semiconductor parametric analyzer (Model HP 4145B). The parameter analyzer was programmed to give the I_D versus V_{DS} and $(I_D)^{1/2}$ versus V_{GS} curves

RESULTS

The thickness of the dielectric films ranged from 75-150 nm depending on the deposition conditions as described in the Table-I. The dielectric breakdown strength was the film was of the order of $2x10^5$ V/cm. The measured dielectric constant ranged from 4.0 - 5.94 for the films. Figures 3 and 4 show the typical I_D versus V_{DS} characteristics of 10 and 20 μm gate length devices. Owing to a minor misalignment during the fabrication process, the gate electrode overlapping the diffused region is slightly offset and hence the drain current was slightly smaller than the expected value. Figure 5 shows $I_D^{1/2}$ versus V_{GS} of a 20 μm device. This device showed the lowest V_T of nearly -0.57 V. Some devices showed more negative V_T. A reduction in the V_T values was observed when the devices were annealed. Further, an increase in drain current was also observed for the annealed devices. A similar trend was observed by Hezel et al. for the post annealed nitride films deposited by chemical vapor deposited films.[13] Figure 6 and 7 show the typical I_D versus V_{DS} and $I_D^{1/2}$ versus V_{GS} characteristics of 10 μm gate silicon-oxynitride device respectively. The device showed a V_T of nearly 0.22 V. The smaller devices had a smaller drain current compared with larger devices, as evident from the MISFET characteristics.

Figure 8 shows the calculated V_T versus gate dielectric thickness for various interface charge densities for silicon nitride. The doping concentration of the p-Si is assumed as in the experimental case. All the calculations were based on a dielectric constant of 5.94 which was the maximum value in the studies. It can be seen that the V_T variation is high for higher interface charge density compared with lower charges. If speed is not the main criteria, then silicon nitride or silicon oxynitride may be used to reduce the threshold voltage of the devices.

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.

WHAT WILL YOU BUILD? | sales@docketalarm.com | 1-866-77-FASTCASE

fastcase® Smarter legal research.