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Deshpande et al.

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(54) **METHOD OF FABRICATING SiO₂ SPACERS AND ANNEALING CAPS**

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(51) **Int. Cl.⁷** **H01L 29/76**

(52) **U.S. Cl.** **257/333; 257/346; 257/387; 257/340; 257/412; 257/388; 438/585**

(58) **Field of Search** **257/333, 346, 257/387, 388, 340, 900, 412; 438/585**

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Primary Examiner—Nathan J. Flynn

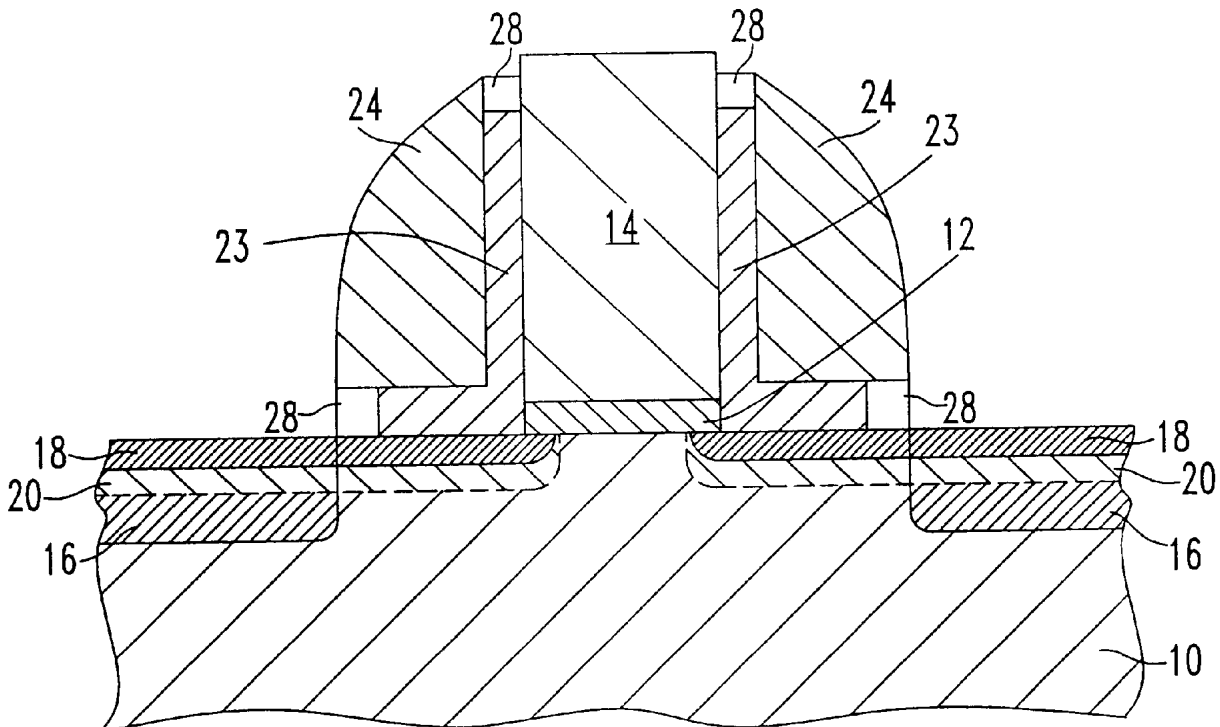
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(57) **ABSTRACT**

Divot fill methods of incorporating thin SiO₂ spacer and/or annealing caps into a complementary metal oxide semiconductor (CMOS) processing flow are provided. In accordance with the present invention, the divot fill processes provide a means for protecting the exposed surfaces of the thin SiO₂ spacer and/or annealing cap such that those surfaces are not capable of being attacked by a subsequent silicide pre-cleaning step. CMOS devices including thin SiO₂ spacer and/or annealing caps whose surfaces are protected such that those surfaces are not capable of being attacked by a subsequent silicide pre-cleaning or other process steps are also provided.

24 Claims, 7 Drawing Sheets



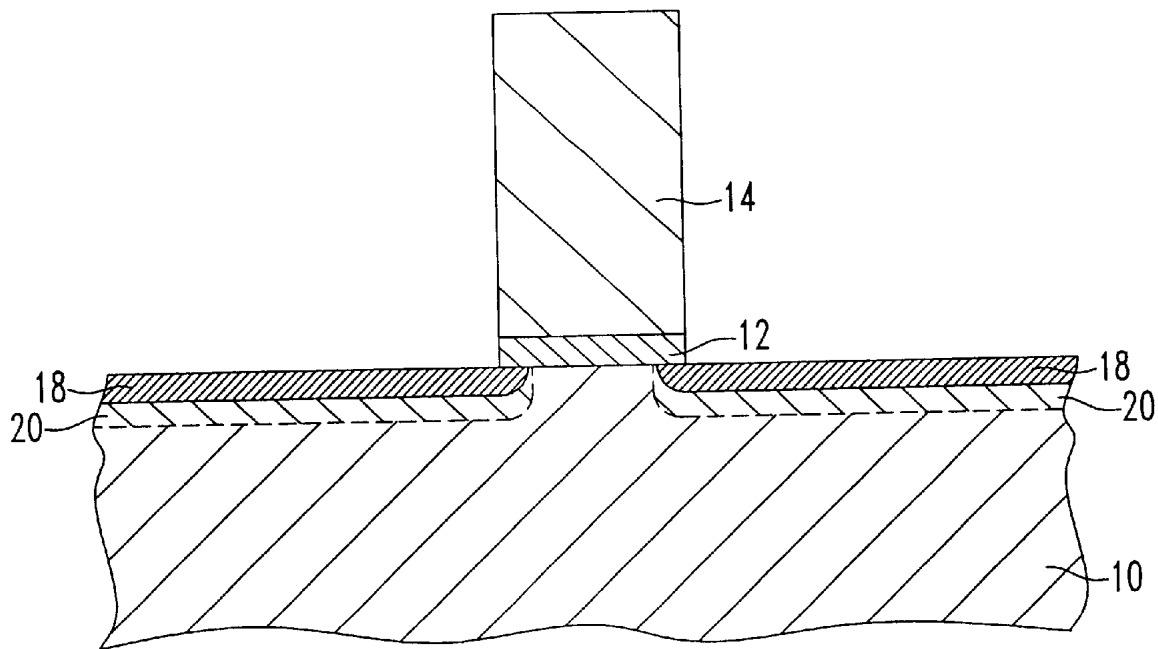


FIG. 1A

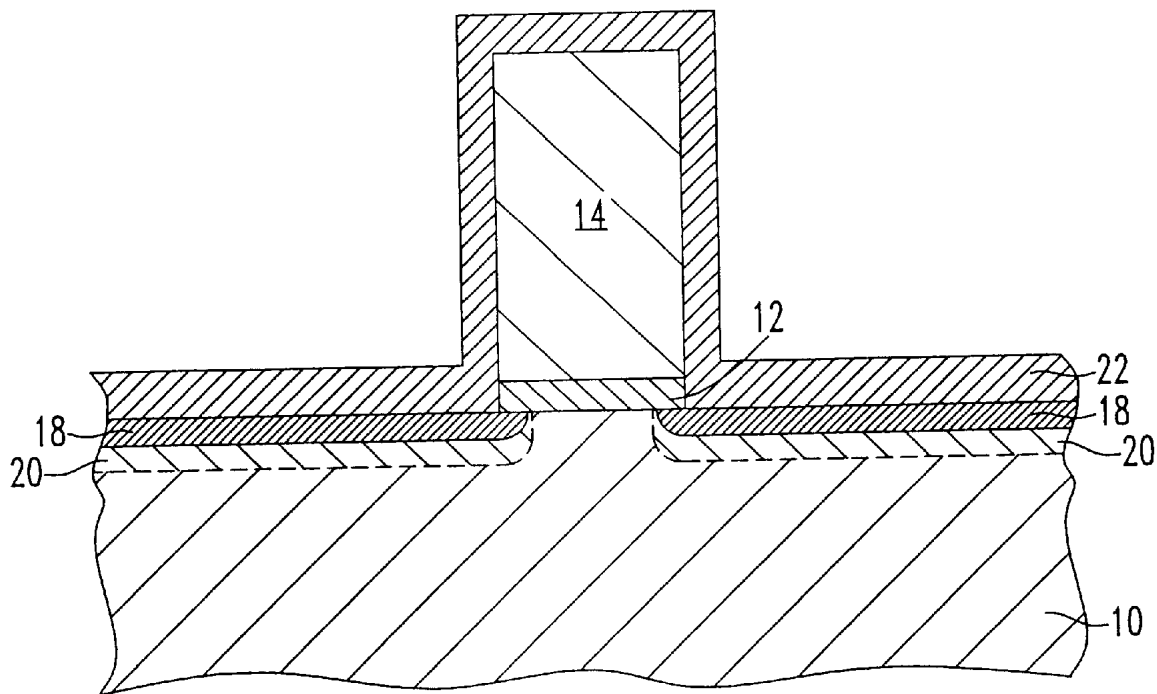


FIG. 1B

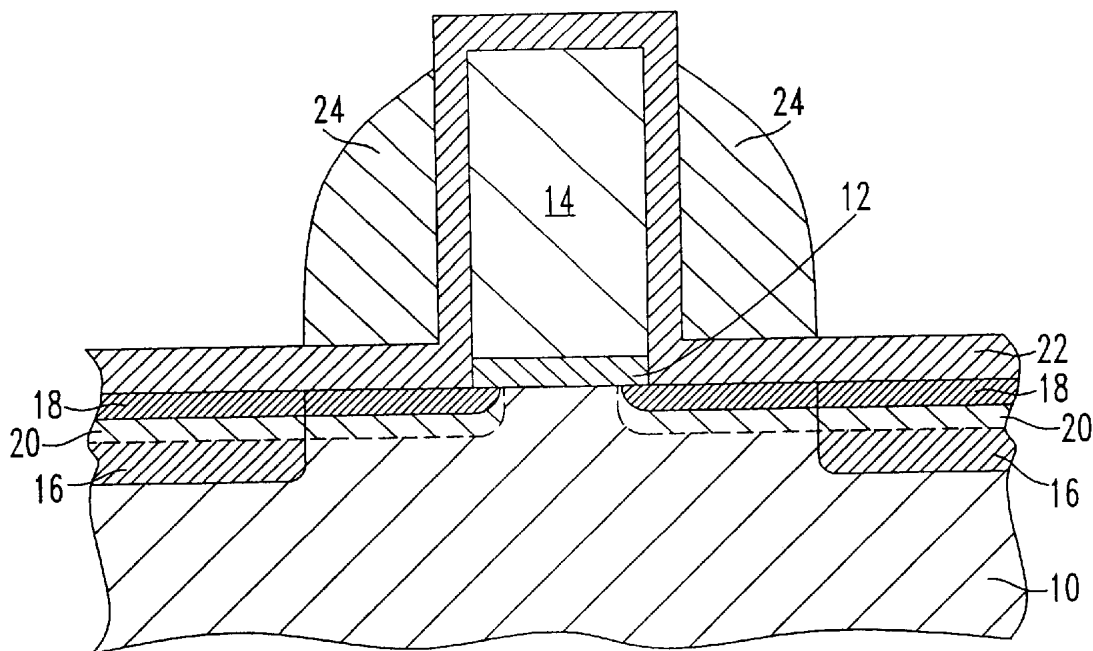


FIG. 1C

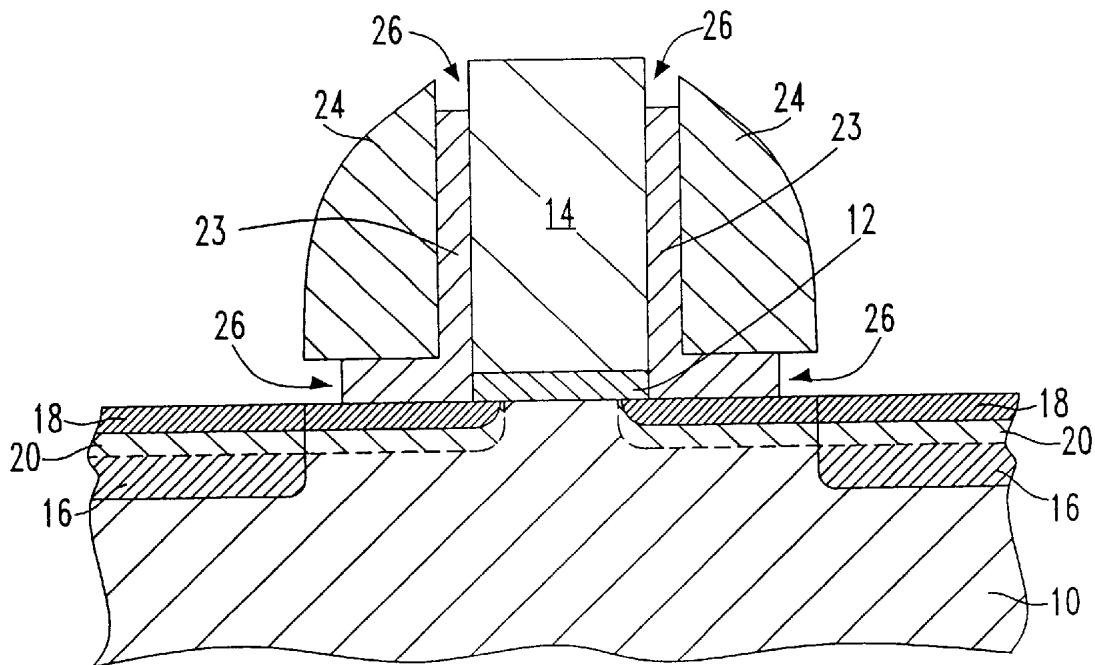


FIG. 1D

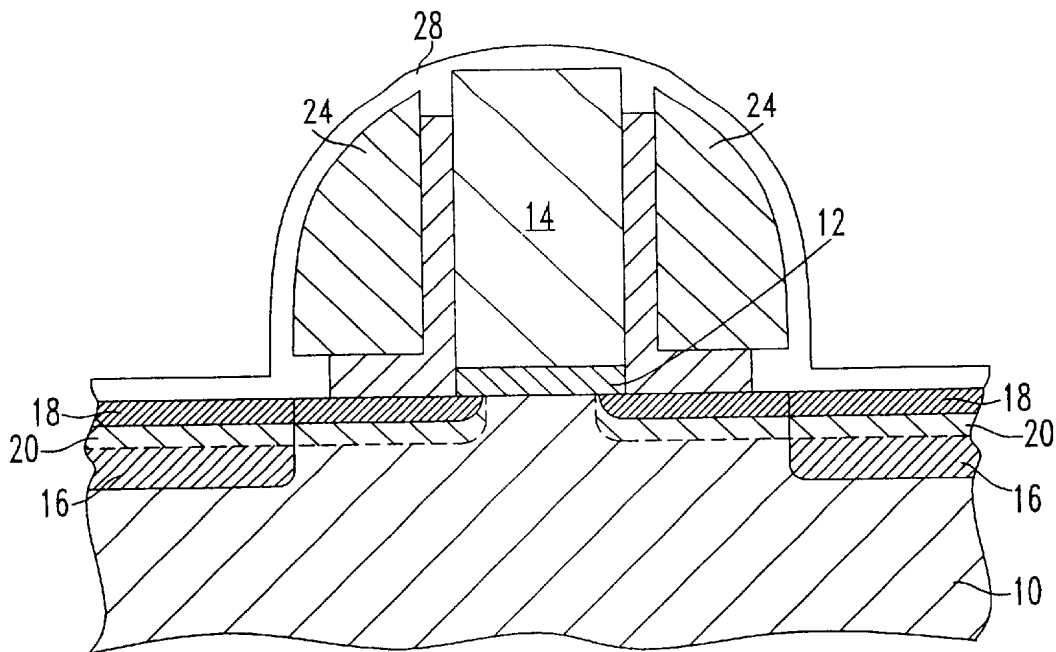


FIG. 1E

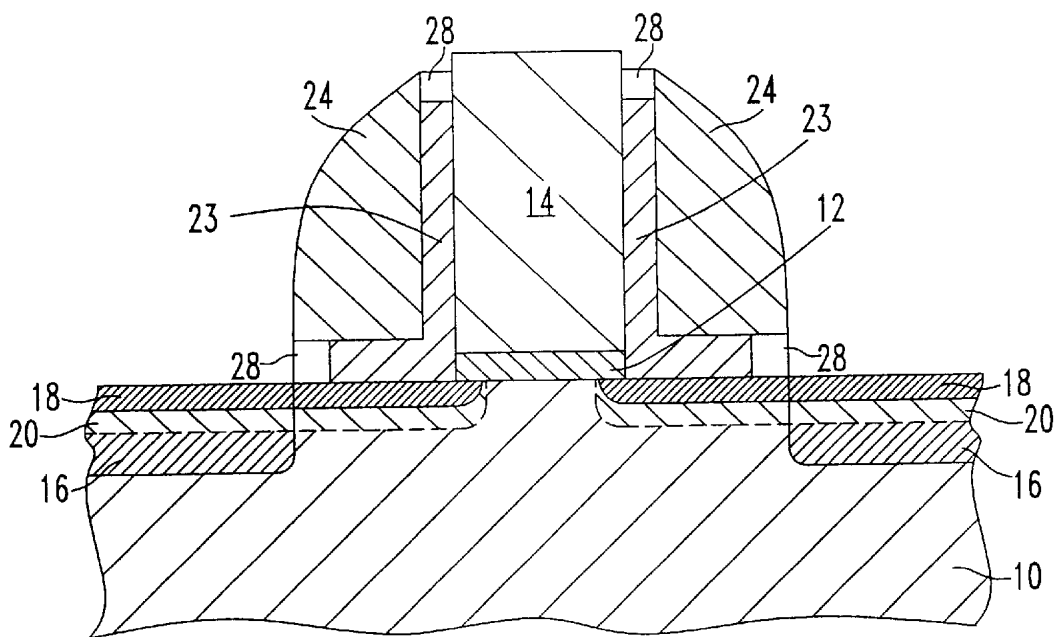


FIG. 1F

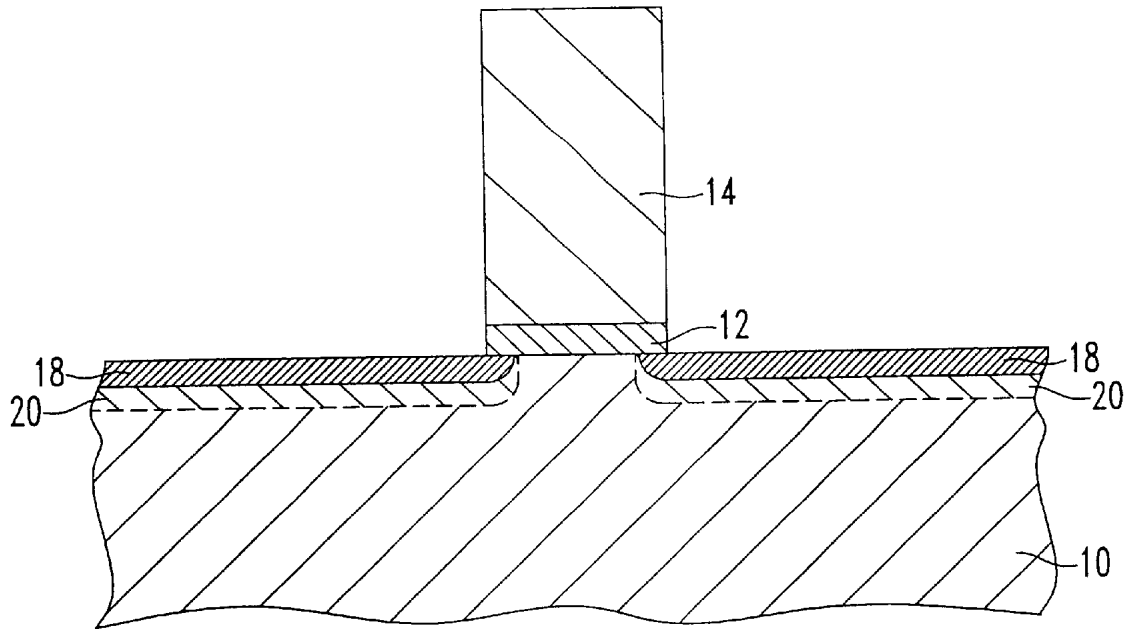


FIG. 2A

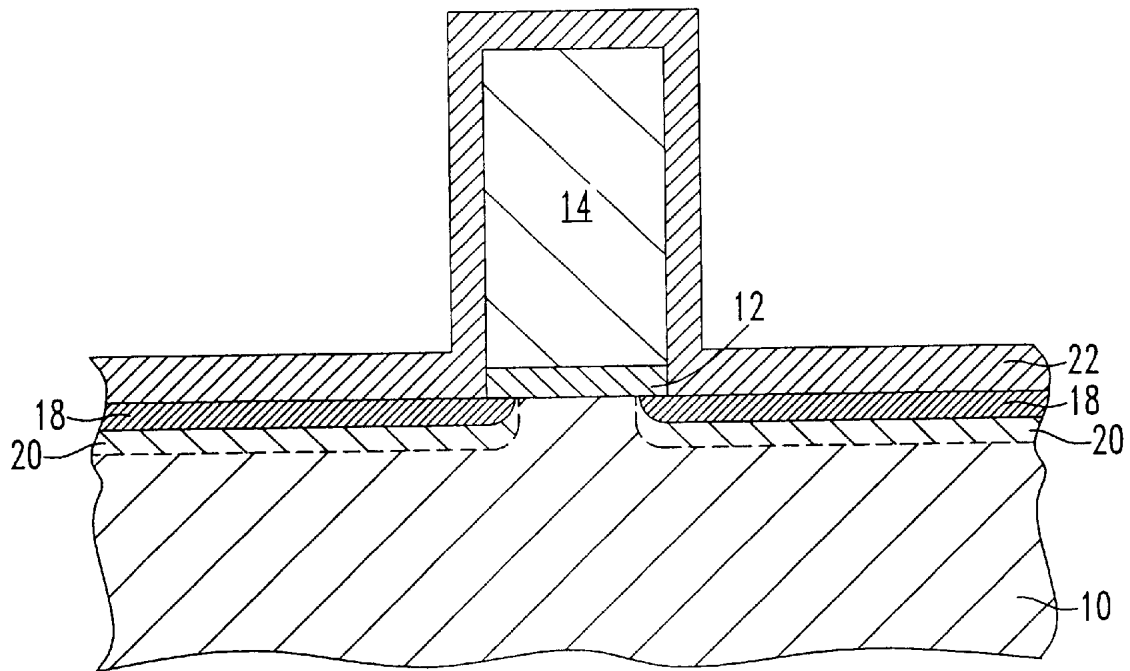


FIG. 2B

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