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Chien et al.

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[54] **PLANARIZATION METHOD FOR SELF-ALIGNED CONTACT PROCESS**

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[30] **Foreign Application Priority Data**

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[51] **Int. Cl.**[7] **H01L 21/44**

[52] **U.S. Cl.** **438/675**; 438/631; 438/697; 438/699; 438/700; 438/702; 438/760; 438/740; 438/959

[58] **Field of Search** 438/700, 702, 438/760, 740, 631, 697, 699, 959, 675

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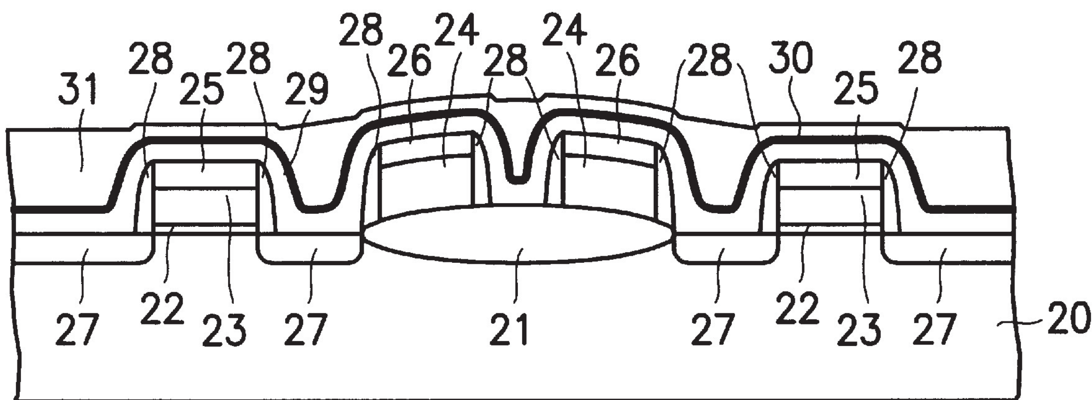
[57] **ABSTRACT**

A planarization method for self-aligned contact process which is suitable for use in DRAM processing. Prior to the formation of the bottom terminal layer of the capacitor, the substrate surface is first planarized, thus avoiding stringer effects and related bridging problems arising from an undulating surface profile, during subsequent etching of the defined pattern. Also according to the method of this invention, by covering the silicon substrate that has MOS transistors laid on top with first a deposition of an oxide layer, then an etch discriminatory layer, and finally a planarization layer, a substrate with a smooth, plane surface is obtained.

27 Claims, 3 Drawing Sheets



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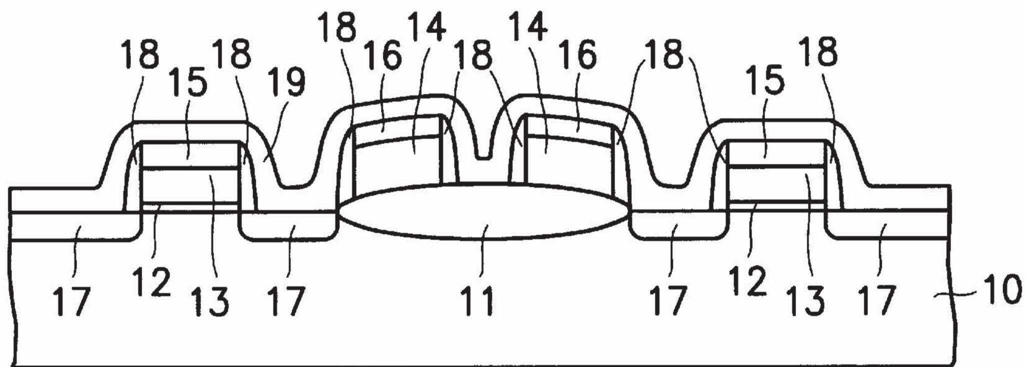

FIG. 1A (PRIOR ART)

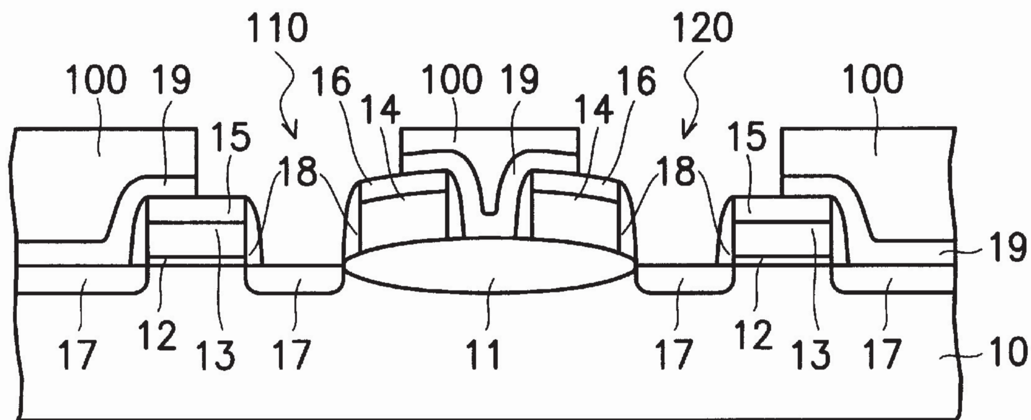

FIG. 1B (PRIOR ART)

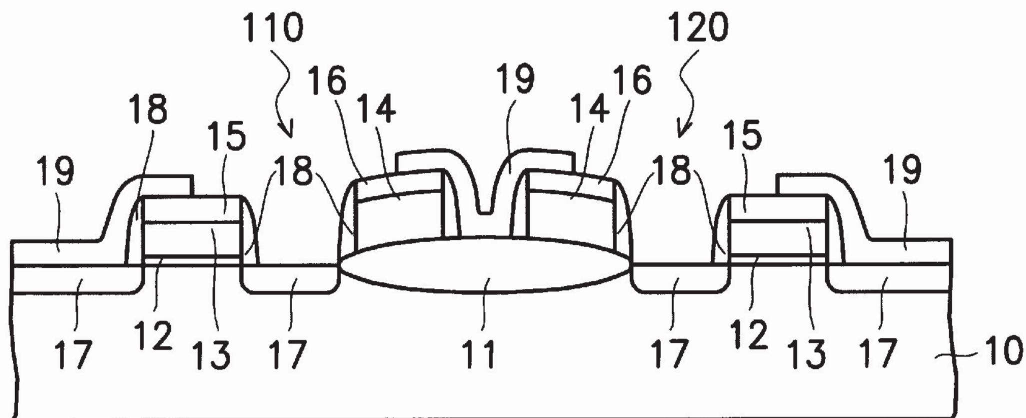

FIG. 1C (PRIOR ART)

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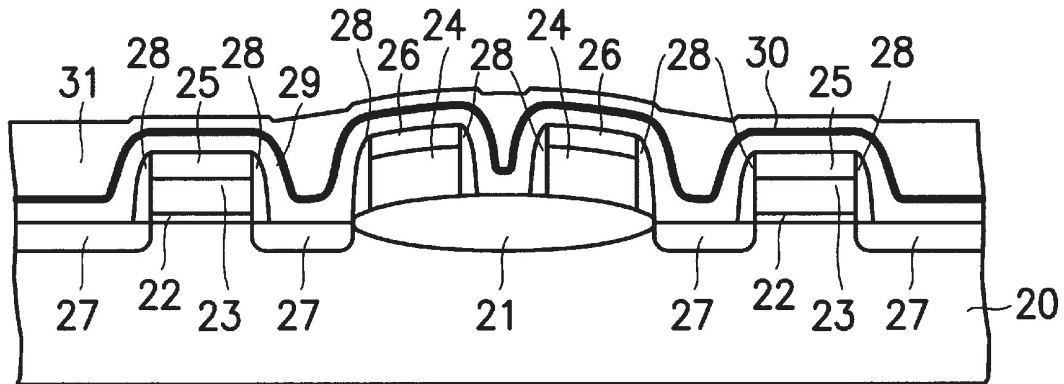

FIG. 2A

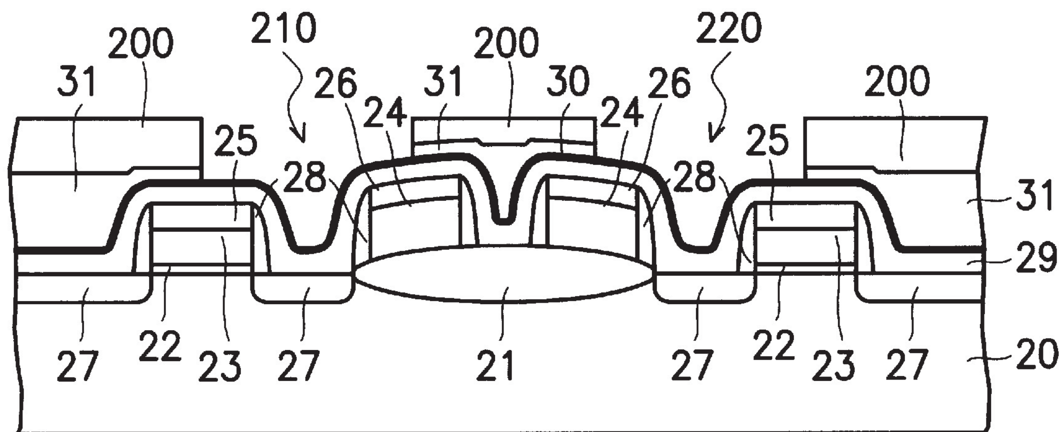

FIG. 2B

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FIG. 2C

FIG. 2D

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PLANARIZATION METHOD FOR SELF-ALIGNED CONTACT PROCESS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates in general to techniques for manufacturing memory integrated circuits, and more particularly to a planarization method for a self-aligned contact process which can avoid stringer effects that may result in bridging phenomena.

2. Description of the Related Art

A conventional DRAM manufacturing process makes use of a technique called self-aligned contact to reduce the layout area of memory components. FIG. 1A to **1**C are cross-sectional views showing how, in conventional processing, the definition of a contact window in a self-aligned contact process is carried out. A DRAM component generally consists of a MOS transistor which acts as a switching element, and a capacitor which acts as a charge storage device. Both of these elements are fabricated on a silicon substrate **10**. As shown in the drawings, a field oxide layer **11** acts as an insulating structure between separate memory components. A gate dielectric layer **12** is produced by thermal oxidation of the surface of silicon substrate **10** and the gate and the connecting wires, labelled as **13** and **14** respectively, are formed by etching away the same heavily implanted polysilicon layer. Capping oxide layer elements **15** and **16** separately cover the surfaces of the gate **13** and connecting wires **14**, respectively. The capping oxide layers **15** and **16** are produced by thermal oxidation of the surface of the polysilicon layer. Source/drain terminals **17** are formed by the implantation of impurities in the silicon substrate **10**. Sidewall spacers **18** are laid on opposite sidewalls of the gates **13** and connecting wires **14**.

First, as shown in FIG. **1**A, a layer of oxide **19** covering the whole surface of the substrate **10** is formed by deposition. Due to the unevenness of the base substrate layer, the surface of the oxide layer **19** also has an undulating profile. Next, a layer of photoresist material **100** is coated on the oxide layer **19**, and by a photolithographic technique, the pattern for the contact windows is defined, providing two openings **110** and **120** as shown in FIG. **1**B. Then, using the photoresist layer **100** as a mask, the oxide layer **19** is etched to expose the desired contacts to the source/drain terminals **17**. Thereafter, the photoresist layer **100** is removed, thereby obtaining the cross-sectional configuration shown in FIG. **1**C. Then, the capacitor of the DRAM component may be formed precisely at the points where the contact windows **110** and **120** are situated. Some of the basic steps in the capacitor formation process include first structurally forming the bottom terminal layer of the capacitor, followed by forming the dielectric layer on top of the bottom terminal layer, and then finally forming the top terminal layer on top of the dielectric layer.

Since in the conventional manufacturing process there is no prior planarization treatment before the stage where the bottom terminal layer of the capacitor is formed, generally the substrate surface undulates. This undulation is especially pronounced for regions such as the narrow groove between two connecting wires **14**. Therefore it is easy, when etching the defined polysilicon layer to form the top and bottom terminal layers of the capacitor, to pick up stringer effects which lead to bridging phenomena. The conventional method for avoiding such stringer effects is to lengthen the etching time. However, this measure will reduce production efficiency. Further, if an additional flushing step is included in the etching process to avoid stringer effects, the reactive gases used, such as Cl and SF, will diminish the capacitor area.

SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a planarization method for self-aligned contact processes, so that just before the bottom terminal layer of the capacitor is defined, the substrate surface is first planarized, thus avoiding the stringer problem in subsequent processes.

To achieve the object mentioned above, a planarization method is provided for a self-aligned contact process, that is suitable for a silicon substrate with a MOS transistor already formed on a rough and uneven surface. The planarization method for self-aligned contact processes includes the first step of forming an oxide layer along the substrate surface. An etch discriminatory layer is then formed along the oxide layer surface and a planarization layer is formed above the etch discriminatory layer. The uneven surface is then filled to create a smooth plane surface and a contact window mask is formed above the planarization layer. Using the contact window mask as a cover, the planarization layer, the etch discriminatory layer, and the oxide layer are sequentially etched. The source/drain terminals of the MOS transistor are then exposed.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features, and advantages of the invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The description is made with reference to the accompanying drawings in which:

FIGS. **1**A to **1**C are cross-sectional views showing the process steps of the conventional self-aligned contact process for defining the contact windows, and

FIGS. **2**A to **2**D are cross-sectional views showing the preferred process steps according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGS. **2**A to **2**D are cross-sectional views illustrating the preferred process steps according to the invention. Because a DRAM component includes a MOS transistor as a switching element, usually the MOS transistor is formed above a silicon substrate **20**. Referring to FIGS. **2**A to **2**D, the field oxide layer **21** is formed by performing local oxidation of silicon (LOCOS) applied to the silicon substrate **20**, and the field oxide layer **21** acts as an insulating structure between adjacent memory components. The gate dielectric layer **22** is formed by thermal oxidation of the surface of the silicon substrate **20**. The gate **23** is composed of polysilicon material and is formed above the gate dielectric layer **22**. Connecting wires **24** are also composed of polysilicon material and are formed together with the gate **23** when etching the same polysilicon layer. Capping oxide layer elements **25** and **26** separately cover the surfaces of gate **23** and connecting wires **24**, respectively. The capping oxide layer is formed by thermal oxidation of the polysilicon surface. Source/drain terminals **27** are formed by doping impurities into the silicon substrate **20**, and can have either a lightly doped drain (LDD) structure or a double diffusion drain (DDD) structure. Sidewall spacers **28** are placed at opposite sidewalls of the gate **23** and connecting wires **24**.

First, as shown in FIG. **2**A, a layer of oxide **29** is deposited covering the entire substrate surface, to a thick-

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