Docket No.: 079195-0566 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Masafumi TSUTSUI, et al.	:	Confirmation Number: 1644
Application No.: 12/170,191	:	Group Art Unit: 2814
Filed: July 09, 2008	:	Examiner: Howard Weiss

For: SEMICONDUCTOR DEVICE INCLUDING MISFET HAVING INTERNAL STRESS FILM (as amended)

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated May 10, 2010, wherein a three-month shortened statutory period for response is set to expire on August 10, 2010, Applicants respectfully request reconsideration of the above-identified application in view of the following amendments and remarks.

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IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application

Listing of Claims

1-14. (Cancelled)

15. (Currently Amended) A semiconductor device, comprising a MISFET, wherein the MISFET includes:

an active region made of a semiconductor substrate;

a gate insulating film formed on the active region;

a gate electrode formed on the gate insulating film;

source/drain regions formed in regions of the active region located on both sides of the gate electrode; and

a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein:

the silicon nitride film is not formed on an upper surface of the gate electrode, and

~~the gate insulating film is formed only under a lower surface of the gate electrode, and~~

~~the source/drain regions include lightly doped impurity regions formed in regions of the active region located on both sides of the gate electrode, and heavily doped impurity regions formed in regions of the active region respectively extending outwardly from the lightly doped impurity regions to be in contact with the lightly doped impurity regions and having a higher impurity concentration than that of the lightly doped impurity regions~~

the gate electrode protrudes upward from a surface level of parts of the silicon nitride film located at both side surfaces of the gate electrode.

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16. (Previously presented) The semiconductor device of claim 15, wherein

the silicon nitride film is for generating a stress in a substantially parallel direction to the gate length direction in a channel region located in the active region under the gate electrode.

17. (Previously presented) The semiconductor device of claim 16, wherein

the substantially parallel direction of the stress includes a direction tilted by an angle of less than 10 degree from a direction in which carriers move.

18. (Previously presented) The semiconductor device of claim 15, wherein

the silicon nitride film is directly in contact with the source/drain regions,

19. (Previously presented) The semiconductor device of claim 15, wherein

the silicon nitride film is formed above the source/drain regions with a thin film interposed therebetween.

20. (Currently amended) The semiconductor device of claim 15, wherein

the source/drain regions include lightly doped impurity regions formed in regions of the active region located on both sides of the gate electrode, heavily doped impurity regions formed in regions of the active region respectively extending outwardly from the lightly doped impurity regions to be in contact with the lightly doped impurity regions and having a higher impurity concentration than that of the lightly doped impurity regions, and a silicide layer.

21. (Currently amended) The semiconductor device of claim 15, further comprising:

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a sidewall formed on the side surface of the gate electrode, wherein

the silicon nitride film is formed over the side surfaces of the gate electrode with the sidewall interposed between the silicon nitride film and the side surface of the gate electrode.

22. (Previously presented) The semiconductor device of claim 15, wherein

a principal surface of the semiconductor substrate is substantially a {100} plane, and

the gate length direction of the gate electrode is substantially a <011> direction.

23. (Previously presented) The semiconductor device of claim 15, further comprising:

an interlevel insulating film formed on the silicon nitride film; and

a contact plug provided so as to pass through the interlevel insulating film and the silicon nitride film and to be connected to the source/drain regions.

24. (Currently amended) The semiconductor device of claim 15, wherein:

the active region is divided by an isolation region formed in the semiconductor substrate, and

the silicon nitride film is formed to extend over the isolation region as well as the source/drain regions.

25. (Previously presented) The semiconductor device of claim 15, wherein

the gate insulating film is a silicon oxide film.

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26. (Previously presented) The semiconductor device of claim 15, wherein the gate insulating film is a silicon oxynitride film.

27. (Previously presented) The semiconductor device of claim 15, wherein the gate electrode has a polysilicon film.

28. (Previously presented) The semiconductor device of claim 15, wherein the gate electrode has a metal film.

29. (Previously presented) The semiconductor device of claim 15, wherein the silicon nitride film is provided so as to cover at least part of at least one of the source/drain regions.

30. (Previously presented) The semiconductor device of claim 15, wherein the silicon nitride film covers at least respective parts of the source/drain regions.

31. (Previously presented) The semiconductor device of claim 15, wherein the silicon nitride film covers at least respective parts of both side surfaces of the gate electrode.

32. (Previously presented) The semiconductor device of claim 15, wherein the MISFET is an nMISFET and the source/drain regions are n-type source/drain regions.

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