Request for Continued Examination (RCE) Transmittal

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Application Number	12/170,191
Filing Date	July 9, 2008
First Named Inventor	Masafumi TSUTSUI, et al.
Art Unit	2814
Examiner Name	Howard Weiss
Attorney Docket Number	079195-0566

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Education (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

      ii. ☐ Other _____

   b. ☒ Enclosed

      i. ☒ Amendment/Reply

      ii. ☐ Affidavit(s)/Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. Miscellaneous

   a. ☐ Suspension of action of the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 500417. I have enclosed a duplicate copy of this sheet.

      i. ☒ RCE fee required under 37 CFR 1.17(e) $810

      ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☐ Other _____

   b. ☐ Check in the amount of $_____ enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature		Date	March 29, 2010
Name (Print/Type)	Takashi Saito	Limited Recognition No.	L0123

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

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This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Docket No.: 079195-0566 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Masafumi TSUTSUI, et al.	:	Confirmation Number: 1644
Application No.: 12/170,191	:	Group Art Unit: 2814
Filed: July 09, 2008	:	Examiner: Howard Weiss

For: SEMICONDUCTOR DEVICE INCLUDING MISFET HAVING INTERNAL STRESS FILM (as amended)

AMENDMENT ACCOMPANYING RCE

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated December 31, 2009, wherein a three-month shortened statutory period for response is set to expire on March 31, 2010, Applicants respectfully request reconsideration of the above-identified application in view of the following amendments and remarks. A Request for Continued Examination is being filed concurrently herewith.

AMENDMENTS TO THE CLAIMS:

A listing of the claims presented in this patent application appears below. This listing replaces all prior versions and listing of claims in this patent application.

1-14. (Cancelled)

15. (Currently Amended) A semiconductor device, comprising a MISFET, wherein

the MISFET includes:

an active region made of a semiconductor substrate;

a gate insulating film formed on the active region;

a gate electrode formed on the gate insulating film;

source/drain regions formed in regions of the active region located on both sides of the gate electrode; and

a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein

the silicon nitride film is not formed on an upper surface of the gate electrode, [[and]]

the gate insulating film is formed only under a lower surface of the gate electrode, and

the source/drain regions include lightly doped impurity regions formed in regions of the active region located on both sides of the gate electrode, and heavily doped impurity regions formed in regions of the active region respectively extending outwardly from the lightly doped impurity regions to be in contact with the lightly doped impurity regions and having a higher impurity concentration than that of the lightly doped impurity regions.

16. (Previously Presented) The semiconductor device of claim 15, wherein

the silicon nitride film is for generating a stress in a substantially parallel direction to the gate length direction in a channel region located in the active region under the gate electrode.

17. (Previously Presented) The semiconductor device of claim 16, wherein

the substantially parallel direction of the stress includes a direction tilted by an angle of less than 10 degree from a direction in which carriers move.

18. (Previously Presented) The semiconductor device of claim 15, wherein

the silicon nitride film is directly in contact with the source/drain regions,

19. (Previously Presented) The semiconductor device of claim 15, wherein

the silicon nitride film is formed above the source/drain regions with a thin film interposed therebetween.

20. (Currently Amended) The semiconductor device of claim 15, wherein

the source/drain regions include ~~a lightly doped impurity region, a heavily doped impurity region and~~ a silicide layer.

21. (Previously Presented) The semiconductor device of claim 15, further comprising:

a sidewall formed on the side surface of the gate electrode.

22. (Previously Presented) The semiconductor device of claim 15, wherein

a principal surface of the semiconductor substrate is substantially a {100} plane, and

the gate length direction of the gate electrode is substantially a <011> direction.

23. (Previously Presented) The semiconductor device of claim 15, further comprising:

an interlevel insulating film formed on the silicon nitride film; and

a contact plug provided so as to pass through the interlevel insulating film and the silicon nitride film and to be connected to the source/drain regions.

24. (Previously Presented) The semiconductor device of claim 15, wherein

the active region is divided by an isolation region formed in the semiconductor substrate.

25. (Previously Presented) The semiconductor device of claim 15, wherein

the gate insulating film is a silicon oxide film.

26. (Previously Presented) The semiconductor device of claim 15, wherein

the gate insulating film is a silicon oxynitride film.

27. (Previously Presented) The semiconductor device of claim 15, wherein

the gate electrode has a polysilicon film.

28. (Previously Presented) The semiconductor device of claim 15, wherein

the gate electrode has a metal film.

29. (Previously Presented) The semiconductor device of claim 15, wherein

the silicon nitride film is provided so as to cover at least part of at least one of the source/drain regions.

30. (Previously Presented) The semiconductor device of claim 15, wherein

the silicon nitride film covers at least respective parts of the source/drain regions.

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