Reduced Hot-Electron Effects in MOSFET's with an Optimized LDD Structure

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Abstract—A comparison of device degradation due to hot-electron injection is made for conventional MOSFET's and lightly doped drain (LDD) structures. The studies indicate that, for an optimized LDD structure, critical device parameters, such as threshold voltage, transconductance, and linear and saturated current drives, show significantly reduced degradation when subjected to accelerated life testing. These results imply long-term stability for LDD devices used in VLSI circuits.

I. INTRODUCTION

INCREASED scaling of feature sizes in VLSI circuits is introducing new concerns about long-term circuit reliability and the degradation of transistor characteristics due to hot-electron injection has been given much attention in recent years.

Many process modifications have been suggested to either reduce the peak electric field in the drain region or to move the region of peak electric field away, from underneath the gate electrode. Such devices are generally known as having lightly doped drains (LDD's). Intuitively, one would expect transistors having an LDD structure to be less susceptible to hot-electron injection, thereby, offering improved long-term reliability. However, little data has been published on the stability of these devices, and it was recently reported that certain LDD structures may actually degrade at a faster rate than conventional MOSFET's [1].

In this letter, we report the results obtained on our optimized LDD structure which show reduced hot-electron trapping effects. When these results are compared to those obtained from a conventional device of similar channel length, we find that the optimized LDD structure offers much improved long-term stability for reliable circuit applications.

II. DEVICE FABRICATION

Both the conventional and LDD devices were fabricated in identical manners except for the inclusion of a "reach through implant" and a 450-nm spacer oxide in the case of the latter. This LDD structure, the details of which we reported in an earlier paper [2], has a gate oxide of 40 nm and an upper electrode consisting of a polysilicon/silicide stack. For the LDD device, the sheet-charge concentration for the n-region was typically 1E13-1E14 cm^{-2}. In both structures a protective overcoat of LPCVD oxide was employed. The use of the oxide avoids instabilities introduced by hydrogen trapped in LPCVD nitride films.

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The effective channel lengths of both devices were determined by using an array of transistors varying in channel lengths and with a width of 25 μm. By plotting $1/\beta$ (gain) versus L design, we were able to extract the electrical length reduction for both LDD and conventional transistors. The data in this letter is for devices of similar L effective and not L design. A previous paper [2] has described a method for determining the effective series resistance of the n-regions in the LDD devices. The threshold voltage values in this study were obtained by solving the linear drain current equation for V_T, β, and θ, where β is the device gain and θ is the mobility degradation.

III. RESULTS AND DISCUSSIONS

The maximum injection of hot carriers into the gate oxide occurs when the substrate current is at a maximum. This maximum occurs with approximately 3 V applied to the gate. For drain voltages ($\geqslant$5 V), the peak is quite broad and relatively insensitive to small changes in V_g. Due to the nature of its structure for any given drain voltage, the maximum substrate current is always less for an LDD device compared with a conventional transistor [2], [4]. In order to eliminate the effect of differing substrate currents, both types of transistors were stressed at the same substrate-current level. This required an applied drain stress voltage of 7 V for the conventional device and 8 V for the LDD device. In reality this means that stressing of the LDD transistor is much more severe than in circuit operation.

We show the measured transconductance (gm) degradation of conventional and LDD devices in Fig. 1, both before and after stress. The gm degradation for the conventional device is significantly larger at low gate voltages. This primarily indicates mobility degradation due to the generated interface charges at the drain junction and the associated surface scattering [3]. The LDD device, due to the graded drain structure, has very little gm degradation, even at higher gate voltages. Therefore, the sharp series resistance increase, as attributed to the localized interface charge generation by Hsu and Grinolds [1], is not observed here. Analysis of the I-V data on this device showed that the total series resistance in the linear region was approximately constant at 1200 $\Omega\cdot\mu$m before and after stress. In other experiments, some LDD devices did exhibit a slight increase (5-10 percent) in the total series resistance after stress but this was not enough to cause significant degradation. Additionally, for the conventional device there is a slight parallel shift of the gm curve with stress, indicating a shift in threshold voltage due to trapped charges. This was confirmed by V_T measurements. The conventional device also

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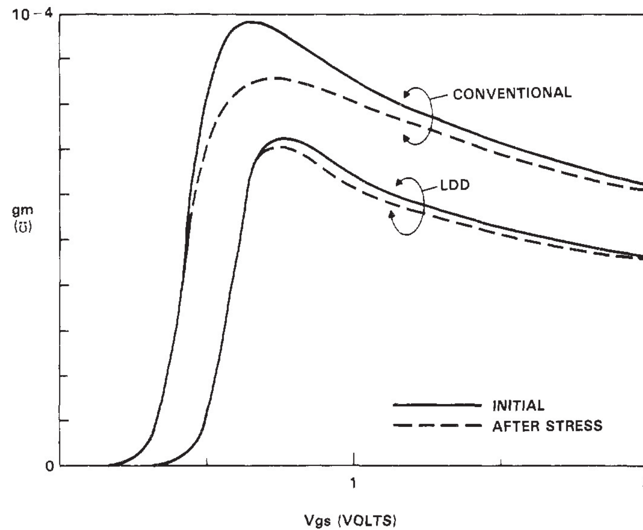

Fig. 1. Transconductance degradation for conventional and LDD devices (measured at V_{DS} = 100 mV) after stressing at peak substrate current for 20 h.

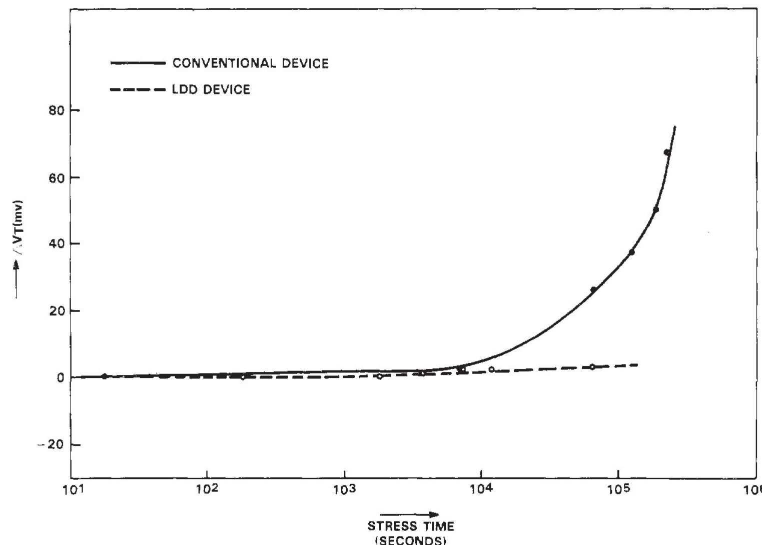

Fig. 2. Threshold voltage shift as a function of stress time for conventional and LDD devices.

displayed a shift in the subthreshold drain-current curve after stress.

Measured linear region threshold voltages at $V_{DS} = 0.1$ V are shown for both devices as a function of stress time in Fig. 2. The dramatic increase in V_T of the conventional device is due to the injection of hot electrons into the gate oxide, whereas for the graded drain device this effect is significantly less. Note, however, that this V_T definition does not include the mobility degradation. Even when the mobility and series resistance degradations are included by defining a pseudo-threshold voltage as the gate voltage required for a drain current of 5 μA/μm at a drain voltage of 0.1 V, the LDD device showed relatively less degradation.

This difference in behavior between LDD and conventional devices is evidenced by the current drive versus stress time plotted for both linear and saturation regions in Fig. 3.[1] In the linear region the drain current degrades considerably more for the conventional device than for the LDD device. This is not unexpected since the linear V_T for a conventional transistor degrades (cf. Fig. 2) in addition to the reduced mobility (cf. Fig. 1). The linear current drives in Fig. 3 were measured at $V_{GS} = 4$ V, in order to represent more realistically the device in circuit operation. Note, however, that an abrupt degradation of the conventional device linear current in the first 10 s of stress is an anamolous effect that is not understood at this time. We have observed this phenomenon on conven-

[1] Some spread in the data is seen for conventional transistors, even when fabricated on the same wafer. Degradation has been seen to vary by up to a factor of 5. Figs. 2 and 3 are representative results.

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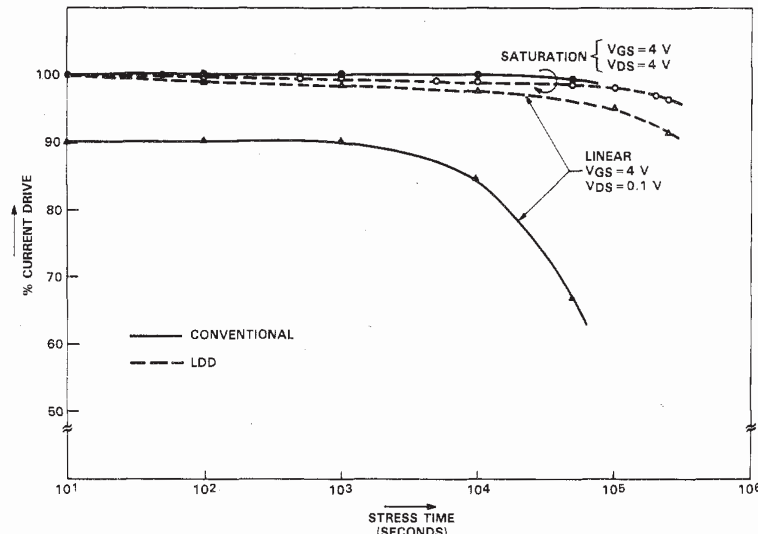

Fig. 3. Linear and saturation current drive as a function of stress time for conventional and LDD devices.

tional devices, stressed at high gate voltages, but never on LDD transistors.

The saturation region current drives for the LDD device does degrade slightly more than for the conventional transistor. This is due to the slight degradation in V_T and mobility. In fact, it is noted from the two dashed lines in Fig. 3 that the linear and saturation current drives of the LDD device track with each other. On the other hand, for the conventional device the saturation current does not degrade similar to its linear current drive. Since it was observed that the mobility and V_T degrade for these conventional devices, this higher saturation current level can be attributed to increased drain effect with stress. Measured I-V curves for the conventional device after stress do indicate an increased punchthrough behavior. In the LDD devices, due to the inserted n-region, the drain depletion region cannot significantly extend towards the source with the application of drain voltage to act as a second back bias and hence has a much smaller drain effect, which does not alter much with stress. In fact, this is an attractive feature of the LDD device which can be utilized by proper design of the n-region doping concentration and length [4] to make it punchthrough limited in breakdown. The details of our optimization procedure are to be described elsewhere [5].

IV. CONCLUSIONS

A comparison has been made to study the hot-electron effects between conventional and optimized LDD structures. Our studies demonstrated that when these devices were stressed at bias conditions for peak substrate current the optimized LDD structure exhibited significantly reduced degradation due to hot electrons than the conventional device. We attribute the superior performance to an optimized LDD fabrication process which allows hot-electron trapping in the gate oxide to have a minimal effect on the long-term performance of short-channel transistors, even under more severe stress conditions.

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