# A New LDD Structure: Total Overlap with Polysilicon Spacer (TOPS)

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*Abstract*—**This letter presents a new fully overlapped lightly doped drain structure—the total overlap with polysilicon spacer (TOPS) structure. The TOPS structure achieves full gate overlap of the lightly doped region with simple processing. TOPS devices have demonstrated superior performance and reliability compared to oxide-spacer lightly doped drain (LDD) devices, with an order of magnitude advantage in current degradation under stress for the same initial current drive or 30% more drive for the same amount of degradation. TOPS devices also show a much smaller sensitivity to $n^-$ dose variation than LDD devices. Gate-induced drain leakage (GIDL) is reported for the first time in fully overlapped LDD devices.**

## I. Introduction

THE long-term reliability of n-channel MOSFET's has been a major concern as device channel lengths have been reduced to submicrometer and deep-submicrometer dimensions [1], [2]. The lightly doped drain (LDD) structure [3] has been widely investigated as a means of reducing the lateral electric field and the associated hot-carrier effects on reliability. Theoretical and experimental investigations [4]–[6] have demonstrated that gate control over the $n^-$ region is a crucial element in both the performance and reliability of LDD devices. This letter presents a new fully overlapped lightly doped drain structure—the total overlap with polysilicon spacer (TOPS) structure. Unlike other proposed fully overlapped structures which require complicated fabrication sequences or unusual fabrication techniques [5]–[7], the TOPS structure achieves full overlap with simple and proven processing techniques.

## II. Device Processing

Fig. 1 shows the critical steps in the fabrication sequence. Gate oxide is grown after LOCOS isolation, and then layers of thin polysilicon, very thin LPCVD oxide, and thick doped polysilicon are deposited. Wafers were cleaned in piranha ($H_2SO_4/H_2O_2$) after thin polysilicon deposition, followed by removal of chemical oxide in dilute HF; the thin oxide deposition was followed directly by thick polysilicon deposition. Gate definition (using the thin LPCVD oxide as an etch stop) is followed by $n^-$ implantation through the thin oxide and thin polysilicon layers, and removal of the thin oxide in dilute buffered HF. Doped polysilicon is then deposited and etched to form the polysilicon spacer. The last etch proceeds until a well-defined endpoint corresponding to gate oxide and field oxide is detected. Both polysilicon etches are very easily controlled and do not require the extremely high selectivity or timed etching of previously reported structures [5], [6]. The oxide-spacer LDD devices were prepared by $n^-$ implantation after gate definition, followed by LPCVD oxide deposition, densification, and etch-back to form the oxide spacer [8]. Control over formation of the TOPS polysilicon spacer is much easier than that of the LDD oxide spacer because of the easily detected endpoint; the oxide spacer etch must be timed. Source/drain $n^+$ implantation, contact formation, and metallization follow a standard process sequence. Although it was not done in this initial study, silicidization of gate, source, and drain could be done by additional process steps after the polysilicon spacer formation.

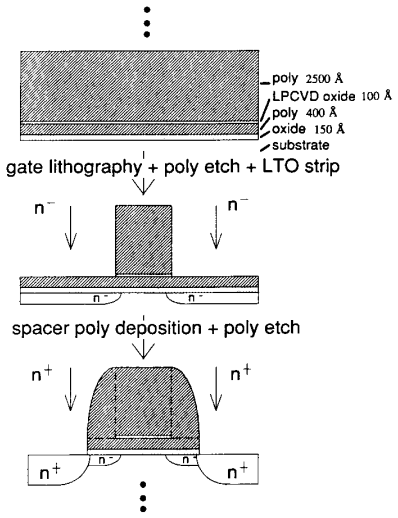


Fig. 1. TOPS structure layered gate and polysilicon spacer formation. Gate and spacer definitions are accomplished by plasma etching with oxide endpoint detection. Typical CVD film thicknesses are shown.

All devices had a gate oxide of 15 nm and were fabricated using the deep-submicrometer optical lithographic technique reported earlier [9]. All spacer lengths were designed to be 0.2 $\mu$m. TOPS devices received $n^-$ doses of 0.5, 1.0, and 3.0 $\times$ $10^{13}$ $cm^{-2}$, and the oxide-spacer LDD devices received doses of 0.5 and 1.5 $\times$ $10^{13}$ $cm^{-2}$. Two types of TOPS devices, having either *in-situ* doped or undoped thin polysilicon, were

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TABLE I
EFFECT OF n⁻ DOSE VARIATION ON PERFORMANCE OF TOPS AND LDD DEVICES
$I_{d\,sat}$ values measured at $V_g$ = 5 V; $g_{msat}$ values measured at $V_d$ = 3 V.

| Structure | Dose ($cm^{-2}$) | Performance* | |
|---|---|---|---|
| | | $I_{dsat}$ (mA/μm) | $g_{msat}$ (mS/mm) |
| TOPS | $0.5 \times 10^{13}$ | 0.45/0.36 | 118/103 |
| | $1.0 \times 10^{13}$ | 0.46/0.36 | 120/104 |
| | $3.0 \times 10^{13}$ | 0.48/0.38 | 122/104 |
| LDD | $0.5 \times 10^{13}$ | 0.36/0.32 | 90/84 |
| | $1.5 \times 10^{13}$ | 0.43/0.36 | 110/98 |

* Dual entries are for $L_{eff}$=0.5 μm and $L_{eff}$=0.8 μm.

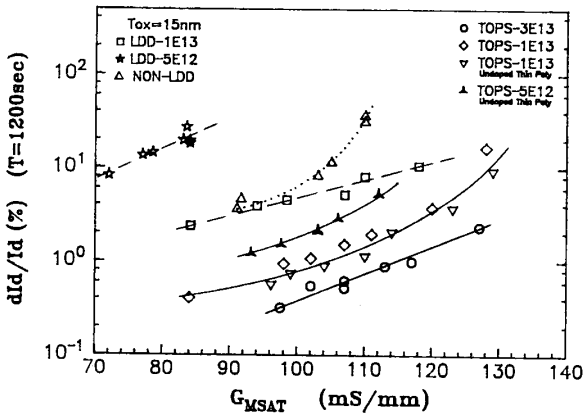


Fig. 2. Overall performance comparison of TOPS, LDD, and non-LDD technologies. Degradation values are for forward linear operation and $g_{msat}$ values are measured at $V_d$ = 3 V.

made in order to investigate the possibility of modifying the gate work function through the doping of the bottom layer of the gate [10]. *In-situ* doped polysilicon was used in all TOPS devices for the thick top layer of the gate and for the polysilicon spacer.

## III. Performance and Reliability

Performance and reliability characteristics of non-LDD, conventional oxide-spacer LDD, and TOPS n-MOSFET devices have been evaluated. Table I contains a comparison of TOPS and LDD device performance for $L_{eff}$ of 0.5 and 0.8 μm. The TOPS structure, due to the fully overlapped gate, shows better current drive and larger transconductance than an LDD structure of comparable channel length. The $g_m$ characteristics of the TOPS devices approach those of non-LDD's in magnitude. At $V_d$ = 3 V the peak $g_m$ of non-LDD, TOPS, and oxide spacer LDD devices were 109, 104, and 98 mS/mm, respectively, for an $L_{eff}$ of 0.8 μm. The drive advantage of TOPS devices over LDD devices was seen to increase with decreasing channel length, with as much as 20% more at $L_{eff}$ = 0.3 μm (0.62 versus 0.52 mA/μm). Importantly, the TOPS devices show a much smaller sensitivity to n⁻ dose variation than the LDD devices do over the range of doses evaluated, as shown in Table I. It should be noted that device and process characteristics have not necessarily been optimized with respect to n⁻ dose and spacer length in this initial feasibility study.

For a given $L_{eff}$ the TOPS device has significantly less substrate current than the non-LDD device. Peak $I_{sub}$ (at $V_d$ = 5 V and $V_g \sim 2$ V; $W$ = 10 μm, $L_{eff}$ = 0.8 μm) was 81, 16, and 8 μA for non-LDD, TOPS, and LDD devices, respectively. Although TOPS devices have more $I_{sub}$ than oxide spacer LDD devices, they exhibit significantly less hot-carrier degradation. After 20 min of stressing at peak $I_{sub}$ and $V_D$ = 6 V, a TOPS device with $L_{eff}$ = 0.8 μm shows a forward linear current degradation of 1.0% compared to 4.4 and 34% for the LDD and non-LDD devices, respectively. Creation of interface traps by hot carriers and subsequent electron trapping is offset in the TOPS device by the overlapped gate, whereas in the LDD device only fringing fields are available to exert control over the resistive n⁻ region. A definitive comparison of performance and reliability among the three device structures is shown in Fig. 2. The superiority of the TOPS devices compared to the LDD and non-LDD devices in this study is clearly demonstrated, with roughly an order of magnitude advantage in degradation for the same drive or 30% more drive for the same amount of degradation. Fig. 2 also shows the effect of n⁻ dose variations for the levels studied. The TOPS structure again appears to be less sensitive to n⁻ dose variability.

The doping of the thin polysilicon layer (as deposited) had no demonstrable effect on the current drive or reliability of the TOPS devices. One plausible explanation for the lack of a noticeable effect of thin polysilicon doping on both performance and reliability is that the undoped thin polysilicon may have been subsequently doped by diffusion from the top gate and spacer polysilicon. The thermal cycle after gate definition and source/drain implant was carefully controlled in order to limit junction drive-in (a total of 30 min at 925°C), but it is possible that dopant diffusion occurred rapidly along polysilicon grain boundaries.

The gate-induced drain leakage (GIDL) [11] behavior of non-LDD, oxide-spacer LDD, and TOPS devices are compared in Fig. 3. Besides hot-carrier degradation, GIDL is considered to be another major factor in limiting the power-supply voltage for deep-submicrometer MOS technologies [2]. The non-LDD MOSFET has the largest GIDL, as expected [11]. Of the remaining two devices, the oxide-spacer LDD is GIDL-free while the TOPS device still shows significant

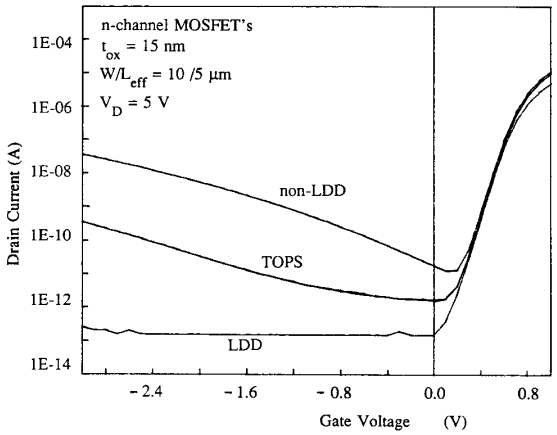


Fig. 3. GIDL behavior of TOPS, LDD, and non-LDD devices. Implanted $n^-$ doses are $3 \times 10^{13}$ and $1.5 \times 10^{13}$ $cm^{-2}$ for the TOPS and LDD devices, respectively.

GIDL. Because the gate would overlap the $n^+$ region in any fully overlapped LDD device such as TOPS, we expect GIDL to be an important design consideration for fully overlapped LDD structures.

## IV. Conclusions

A new fully overlapped LDD structure—TOPS—has been fabricated and characterized. TOPS devices produce more current drive and better transconductance than oxide-spacer LDD devices of equivalent size. A major advantage of TOPS over LDD is its improved reliability. Even though the TOPS devices had greater $I_{sub}$ than LDD devices, current degradation under hot-electron stressing conditions is significantly less for the TOPS devices. The choice of $n^-$ dose is less critical for the TOPS structure than for the LDD structure in the results reported here, implying less overall process sensitivity. GIDL was noted in the TOPS devices, the first such report of this behavior in fully overlapped LDD devices. This represents an important design constraint for submicrometer devices. The superior performance and reliability characteristics of the TOPS structure merit further investigation for deep-submicrometer applications.

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