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Jang et al.

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[54] **BORDERLESS CONTACT STRUCTURE**

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[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **09/163,382**

[22] Filed: **Sep. 30, 1998**

Related U.S. Application Data

[62] Division of application No. 08/616,411, Mar. 15, 1996, Pat. No. 5,840,624.

[51] **Int. Cl.**[7] **H01K 23/04**

[52] **U.S. Cl.** **257/698**; 257/698; 257/760; 438/634

[58] **Field of Search** 257/698, 760; 438/634

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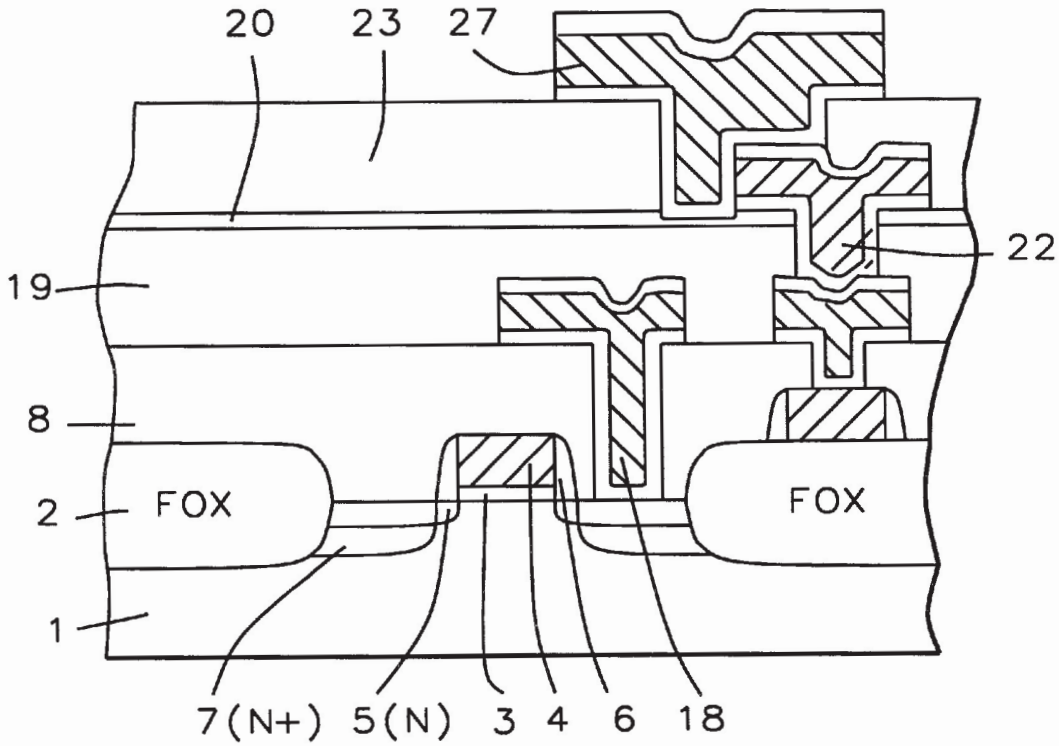
[57] **ABSTRACT**

A method for forming a borderless, contact or via hole, has been developed, in which a thin silicon nitride layer is used as an etch stop to prevent attack of an underlying interlevel dielectric layer, during the opening of the borderless, contact or via hole, in an overlying, interlevel dielectric layer. The thin silicon nitride layer is the top layer of an interlevel dielectric composite layer, used between metal interconnect levels.

3 Claims, 6 Drawing Sheets



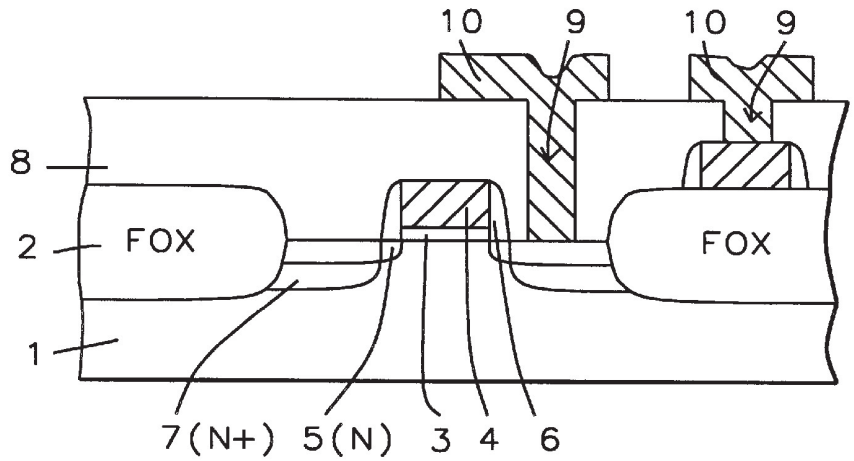


FIG. 1

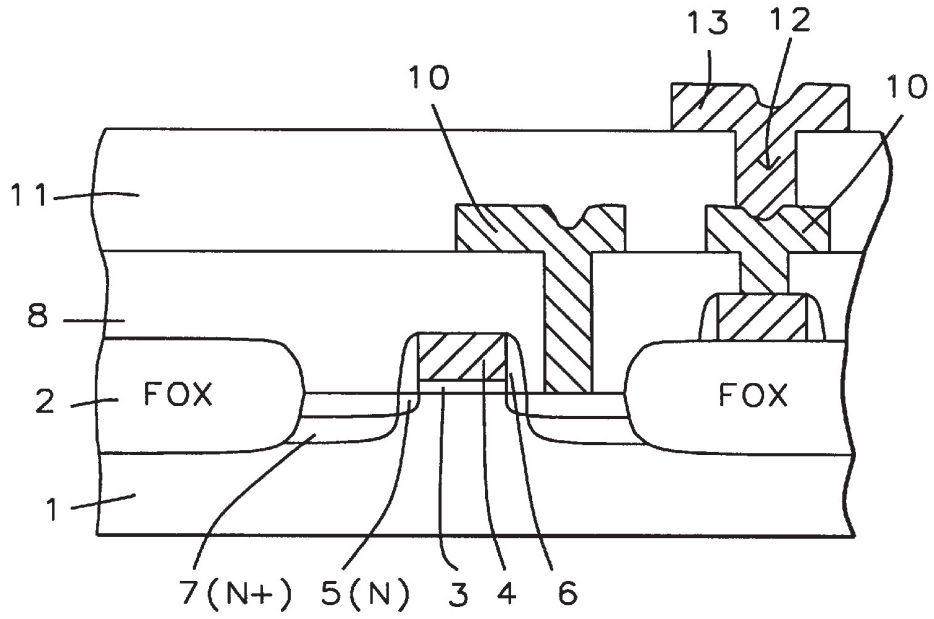


FIG. 2 – Prior Art

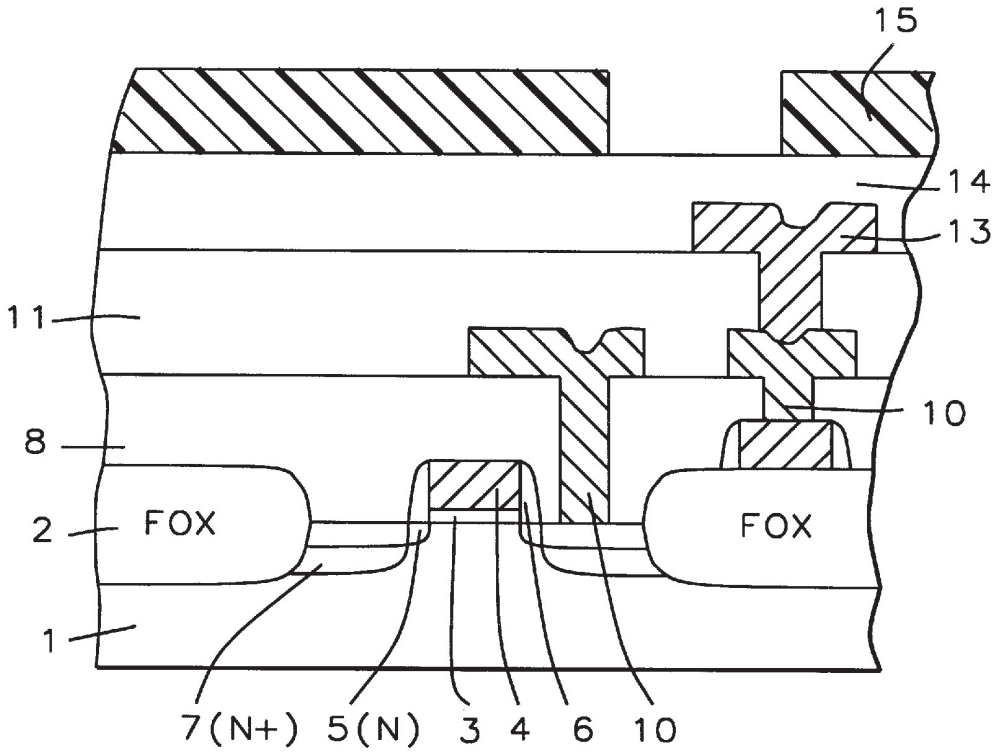


FIG. 3 – Prior Art

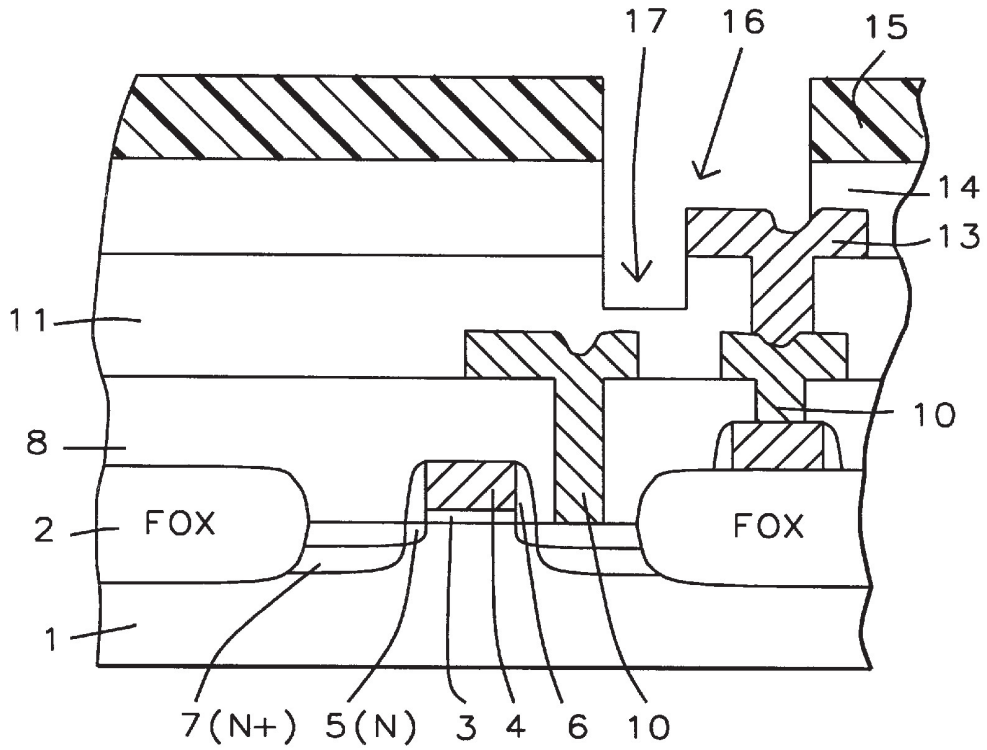


FIG. 4 – Prior Art

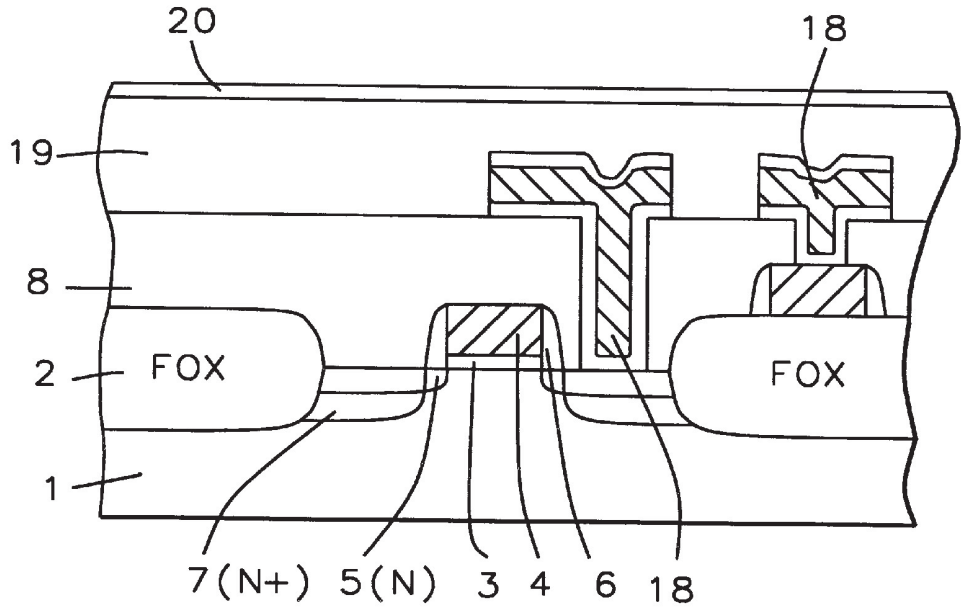
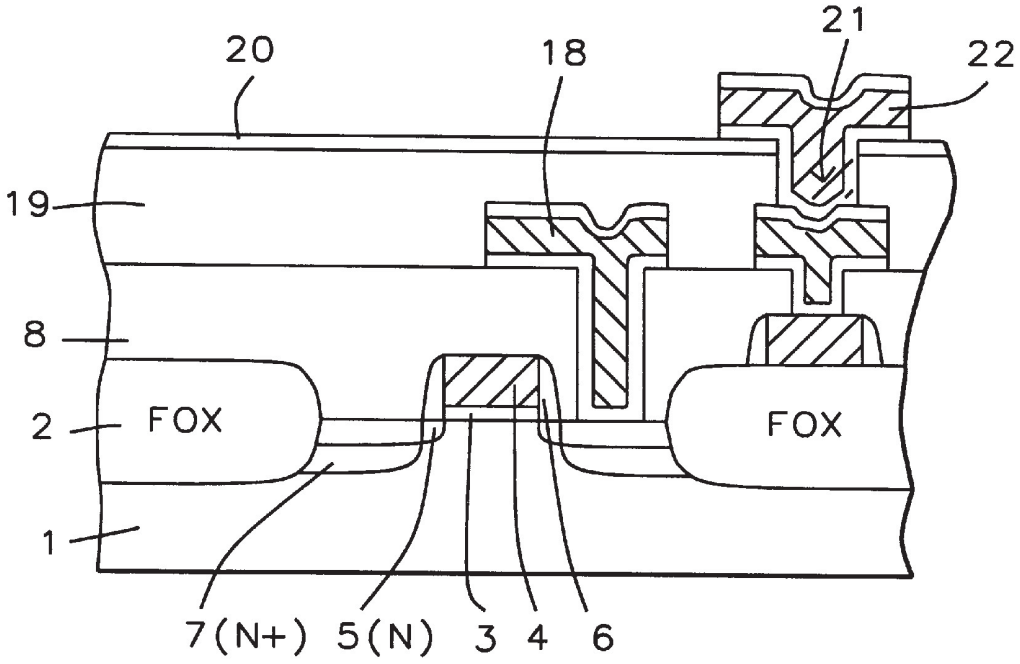

20
18
19
8
2
FOX
FOX
1
7(N+)
5(N)
3
4
6
18

FIG. 5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19
8
2
FOX
FOX
1
7(N+)
5(N)
3
4
6

FIG. 6

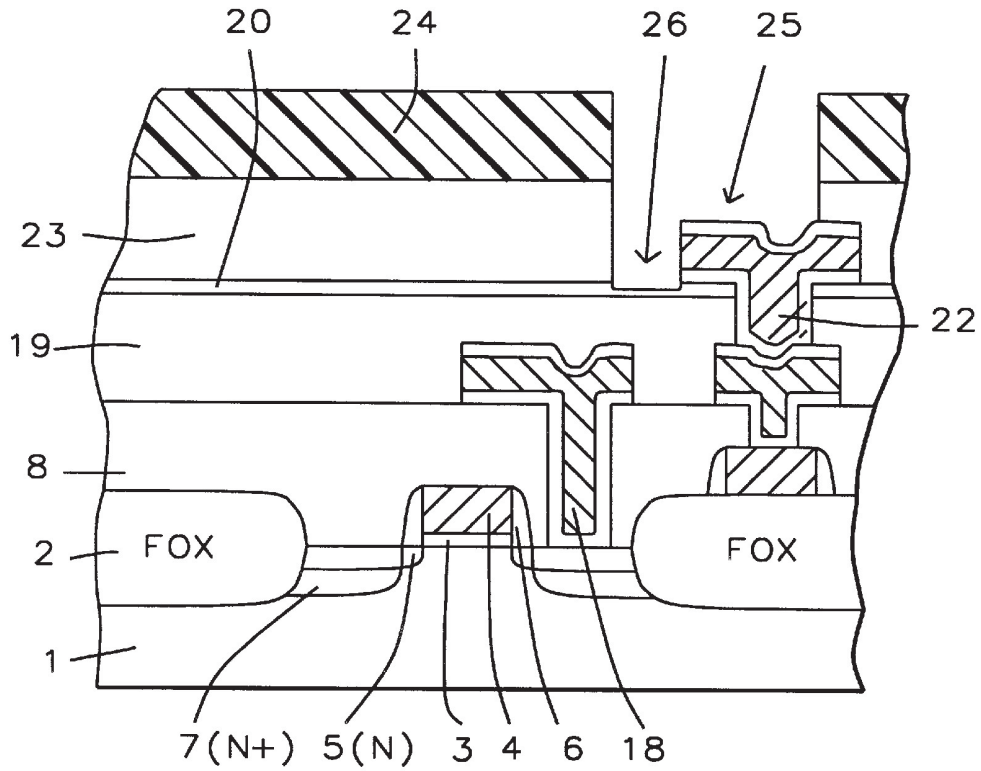

FIG. 7

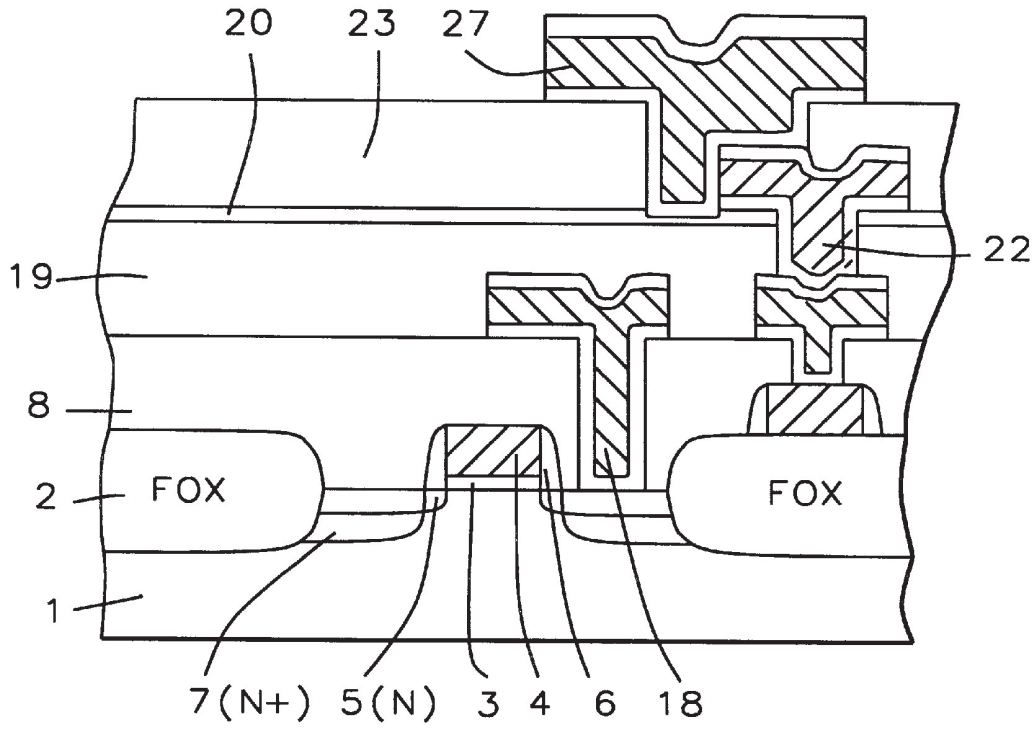

FIG. 8

BORDERLESS CONTACT STRUCTURE

This application is a divisional application of Ser. No. 08/616,411, filed on Mar 15, 1996, and issued as U.S. Pat. No. 5,840,624, on Nov. 24, 1998.

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to methods used to fabricate semiconductor devices, and more specifically to a process used to form via holes.

(2) Description of Prior Art

The major objectives of the semiconductor industry has been to continually increase the device and circuit performance of silicon chips, while maintaining, or even decreasing, the cost of producing these same silicon chips. These objectives have been successfully addressed by the ability of the semiconductor industry to fabricate silicon devices, with sub-micron features. The ability to use sub-micron features, or micro-miniaturazation, has allowed performance improvements to be realized by the reduction of resistances and parasitic capacitances, resulting from the use of smaller features. In addition, the use of sub-micron features, results in smaller silicon chips with increased circuit densities, thus allowing more silicon chips to be obtained from a starting silicon substrate, thus reducing the cost of an individual silicon chip.

The attainment of micro-miniaturazation has been basically a result of advances in specific semiconductor fabrication disciplines, such as photolithography and reactive ion etching. The development of more sophisticated exposure cameras, as well as the use of more sensitive photoresist materials, have allowed sub-micron features in photoresist layers to be routinely achieved. In addition similar developments in the dry etching discipline, has allowed these sub-micron images in photoresist layers, to be successfully transferred to underlying materials, used for the creation advanced semiconductor devices. However the use of sub-micron features, although improving silicon device performance and decreasing silicon chip cost, introduces specific semiconductor fabrication problems, not encountered with larger featured counterparts. For example, specific designs sometimes require that metal filled via holes, in insulator layers, used to connect an overlying metallization structure to an underlying metallization structure, not always be fully landed. That is the metal filled via, not being placed entirely on the underlying metallization structure. The inability to fully land a via on an underlying metal structure, places a burden on the process used to create the via hole. For example if the chip design demands a non-fully landed, or a borderless contact, the dry etching procedure, used to create the via, has to be able to insure complete removal of insulator material from the area where the via landed on the underlying metal structure, therefore necessitating the use of an overetch cycle. The overetch cycle however, can create problems in the area where the via missed the underlying metal structure, and resided partially on an underlying insulator layer. The underlying insulator layer, may be identical, or similar, to the insulator used for the via formation. The extent of the via hole overetch cycle can then result in severe etching of the underlying insulator layer, to a point where a lower level metallization structure may be exposed. Subsequent metal filling of the via hole can then result in interlevel leakages or shorts. In addition the above phenomena can even occur, due to photolithographic misalignment situations, with fully landed contacts.

Shibata, et al, in U.S. Pat. No. 5,350,712 describe a process for alleviating the consequences of the via hole misalignment, or borderless contact phenomena. However this present invention will describe a different approach to the misalignment or borderless contact, via hole phenomena. An approach which offers protection from misalignment problems, with little added cost or complexity.

SUMMARY OF THE INVENTION

It is an object of this invention to fabricate silicon devices using metal filled via holes that are not always fully landed, on underlying metal structures, as a result of a borderless contact design, or as a result of misalignment.

It is another object of this invention to open a borderless contact, or misaligned via hole, in an overlying interlevel dielectric layer, to an underlying metal structure, while exposing a composite underlying interlevel dielectric layer in the area of misalignment, or in the area of borderless design at end point.

It is still another object of this invention to use a composite underlying interlevel dielectric layer consisting of a top layer of insulator, that has a slower etch rate than the overlying interlevel dielectric layer.

It is still yet another object of this invention to open the borderless, or misaligned via, in the overlying interlevel dielectric layer, using a dry etching procedure, and being able to perform an overetch cycle to insure complete removal of the overlying interlevel dielectric layer, while not removing the top layer of the underlying, composite interlevel dielectric layer, in an area of misalignment, or borderless design.

In accordance with the present invention a process is described for fabricating silicon devices using a borderless contact, or via process, in which an etch stop layer is provided to protect underlying structures from attack during the borderless contact, dry etching process. A first, interlevel dielectric composite layer, comprised of a overlying thin, silicon nitride layer, and an underlying thick, silicon oxide layer, is deposited on an underlying metal structure, used to electrically contact an underlying active device region. A first via hole is opened in the first interlevel dielectric composite layer, followed by deposition of a metallization layer, and patterning to form a metal structure. A second interlevel dielectric layer of silicon oxide is deposited on the underlying metal structure, as well as on the thin silicon nitride layer, of the first interlevel dielectric composite layer. A second via hole is opened, via selective, dry etching procedures, in the second interlevel dielectric layer, exposing the top surface of the metal structure, and the surface of the thin silicon nitride layer, in regions where the borderless, or misaligned via hole did not overlay the metal structure. A selective dry overetch procedure, used to insure complete removal of the second interlevel dielectric layer, from the surface of the metal structure, is performed without removing the thin silicon nitride layer. The second via hole is then filled with a metal, and patterned to form another overlying metal structure.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the preferred embodiment with reference to the attached drawings that include:

FIG. **1**, which schematically, in cross-sectional style, shows an N channel MOSFET device, through contact level metal patterning.

FIGS. **2–4**, which schematically, in cross-sectional style, show prior art, and attempts at opening borderless contacts, or misaligned vias, to a first level metal structure, exposing an underlying contact level metal structure, in the region of via hole misalignment.

FIGS. **5–8**, which schematically, in cross sectional style, show the stages of fabrication used to create metal filled vias, in which the vias were of a borderless design, or misaligned, but did not result in exposure of underlying metal structures, during the dry etching procedure, due to the incorporation of a thin silicon nitride etch stop layer.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The method of fabricating via holes, using a borderless contact design, in which an etch stop layer is provided to protect against over etching and exposure of underlying metal structures, during the opening of the borderless contact, or via hole, will now be covered in detail. This invention can be used as part of metal oxide semiconductor field effect transistors, (MOSFET), devices, that are now being manufactured in industry, therefore only the specific areas, unique to understanding this invention will be covered in detail. FIG. **1**, schematically shows a typical N channel, (NFET), device, that this invention can be used with. A P type, substrate, **1**, with a <100> crystallographic orientation, is used. Thick field oxide regions, **2**, (FOX), are formed via conventional photolithographic and dry etching patterning of a composite insulator layer of silicon nitride and silicon dioxide, and then using the composite insulator layer as an oxidation mask, to thermally grow between about 4000 to 6000 Angstroms of FOX insulator, **2**, in the unmasked regions. After removal of the composite insulator, oxidation mask, a silicon oxide layer, **3**, is thermally grown to a thickness between about 50 to 300 Angstroms, and used as the gate insulator of the MOSFET device. A polysilicon layer is next deposited, using low pressure chemical vapor deposition, (LPCVD), procedures, to a thickness between about 2000 to 4000 Angstroms, and doped via ion implantation of arsenic or phosphorous, at an energy between about 50 to 100 Kev., at a dose between about 1E15 to 1E16 atoms/cm^2. The polysilicon layer is then patterned using conventional photolithographic and reactive ion etching, (RIE), processing, to create polysilicon gate structure, **4**, shown schematically in FIG. **4**.

A lightly doped source and drain region, **5**, is then formed via ion implantation of phosphorous at an energy between about 30 to 60 Kev., at a dose between about 1E12 to 5E13 atoms/cm^2. A layer of silicon oxide is deposited using either LPCVD or plasma enhanced chemical vapor deposition, (PECVD), processing, to a thickness between about 1500 to 4000 Angstroms, and subjected to an anisotropic RIE procedure, in CHF_3, to create insulator spacer, **6**, shown in FIG. **1**. A heavily doped source and drain region, **7**, is then formed, via ion implantation of arsenic at an energy between about 50 to 100 Kev., at a dose between about 1E14 to 5E15 atoms/cm^2. Another silicon oxide layer, **8**, is deposited using LPCVD or PECVD processing, at a temperature between about 400 to 800° C., to a thickness between about 3000 to 6000 Angstroms, followed by a photolithographic and RIE procedure, using CHF_3 as an etchant, and used to create contact hole, **9**. After photoresist removal, using plasma oxygen ashing, followed by careful wet cleans, a metallization layer of aluminum, containing between about 1 to 3% copper, and between about 0.5 to 1% silicon, is deposited via r.f. sputtering, to a thickness between about 4000 to 8000 Angstroms. The metallization layer can also be LPCVD tungsten, deposited via the decomposition of tungsten hexafluoride. Patterning of the metallization layer is performed by again using conventional photolithographic and RIE processing, using Cl_2 as an etchant, to create metal structure, **10**, shown schematically in FIG. **1**. Photoresist removal is accomplished via plasma oxygen ashing followed by careful wet cleans.

FIGS. **2–4**, will show prior art, and attempts at creating borderless contacts, or misaligned vias, to underlying metal structures, resulting in severe over etching of underlying insulators, due to the non-selectivity of the materials and dry etchants used. A layer of PECVD, silicon oxide, **11**, is deposited at a temperature between about 400 to 600° C., to a thickness between about 3000 to 6000 Angstroms. A first via hole, **12**, is created in silicon oxide layer, **11**, to metal structure, **10**, using conventional photolithographic and RIE processing, using CHF_3 as an etchant. After photoresist removal, via plasma oxygen ashing and careful wet cleans, another metallization layer of aluminum, containing between about 1 to 3% copper, and between about 0.5 to 1% silicon is deposited using r.f. sputtering, to a thickness between about 4000 8000 Angstroms. This metallization layer can also be LPCVD tungsten, using a tungsten hexafluoride source, if desired. Patterning of the metallization layer, to form metal structure, **13**, is accomplished again via conventional photolithographic and RIE procedures, using Cl_2 as an etchant. FIG. **2**, schematically shows this structure after photoresist removal using plasma oxygen ashing and careful wet cleans.

An insulator layer of silicon oxide, **14**, is deposited again using PECVD processing, at a temperature between about 400 to 600° C., to a thickness between about 3000 to 6000 Angstroms. The desired opening to metal structure, **13**, is next addressed by opening a hole in photoresist layer, **15**. The opening in photoresist layer can either be intentionally designed to be borderless, that is not open entirely on the top surface of metal structure, **13**, or can suffer from misalignment problems, and again not open entirely over metal structure, **13**. This is shown in FIG. **3**. The dry etching procedure, used to open a second via, **16**, in silicon oxide layer, **14**, is next performed using CHF_3 as an etchant. At the conclusion of the RIE procedure, or when end point is determined by the observance of the top surface of metal structure, **13**, an additional overetch cycle is used to insure complete removal of silicon oxide, **14**, from the top surface of metal structure, **13**, in areas where poor uniformity of the PECVD silicon oxide layer, **14**, may have existed. The overetch cycle does not adversely effect metal structure, **13**, since the etchant used to create second via, **16**, will not attack the metal. However the overetch cycle can severely attack the underlying silicon oxide layer, **11**, in regions where the second via did not overlie metal structure, **13**. The overetch creates a gouge or crevice, **17**, shown schematically in FIG. **4**. The extent of this defect, when subsequently filled with an overlying metallization, can result in either deleterious leakage, or even shorts, between the overlying metallization and an underlying metal structure, used to electrically contact an active device region of the MOSFET structure, different then the active device region being addressed by a metal structure in second via, **16**.

A solution to the crevicing or gouging phenomena, occurring as a consequence of borderless contacts, or misaligned via holes, is now addressed. FIG. **5**, again shows the creation of a metal structure, contacting both a polysilicon gate structure, **4**, and a source and drain region, **7**, through an opened contact hole, in silicon oxide layer, **8**. The metallization used is an underlying layer of titanium nitride,

between about 200 to 500 Angstroms, a layer of aluminum, between about 4000 to 8000 Angstroms, containing between about 1 to 3% copper, and between about 0.5 to 1% silicon, and an overlying layer of titanium nitride, again between about 200 to 500 Angstroms. The titanium nitride layers offer, adhesive, barrier, and electromigration enhancements. The metallization layer is then patterned using conventional photolithographic and RIE procedures, using Cl_2 as an etchant to create metal structure, **18**. Photoresist removal is performed using plasma oxygen ashing and careful wet cleans. A composite interlevel dielectric layer is then deposited, consisting of an underlying silicon oxide layer, **19**, obtained via PECVD processing, at a temperature between about 400 to 600° C., to a thickness between about 3000 to 6000 Angstroms, and an overlying layer of silicon nitride, **20**, obtained via PECVD processing, at a temperature between about 400 to 600° C., to a thickness between about 500 to 1000 Angstroms.

A first via hole, **21**, is next opened in the composite interlevel dielectric layer, to expose metal structure, **18**, which in turn is contacting an underlying polysilicon gate structure, **4**, via use of conventional photolithographic and RIE procedures, using Cl_2 for silicon nitride layer, **20**, and CHF_3, for silicon oxide layer, **19**, as etchants. After removal of photoresist via plasma oxygen ashing and careful wet cleans, another layer of titanium nitride—aluminum, with copper and silicon,—titanium nitride, is deposited using process conditions, and film thicknesses, identical to those previously supplied for the metallization layer used to create metal structure, **18**. Photolithographic and RIE procedures, again using Cl_2 as an etchant are used to define metal structure, **22**, shown schematically in FIG. **6**. Photoresist removal is again accomplished using plasma oxygen ashing and careful wet cleans.

A silicon oxide layer, **23**, is deposited using PECVD processing, at a temperature between about 400 to 600° C., to a thickness between about 3000 to 6000 angstroms. Photoresist layer, **24**, is applied and exposed to open a region to be used for an intentional borderless contact. The opening may be also be misaligned, which will create an unintentional borderless contact. A RIE procedure is next used to open second via hole, **25**, in is silicon oxide layer, **23**. The chemistry of the etchant used, CHF_3 for silicon oxide layer, **23**, and the RIE conditions are chosen to result in a selectivity of silicon oxide layer, **23**, to underlying silicon nitride layer, **20**, of between about 3 to 1, in the CHF_3 ambient. The enhanced selectivity between silicon oxide and the underlying silicon nitride layer, allows a robust overetch cycle to be performed to insure complete removal of thick regions of silicon oxide from the top surface of metal structure **22**, without creating a severe gouge or crevice in the underlying composite interlevel dielectric layer, in regions where the second via, **25**, did not overlie metal structure, **22**. The minimum crevice or gouge, **26**, is confined to the thin silicon nitride etch stop layer, **20**. This is schematically shown in FIG. **7**. Photoresist removal is performed using plasma oxygen ashing and careful wet cleans.

Another metallization is performed via r.f. sputtering, of overlying and underlying layers of titanium nitride, at a thickness between about 200 to 500 Angstroms, and a core layer of aluminum, containing between about 1 to 3% copper, and between about 0.5 to 1% silicon, at a thickness between about 4000 to 6000 Angstroms. Once again patterning of the metallization layer is accomplished via standard photolithographic and RIE procedures, using Cl_2 as an etchant, to create metal structure, **27**. Photoresist removal is again performed using plasma oxygen ashing, followed by careful wet cleans. FIG. **8**, schematically shows that silicon nitride etch stop layer, **20**, preventing crevicing or gouging of silicon oxide layer, **19**, and thus prevented leakage or shorts between metal structure, **27**, connected to a polysilicon gate structure, and metal structure, **18**, connected to a source and drain region, of a MOSFET device structure.

Although this process for creating borderless contacts, using a silicon nitride etch stop, to prevent metal leakages and shorts, has been shown for an N channel, (NFET) device, it can also be applied to P channel, (PFET), devices, complimentary, (CMOS), devices, as well as to BiCMOS devices.

While this invention has been particularly shown and described with reference to, the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of this invention.

What is claimed is:

1. A MOSFET device structure, with a borderless contact structure, on a semiconductor substrate, featuring a notch, in a thin silicon nitride stop layer, protecting the integrity of an underlying insulator layer, while insuring complete sidewall contact of said borderless contact structure, to an adjacent metal structure, comprised of:

field oxide regions in said semiconductor substrate;

a device region between said field oxide regions;

a first polysilicon gate structure in center of said device region, and a second polysilicon gate structure on a first field oxide region;

a source and drain region in said device region, located between said first field oxide region, and said first polysilicon gate structure;

a first insulator layer on said field oxide regions, on said source and drain region, on said first polysilicon gate structure, and on said second polysilicon gate structure;

a contact hole in said first insulator layer, exposing a portion of the top surface of said second polysilicon gate structure;

a contact level metal structure, comprised of a first portion of said contact level metal structure, completely filling said contact hole, in said first insulator layer, and a second portion of said contact level metal structure, located on said first insulator layer;

a composite, second insulator layer, comprised of said thin silicon nitride, stop layer, overlying a thick silicon oxide, underlying layer, located on said second portion of said contact level metal structure, and on the portion of said first insulator layer, not covered by said second portion of said contact level metal structure;

a first via hole in said composite, second insulator layer, exposing a portion of the top surface of said second portion of said contact level metal structure;

a first level metal structure, comprised of a first portion of said first level metal structure, completely filling said first via hole, and a second portion of said first level metal structure, located on the top surface of said composite, second insulator layer;

a third insulator layer, located on second portion of said first level metal structure, and on the portion of said composite, second insulator layer, not covered by said second portion of said first level metal structure;

a borderless via hole comprised of; a first portion of said borderless via hole, in a top portion of said third insulator layer, exposing a portion of the top surface of said second portion of said first level metal structure;

and a second portion of said borderless via hole, in said third insulator layer, and in a top portion of said thin silicon nitride stop layer, featuring said notch in the top portion of said thin silicon nitride stop layer, and with said second portion of said borderless via hole exposing a complete side of said second portion of said first level metal structure; and

said borderless contact structure, comprised of a first portion of said borderless via hole structure, completely filling said first portion of said borderless via hole, and completely filling said second portion of said borderless via hole contacting the complete side of said second portion of said first level metal structure, and contacting the top portion of said second portion of said first level metal structure, exposed in said borderless via hole, and comprised of a second portion of said borderless contact structure, overlying a portion of the top surface of said third insulator layer.

2. The MOSFET device structure of claim **1**, wherein said composite, second insulator layer, is comprised of an overlying layer of silicon nitride, between about 500 to 1000 in thickness, and an underlying layer of silicon oxide, between about 3000 to 6000 Angstroms in thickness.

3. The MOSFET device structure of claim **1**, wherein said third insulator layer is silicon oxide, between about 3000 to 6000 Angstroms in thickness.

* * * * *