US006228777B1

(12) United States Patent
Arafa et al.

(10) Patent No.: **US 6,228,777 B1**
(45) Date of Patent: **May 8, 2001**

(54) **INTEGRATED CIRCUIT WITH BORDERLESS CONTACTS**

(75) Inventors: **Mohamed Arafa**, Hillsboro; **Scott Thompson**, Portland, both of OR (US)

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/328,190**

(22) Filed: **Jun. 8, 1999**

(51) Int. Cl.^{7} **H01L 21/302**
(52) U.S. Cl. **438/740**; 438/740
(58) Field of Search 438/664, 666, 438/683, 674, 704, 740, 970, 634, 675, 655, 221, 437, 291, 910

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,208,780	6/1980	Richman	29/571
4,441,247	4/1984	Gargini et al.	29/571
4,557,036	12/1985	Kyuragi et al.	29/571
4,650,696	3/1987	Raby .	
4,732,801	3/1988	Joshi	428/198
4,749,631	6/1988	Haluska et al.	428/704
4,755,480	7/1988	Yau et al. .	
4,866,003	9/1989	Yokoi et al. .	
4,920,073	4/1990	Wei et al. .	
4,948,482	8/1990	Kobayashi et al.	204/192
4,966,870	10/1990	Barber et al. .	
4,997,518	3/1991	Madokoro	156/643
5,089,432	2/1992	Yoo .	
5,180,688	1/1993	Bryant et al. .	
5,268,330	* 12/1993	Givens et al.	438/675
5,275,972	1/1994	Ogawa et al. .	
5,285,103	2/1994	Chen et al.	257/644
5,314,847	5/1994	Watanabe et al. .	
5,372,969	12/1994	Moslehi .	
5,409,858	4/1995	Thakur et al. .	
5,474,955	12/1995	Thakur .	
5,633,202	5/1997	Brigham et al.	438/763
5,652,176	* 7/1997	Maniar et al.	438/970
6,090,671	* 7/2000	Balasubramanyam	438/291
6,096,642	* 8/2000	Wu	438/655

FOREIGN PATENT DOCUMENTS

2116132	4/1990	(JP) .
4129223	4/1992	(JP) .
5029252	2/1993	(JP) .

OTHER PUBLICATIONS

R.C. Sun, J.T. Clemens, J.T. Nelson, "Effects of Silicon Nitride Encapsulation on MOS Device Stability". JEEE 18th Annual Proceedings Reliability Physics 1980, pp. 244–251.

A. Hamada, E. Takeda, "AC Hot–Carrier Effect Under Mechanical Stress", IEEE Symposium on VLSI Technology Digest of Technical Papers, Jun. 1992, pp. 98–99.

M. Shimbo, T. Matsuo, "Thermal Stress in CVD PSG and SiO$_2$ Films on Silicon Substrates", Journal of the electrochemical Society, vol. 130 No. 1, Jan. 1983, pp. 135–138.

K. Okuyama, K. Kubota, T. Hashimoto, S. Ikeda, A. Koike, "Water–Related Threshold Voltage Instability of Polysilicon TFTs", IEDM International Electron Devices Meeting, Dec. 1993, p 527–530.

N. Lifshitz, G. Smolinsky, "Water–Related Charge Motion in Dielectrics", Journal of the Electrochemical Society, vol. 136, No. 8, Aug. 1989, pp. 2335–2340.

(List continued on next page.)

Primary Examiner—David Nelms
Assistant Examiner—David Nhu
(74) *Attorney, Agent, or Firm*—Mark Seeley

(57) **ABSTRACT**

An integrated circuit comprising a conductive region formed on a semiconductor substrate, a silicate glass layer formed on the conductive region, and an etch stop layer formed on the silicate glass layer. The integrated circuit also includes a borderless contact that is coupled to the conductive region.
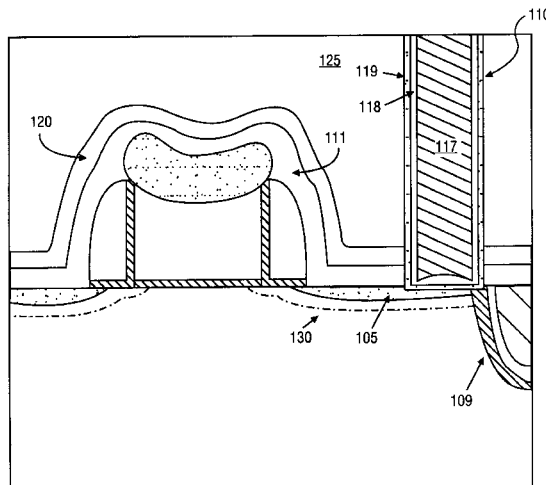
10 Claims, 3 Drawing Sheets

OTHER PUBLICATIONS

M. Noyori, et al, "Comparisons of Instabilities in Scaled CMOS Devices Between Plastic and Hermetically Encapsulated Devices", IEEE Transactions on Electron Devices, Oct. 1983 pps.

W. H. Stinebaugh, Jr., et al, "Correlation of Gm Degradation of Submicrometer MOSFET's with Refractive Index and Mechanical Stress of Encapsulation Materials".

IEEE Transactions on Electron Devices, Vo. 36, No. 3, Mar. 1989, pp. 542–547.

C.E. Blat, E.H. Nicollian, E.H. Poindexter, "Mechanism of Negative–Bias–Temperature Instability", Journal of Applied Physics, vol. 69, No.3, 2/91, pp. 1712–1720.

J. Takahashi, K. Machida, N. Shimoyama, K. Minegishi, "Water Trapping effect of Point Defects in Interlayer Plasma CVD SiO2 Films", Proceedings Ninth International VLSI Multilevel Interconnection Conference (VMIC), Jun. 1992, pp. 331–336.

N. Stojadinovic, S. Dimitrijev, "Instabilities in MOS Transistors", Microelectroncs and Relibility, 1989, vol. 29, No. 3 pp. 371–380.

K. Shmokawa, T. Usami, S. Tokitou, N. Hirashita, M. Yoshimaru, M. Ino, "Supression of the MoS Transistor Hot Carrier Degradation Casued by Watdr Desorbed from Inter-metal Dielectric", IEEE Symposium on VLSI Technology Digest of Technical Papers, Jun. 1992, pp. 96–97.

A.N. Saxena, K Ramkumar, S.K. Ghosh, "Stresses in TEOS Based SiO2 Films and Reliability of Multilevel Metalizations", Proceedings Ninth International VLSI Multilevel Interconnection Conference (VMIC, Jun. 1992, pp. 427–429.

V. Jain, D. Praminik, "Impact of Inter Metal Oxide Structures and Nitride Passivation on Hot Carrier Reliability of Sub–Micron MOS Devices", proceedings Ninth International VLSI Multilevel Interconnection Conference (VMIC), Jun. 1992, pp. 417–419.

N. Shimoyama, K. Machida, K. Murase, T. Tsuchiya, "Enhanced Hot–Carrier Degradation Due to Water in TEOS/O3–Oxide and Water Blocking Effect of ECR–SiO2", IEEE Symposium on VLSI Technology, Jun. 1992, pp. 94–95.

A. Hamada, T. Furusawa, E. Takeda, "A New Aspect on Mechanical Strress Effects in Scaled MOS Devices", IEEE Symposium on VLSI Technology Digest of Technical Papers, 6/90 p.

M. Noyori, T. Ishihara, H. Higuchi "Secondary Slow Trapping–A New Moisture Induced Instability Phenomenon in Scaled CMOS Devices", IEEE 20th Annual Proceedings Reliability 1982, p.

J. Mitsuhashi, H. Muto, Y. Ohno, T. Matsukawa, "Effect of P–SiN Passivation Layer on Time–Dependent Dielectric Breakdown in SiO2", IEEE 25th Annual Proceedings Reliability Physics, Apr. 1987, pp. 60–65.

K.P. MacWilliams, L.E. Lowry, D.J. Swanson, J. Scarpulla, "Wafer–Mapping of Hot Carrier Lifetime Due to Physical Stress Effects", IEEE Symposium on VLSI Technology, Digest of Technical Papers, Jun. 1992, pp. 100–101.

J. Mitusuhashi, S. Kakao, T. Matsukawa, Mechanical Stress and Hydrogen Effects on Hot Carrier Injection, IEE–IEDM Tech Digest, International Electron Devices Meeting 12/86, p.

Y. Ohno, A. Ohsaki, T. Kaneoka, J. Mitsuhashi, M. Hirayama, T. Kato, "Effect of Mechanial Stress for Thin SiO2 Films in TDDB and CCST Characteristics", IEE 27th Annual Proceedings Reliability Physics, Apr. 1989, pp. 34–38.

W. Abadeer, W. Tonti, et al, Bias Temperature Reliability of N+ and P+ Polysilicon Gates NMOSFETs and POMSFETs, IEEE 31st Annual Proceedings Reliability, 8/93, pp. 147–149.

K.O. Jeppson, C.M. Svensson "Negative bias stress of MOS devices at high electric fields and degradation of MNOS devices" Journal of Applied Physics V48, #5, 5/77 pp. 2004–2014.

R.T. Fuller, W.R. Richards, Y. Nissan–Cohen, J.C. Tsang, P.M. Sandow, "The Effects of Nitride Layers On Surface State Density and the Hot Electron Lifetime of Advanced CMOS Circuits" IEEE 1987, Custom Intefrated Circuits Conference, pp. 337–340.

S. Fujita, Y. Uemoto, A. Sasaki, "Trap Generation in Gate Oxide Layer of MOS Structures Encapsulated by Silicon Nitride", IEDM–IEEE 1985, pp. 64–67.

Stanley Wolf, "Silicon Processor the VLSI Era", vol. 1, pp. 191–195/514–515.

Stanley Wolf, "Silicon Processing for the VLSI Era", vol. 2, pp. 132–133, 144–145, 164–165, 188–189, 194–195, 392–396.

M. Noyori, et al., "Characteristics & Analysis of Instability Induced by Secondary Slow Trapping in Scaled CMOS Devices", IEEE Transactions Reliability, 8/83 pp. 323–329.
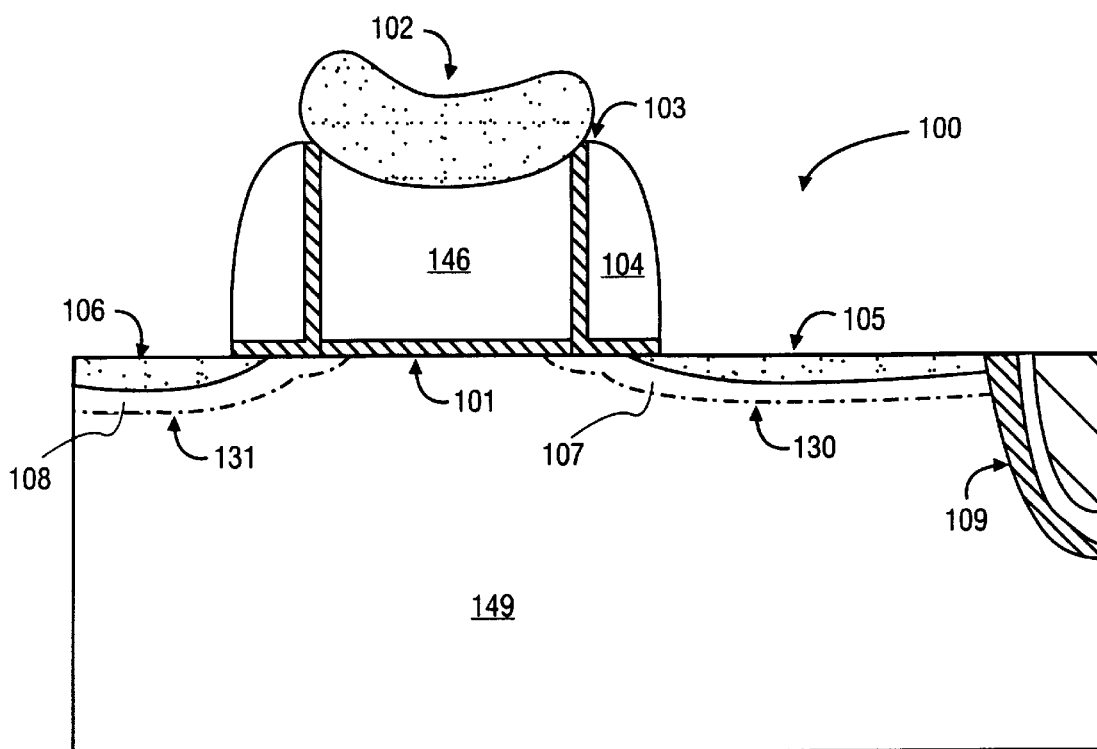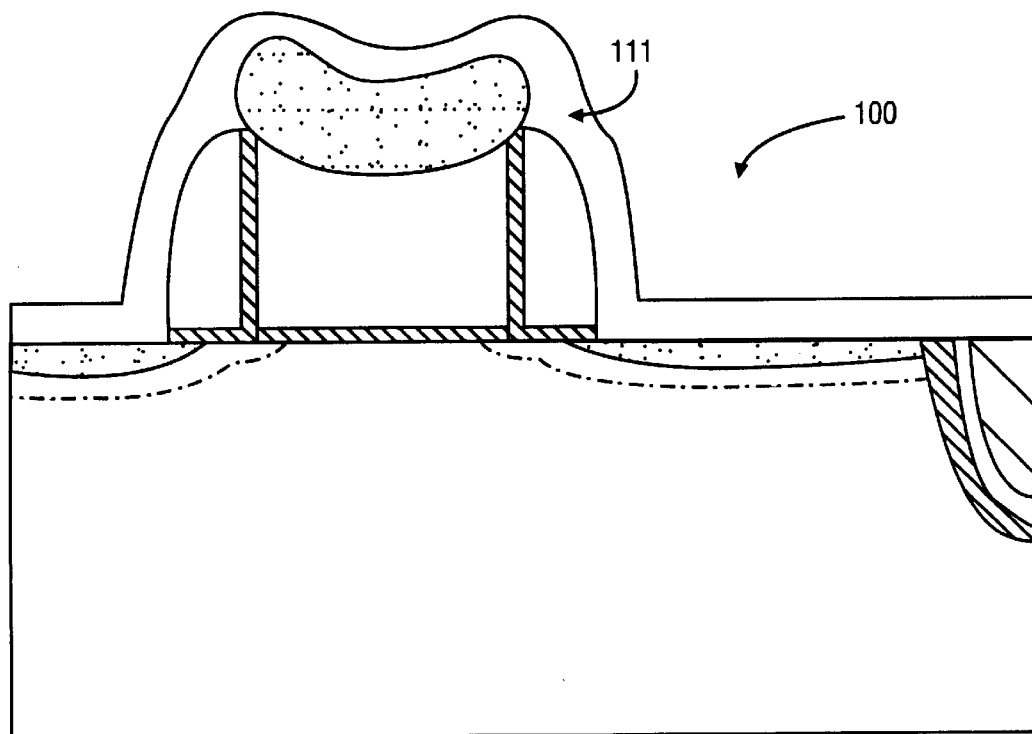
* cited by examiner

102
103
100
146
104
106
105
101
108
131
107
130
109
149

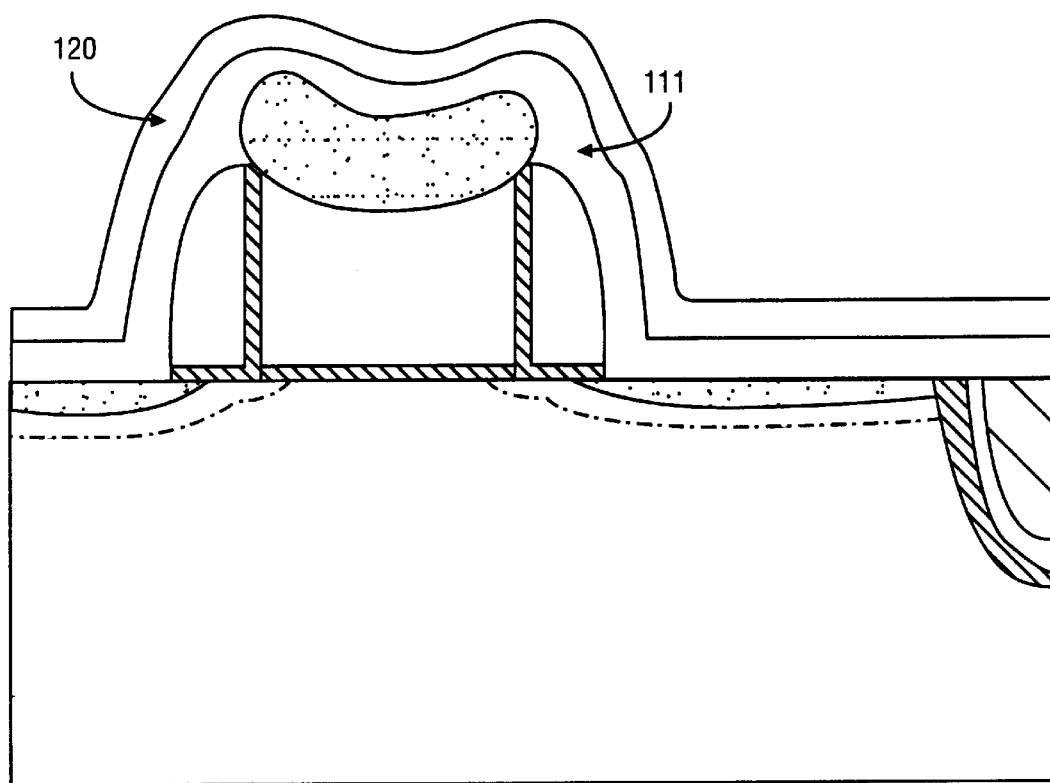**FIGURE 1**
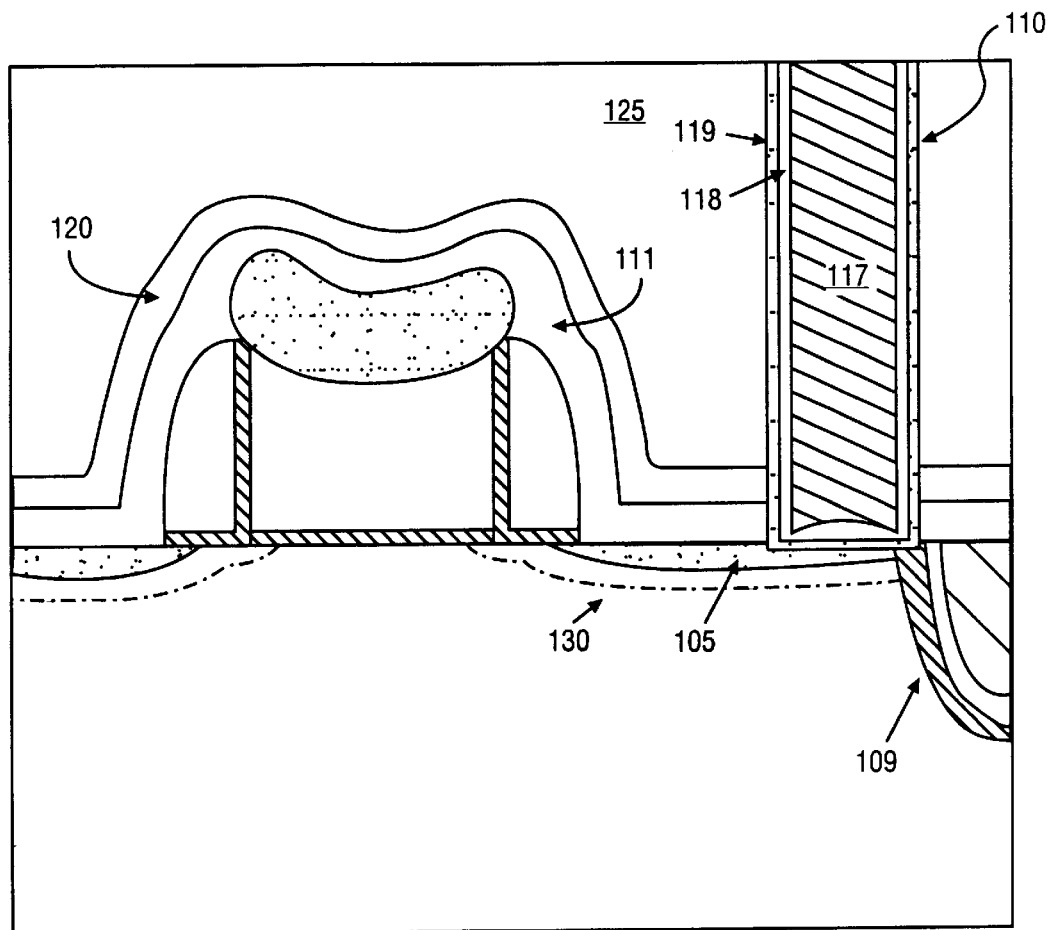

111
100

FIGURE 2

FIGURE 3

FIGURE 4

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.

fastcase®
Smarter legal research.