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(12) **United States Patent**  
**Arafa et al.**

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- (54) **INTEGRATED CIRCUIT WITH BORDERLESS CONTACTS**
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- (\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(57) **ABSTRACT**

An integrated circuit comprising a conductive region formed on a semiconductor substrate, a silicate glass layer formed on the conductive region, and an etch stop layer formed on the silicate glass layer. The integrated circuit also includes a borderless contact that is coupled to the conductive region.

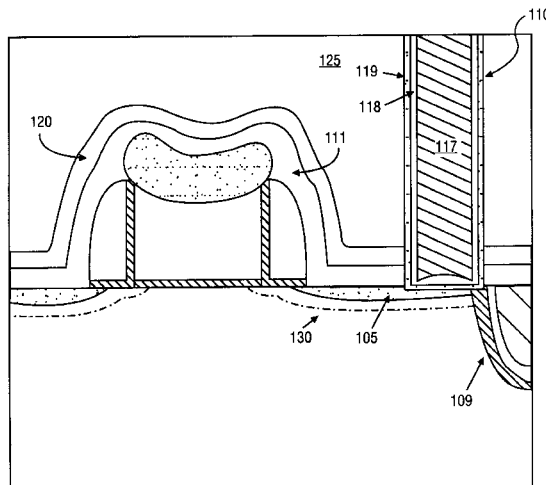
**10 Claims, 3 Drawing Sheets**

- (21) Appl. No.: **09/328,190**
- (22) Filed: **Jun. 8, 1999**
- (51) **Int. Cl.**<sup>7</sup> ..... **H01L 21/302**
- (52) **U.S. Cl.** ..... **438/740; 438/740**
- (58) **Field of Search** ..... 438/664, 666, 438/683, 674, 704, 740, 970, 634, 675, 655, 221, 437, 291, 910

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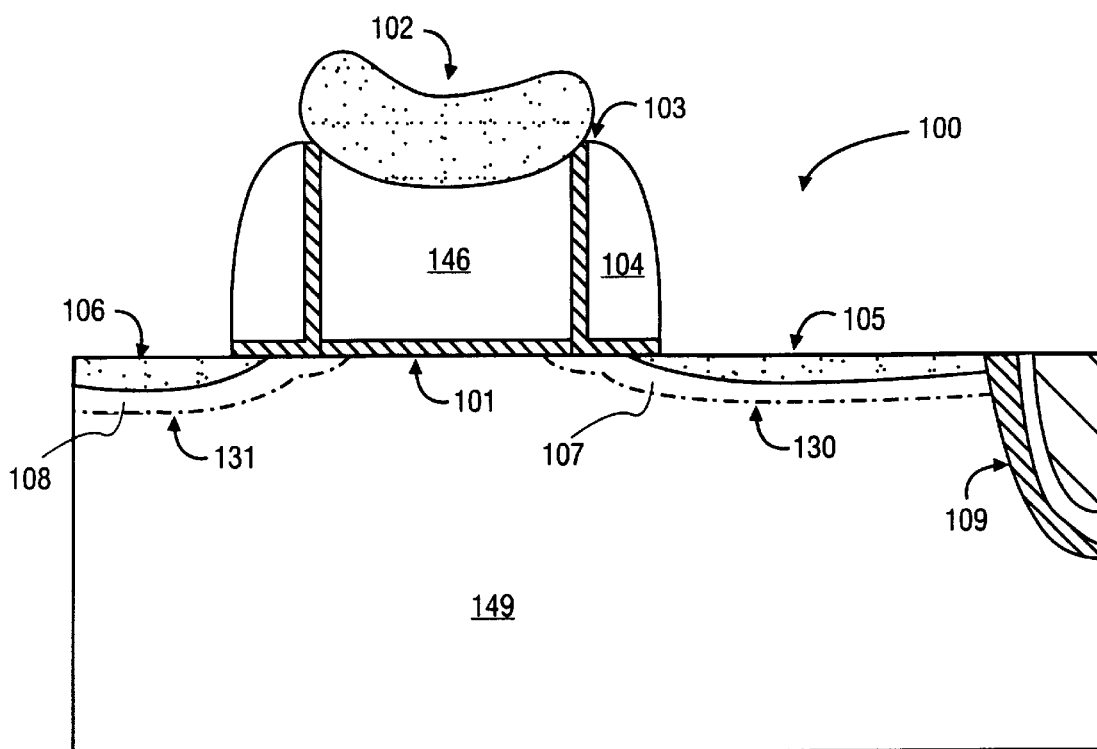


FIGURE 1

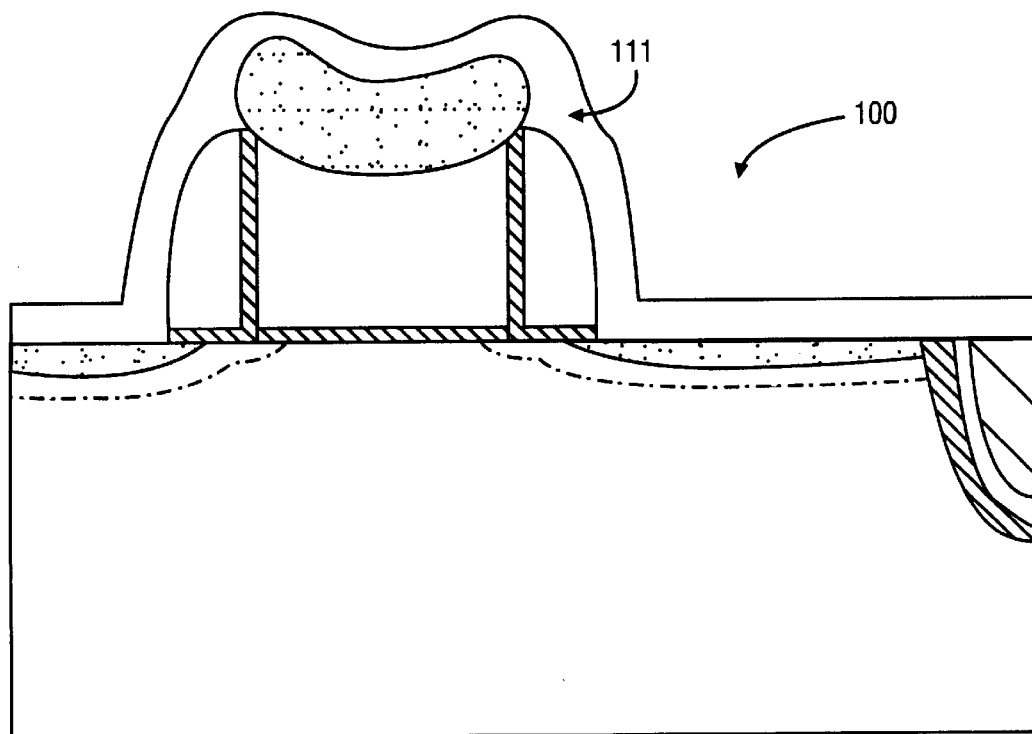


FIGURE 2

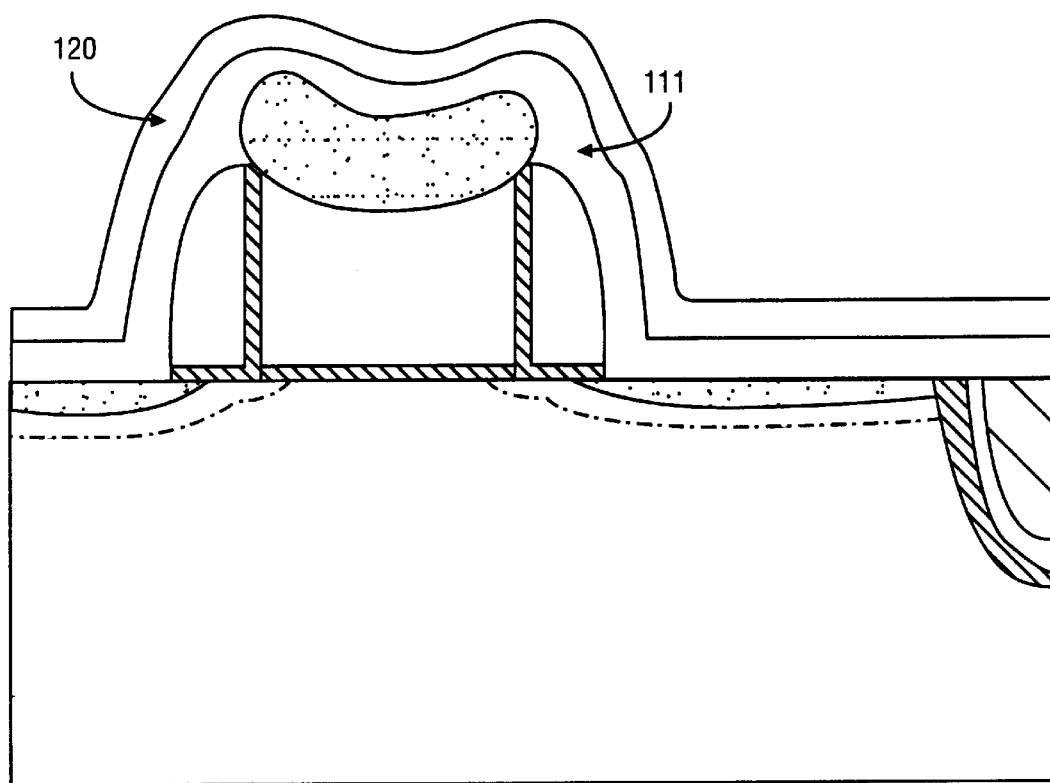


FIGURE 3

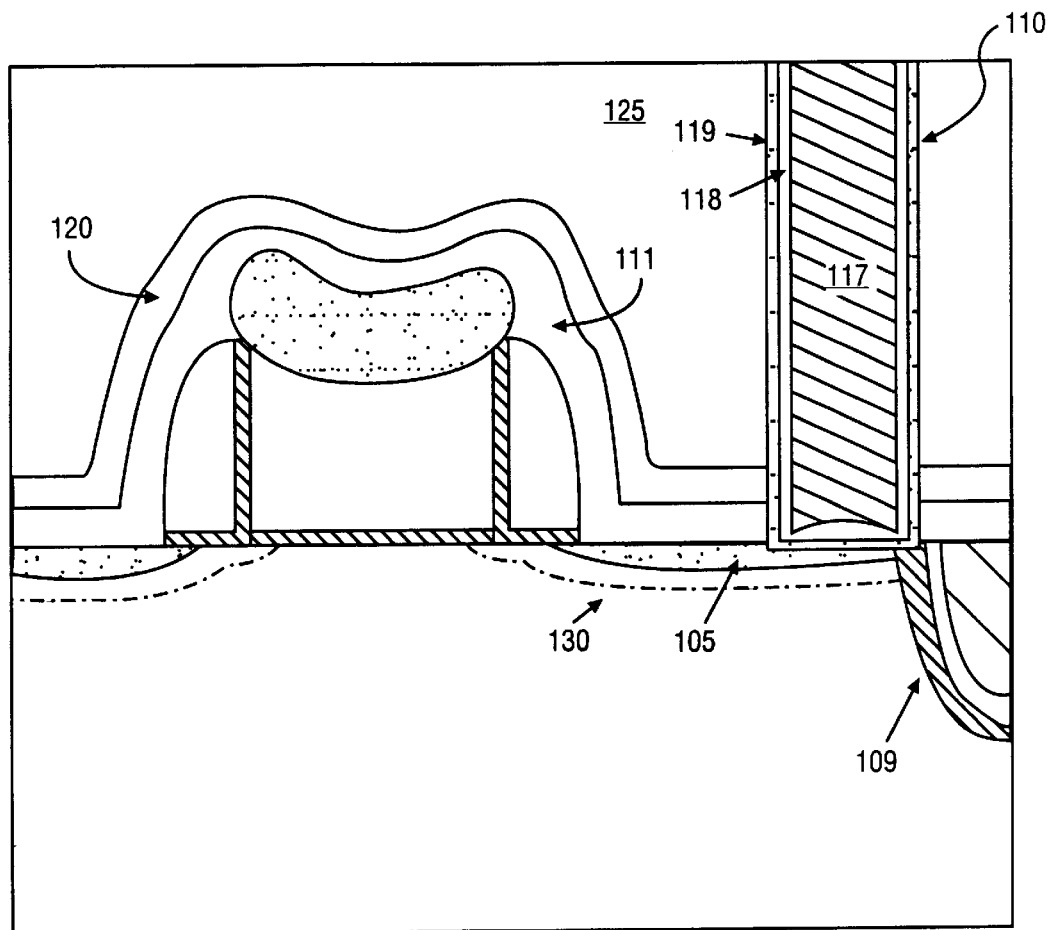


FIGURE 4

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