UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.;

MICRON TECHNOLOGY, INC.; and

SK HYNIX INC.

PETITIONERS

V.

ELM 3DS INNOVATIONS, LLC

PATENT OWNER

CASE IPR2016-00386

PATENT No. 8,653,672

DECLARATION OF ALEXANDER D. GLEW, Ph.D. REGARDING PATENT OWNER RESPONSE FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,653,672

I, Dr. Alexander D. Glew, hereby declare as follows:

1. I received a Bachelor of Science degree in Mechanical Engineering from University of California, Berkeley in 1985; a Master of Science degree in Mechanical Engineering from University of California, Berkeley in 1987; a Master of Science in Materials Science and Engineering from Stanford University in 1995; and Doctor of Philosophy degree in Materials Science and Engineering from Stanford University in 2003. A copy of my Curriculum Vitae ("CV") is attached to this report as **Exhibit A**.

2. The subject matter of my doctoral dissertation at Stanford University related to chemical vapor deposition ("CVD") of dielectric films. CVD generally consists of mixing two or more gases in a process reactor or chamber, and having the gases meet on the surface of a substrate to deposit a thin film. Many of the CVD films that I worked on were deposited on undoped silicon glass (SiO_2) and boron and phosphorous doped glass. For my doctoral dissertation, I constructed a CVD reactor. Then, I developed CVD processes for certain low-k dielectric films such as diamond like carbon and fluorinated amorphous carbon. Further, I characterized those thin films for their engineering properties, optical, electrical, and mechanical. Also, I analyzed the chemical composition of the thin films.

3. From 1987-1997, I was employed by Applied Materials, Inc. ("Applied Materials"), one of the world's largest and most advanced manufacturers of, among other things, CVD-related equipment. I was hired by the CVD division. The first process tool that I worked on was the Precision 5000 CVD tool. It was the first cluster tool, a tool with multiple CVD processing chambers. Because this tool demonstrated the major advance in tool architecture, multiple chambers attached to a central vacuum load lock chamber, resulting in the ability to process one workpiece at a time instead of in batch, it was eventually placed in the Smithsonian Institute, Natural History Museum.

4. From approximately 1987-1989, I was a Systems Engineer for Applied Materials. In this position, I designed semiconductor processing equipment, and worked with all aspects of the process tool. After a period of time, along with the product marketing manager, I signed off on every tool or machine that we shipped. My signature was required to ensure that the manufactured process tool and the chemical processes it produced matched what was required by the purchase order, and that it was built accordingly and safely.

5. Subsequent to being a Systems Engineer, from approximately 1989-1991, I was an Engineering Manager at Applied Materials responsible for customer engineering specials ("CES"). This included customization of equipment to meet

customer requests and specifications. The CES requests were diverse and covered nearly all aspects of the equipment, ranging from modifying process chambers, gas panels, wafer handlers/robotics, wafer storage elevators, sensors, vacuum systems, framing, and other. We worked on very tight schedules, and exercised disciplined project management. If our engineering work was not completed on time, and the materials not procured, then it would hold up the shipment of a multimillion dollar CVD process tool. Because we exercised disciplined project management, such delays rarely happened. We also had to accurately estimate the cost of our work, materials, and labor, because the CES projects were billed to the customer.

6. Next, I was the manager of the engineering design and support group for the CVD division of Applied Materials. In this capacity, I was in charge of all of the designers and drafters, generating all of the engineering drawings, and reviewing all of the engineering design work. I am intimately familiar with computer aided design ("CAD") and engineering documentation.

7. In the early 1990s, I was awarded the position of Core Technologist (one of only 15 in Applied Materials). My area of expertise was gas and chemical systems and components. The gas and chemical systems largely delivered ultra-high purity fluids to the process chambers and reactors. Components used in the systems included the following: valves, flow controllers, pressure regulators,

filters, purifiers, pressure transducers and related devices, and systems as a whole. As a core technologist, I was responsible for consulting with different divisions during the design of new products, testing fluid delivery components, reviewing invention disclosures, and reviewing papers written by Applied Materials personnel, holding meetings across the divisions for workers in the field, setting technology trends with suppliers, and reviewing technology trends with customers. Our different divisions included product lines such as at least CVD, ETCH, CMP, implant, TFT, and more. I also represented the company at industry consortium meetings. The core technology group met monthly with the president or other senior executives of the company.

8. From 1994-1996, I managed a project funded by SEMATECH[1] that I proposed to its factory working group. These efforts resulted in the publication of two SEMATECH technology transfer standards. The goal of this project was to develop industry standard methods to determine the effects of trace chemicals and contamination on semiconductor processing and on semiconductor equipment reliability. As part of this project, I designed, built, and tested gas delivery systems,

---

[1] SEMATECH stands for "Semiconductor Manufacturing Technology," a non-profit consortium that performs research into semiconductor manufacturing.

including the components contained therein, such as filter cartridges or assemblies, flow controllers, valves, and pressure regulators, and tested them to failure. Approximately 90% of wafer yield loss is from particles, so the industry was very interested in the particle effect of the chemical delivery system. I also tested the effect of micro-contamination in the process gas stream on tungsten CVD deposition and on metal etching. In some of the tests, we introduced controlled amounts of fluid into corrosive gas streams, and then measured the effect on system reliability, including particle generation.

9. As part of the SEMATCH project, we studied the effects of trace chemical contamination on tungsten CVD processing and on metal etching. We introduced trace chemicals into a standard process, measured the amounts of chemical in the process chamber by residual gas analyzer (RGA), and then measured the resulting film quality and properties by multiple techniques, and incorporation of the trace chemicals into the deposited layers.

10. From 1994-1997, I was a CVD Supplier Quality Engineering Manager at Applied Materials. During this time, I was the engineering manager responsible for the suppliers of the components of the fluid delivery systems, such as valves, flow controllers, pressure regulators, filters, purifiers, pressure transducers and

related devices, and systems as a whole. I tested and evaluated fluid delivery components. I both supervised and personally conducted this testing.

11. Since leaving Applied Materials in 1997 and until the present, I have served as president of Glew Engineering Consulting, Inc. ("Glew Engineering") of Mountain View, California. Glew Engineering provides consulting and engineering services relating to various technology or engineering areas, including CVD technology. My responsibilities at Glew Engineering include acting as a consultant and as a principal managing the company.

12. At Glew Engineering, I have worked on projects that include: project turnaround for failed projects, testing / metrology, gas panel design, integrated circuits failures, semiconductor equipment failures, Excimer laser sources for photolithography, KrF and Arf. I have assisted component suppliers, and equipment suppliers, and to a lesser extent, investors.

13. Glew Engineering's practice also includes multi-physics finite element analysis (FEA), computational fluid dynamics (CFD), and computer aided design (CAD) modeling. This is typically used for three dimensional modeling of equipment and processes, and analysis of the heat transfer, radiation, fluid flow, resultant stresses and strains from running such equipment and processes.

14. I am or have been a member of a number of professional organizations including: American Society of Mechanical Engineers, Materials Research Society, IEEE (Institute of Electrical and Electronics Engineers), and International Microelectronics and Packaging Society (IMAPS). In addition to being a member of these professional organizations, I have served on committees at SEMATECH.

15. I have authored or co-authored dozens of papers, reports, and presentations relating to semiconductor processing, semiconductor equipment, fluid delivery components in semiconductor processing, and equipment reliability.

16. I am an inventor of four issued U.S. Patents, Nos. 6,679,476, related to a high-purity control valve; 6,204,174, related to semiconductor processing; 7,118,090, related to a high-purity fluid control valve; and 9,224,626, related to design of CVD equipment components.

17. For more aspects of my qualifications and publications, see my CV, attached hereto as Exhibit A.

I. Technology Background

A. The Development Of Integrated Circuits

18. Today's high-density integrated circuits trace their lineage back to the first electronic computers of the 1940s, which used vacuum tubes to perform two

important electrical functions: switching (*i.e.*, turning electrical current on and off) and amplification (increasing the amplitude of a signal while retaining its electrical characteristics). (Ex. 2158 at 2). Because vacuum tubes were large, power-hungry, fragile, and had limited operating time, scientists soon developed solid-state transistors to perform the functions of and replace vacuum tubes. (Ex. 2158 at 3).

19. Where the earlier tubes used a vacuum to control the flow of electrons, the first solid-state devices instead used semiconducting material. (Ex. 2158 at 3). In addition, they were "discrete" because they had only one device (such a transistor, diode, capacitor, or resistor) per semiconductor chip. (Ex. 2158 at 2-3). As a result, more than one discrete semiconductor chip was needed to form a complete circuit. (Ex. 2158 at 2). Although discrete solid-state transistors were an improvement over vacuum tubes, the resulting circuits and computers were still relatively large. (*See* Ex. 2158 at 2-3).

20. In 1959 when Jack Kilby at Texas Instruments combined several transistors, diodes, and capacitors (five components total) to form a complete circuit on a single semiconducting chip, which itself was used as a circuit resistor. (Ex. 2158 at 4). Kilby's invention included an "integrated circuit," meaning an integration of a completed circuit in and on the same piece of semiconducting material. (Ex. 2158 at 4).

21. The Kilby chip differed from modern integrated circuit chips in that it was not flat, but instead connected its components using individual wires. (Ex. 2158 at 4-5). Scientists at Fairfield Camera developed a way of using metal patterns instead of individual wires to connect the circuit components, thereby modifying the Kilby integrated circuit to the form still prevalent today.

B. The Four Stages Of Integrated Circuit Manufacture

22. In 1959, Kilby's first integrated circuit had five components. (Ex. 2158 at 4). Through continued efforts to improve manufacturing processes to allow smaller components and circuits, by 1995, a single integrated circuit could include more than 250 million components. (Ex. 2158 at 5-6).

23. The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be generally divided into four distinct stages: (1) material preparation; (2) crystal growing and wafer preparation; (3) wafer fabrication; and (4) packaging. (Ex. 2158 at 13). Around the '672 Patent's filing date, each of these steps was typically done by separate manufacturers at separate plants. (Ex. 2158 at 12-13, 15-16).

24. In the first stage, the semiconductor material itself is created. (Ex. 2158 at 13). For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. (Ex. 2158 at 13).

25. In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters and then sliced into thin disks called "wafers." (Ex. 2158 at 13-14). In 1995, each of these generally round silicon wafers were generally 8 to 10 inches in diameter. (Ex. 2158 at 8). Wafer manufacturers typically also oxidize each wafer before shipping because the resulting dielectric layer of silicon dioxide protects the wafer during shipment. (Ex. 2158 at 65). In addition, because growing a dielectric layer on the wafer is usually the first step of wafer fabrication (the next manufacturing stage), buying a wafer that already has a silicon dioxide layer saves the fabricating company a manufacturing step. (Ex. 2158 at 65).

26. The third stage is wafer fabrication, during which individual integrated circuits are formed on the surface of the silicon wafer. (Ex. 2158 at 14). Around the filing date of the '672 Patent, several hundred to several thousand identical integrated circuits could be formed on the surface of a single wafer. (Ex. 2158 at 14). The area of the wafer occupied by a single integrated circuit is known as a "die" or "chip." (Ex. 2158 at 14).

27. Following fabrication, each of the dies on the wafer is electrically tested in a process known as a "wafer sort." (Ex. 2158 at 14). Wafer sort is sometimes considered as the last step in the wafer fabrication, sometimes as the

first step in the fourth and last manufacturing stage, which is packaging. (Ex. 2158 at 14).

28. In the packaging stage, the wafer is separated into individual dies. (Ex. 2158 at 14-15). Circa the '672 Patent's priority date, each individual die that passed the wafer sort typically would then be placed into an individual protective package. (Ex. 2158 at 14-15). This protective package not only protects the integrated circuit chip from damage and contaminants, it also provides an electrical lead system that allows the chip to be connected to a printed circuit board or directly into an electronic product. (Ex. 2158 at 15).

C. The Wafer Fabrication Stage Of Integrated Circuit Manufacture

29. The third manufacturing stage, wafer fabrication, takes several thousand individual steps, which can be divided into two primary phases: front end of the line and back end of the line. (Ex. 2158 at 14). In the front end of the line (FEOL), the transistors and other devices are formed in the wafer's surface. (Ex. 2158 at 14). In the back end of line (BEOL), the devices are wired together with metallization processes and the circuit is then sealed with a protective layer. (Ex. 2158 at 14).

30. The possibly thousands of steps involved in wafer fabrication are generally done using three categories of materials (conductors, semiconductor, and

dielectrics) in four basic operations (layering, patterning, doping, heat treatments). (*See* Ex. 2158 at 29-31, 71).

1. Wafer Fabrication Materials

31. A material's conductivity is its ability to allow the flow of electrical current, and materials may be divided into three categories based on their electrical conductivity: conductors, dielectrics, and semiconductors. (Ex. 2158 at 29-31).

32. In a conductor, electric current can flow freely; in other words, it has high conductivity and low resistance. (Ex. 2158 at 29). Materials that are good conductors include copper, silver, and aluminum. (Ex. 2158 at 29, 398-400).

33. A dielectric is a material at the opposite end of the conductivity spectrum from a conductor and has very low conductance and high resistance to the free flow of electrical current. (Ex. 2158 at 30). Dielectrics are therefore used as insulators in electrical circuits, and examples of dielectrics include glass (such as silicon dioxide) ceramics (such as silicon nitride), and plastics. (Ex. 2158 at 30, 36, 73).

34. As the name implies, semiconductors fall between conductors and dielectrics and have some conducting (and some resisting) ability. (Ex. 2158 at 31). Examples of semiconductors include silicon and germanium. (Ex. 2158 at 31).

2. Basic Wafer Fabrication Operations

35. To perform the possibly thousands of steps necessary for wafer fabrication, manufacturers generally use four basic operations in different sequences and variations: layering, patterning, doping, and heat treatments. (Ex. 2158 at 71).

36. Layering is the operation used to add thin layers to the wafer surface. (Ex. 2158 at 72). For example, the simple transistor structure shown in cross-section below shows a number of layers that have been added to the wafer surface. (Ex. 2158 at 72). The layers may be conductors, semiconductors, or dielectrics, and as discussed below, they can have a large variety of functions and be made in a large variety of ways. (Ex. 2158 at 72).

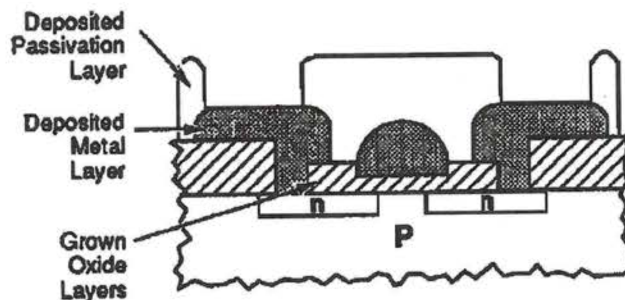


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

37. Patterning is the series of steps that results in the removal of selected portions of one or more layers of materials that were added during one or more prior layering operations. (Ex. 2158 at 72-73). This removal of select portions of layered material creates a pattern on the wafer surface. (Ex. 2158 at 72-73). As

illustrated below, the patterning may result in one or more holes in the layered material or one or more remaining islands of material. (Ex. 2158 at 72-73).

Figure 4.7 Patterning.

38. The repeated combination of layering and patterning in different sequences and variations is critical to the formation of the physical part parts of transistors, diodes, capacitors, resistors, and metal conduction systems in and on the wafer surface. Van Zant teaches:

> "these parts are created one layer at a time by the combination of putting a layer on the surface and removing portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts." (Ex. 2158 at 73).

39. Doping is the process that puts specific amounts of "dopants" in the wafer surface through openings in the surface layer created by patterning. (Ex. 2158 at 73-74). The "dopant" is a substance inserted into a pure semiconductor to

produce a desired electronic characteristic. (Ex. 2158 at 31-32). For example, doping pure silicon can create areas of very precise resistivity values in the semiconductor material. (Ex. 2158 at 32-34). Doping is also used to make polysilicon into a conductor or "metal;" this is a different application than doping to modify a semiconductor.

40. In addition, doping is used to create pockets in the wafer surface that are either rich in electrons or rich in electrical holes. (Ex. 2158 at 16). This is critical to the formation of the structure that makes semiconductor devices function, the "junction." (Ex. 2158 at 16). A transistor requires two junctions to work, and each junction is formed by creating a "n-type" region that is rich in electrons (has negative polarity) next to a "p-type" region that is rich in holes (or put another way, is missing electrons and thus has a positive polarity). (Ex. 2158 at 16).

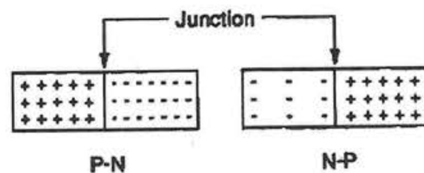


Figure 1.24 P-N and N-P junctions.

41. There are more than one doping techniques. One doping technique is thermal diffusion, which is a chemical process that takes place when the wafer is heated to roughly 1000°C and exposed to vapors of the proper dopant through a

hole created by layering and pattering. (Ex. 2158 at 74). Another doping technique is ion implantation, in which ionized dopants are shot at the wafer at high speeds, like a bullet from a gun. (Ex. 2158 at 74). Ion implantation is followed by a high temperature anneal. (See Ex. 2159 at 494).

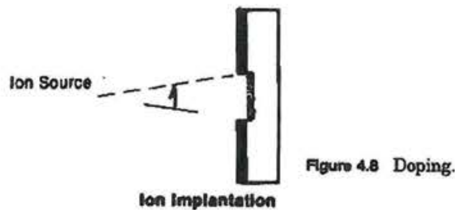


Figure 4.8 Doping.

42. Using thermal diffusion or ion implantation doping to create n-type and p-type pockets in the wafer surface allows the formation of the electrically active regions and N-P junctions required for operation of the transistors, diodes, capacitors, and resistors of the integrated circuit. (Ex. 2158 at 74).

43. Heat treatments are the operations by which the wafer is heated and then cooled to achieve specific results. (Ex. 2158 at 74). For example, one important heat treatment takes place after ion implantation. (Ex. 2158 at 75). Because implantation of the ionized dopant materials causes a disruption of the wafer's crystal structure, after the doping the wafer is heated to about 1000°C to

repair the disruption. (Ex. 2158 at 75). This type of restorative heat treatment is known as an "anneal." (Ex. 2158 at 75).

3. Exemplary Fabrication

44. To illustrate how these different categories of materials and basic manufacturing operations can be used in fabrication, the following is a simplified description of the primary steps for making a simple Metal Oxide Semiconductor (MOS) silicon-gate transistor structure.

45. As depicted below, the illustrative MOS silicon-gate transistor comprises three regions, specifically an n-type source region and an n-type drain region formed in a p-type wafer. (Ex. 2158 at 510-513). A doped polysilicon gate connects the source and the drain regions such that when threshold voltage is applied to the gate, current travels from the source region through the gate to the drain. (Ex. 2158 at 510-513).

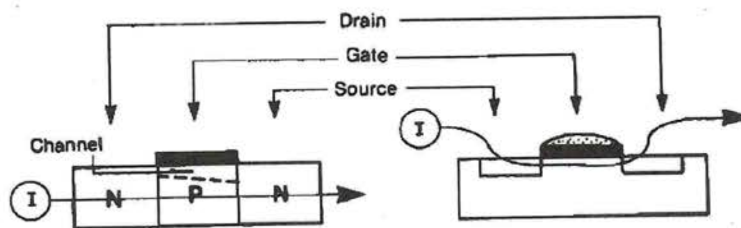
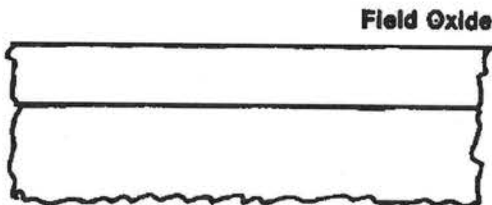


Figure 16.18 MOS transistor operation.

46. The following simplified steps (which could in fact take thousands of discrete steps) show how layering, masking, doping and heat treatments could be

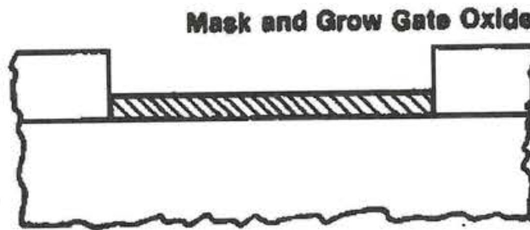
used with dielectrics, semiconductors, and conductors to make such a MOS silicon-gate transistor on a wafer surface. (Ex. 2158 at 510-513).

47. *Layering Operation*: To begin the front end of line phase of the fabrication, a layer of dielectric (silicon dioxide) is grown on the silicon semiconductor wafer. (Ex. 2158 at 80-81). This dielectric is called the field oxide and serves as a protective layer and doping barrier. (Ex. 2158 at 80-81).

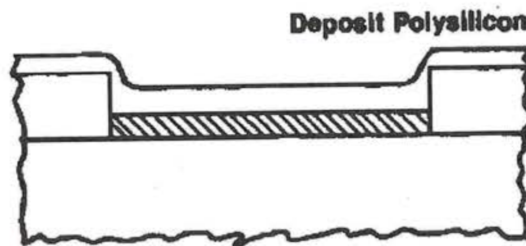


48. *Patterning Operation*: A patterning process is then used to create a hole in the field oxide dielectric that defines the location of the source, gate, and drain areas of the transistor. (Ex. 2158 at 80-81).

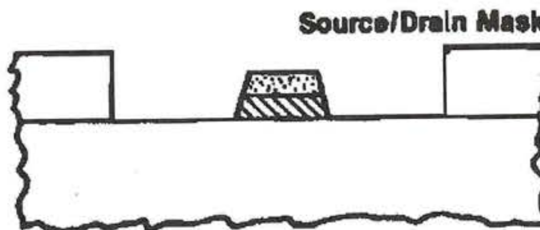
49. *Layering Operation*: After the hole is made in the field oxide, another dielectric is grown over the exposed silicon. (Ex. 2158 at 80-81). This silicon dioxide layer will serve as the gate oxide. (Ex. 2158 at 80-81).



50. *Layering Operation*: Another layering operation is then used to deposit a layer of polycrystalline silicon (polysilicon) over the gate oxide dielectric. (Ex. 2158 at 80-81). This semiconductor material will become part of the gate structure. (Ex. 2158 at 80-81).



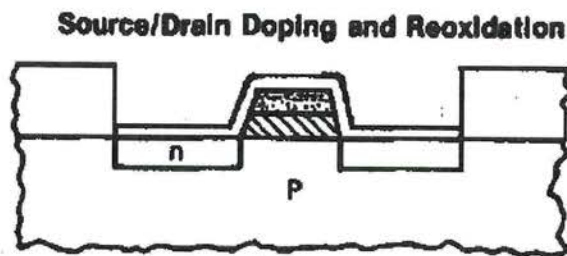
51. *Patterning Operation*: Next, patterning is used to create two openings in the masking oxide and polysilicon layers. (Ex. 2158 at 80-81). These openings define the source and drain areas of the transistor. (Ex. 2158 at 80-81).



52. *Doping Operation*: A doping operation is then used to create n-type pockets in the source and drain areas. (Ex. 2158 at 80-81).

53. *Layering Operation*: Following the doping, yet another layer of dielectric (silicon dioxide) is layered over the source and drain areas. (Ex. 2158 at 80-81).

Source/Drain Doping and Reoxidation



54. *Patterning Operation*: Patterning is then used to create holes (called "contact holes") through the dielectric in the source, gate, and drain areas. (Ex. 2158 at 80-81).

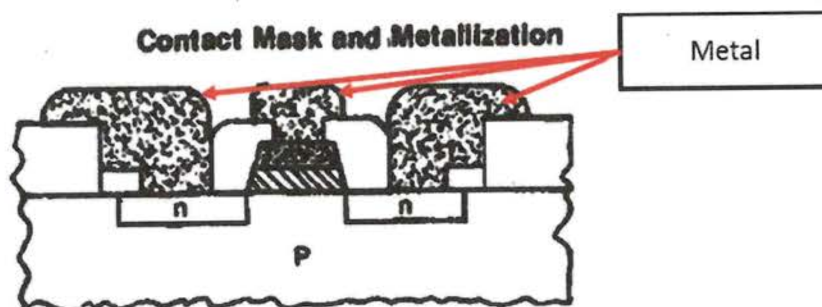
55. *Heat Treatment Operation*: The wafer is next heated at a very high temperature in a nitrogen gas atmosphere to create a layer of silicide over the exposed contacts in the source and drain regions. (Ex. 2158 at 80-81). This silicide is necessary to ensure a good electrical contact with the metal layer that will be deposited in the following phases. (Ex. 2158 at 80-81).

56. This is the end of the "front end of line" phase (the fabrication of the active and passive parts of the transistor and other components of the circuit), and

the next step marks the beginning of the "back end of line" phase (the addition of the metal systems necessary to connect the different components). (Ex. 2158 at 14, 395).

57. *Layering Operation*: In the first step of the back end of line phase, a thin layer of conducting material (such as an aluminum alloy) is deposited over the entire wafer. (Ex. 2158 at 80-81).

58. *Patterning Operation*: After the deposition of the aluminum alloy, that metallization layer is patterned so as to leave only the portions necessary to connect the surface components. (Ex. 2158 at 80-81).



59. *Layering Operation*: The final layer is a protective layer known as the "passivation layer" (not shown in the above figures), which is often a dielectric and is used to protect the components during testing, packaging, and use. (Ex. 2158 at 80-81).

60. As this transistor is being formed, the other components required for the circuit (such as diodes, resistors, capacitors, and other transistors) are also

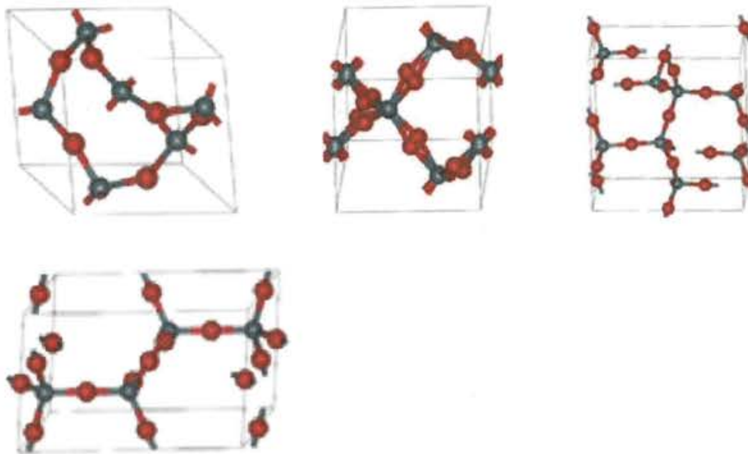
formed in other areas of the circuit in a similar manner, using similar operations. (Ex. 2158 at 82).

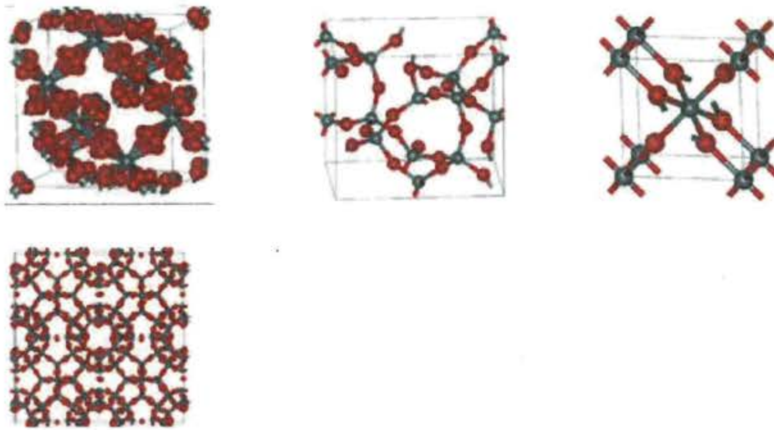
D. Different Techniques For Producing And Layering Dielectrics

61. As the foregoing example illustrates, different dielectric materials are layered throughout the fabrication process, with each dielectric layer having a different location, each being created at a different stage, and each serving a different specific purpose. (Ex. 2158 at 72-73, 79, 81-82). As a result, each layered dielectric needs to have certain specific properties, depending on where and when it is produced and the purposes it must serve. (Ex. 2162 at 47-48 of 895; *see also* Ex. 2164 at 78:21-79:1 ("There is likely quite a long list of factors that go into choosing between [dielectrics], and an engineer would weigh those using his knowledge and skills.")).

62. These dielectrics can be produced and layered using a large number of techniques, and the particular technique used will greatly impact the properties of the resulting dielectric (and, therefore, its usefulness for any particular dielectric layer and purpose). For example, dielectric silicon dioxide layers can be produced and applied in hundreds of different ways, each resulting in a silicon dioxide with different properties (and potential uses). (Ex. 2158 at 154; Ex. 2146 at 225, 306; Ex. 2159 at 55).

63. For these reasons, dielectrics are not created equal: each silicon dioxide dielectric, for example, may have the same chemical formula—SiO_2—but any one SiO_2 can have vastly different characteristics and behaviors from any other SiO_2, depending on how it is made and its resulting molecular structure and form. (Ex. 2165 at 72, 74-76 of 700; Ex. 2164 at 54:14-18). Indeed "silicon dioxide more than almost any material exists in many polymorphs." (Ex. 2163 at 9). The following are just a few examples of the many different structures that SiO_2 can take, depending on how it is made:





(Ex. 2163 at 9, 10 of 13).

64. There is "many variations" in the way silicon dioxides are formed, and the properties of the silicon dioxide "may be differen[t] depending on the details of the formulation and processing parameters" used. (Ex. 2164 at 133:8-20.) The primary techniques for forming and layering different types of dielectrics in semiconductor fabrication fall into one of two general categories: (1) growing dielectrics; and (2) depositing dielectrics. (Ex. 2158 at 72).

1. Growing Dielectrics Using Thermal Oxidation

65. To grow a dielectric is to form it from and on the material of the wafer surface itself. (Ex. 2158 at 157-158). There a numerous ways of growing dielectrics, including thermal oxidation and nitridation. (Ex. 2158 at 72).

66. Thermal oxidation is a prevalent technique for growing a silicon dioxide dielectric from a silicon wafer. (Ex. 2158 at 72, 157). Oxidation is performed by exposing a silicon wafer's surface to oxygen, which converts the

pure silicon into silicon dioxide. (Ex. 2158 at 157; Ex. 2159 at 53). This can be done by exposing a silicon wafer to air (dry oxidation) or water (wet oxidation). (Ex. 2159 at 53). In fabrication, this exposure is done at temperatures between 900 °C and 1200 °C. (Ex. 2158 at 157).

67. As a result of the growth conditions of thermal oxides, the resulting silicon dioxide possesses a very dense and pure molecular structure. (Ex. 2158 at; Ex. 2159 at 53). Purity is equivalent to having no or extremely low levels of unwanted chemical elements or molecules in the film and the exclusion of mobile ionic contaminants and particulates. (Ex. 2158 at 363).

68. Another characteristic of silicon dioxides grown using thermal oxidation is that they exhibit internal compressive stress when returned to lower temperatures. (Ex. 2159 at p. 58-59; Ex. 1040 at 128; Ex. 2160 at 233). Stress is an internal force (per area) on a material and may be either tensile or compressive. (Ex. 1040 at 114). If the force pushes inwardly along a layer's horizontal plane, it creates compression and is a "compressive" stress. (Ex. 1040 at 114). If the force pulls outwardly along a layer's horizontal plane, it creates tension and is a "tensile" stress. (Ex. 1040 at 114). Tensile stress can cause cracking far more readily than compression, while excess compressive stress can cause buckling. (Ex. 1040 at 114, 117; Ex. 2146 at 195 ("the preferred stress [in a dielectric] is

compressive...since dielectric films under tensile stress exhibit more of a tendency to crack")). Silicon fractures approximately four times more readily in tension than compression.

69. Other typical and important characteristics of silicon dioxides grown using thermal oxidation include: the ability to withstand high temperatures without changing its form; and properties of good adhesion (the ability to stick well to other materials such as a silicon wafer).

2. Depositing Dielectrics

70. In semiconductor fabrication, deposition refers to any process in which a material is physically deposited on the wafer. The list of methods for depositing dielectrics is extensive. Some primary deposition methods include evaporation, sputtering, spin-on processes, and chemical vapor deposition techniques ("CVD"). (Ex. 2158 at 72; Ex. 2159 at 121). These "CVD-deposited silicon dioxide films vary in structure and stoichiometry from thermally grown oxides." (Ex. 2158 at 382).

71. There are many different kinds of CVD techniques, each resulting in different dielectric qualities, but each shares some of the same basic processing cycles. First, wafers are loaded into a chamber, usually containing an inert atmosphere. Next, chemical vapors that include the atoms or molecules to be

deposited are introduced into the chamber and energy is added to cause a CVD reaction, resulting in the deposition of those atoms or molecules on the wafer surface. Once the appropriate amount of deposition has occurred, the chemical source vapors are flushed out and the wafers are removed. (Ex. 2158 at 366).

72. The many different CVD techniques can be categorized by the type of energy source used in the process: thermal energy or plasma energy. (Ex. 2158 at 366).

a. Thermal CVD

73. Thermal CVD can be done at either atmospheric pressure (known as atmospheric pressure CVD, or "APCVD") or at an artificially lowered pressure (low pressure CVD or "LPCVD"). (Ex. 2158 at 366). In addition, the source of thermal energy can come from a variety of different sources, such as tube furnaces, hot plates, and RF induction. (Ex. 2158 at 366).

74. Another variable is how the heat is applied during the CVD process. (Ex. 2158 at 366). In "cold-wall" thermal CVD, the wafer itself is directly heated and the walls of the chamber remain cold (or cooler). (Ex. 2158 at 366). In "hot-wall" thermal CVD, the heat is applied to the wafers, the wafer holder, and the chamber walls. (Ex. 2158 at 366).

75. Thermal CVD processes can be performed at high temperatures (800 °C -1000 °C) to deposit a silicon dioxide dielectric. (Ex. 2159 at p. 130). When performed at these high temperatures, thermal CVD can result in silicon dioxide that has similar properties to a thermally grown silicon dioxide, such a purity, compressive strength, resistance to high temperatures, and adhesion. (Ex. 2159 at 140). For this reason, high temperature thermal CVD is often used as substitute for thermal oxidation where oxidation cannot be used (such as, for example, where there is no available silicon surface on which to grow the desired silicon dioxide).

b. Plasma Enhanced CVD

76. A chemical vapor deposition process that uses plasma as an energy source is known as Plasma-Enhanced CVD ("PECVD"). PECVD is a vacuum process LPCVD (it is performed at low pressure, not atmospheric pressure), and because of the supplemental energy provided by the use of plasma, is able to be performed at low temperatures of 400°C or less. (Ex. 2158 at 373; Ex. 2159 at 130). Plasma deposited layers contain higher percentages of extraneous reaction components that would be expected of high-temperature CVD deposition.

77. Because plasma CVDs are performed at low temperatures, they can be used where the use of higher temperatures may adversely affect previously fabricated parts and components. (Ex. 2158 at 373). However, this comes at a

cost, as dielectrics, including silicon dioxides, deposited using PECVD include impurities that make them unusable for a variety of applications requiring higher purity. (Ex. 2160 at 233; Ex. 2158 at 363).

78. In addition to being relatively impure, silicon dioxide dielectrics deposited using PECVD also are unable to withstand the higher temperatures used in front of line processing without changing form. (Ex. 2169 at 29-30). Separately, they also will suffer from higher dielectric constants, lack of planarization, susceptibility to pinholes, slow deposition rates, and high cost of process gases. (Ex. 2162 at 303). In addition, low processing temperatures result in a soft and porous deposit. (Ex. 2159 at 140). Moreover, when using PECVD to deposit tensile films, it was known that the "[l]ow density tensile films tend to pick up water and form SiOH groups." (Ex. 1049 at 5). This causes degradation of electrical and mechanical properties.

79. At the time of the '672 Patent's priority date, it was typical to try to alleviate some of these problems by depositing PECVD layers in moderate compressive stress (rather than tensile) to enhance conformality, reduce pinhole counts, and improve adhesion. (Ex. 2133 at 10, 11; Ex. 1040 at 106). Further, Novellus taught creating compressive stressed films with PECVD because, unlike tensile films, "films deposited with an intrinsic compress stress are stable and are

even able to withstand boiling water without increasing the SiOH content or absorbing water." (Ex. 1049 at 5).

E. Different Kinds and Uses of Dielectrics

80. As I discussed above, the properties and behaviors of a layered dielectric such as silicon dioxide will vary greatly based on which of the many available layering techniques is used. The chosen method of layering can affect at least the following properties of a dielectric: (1) dielectric constant (the dielectric's ability to store electrical energy in an electric field), (2) breakdown field strength, (3) leakage, (4) surface conductance, (5) moisture absorption or permeability to moisture, (6) stress, (7) adhesion to aluminum, (8) adhesion to dielectric layers above or below, (9) stability, (10) etch rate, (11) permeability to hydrogen, (12) amount of incorporated electrical charge or dipoles, (13) amount of impurities, (14) quality of step coverage, (15) the thickness and uniformity of the film, (16) ability to provide good doped uniformity across a wafer, (17) defect density, (18) amount of residual constituents that outgas during later processing. (Ex. 2146 at 195). And where a PMD is deposited a subsequent anneal process will be performed. (*See* Ex. 2169 at 29 ("Subsequent high-temperature annealing at 700˚C-1000˚C causes densification of the oxide films, and leads to chemical properties similar to thermal oxides. Such a densification process not only changes film thickness and

film density … but also causes chemical reconstruction of the film [], leading to compressive film stress.")).

81. All of these properties are taken into consideration when selecting which material and layering method is used to produce a particular dielectric layer, and that selection is highly context dependent. Which factors are the most important—and thus which techniques can and cannot be effectively used—will depend on the type and use of the dielectric desired, such as whether the dielectric layer being produced is intended to be used, for example, as a field oxide, gate oxide, pre-metal dielectric, intermetal dielectric, or passivation layer. (Ex. 2158 at 154; Ex. 2146 at 225, 306; Ex. 2159 at 55).

1. Front End Of Line Dielectrics

82. As I discussed above, the wafer fabrication stage can be divided into two primary phases: front end of the line and back end of the line. (Ex. 2158 at 14). In the front end of the line (FEOL), the transistors and other devices are formed in the wafer's surface. (Ex. 2158 at 81). Types and uses of dielectrics produced and layered during the front end of line phase include field oxides, gate oxides, dopant barriers, and pre-metal dielectrics. (Ex. 2158 at 81).

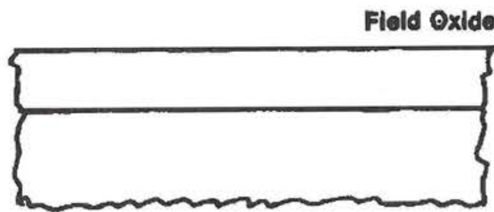
83. Because of their functions and placement, these types/uses of dielectrics share some similar basic requirements. For example, due to their direct

contact or close proximity to the surface of the silicon wafer, each must be extremely pure. In addition, because FEOL steps are often performed at high temperatures, dielectrics that are formed during front end of line phase must be able to withstand the multiple high-heat steps of around 1000ºC without altering their structure and properties. (Ex. 2169 at 29-30). Because of these requirements, growth by thermal oxidation or nitridation is the favored technique for layering dielectrics during FEOL. (*E.g.*, Ex. 2160 at 75 ("the best and most dense oxides are produced by thermal oxidation")).

84. If the dielectric cannot be grown (for example, because there is no an available silicon surface on which to grow the desired silicon dioxide), then high temperature thermal CVD is typically used. Because Plasma CVD (such as that used in *Leedy '695*) results in low purity dielectrics that cannot withstand high heat without changing their structure or properties (among other disadvantages), Plasma CVD cannot be used to produce FEOL dielectrics such as field oxides, gate oxides, dopant barriers, and pre-metal dielectrics.

a. Field Oxide Dielectrics

85. A field oxide is a layer of dielectric (such as silicon dioxide) that is grown covering the top surface of the semiconductor wafer during the initial steps of FEOL. (Ex. 2158 at 80-81). They are very dense (nonporous) and very hard.



86. A field oxide dielectric layer serves a number of purposes, including protecting the silicon wafer. (Ex. 2158 at 140). The field oxide also serves to define the active regions that are later subject to doping and to prevent channels from forming between adjacent transistors. (Ex. 2158 at 81). The field oxide must be thick enough to prevent a phenomenon known as induction. Induction can occur when the oxide is thin enough to allow an electrical charge in a metal layer to cause a buildup of charge in the wafer surface. Surface charge can cause shorting and other unwanted electrical effects. (Ex. 2158 at 156).

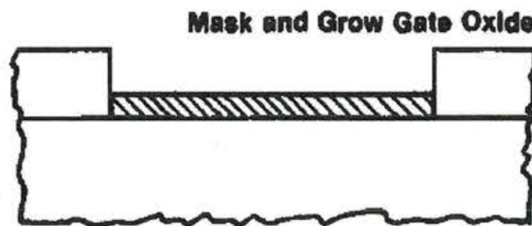
87. Because silicon dioxide field oxides are in direct contact with the silicon, a high degree of purity is required to avoid degradation of the silicon. Moreover, field oxides must be able to adhere well to the semiconductor wafer's surface and withstand subsequent heating steps of around 1000°C or higher without significant change in their structure and properties. (Ex. 2169 at 29-30).

88. As a result, field oxides must be grown using techniques such as thermal oxidation or nitridation. Plasma CVD (such as that used to produce the *Leedy '695* dielectric) cannot be used to produce and layer a field oxide because

the resulting dielectric would not (1) be sufficiently pure; (2) have the ability to adhere sufficiently to the semiconductor wafer; and (3) be able to withstand high temperatures of the remaining FEOL steps without changing its form. Additionally, Plasma CVD cannot be used because positive ions (and energetic neutral species) present in the plasma can strike and damage the wafer itself. (Ex. 2159 at 139).

b. Gate Oxide Dielectrics

89. During FEOL, a portion of the field oxide dielectric is etched away over the gate region of the wafer surface so that a dielectric such as a silicon dioxide can be grown directly on the wafer surface to form the gate of the transistor. This silicon dioxide layer is known as the gate oxide. (Ex. 2158 at 80-81, 156).



90. Gate oxide growth is substantially more involved than other oxide growth steps. (Ex. 2159 at 48). After the gate regions are cleared of thick field oxide, a sacrificial oxide (dummy oxide) is grown and stripped before gate oxidation to clean the silicon. (Ex. 2159 at 49). The gate oxide dielectric then must

be grown to a thickness chosen specifically to allow induction of a charge in the gate region under the oxide. (Ex. 2158 at 142).

91. Moreover, gate oxides, even more so than field oxides, need to be exceptionally pure. (Ex. 2158 at 173). Silicon dioxide gate oxides are therefore thermally grown at about 1000ºC, and "[t]he growth of the gate oxide is a critical step, as defect-free, very thin (15-100 nm), high quality oxide without contamination is essential for proper device operation." (Ex. 2146 at 331).

92. Thus, as with field oxide dielectrics, gate oxide dielectrics must be using techniques such as thermal oxidation or nitridation. Plasma CVD (such as that used to produce the *Leedy '695* dielectric) cannot be used to produce and layer a gate oxide dielectric because the resulting dielectric would not (1) be sufficiently pure; (2) have the ability to adhere sufficiently to the semiconductor wafer; and (3) be able to withstand high temperatures of the remaining FEOL steps without changing its form. Also, Plasma CVD also cannot be used because positive ions (and energetic neutral species) present in the plasma can strike and damage the wafer itself. (Ex. 2159 at 139).

c. Pre-metal Dielectrics

93. Dielectrics that are layered between the transistors and other devices on the surface of the silicon wafer and the first overlaying metal layer are called

"pre-metal dielectric" (PMD). (Ex. 2158 at 81, 397; Ex. 2146 at 188-189). Before that metal layer is deposited, patterning is used to create holes ("contact holes") through the pre-metal dielectric in areas where conductivity is required, such as over the source, gate, and drain of a MOS transistor. (Ex. 2158 at 80-81). Before metal is deposited, the wafer is heated at a very high temperature in a nitrogen gas atmosphere to create a layer of silicide over the exposed contacts in the source and drain regions to ensure that those areas will make good electrical contact with the metal layer that will be deposited in the following phases. (Ex. 2158 at 80-81).

94. Because of its proximity to the silicon and components, a pre-metal dielectric must have relatively high purity. In addition, because it will be exposed to high levels of heat after it is layered and planarized (made level), a pre-metal dielectric must also be able to withstand high temperature reflows of over 800-1000ºC. (Ex. 2146 at 194-95, 208). Other characteristics and behaviors a pre-metal dielectric should possess include easy reflow planarization, and low moisture absorption. (Ex. 2146 at 195, 261-62) (*See* Ex. 2159 at 143 – 145).

95. For these reasons, it is preferred to produce and layer a pre-metal dielectric by growing it using thermal oxidation or, where thermal oxidation cannot be used, by depositing it using high temperature thermal CVD. Plasma CVD cannot be used to produce and deposit a silicon dioxide pre-metal dielectric

because the resulting dielectric would not (1) be sufficiently pure; (2) have the ability to adhere sufficiently to the semiconductor wafer; and (3) be able to withstand high temperatures of the remaining FEOL steps without changing its form. Plasma CVD also cannot be used because positive ions present in the plasma can strike and damage the wafer itself. (Ex. 2159 at 139).

2. Back-End-Of-Line Dielectrics

96. Turning now to the back end of line (BEOL) phase of fabrication, the devices are wired together with metallization processes and the circuit is then sealed with a protective layer. (Ex. 2158 at 14). The switch from front end of line to back end of line is marked by the deposition of the first metallization layer, and is performed at lower temperatures. (Ex. 2146 at 194).

97. Many devices require more than one level of metallization. The device below has two levels of metallization, labeled "Metal 1," and "Metal 2" respectively as shown below. (Ex. 2146 at 188). Connecting those levels are columns of metal, labeled as "vias."

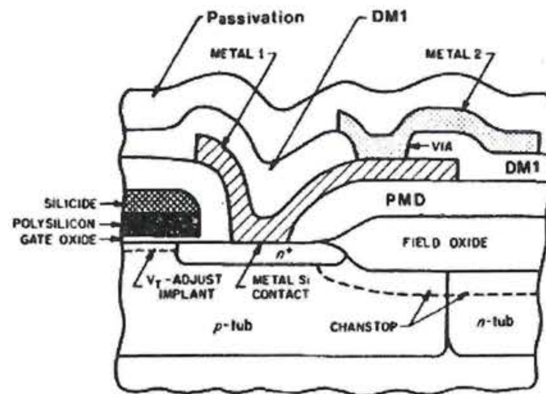


Fig. 4-7 Terminology of double-level-metal interconnects.

98. Dielectric materials produced and layered during the BEOL phase of fabrication include intermetal dielectrics (which are layered between two levels of metallization) and passivation dielectrics (where the passivation layer covering and protecting the top of the device is a dielectric). (Ex. 2158 at 397-98). In the illustration above, the intermetal dielectric is labeled DM1. (Ex. 2146 at 188).

99. Because the metals used in metallization have relatively low melting temperatures, the BEOL is done at much lower temperatures than the FEOL processes. (Ex. 2158 at 398-99). This affects the techniques available for layering and producing dielectrics in the BEOL phase.

a. Intermetal Dielectrics

100. Intermetal dielectrics are used to electrically isolate one level of conductor from another in multilevel-interconnect systems. A person of ordinary skill at the time of the invention would have known that the list of requirements for

these dielectric layers is "long and stringent." (Ex. 2146 at 194). The desired properties for intermetal dielectrics include: (1) low dielectric constant; (2) compressive stress; (3) good adhesion to aluminum; (4) stable; (5) good step coverage; (6) good uniform thickness; (7) low density of pinholes and particles; high breakdown field strength; (9) low leakage; and (10) easily etched. (Ex. 2146 at 195).

101. At the time of the '672 Patent's filing date, Wolf taught that intermetal dielectrics should be in compressive stress "since dielectric films under tensile stress exhibit more of a tendency to crack." (Ex. 2146 at 195). In addition, conventional thinking was that intermetal dielectrics had to be formed to have moderate compressive stress in order to balance out the moderate tensile stress of the metal layers: "moderate compressive stress [is] desirable to partially compensate tensile stress in the metal interconnects, thus avoiding film cracking." (Ex. 2160 at 233).

b. Passivation Dielectrics

102. Following fabrication of the final metal layer, a passivation layer is deposited over the entire surface of the wafer. (Ex. 2158 81-82). "This is an insulating, protective layer that prevents mechanical and chemical damage during assembly and packaging." (Ex. 2146 at 273). At the time of the invention,

passivation layers were typically silicon nitride because "it provides an impermeable barrier to moisture and mobile impurities (e.g., sodium) and also forms a tough coat that protects the chips against scratching." (Ex. 2146 at 274). This contrast sharply with silicon oxide dielectrics formed by Plasma CVD, which are typically porous and soft and therefore unsuitable to be used as a passivation layer. Moreover, because passivation layers are the outermost layers and serve to protect the chip, they must resist cracking and water absorption, and are therefore deposited in a compressive stress, unlike the tensile dielectric of Leedy '695. (Ex. 1049 at 3, 5).

II. The '672 Patent

103. I understand the '672 Patent is titled "Three Dimensional Structure Memory" and issued to Glenn J. Leedy, President of Patent Owner Elm 3DS Innovations, LLC. (Ex. 1001 at Title Page).

104. I understand the '672 Patent has an effective filing date of April 4, 1997, and is part of a large family of related continuation applications and issued patents sharing the same substantive specification. (Ex. 1001 at Title Page).

A. The '672 Patent Discloses Novel Substantially Flexible Stacked Circuit Layers

105. As explained in the '672 Patent, at the time of its filing date (and indeed at all times prior to and since), integrated circuit manufacturers sought to

increase the number of circuit devices they were able to fit in the area of an integrated circuit while still allowing for increased processing speed and performance of the resulting integrated circuit. (Ex. 1001 at 1:10-24, 2:44-63). Other overriding goals were lower fabrication costs (more integrated circuits per wafer) and greater yields (more non-defective integrated circuits per wafer). (Ex. 1001 at 1:42-58, 2:44-63).

106. The '672 Patent describes that one approach to reaching these and other goals is to stack and connect integrated circuits on top of one another (a "Three Dimensional Structure"), thereby allowing the inclusion of more devices per single integrated circuit footprint. (*E.g.*, Ex. 1001 at 2:21-34). The '672 Patent also describes that additional benefits can be gained by dividing functionality between the different circuit layers, with one layer containing the controller circuitry and the other layers containing memory circuitry. (*E.g.*, Ex. 1001 at 3:1-3, 4:17-24). The benefits identified for this approach include the ability to fabricate the memory circuit layers separately and independently from the controller circuit layer, thereby allowing the different manufacturing methods to be used for and tailored to each type of circuit layer. (*E.g.*, Ex. 1001 at 6:16-34; *see also* Ex. 1001at 6:7-15).

107. The '672 Patent also described a novel structure for such stacked integrated circuits, including flexible semiconductor substrates that could be stacked atop each other to make a flexible stacked circuit. (*E.g.*, Ex. 1001 at 3:5-10, 4:22-24, 6:16-29, 7:14-23, 8:34-44, 10:28-67). For example, the '672 Patent describes simultaneously making individual flexible memory circuits, each having a flexible semiconductor substrate, and stacking those flexible memory substrate circuit layers. (*E.g.*, Ex. 1001 at 6:16-29, 7:14-23, 8:34-44, 10:28-67). As described in the '672 Patent, those flexible memory substrates circuit layers could be stacked on a common substrate, which itself could be another flexible memory substrate circuit layer or a common (shared) flexible controller substrate circuit layer. (*E.g.*, Ex. 1001 at 7:14-23, 8:34-44, 10:28-67).

B. The '672 Patent Discloses A Novel Method And Structure For Substantially Flexible Stacked Circuit Layers

108. In addition, the '672 Patent discloses preferred structures and techniques for making such flexible semiconductor substrate circuit layers, such as a thinned substrate that is polished and made with a dielectric in low tensile stress. One such flexible semiconductor substrate circuit layer is depicted in Figure 4, reproduced below:

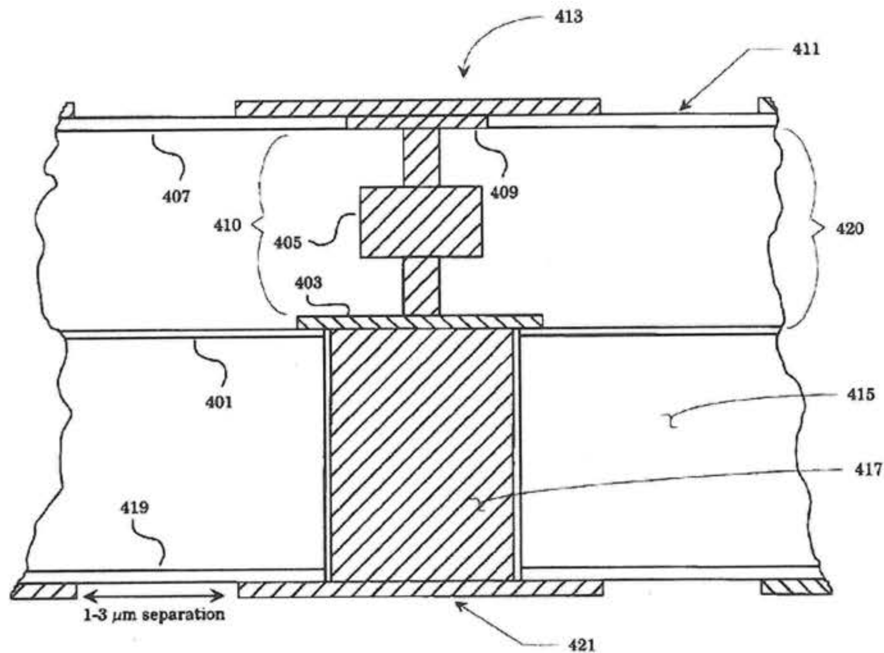


Figure 4

109. As depicted in Figure 4, this illustrative flexible semiconductor substrate circuit layer comprises a silicon substrate 415 that has been thinned and polished, as well as intermetal dielectric layers 420 that are in low tensile stress. The polishing removes defects that would cause the semiconductor substrate circuit layer to crack rather than flex when released from a rigid support substrate.

110. The use of the low tensile stress dielectric likewise allows the semiconductor substrate circuit layer to flex instead of crack when released from a rigid support substrate. The use of such a low tensile stress dielectric was against the conventional wisdom of the time, which held that such dielectrics should not be used for a number of reasons. For example, conventional wisdom included that:

- intermetal dielectrics should be in compressive rather than tensile stress "since dielectric films under tensile stress exhibit more of a tendency to crack" (Ex. 2146 at 195);
- Plasma-enhanced CVD should be used to change "intrinsic film stress from tensile to compressive [to] increase the film density" "in order to reduce stress cracking" (Ex. 1049 at 3);
- intermetal dielectrics should be formed to have moderate compressive stress in order to balance out the moderate tensile stress of the metal layers: "moderate compressive stress [is] desirable to partially compensate tensile stress in the metal interconnects, thus avoiding film cracking" (Ex. 2160 at 233); and
- "[l]ow density tensile films tend to pick up water and form SiOH groups. This causes degradation of electrical and mechanical properties." (Ex. 1049 at 5).

111. Conventional wisdom warned against using tensile stress dielectrics rather than a compressive one because "the compressive stress in the film cancels the intrinsic tensile stress of metal films and produces a flat substrate." (Ex. 2162 at 303).

C. The Asserted References

112. Each of the Instituted Grounds relies on combining the Leedy '695 reference with one of two primary references, either *Bertin* or *Yu*.

1. Leedy '695

113. I understand Leedy '695 issued to the same inventor as the challenged patent, and is titled "Membraned dielectric isolation IC fabrication," and was incorporated by reference into the '672 Patent. *Leedy '695* discloses a low tensile stress dielectric membrane, which Petitioners argue would have been obvious to substitute for specific dielectrics in the *Bertin* and *Yu* references.

114. Leedy '695 discloses producing and using a low tensile stress dielectric membrane in the context of an "approach to IC fabrication [that] falls under the generic industry-established title known as Dielectric Isolation (DI)." (Ex. 1006 at 1:21-23). Dielectric isolation is an alternate technique for producing integrated circuits that is distinctly different from – and was considered distinctly inferior to—the semiconductor substrate techniques discussed above; in the '672 Patent; and the *Bertin* and *Yu* references. (Ex. 2146 at 12, 67).

115. *Leedy '695*'s approach to dielectric isolation is a free-standing, flexible membrane, as opposed to a traditional rigid semiconductor substrate. (Ex.

1006 at 1:7-8). *Leedy '695* calls these "circuit membranes," which, as illustrated in *Leedy '695* Figure 3a, is "typically framed or suspended or constrained at its edges by a substrate frame or ring" like a drum. (Ex. 1006 at 34-37).

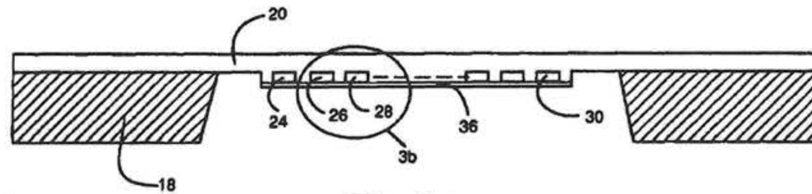
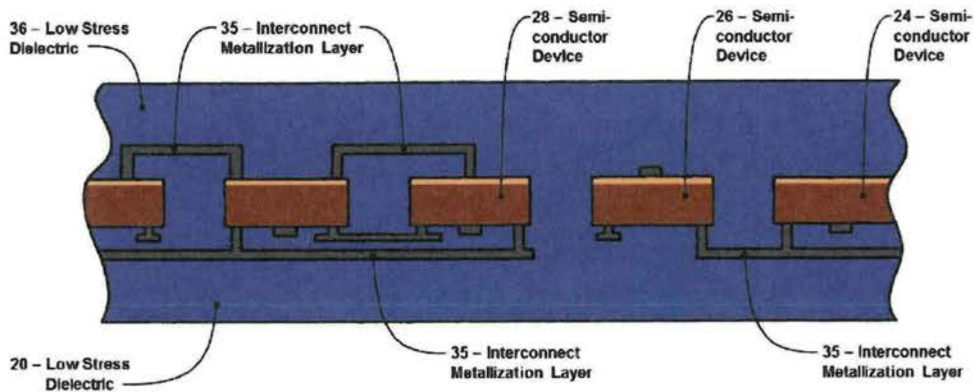


Fig_3a

116. As illustrated in annotated Figure 3, each membrane does not include a semiconductor substrate but instead encapsulates tiny silicon transistor "islands" in a sea of low tensile stress dielectric. (Ex. 1006 at Figure 3B, 3:23-33, 24:20-32).



a. Leedy '695's Low Tensile Stress Dielectric

117. The *Leedy '695* low stress dielectric:

- is created using Plasma-Enhanced CVD;
- is in tensile, not compressive, stress;

- cannot withstand temperatures in excess of approximately 400°C.

118. *Plasma-Enhanced CVD*: Notably, the *Leedy '695* low tensile stress dielectrics are created at low temperatures using plasma-enhanced CVD. (Ex. 1006 at 11:29-31). *Leedy '695* explains that "these membranes were produced on Novellus Systems Inc. (San Jose, Calif.) Concept One dielectric deposition equipment" (Ex. 1006 at 11:29-31), which was a commonly available plasma-enhanced CVD system. Novellus taught that "[l]ow density tensile films tend to pick up water and form SiOH groups. This causes degradation of electrical and mechanical properties." (Ex. 1049 at 5). Novellus was using PECVD to create compressive stressed films because, unlike tensile films, "films deposited with an intrinsic compressive stress are stable and are even able to withstand boiling water without increasing the SiOH content or adsorbing water." (Ex. 1049 at 5). Despite the problems inherent with tensile films, *Leedy '695* uses PECVD to create *only* tensile films. This is because tensile films, despite their shortcomings, are needed to provide structure to free-standing flexible membranes. (Ex. 1006 at 5:68-6:5).

119. *Low Tensile Stress*: If these free-standing membranes were in compressive stress, which is the traditional stress condition for silicon dioxide thin films, the membranes would lack the necessary surface flatness and structural integrity needed for subsequent device fabrication steps. (Ex. 1006 at 5:68 – 6:5).

To give structure to the free-standing membrane, therefore, *Leedy '695* required the free-standing membrane to be in tensile stress. (Ex. 1006 at 5:68 – 6:5. ("If the membrane is not in tensile stress, but in compressive stress, surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane.") .

120. *Inability To Withstand High Temperatures: Leedy '695* describes that the temperature threshold of its low tensile stress dielectric is not much higher than 400°C: the "membrane is able to withstand a wide range of IC processing techniques and processing temperatures (of at least 400°C) without noticeable deficiency in performance." (Ex. 1006 at 2:37-40). Even absent this disclosure, one of ordinary skill would understand that a dielectric deposited by PECVD at 400°C (like the *Leedy '695* dielectric) would not be able to withstand temperatures above deposition temperature without changing its form to compressive stress. For example, Wolf states that for the PECVD-deposited silicon nitride deposited at 300°C, the thermal stability is "variable" at temperatures exceeding 400°C. (Ex. 1040 at 192). And Leedy '695 is a silane based PECVD having poor gap fill. (Ex. 2133 at 438).

b. Applications Of The Leedy '695 Circuit Membrane

121. *Leedy '695* describes several applications for its circuit membranes, including an "electrical interconnect" and in "three-dimensional [integrated circuit] structures." (*E.g.*, Ex. 1006 at Abstract, 25:15-26:68, 45:49-47:9).

122. *Electrical Interconnect*: The Abstract states that the membrane can be used as "an electrical interconnect for conventional integrated circuit die bonded thereto." In this application, the membrane is manufactured to encapsulate interconnects rather than active circuitry. (Ex. 1006 at 25:15-42). In this application, illustrated in Figure 13a below, various individual integrated circuit die 322a, 322b, and 322 c (which were already fabricated using conventional fabrication methods) can be attached to the Leedy membrane and thereby connected to one another using that membrane's internal interconnects. (Ex. 1006 at 25:33-41, 25:58-62).

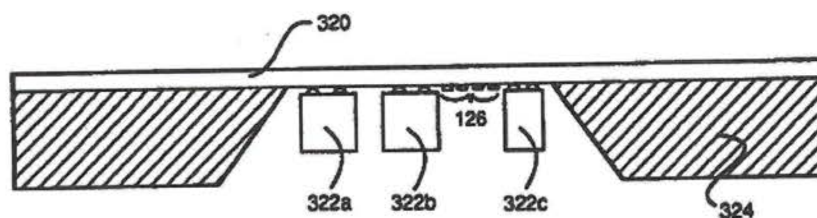


Fig_13a

123. This membrane is not serving as an intermetal dielectric in the fabrication of an integrated circuit on a semiconductor substrate; rather, it is being

used in the packaging phase to connect and hold various integrated circuits that have already been fabricated through conventional means. (*See, e.g.*, Ex. 1006 at 25:33-41, 25:58-62).

124. *Three-Dimensional IC Structures*: In another application, the free-standing membranes may be stacked on top of one another to form a three-dimensional integrated circuit structure. (Ex. 1006 at 46:59-47:10). In one embodiment of this application shown in Figure 32c below, the stack circuit members may be bonded to a common "rigid" substrate during final packaging. (Ex. 1006 at 46:59-47:10).

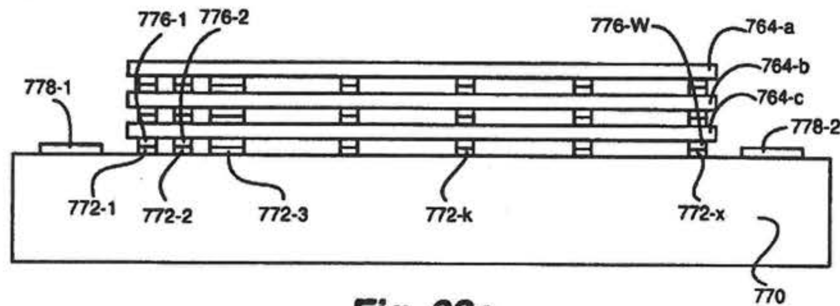


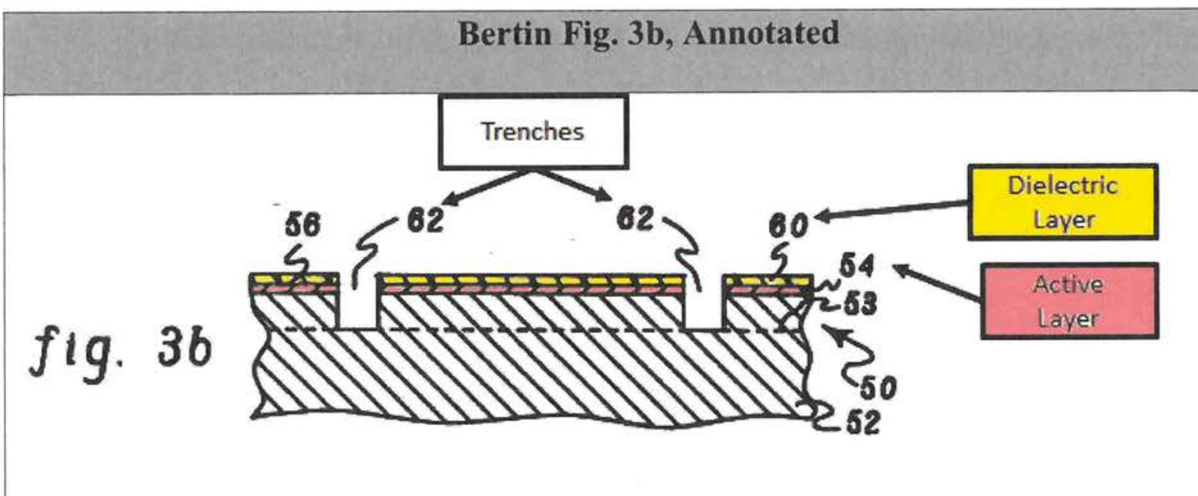
Fig_32c

2. Bertin

125. *Bertin* describes "semiconductor chips interconnected at least partially by means of a plurality of metalized trenches in the semiconductor chips." (Ex. 1004 at 1:7-15).

a. Bertin's "dielectric layer 60" Was Grown Using Thermal Oxidation And Could Not Be Produced And Layered Using Plasma-Enhanced CVD

126. As depicted in *Bertin*'s Figure 3b reproduced below, *Bertin* describes a "dielectric layer 60." Instituted Ground 1a is based on Petitioners' argument that it was obvious to replace *Bertin*'s dielectric layer 60 with the *Leedy '695*'s low-tensile-stress Plasma-CVD dielectric.



Bertin Fig. 3b, Annotated

127. With regards to the composition, purpose and ultimate utility of dielectric layer 60, Bertin is unreliable. Layer 60 is present in fig. 3a and is shown to be etched as a part of trenches 62 in fig. 3b. However, in fig. 3c layer 60 reappears on top of polysilicon plug 64. There is no reference in the text that discloses the regrowth of layer 60 at this stage. Furthermore, layer 60 is no longer present in fig. 3d, having been replaced in the figure with completed

oxidation/metallization layer 63. Presumably it is not in the final product. Bertin does not specify whether layer 60 is removed or is incorporated into layer 63. Although Bertin's representation of dielectric layer 60 is unreliable, for the purposes of rebutting the Petitioners' argument I will adopt their interpretation of layer 60. Petitioners' do not attempt to identify the type or use of *Bertin*'s "dielectric layer 60." However, a person of ordinary skill in the art would understand that dielectric layer 60 is a high-purity silicon dioxide grown via thermal oxidation at high temperatures during the front-end-of-line phase of fabrication. First, *Bertin* specifies that dielectric layer 60 is "grown," not deposited, and is a silicon dioxide. (Ex. 1004 at 3:60-62). Based on this description, one of ordinary skill in the art would know that the dielectric layer 60 was produced and layered using thermal oxidation to grow exposed silicon components into silicon dioxide. (Ex. 2158 at 102-103).

128. Second, if a silicon dioxide dielectric contacts circuit components, the silicon dioxide must be high-purity to not damage the circuit components. (Ex. 2158 at 68-70; Ex. 2159 at 54). Therefore, because *Bertin* describes the silicon dioxide dielectric layer 60 as being grown directly over active silicon components (such as a silicon source, gate, or drain), one of ordinary skill also would

understand that the dielectric layer 60 needs to be highly pure, which again would mean it was grown at high temperatures using thermal oxidation.

129. Third, the change from front end of line (which requires high purity and high temperatures) to back end of line is marked by the deposition of the first metallization connection layer. (Ex. 2158 at 14). Accordingly, one of ordinary skill would understand that dielectric layer 60 was grown using thermal oxidation during the front end of line phase because *Bertin* describes the layer as being grown several steps before the deposition of the connecting metallization and wiring, which would mark the end of the front end of line phase and the start of the back end of line phase. (Ex. 1004 at 3:60-62, 4:30-40).

130. And just as one of ordinary skill in the art would understand that dielectric layer 60 was grown using thermal oxidation during the front end of line phase, one would also understand that it could not be deposited using a Plasma-Enhanced CVD such as that described in *Leedy '695*. Plasma-Enhanced CVD cannot be used during front end of line to produce and deposit a high-purity silicon dioxide dielectric over active circuit components because the resulting dielectric would not (1) be sufficiently pure; (2) have the ability to adhere sufficiently to the semiconductor wafer; and (3) be able to withstand high temperatures of the remaining FEOL steps without changing its form. (Ex. 2169 at 29-30). Plasma-

Enhanced CVD also cannot be used because positive ions present in the plasma can strike and damage the wafer and the exposed active components in and on its surface. (Ex. 2159 at 139).

b. Bertin's "dielectric layer 60" Is Removed From The Chip

131. *Bertin*'s dielectric layer 60 is removed during subsequent processing and is not part of the final integrated circuit. *Bertin* describes that dielectric layer 60 is formed on top of active layer 54, then high-aspect ratio trenches 62 are formed, trench walls are oxidized, and the trenches are filled with conductor 64. (Ex. 1004 at 4:11-33). To complete the device, *Bertin* shows that dielectric layer 60 is replaced with an oxidation/connecting metallization layer 63. (Ex. 1004 at figure 3c and 3d). It is common to create a dielectric layer and subsequently remove it during fabrication. (Ex. 2158 at 141). Because dielectric layer 60 is removed during processing, it is not included in the final package.

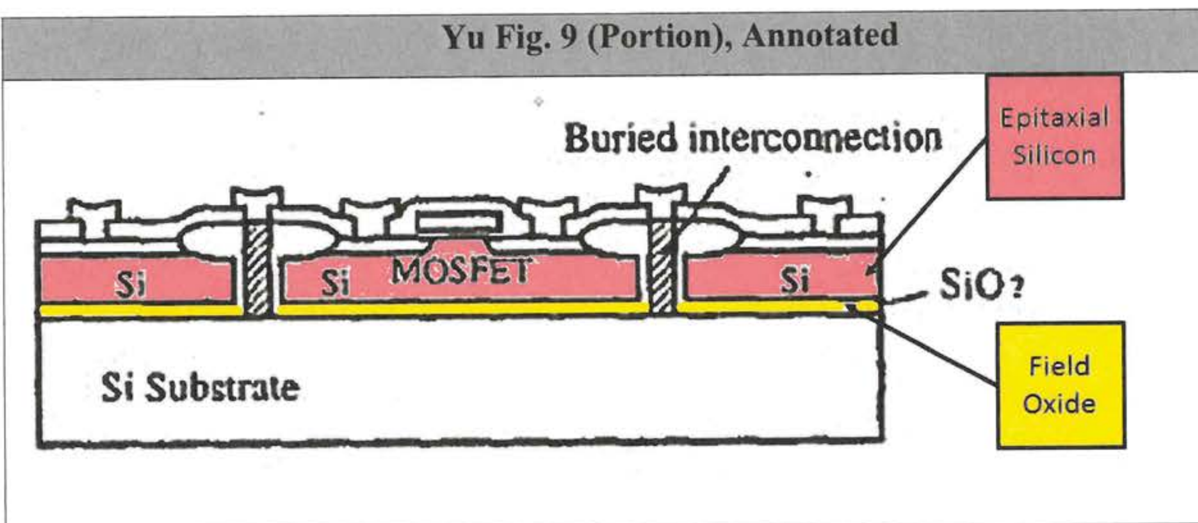
3. Yu

132. *Yu* describes a microvision system for analyzing image data in real time (Ex. 1009 at 831). *Yu* describes that the microvision system is fabricated using "micro-bumps" to bond a thinned wafer to a thick wafer. (Ex. 1009 at 831, 834).

a. Yu's "field oxide" Was Grown Using Thermal Oxidation And Could Not Be Produced And Layered Using Plasma-Enhanced CVD

133. *Yu*'s Figure 9 reproduced below depicts a layer of "SiO_2," which *Yu* describes as a layer of "field oxide." (Ex. 1009 at 834). Instituted Ground 2 is based on Petitioners' argument that it was obvious to replace this field oxide with the *Leedy '695*'s low-tensile-stress Plasma-CVD dielectric.

Yu Fig. 9 (Portion), Annotated



134. Petitioners do not address that the layer of "SiO_2" on which they rely is described in *Yu* a "field oxide," nor do they otherwise attempt to identify the type or use of this particular silicon dioxide dielectric. (Ex. 1009 at 834 ("The buried interconnections are formed by depositing n^+ poly-Si into trenches which are formed through the field oxide."). One of ordinary skill would understand that, by definition, a silicon dioxide field oxide is grown directly on the "Si Substrate" at high temperatures using thermal oxidation. (Ex. 2158 at 102-103).

135. This is confirmed by the fact that *Yu* illustrates the silicon dioxide field oxide as directly atop the silicon substrate. (Ex. 1009 at 834, Fig. 9). Because it is touching the silicon substrate, the silicon dioxide "field oxide" must have high purity, which again means a person skilled in the art would understand it was grown at high temperatures using thermal oxidation. Ex. 2158 at 68-70; Ex. 2159 at 54).

136. A person of ordinary skill also would understand that the *Yu* "field oxide" must be able to withstand high temperatures such as those used in the front end of line phase of fabrication. For example, *Yu* describes that a thermal CVD process, which is performed at temperatures in excess of 800˚C, is used deposit silicon on top of the field oxide, thereby forming the epitaxial silicon layer. (Ex. 2159 at 140; Ex. 2158 at 382; Ex. 1009 at 834). Trenches are formed then through the field oxide and filled with n+ doped poly-silicon, which is performed at temperatures in excess of 600 ˚C. (Ex. 1009 at pg. 834; Ex. 2158 at 389-90). Circuit components (*e.g.,* MOSFET source, drain, and gate) are formed and Ohmic contacts are created using a silicide process, which is performed at temperatures in excess of 700˚C. (Ex. 2160 at 328; Ex. 2158 at 396, 507). The field oxide thus must, without changing its relevant properties, withstand subsequent processes including thermal CVD of epitaxial silicon, deposition of poly-silicon, and

formation of Ohmic contacts via a silicide process, all of which exceed the 400°C limit of dielectrics deposited by PECVD as disclosed in Leedy '695.

137. And just as one of ordinary skill in the art would understand that *Yu*'s "field oxide" was grown using thermal oxidation during the front end of line phase, one would also understand that it could not be deposited using a Plasma-Enhanced CVD such as that described in *Leedy '695*. Plasma-Enhanced CVD cannot be used during front end of line to produce and deposit a high-purity silicon dioxide dielectric over a silicon substrate because the resulting dielectric would not (1) be sufficiently pure; (2) have the ability to adhere sufficiently to the silicon substrate; and (3) be able to withstand high temperatures of the remaining FEOL steps without changing its relevant properties. (Ex. 2169 at 29-30). Plasma-Enhanced CVD also cannot be used because positive ions present in the plasma can strike and damage the surface of the silicon substrate. (Ex. 2159 at 139). Even if one tried to substitute the *Leedy '695* low-tensile membrane for the dielectric in this reference, the subsequent FEOL heating steps and anneals would change the properties of the membrane such that it would become compressive stressed—thus removing any perceived benefits of tensile stress. (Ex. 2169 at 29-30).

III. All Challenged Claims: The Proposed Combinations Are Not Even Possible, Much Less Obvious

138. One of ordinary skill in the art would not have found it obvious to substitute the low tensile stress dielectric disclosed in Leedy '695 for particular dielectrics in *Bertin* and *Yu*. Further, the proposed combinations are not even possible, much less obvious.

139. When selecting a dielectric and method of formation, many of the following dielectric properties must be evaluated: (1) dielectric constant, (2) breakdown field strength, (3) leakage, (4) surface conductance, (5) moisture absorption or permeability to moisture, (6) stress, (7) adhesion to aluminum, (8) adhesion to dielectric layers above or below, (9) stability, (10) etch rate, (11) permeability to hydrogen, (12) amount of incorporated electrical charge or dipoles, (13) amount of impurities, (14) quality of step coverage, (15) the thickness and uniformity of the film, (16) ability to provide good doped uniformity across a wafer, (17) defect density, (18) amount of residual constituents that outgas during later processing. One of ordinary skill in the art choosing a dielectric would consider many of these factors and would have knowledge of how the different techniques of applying dielectrics affected those qualities.

140. Without knowledge of these factors and how different techniques of applying dielectrics affect those qualities, one cannot conclude that it was obvious

to substitute the Leedy '659 dielectric for particular dielectrics in *Bertin* and *Yu*. Indeed, were they to do so, they could not, because *Leedy '695* does not address or disclose most of these properties and they are therefore unknown for the *Leedy '695* dielectric.

A. Ground 1a: The Leedy '695 Dielectric Could Not And Would Not Be Substituted For the Bertin Thermal Oxide Dielectric

141. Instituted Ground 1a is based on Petitioners' argument that it was obvious to replace *Bertin*'s dielectric layer 60 with the *Leedy '695*'s low-tensile-stress Plasma-CVD dielectric. Petitioners' do not even attempt to identify the type or use of *Bertin*'s "dielectric layer 60," which, as I have established above, a person of ordinary skill in the art would understand is a high-purity silicon dioxide grown over active circuit components via thermal oxidation at high temperatures during the front-end-of-line phase of fabrication.

142. One of ordinary skill in the art also would understand that that dielectric layer 60 could not be deposited using a Plasma-Enhanced CVD such as that described in *Leedy '695*. Plasma-Enhanced CVD cannot be used during front end of line to produce and deposit a high-purity silicon dioxide dielectric over active circuit components because the resulting dielectric would not (1) be sufficiently pure; (2) have the ability to adhere sufficiently to the semiconductor wafer; and (3) be able to withstand high temperatures of the remaining FEOL steps

without changing its form. Plasma-Enhanced CVD also cannot be used because positive ions present in the plasma can strike and damage the wafer and the exposed active components in and on its surface.

143. Finally, there was significant teaching away from using tensile stressed dielectrics, as it was known in the art that tensile stressed dielectrics were inferior. (Ex. 1040 at 114, 117; Ex. 2146 at 195 ("the preferred stress [in a dielectric] is compressive…since dielectric films under tensile stress exhibit more of a tendency to crack")). "[l]ow density tensile films tend to pick up water and form SiOH groups." (Ex. 1049 at 5). This causes "degradation of electrical and mechanical properties." *Id.*

144. At the time of the filing date, it was typical to try to alleviate some of these problems by depositing PECVD layers in moderate compressive stress (rather than tensile) to enhance conformality, reduce pinhole counts, and improve adhesion. (Ex. 2133 at 10, 11; Ex. 1040 at 106). Further, it was known to use compressive stressed dielectrics because, unlike tensile films, "films deposited with an intrinsic compress stress are stable and are even able to withstand boiling water without increasing the SiOH content or absorbing water." (Ex. 1049 at 5).

145. Even if there was a reason to using tensile stress films, which there is not in this reference, substituting the *Leedy '695* membrane would not work. The

subsequent FEOL heating steps and anneals would necessarily change the properties of the membrane such that it would become compressive stressed—thus removing any perceived benefits of tensile stress.

146. For each and any of these reasons, one of ordinary skill would not have been motivated to use Leedy '695 dielectric as Petitioners propose; to the contrary, one of ordinary skill would understand that Leedy '695 dielectric could not be used as to replace *Bertin*'s "dielectric layer 60."

B. Ground 2: The *Leedy '695* Dielectric Could Not And Would Not Be Substituted For the Yu Field Oxide Dielectric

147. Instituted Ground 2 is based on Petitioners' argument that it was obvious to replace *Yu*'s field oxide dielectric with the *Leedy '695*'s low-tensile-stress Plasma-CVD dielectric. But Petitioners do not address that the layer of "SiO_2" on which they rely is described in *Yu* as a "field oxide," nor do they otherwise attempt to identify the type or use of this particular silicon dioxide dielectric. (Ex. 1009 at 834). One of ordinary skill would understand that, by definition, *Yu*'s silicon dioxide field oxide is grown directly on the "Si Substrate" at high temperatures using thermal oxidation.

148. One of ordinary skill in the art also would understand that that *Yu*'s field oxide could not be replaced with a dielectric deposited using a Plasma-Enhanced CVD such as that described in *Leedy '695*. Plasma-Enhanced CVD

cannot be used during front end of line to produce and deposit a high-purity silicon dioxide dielectric over a silicon substrate because the resulting dielectric would not (1) be sufficiently pure; (2) have the ability to adhere sufficiently to the silicon substrate; and (3) be able to withstand high temperatures of the remaining FEOL steps. Plasma-Enhanced CVD also cannot be used because positive ions present in the plasma can strike and damage the surface of the silicon substrate. (Ex. 2159 at 139).

149. Finally, there was significant teaching away from using tensile stressed dielectrics, as it was known in the art that tensile stressed dielectrics were inferior. (Ex. 1040 at 114, 117; Ex. 2146 at 195 ("the preferred stress [in a dielectric] is compressive…since dielectric films under tensile stress exhibit more of a tendency to crack")). "[l]ow density tensile films tend to pick up water and form SiOH groups." (Ex. 1049 at 5). This causes "degradation of electrical and mechanical properties." *Id.*

150. At the time of the filing date, it was typical to try to alleviate some of these problems by depositing PECVD layers in moderate compressive stress (rather than tensile) to enhance conformality, reduce pinhole counts, and improve adhesion. (Ex. 2133 at 10, 11; Ex. 1040 at 106). Further, it was known to use compressive stressed dielectrics because, unlike tensile films, "films deposited

with an intrinsic compress stress are stable and are even able to withstand boiling water without increasing the SiOH content or absorbing water." (Ex. 1049 at 5).

151. Even if there was a reason to using tensile stress films, which there is not in this reference, substituting the *Leedy '695* membrane would not work. The subsequent FEOL heating steps and anneals would necessarily change the properties of the membrane such that it would become compressive stressed—thus removing any perceived benefits of tensile stress. (Ex. 2169 at 29-30).

152. For each and any of these reasons, one of ordinary skill would not have been motivated to use Leedy '695 dielectric as proposed; to the contrary, one of ordinary skill would understand that Leedy '695 dielectric could not be used as to replace *Yu*'s field oxide dielectric.

IV. Conclusion

153. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: 2016.10.14 16:38:57 -07'00'

Dated: October 14, 2016

Dr. Alexander D. Glew

Exhibit A

Curriculum Vitae

Alexander D. Glew, Ph.D., P.E.

Expertise

• **Materials Science Engineering, Thin Films & Equipment, Semiconductor**	• **Mechanical Engineering**
• Semiconductor Equipment and processing: CVD, Etch, RIE, CMP, SOD, EPI, MBE, RTP, and others	• Licensed Professional Engineer (PE) in California, Mechanical Engineering
• Chemical vapor deposition (CVD): plasma, ICP, thermal, MOCVD, LPCVD and others	• CAD, drafting standards, and related.
• Thin film processing for solar, LED, and optics.	• Computation Fluid Dynamics (CFD) Fluid flow, radiation analysis
• Diamond Like Carbon (DLC), fluorinated amorphous carbon (FLAC)	• Finite Element Analysis (FEA), multi-physics and event simulation
• Dielectric Deposition: Low k dielectric films, SiO2 (glass), fluorinated glass (FSG), BPSG, USG	• Product Design & Testing
• Excimer Laser Sources	• Project management and turnaround
• Laboratory analysis: SEM, TEM, FTIR, SIMS, AES, and others.	• Ultra High Purity Gas and Chemical Delivery Systems
• Materials processing	• Piping, valve, and chemical systems
• Metal deposition	• Metrology: Flow, pressure, optical properties, thin film properties …
• Plasma and Thermal Processes	• Reverse Engineering
• Thin Film Characterization: stress, strain, thickness, optical and dielectric properties, structure, composition …	• Safety analysis, interlocks, failure mode effects, standards and code analysis.

Curriculum Vitae

Employment History

From:	1997	**Glew Engineering Consulting, Inc.**
To:	Present	Mountain View, California
	Position:	President
		Clients include companies from semiconductor equipment, plasma generation, vacuum systems, fluid delivery systems, flow and pressure component suppliers, laser manufacturers, consumer electronics, industrial electronics, and others. Consulting work includes thin film characterization, process development, project turn-around/rescue, gas flow and vacuum metrology, design of experiments, corrosive gas applications, finite element analysis and related market analysis.
From:	Aug 1987	**Applied Materials, Inc.**
To:	Jan 1997	Santa Clara, California
	Titles	Engineering Manager, Core-Technologist
	Project Mgr. Jan 1996 to Jan 1997	• Sat on corporate engineering/technology (ET) council, one of 15 council members. Responsible for corporate direction in gas delivery technology for all divisions, including CVD, EPI, PVD, RTP, etch, thermal and others. Also, qualified gas and vacuum component selections. Consulted with all divisions on gas and vacuum systems, liquid source delivery systems, components, and supplier selections.
		• Received patent for improved tungsten (W) CVD deposition.
	CVD Supplier Quality Engineering Manager Core Technologist	• Successfully proposed and executed a project that SEMATECH S100 funded. The goal was to develop industry methods to determine the effects of trace chemicals on semiconductor processing and equipment reliability. This resulted in two SEMATECH Technology Transfers listed below. First, ppb levels of impurities were introduced into both a Tungsten CVD deposition process and an aluminum etching process. The effect on particle generation, deposition rate, uniformity, selectivity and incorporation into the film were examined. This work resulted in a 30% increase in deposition rate. Similarly, ppb-ppm levels of impurities were introduced into HBr gas systems and accelerated lifetime tests were conducted at three sites across the country. Measured by quadrapole mass spectrometry gas composition in situ of Tungsten CVD and Al Etch process.
	CVD Engineering Manager	• Responsible for gas, vacuum and chemical components evaluation, testing and supplier quality management. Managed an engineering group that tested and recommended gas, vacuum and chemical components for the CVD division, and developed

process controls at suppliers. Supervised laboratory and trained individuals to develop specialized testing capabilities to characterize gas delivery and vacuum components. Also supported Etch, PVD and other divisions with common suppliers including vacuum pumps, vacuum transducers, flow controllers, valves and similar.

Systems Engineer

- Managed group of engineers and support personnel who developed gas panels and liquid source delivery systems for dielectric deposition. Delivered TEOS, TMP, TMB and many other organometallic precursors for SG, BPSG dielectric deposition. Developed organometallic CVD systems extensively. Designed multiple liquid source delivery systems for organometallic chemical precursors, i.e. bubblers, boilers, injectors.
- Managed CVD division design support group: CAD designers, drafters and CAD systems for division. Brought in first 3D CAD systems. Brought in first FEA program.
- Established and managed the customer engineering special group for the CVD division, which engineered all equipment modifications to meet customer specifications. These modifications included changes across the entire system, including process chambers, vacuum systems, gas delivery, power distribution, safety and robotics.
- Worked on the development and release of the landmark product, Precision 5000 CVD, one of which is now in the Smithsonian Institute. This was the first cluster tool for semiconductor manufacturing.
- Developed dielectric layers of silicon dioxide (glass or USG), boron phosphorous silicon glass (BPSG), phosphorous silicon glass (PSG), nitride, oxy-nitride, and others.
- Responsible for flow and vacuum equipment suppliers for company including MFC, valves, mechanical vacuum pumps, cryo-pumps, dry pumps, and others. Supported multiple divisions on these matters.

Doctoral Dissertation:

From: 1996
To: 2002

Stanford University
Stanford, California
Ph.D.
Completed a dissertation in the department of Materials Science & Engineering leading to the Ph.D. degree.
Research includes:

- Plasma Deposition of Diamond-Like Carbon and Fluorinated Amorphous Carbon and the Resultant Properties and Structure

- Characterized stress, strain and hardness of films. Related the stress energy state to the diamond like nature of the thin films.
- Investigation of deposition mechanism fluorinated amorphous carbon (FLAC) and diamond-like carbon (DLC), low k dielectric materials.
- Modeled and conducted experiments on mechanism of ion energy, momentum and flux dependence for FLAC and DLC film synthesis in radio-frequency plasma discharges, including competing mechanisms of sub-plantation, ion-peening, sputtering, and etching.
- Constructed and instrumented a multi-purpose processing chamber for CVD, etch, and sputtering with measurement capability.
- Fabricated MIS capacitors to investigate the dielectric properties of fluorinated amorphous carbon (FLAC). Performed all wafer processing to construct MIS capacitors, including lithography, etch, CVD and PVD.
- Conducted thin film analysis including UV absorption spectroscopy, spectral ellipsometry, multi incident angle ellipsometry, Fourier transform infrared spectroscopy, profilometry, nano-indentation, and gravimetric measurements.
- Modeled dielectric properties and dispersion relationship of fluorinated amorphous carbon (FLAC), and compared spectral ellipsometric measurements to results of electrical CV tests and thickness measurements by profilometry using MIS structures.

Consulting History (Partial)

From 2016
To: Ongoing

Champion Telecom

Engineering support of Cell Towers on Wheels (COWs)

From 2016
To: Ongoing

CarbonTech

Pursue UL listing for thin film carbon heaters. Help productize the technology. Review codes for domestic use.

From 2015
To: 2016

Phiston Engineering

Review ability of equipment to destroy flash memory. Generate report to submit to NSA.

From 2015
To: 2015

United States Air Force
Concluded

	Duties	Advanced semiconductor process equipment engineering for Air Force Laboratory.
From	2013	United States Department of Justice, Antitrust Division
To:	2014	
	Duties	Served as the expert for the DOJ in their investigation of the proposed merger between Applied Materials and Tokyo Electron.
From	2015	VADA
To:	Ongoing	
	Duties	Fluid analysis of venting device.
From	2014	Chemithon
To:	Completed	
	Duties	Finite element analysis (FEA) and computational fluid dynamics (CFD) analysis of thermal and stress analysis of large industrial sized heat exchangers. Redesign to meet structural and performance needs.
From	2013	Barrick Cortes Mines
To:	2013	
	Duties	Analysis of equipment using in mining operations.
From	2013	Life Technologies
To:	2013	
	Duties	Concept design for a portion of a medical device: centrifuge assembly for separation in PCR DNA application.
From	2012	Light failures
To:	2012	
	Duties	Reliability analysis of thermal issues causing light sealing failures for glass metal interface.
From	2012	Legion Industries
To:	2012	
	Duties	Review of electrical surge issues at Google campus.
From	Dec. 2011	CareFusion
To:	2012	
	Duties	Reliability analysis of medical device.
From	June 2011	Watlow
To:	2012	
	Duties	Heater and chuck assembly design for use in semiconductor processing.

From	June 2011	Limited Brands
To:	June 2012	
	Duties	Design review of prototype consumer electronics products. Perform engineering analysis of weaknesses and risks in product design.
From	April 2011	EFCI/Environmental Protection Agency
To:		
	Duties	Subject matter expert for green house gas emissions from the electronics industry.
From	June 2011	Intrimed
To:	Current	
	Duties	Consult for Exec. VP on thin film technology in medical devices.
From	April 2010	Zoll Circulation
To:	June 2010	
	Duties	Analysis of electrical contacts in a medical device, cardiac life support pump.
From:	June 2008 Sept. 2008	Teardown and analysis of IC packaging.
From	Oct 2008	VModa
To:	Feb 2009	
	Duties	Engineering analysis of headset/earbuds used for iPhone. Performed finite element analysis (FEA) of plug to determine why the plug/cable contacts were breaking. Reviewed designs of a number of competing earbuds, and other musical equipment plugs, and their respective designs for plug reliability improvements.
From	Sep 2008	Malema Sensor
To:	Oct 2008	
	Duties	Safety Analysis of Fluid dispense system for semiconductor equipment.
From	Dec 2007	Damage analysis for insurance valuation.
To:	Jan 2008	
	Duties	Analysis of damage to equipment from a chemical leak.
From:	Apr 2007	Epicrew
To:	Oct 2008	
	Duties	Finite element analysis of temperature distribution in process chamber, and leading to safety issues and analysis of emergency conditions in epitaxial equipment. Multi-physics transient radiation, conduction and convection analysis.

Curriculum Vitae

From:	Apr 2007	Unicor
To:	Oct 2007	
	Duties	Analysis by FEA and approval of automotive lifting devices as a licensed mechanical engineer.
From:	2007	Altcatel
To:	2008	
	Duties:	Consulting on semiconductor foundry processes, low-k spin on dielectrics, that lead to IC failures.
From:	2002	
To:	Present	Consulting with financial analysts on semiconductor industry through Gerson Lehrman Group.
	Duties:	Provided on the spot analysis of new technologies, companies, and products within the semiconductor and related industry.
	March	AIU (Now Chartis Insurance.)
From:	2004	
To:	2009	Hsinchu, Taiwan
	Duties:	Analysis of complete destruction of FAB due to facility design, equipment design, installation, process monitoring and control, etc. International Arbitration.
From:	June 2004	Rosemont Process, Division of Emerson Electric, Inc.
To:	Nov 2004	Minneapolis, MN.
	Duties:	Market analysis of process monitoring and control needs.
From:	Oct 2000	Brooks Instrument, Division of Emerson Electric, Inc.
To:	March 2001	Hattfield, PA, and Minneapolis, MN.
	Duties:	Market analysis of semiconductor equipment needs with respect to fluid handling components.
From:	Apr 2000	Lebar, Inc.
To	Oct 2000	Sunnyvale, CA
	Duties:	System design and fluid delivery system design for plasma based photoresist strip (photoresist removal).
From:	Dec 1999	High Speed Industries, Inc.
To	2000	Lake Elsinore, CA
	Duties:	Market analysis of semiconductor equipment needs with respect to fluid handling components.
From:	May 1999	Aeroquip (Division of Eaton Corp.) Ann Arbor, MI

	Duties:	Reviewed new product entry (semiconductor fluid handling) prior to product engineering.
From:	Sep 1999	Steag RTP Systems, Inc.
To:	Nov 1999	San Jose, CA.
	Duties:	Materials evaluation and testing for metallic reduction in thermal SiO_2 films produced by rapid thermal processing (RTP) with steam.
From:	Sep 1998	Cymer, Inc.
To:	Aug 1999	San Diego, CA
	Duties:	Project manager responsible for leading team through concept and feasibility studies for major product enhancement to Excimer laser used in deep ultraviolet lithography.
From:	Jan 1997	Millipore, Inc.
To:	Sep 1998	Rancho Bernardo, CA
	Duties:	• Established a metrology group responsible for vacuum and flow measurements. The metrology is used in the manufacture and service of instruments for semiconductor process equipment. Established statistical process control for production metrology equipment. Established statistical process control on factory floor. • Led development team for new mass flow control device.

Litigation Support Experience

Client	DiamondOP
Case	DiamondOP v. Delta Civil Action No. 2:15-cv-1231-JRG
Project	Patent infringement involving Diamond Like Carbon thin film coatings..
Dates	2016.
Status	Completed.

Client	Ricoh America Corp
Case	Ricoh America Corp v. Round Rock Research LLC.
Project	Three INTER PARTES REVIEW at the USPTO. Patents semicenoductor processing and devices.
Dates	2016.
Status	Reports written. In progress..

Client	Elm 3DS Innovations
Case	Elm v. Samsung Electronics, Hynix and Micron C.A. No. 14–cv-01430–LPS-CJB
Project	Patent infringement involving thinned and stacked wafers, low stress dielectric materials and other topics of IC memory.
Dates	2014 -

Client	Antitrust Division, US Department of Justice
Case	Proposed merger of Applied Materials and Tokyo Electron
Project	Served as technical expert/industry expert for US DOJ regarding proposed merger of the two largest semiconductor equipment companies.
Dates	2014 -2015

Client	Russ, August & Kabat (Semcon)
Case	Semcon v. Micron Inc. CASE NO. 12-532-RGA UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE
Project	Advanced process control and metrology in semiconductor processing patent case regard CMP.
Dates	2013
Status	Expert report, deposed, completed.

Client	Baker & Hostetler (Caterpillar Inc.)
Case	Miller UK Limited v. Caterpillar Inc. CASE NO. 10-cv-3770 UNITED STATES DISTRICT COURT FOR THE NORTHERN DISTRICT OF ILLINOIS EASTERN DIVISION
Project	Trade secret case.
Dates	2013
Status	Testified at trial. Completed.

Client	Carr & Farrell (LAM Research)
Case	LAM RESEARCH CORPORATION v. XYCARB CERAMICS CASE NO. 3:03-cv-1335 CRB UNITED STATES DISTRICT COURT NORTHERN DISTRICT OF CALIFORNIA SAN FRANCISCO DIVISION
Project	Review product for patent infringement.
Dates	2013
Status	Settled

Client	Jenner & Block (Nissan)

Case	Diamond Coating Technologies LLC v Nissan North America, Nissan Motor Co Ltd., SACV13-01481 JVS (JPRx) UNITED STATES DISTRICT COURT CENTRAL DISTRICT OF CALIFORNIA SOUTHERN DIVISION
Project	Diamond-like and hard carbon thin films.
Dates	2014
Status	Patent invalidated.
Description	Patent infringment

Client	Radusescu LLP (Zond)
Case	Zond Inc. v. Gillette Company et al., 1:13CV11567 U.S. DISTRICT COURT, DISTRICT OF MASSACHUSETTS (BOSTON)
Project	Plasma processing and power supply patents, breach of contract.
Dates	2013 – 2014
Status	Completed. Summary judgement.

Client	Morgan Lewis. (MTI)
Case	Powerwave v. MTC
Project	Telecom PCB patent case.
Dates	2013
Status	Settled

Description	Patent Re-Exam

Client	McDermott, Will & Emory. (HTC)
Case	Nokia v. HTC
Project	Cell phone displays patent case.
Dates	2013 – present
Status	Completed
Description	ITC Matter

Client	Schwegman, Lundberg & Woessner, P.A. (Amkor)
Case	Tessera v. Amkor
Project	Semiconductor manufacturing technology.
Dates	2013 – present
Status	Expert report, deposed, settled.
Description	Petition for *inter partes* review of U.S. patent at USPTO

Client	Shore, Chan Bragalone & DePumpo LLP. (Xicor)
Case	Xicor v. SST
Project	Semiconductor manufacturing technology.
Dates	2011 – 2012
Status	Completed.

Description Trade secret case.

Client Shore, Chan Bragalone & DePumpo LLP. (Nanya)
Case ADA v. Nanya
Project Semiconductor manufacturing technology.
Dates 2012
Status Complete
Description Patent case.

Client Shore, Chan Bragalone & DePumpo LLP. (ITRI)
Case ITRI v. LG
Project Heat transfer technology.I
Dates 2011 - present
Status Completed.
Description Patent case.

Client Fish & Richardson (3M)
Case TransWeb v. 3M, District Court of NJ, 2:10-cv-04413 (FSH/PS)
Project Litigation for plasma fluorinated electrets.
Dates 2011
Status Expert report, deposed, trial.
Description Patent litigation for plasma fluorination of electrets and filters media, woven polymer fabric forming HEPA filters.

Client Allegaert Berger & Vogel LLP (Taiwan Glass)
Case CVD Equipment v. Taiwan Glass, 10 Civ. 0573 (RH-I) (RLE), Eastern District of NY
Project Litigation for breach of contract in equipment used in the manufacture of low emissivity window glass and solar glass.
Dates 2010
Status Expert report, deposed, judgement.
Description Chemical vapor deposition equipment for transparent conducting oxide (TCO) used in solar cells, and low emissivity glass (low E).

Client Knobbe, Martens, Olson & Bear (ATS)
Case ATS v. AMI SACV07-1384 JVS (JWJx)
Project Litigation for correction of inventor-ship of patents, and breach of contract, for heat exchangers used in semiconductor processing equipment.
Dates 2009
Status Expert report, deposed, Trial.
Submitted and testifiedTestified.

Client Lee and Li (American Insurance Underwriters.)
Case AIU v. Applied Materials, Centrotherm, M&W and others.

Project	Insurance claims re destruction of Semiconductor Fab. Reviewed plans, standards, equipment, processes and related.
Dates	2009
Status	Report, Tried in High Court of Taiwan. Testified.

Client	Robbins, Kaplan, Miller, & Ciresi (AMD)
Case	AMD v. Samsung
Project	Patent litigation for AMD Semiconductor TiN patent relating to DRAM and FLASH memory products.
Dates	2007-2010
Status	Expert report, deposed, settled.

Client	King & Spalding, Redwood Shores, CA (Qimonda)
Case	Qimonda v. LSI and others at the International Trade Commission, *Certain Semiconductor Integrated Circuits And Products Containing Same*, Inv. No. 337-TA-665
Project	Semiconductor processing patent relating to crack stop patents in silicon oxide glass layers.
Dates	2009
Status	Expert report, deposed, trial, testified at ITC.

Client	Wilmer Hale, Palo Alto, CA (IDT)
Case	LSI v. IDT at the International Trade Commission, *Certain Semiconductor Integrated Circuits Using Tungsten Metallization And Products Containing Same*, Inv. No. 337-TA-648
Project	Semiconductor processing patent relating to TiN patents.
Dates	2008
Status	Expert report, deposed, trial, testified at ITC.

Client	Morrison and Forrester (Advance Micro-Fabrication Equipment)
Case	Applied Materials v. Advanced Micro-Fabrication Equipment C07 05248 JW (PVT)
Project	Semiconductor equipment manufacturer trade secret case. Reviewed numerous CAD documents related to equipment design.
Dates	2008
Status	Expert report, deposed, settled.

Client	Ropes and Gray (Entegris)
Case	Pall v. Entegris, 05-CV-5894 (BMC)(WDW), United States District Court, Eastern District of New York
Project	Patent dispute, filter patents.
Dates	2006 to present
Status	Settled.

Client	Thelen Reid and Priest, San Jose, CA (Celerity)

	Keith Slenkovich (attorney)
Case	Celerity vs. Ultra-Clean Technologies CASE NO. 05-CV-04374 MMC, United States District Court, Northern District of California
Project	Patent disputes, semiconductor processing equipment, ultra high purity gas delivery systems.
Dates	2005-2007
Status	Tried. Testified.

Client	Foran Glennon Palandech and Ponzi, Chicago, IL (American Insurance Underwriters) James Glennon (attorney)
Case	International Arbitration, Tokyo
Project	Analysis of complete destruction of FAB due to facility design, equipment design, installation, process monitoring and control, etc.
Dates	2004-2007
Status	Arbitrated. Testified in International Arbitration.

Client	Hollister & Brace and White & Case (AMS)
Case	Sputtered Films Inc. vs. Advanced Modular Systems
Project	Trade secrets regarding semiconductor processing/equipment used for manufacturing cell phone ICs.
Dates	2007
Status	Settled.

Client	Thelen Reid and Priest, San Jose, CA (Genmark) Rorbert Camors (attorney)
Case	Genmark Automation vs. Innovative Robotics Systems Inc. Case No. C07 05248 JW (PVT), United States District Court Northern District of California, San Jose Division
Project	Patent disputes, semiconductor processing equipment, wafer handling.
Dates	2005-2006
Status	Settled.

Client	Morgan & Finnegan LLP, NY, NY (ATMI) Kramer, Levin, Naftalis & Frankel LLP Ted Mlynar (attorney)
Case	ATMI vs. Praxair, Case No. 03 CV 5161, US District Court, Delaware
Project	Patent dispute, high purity hazardous chemical cylinder patents.
Dates	2004-2006
Status	Tried. Testified.

Client	Morgan & Finnegan LLP, NY, NY (DuPont) William Feiler (attorney)

	Civil Action No. 04-C-4049, US District Court, Northern District of Illinois Eastern Division
Case	Rapak vs. DuPont
Project	Patent disputes.
Dates	2006
Status	Settled.

Client	Cooley Goddard LLP, Broomfield, CO (Advanced Energy) Jim Brogan (attorney)
Case	MKS Instruments Inc. vs. Advanced Energy C.A. No. 03-469 (JJF), US District Court, Delaware
Project	Patent dispute.
Dates	2004-2005
Status	Tried. Testified

Client	Kerr & Wagstaffe LLP, Attorneys (HT Components)
Case	General Components, Inc. V. HT. Components, U.S.A., Inc. Case No. C 01-20925 JF
Project	Review of breach of contract for semiconductor equipment components. Reviewed CAD drawings for fittings.
Dates	Approximately 2002
Status	Settled

Client	Shannon, Gracey, Ratliff & Miller LLP, Fort Worth, TX, (Thompson & Knight)
Case	Lawrence J. Knipp and Nykar Technologies L.P. vs. Raymond M. Galasso and Thompson & Knight, LLP Cause No. 153-191270-02
Project	Reviewed patent prosecution malpractice.
Dates	Approximately 2002
Status	Settled

Client	Frommer Lawrence & Haug, New York, NY (TEL)
Case	Semitool Inc. vs. Tokyo Electron America, Tokyo Electron Kyushu Limited, Tokyo Electron Limited Stephen Lieb (attorney) Civil Action No. C 02 0288 CW (EMC)
Project	Patents: 4,985,722 Apparatus for coating a photo-resist film and/or developing it after being exposed 5,442,416 Resist processing method
Dates	Approximately 2002-2003
Status	Settled

Client	Keker & Van Nest, San Francisco, CA, (ASM) ASM America, Inc. et al v. Genus, Inc.

	Stuart Gassner (attorney)
Case	Civil Action No. C 01-02190 EDL
Project	Patents: 6,015,590 Method for growing thin films. 5,916,365 Sequential Chemical Vapor Depositions.
Dates	2001-2002
Status	Settled
Client	Orrick Herrington & Sutcliffe, LLP (Applied Materials) Gary Weiss (attorney)
Case	Applied Materials, Inc. v. LTD Ceramics et al U.S.D.C. Case No. C01-20478 JF PVT ADR
Project	Misappropriation of trade secrets. Reviewed numerous CAD documents related to equipment design.
Dates	2001-2003
Status	Settled
Client	Knobbe Martens, Olsen Bear, Newport Beach, CA, (Air Products)
Case	Advanced Delivery & Chemical Systems v. Air Products and Chemical, Inc. Case A 99-CA-406 SS
Project	Patents for chemical delivery.
Dates	2000-2001
Status	Settled
Client	Mitsubishi Silicon America vs. Semitool, Inc. Harrang Long Gary Rudnick (Salem, OR)
Case	CV 98-826-AA
Project	Semiconductor equipment breach of contract.
Dates	1999-2000
Status	Settled
Client	Semitool, Inc. vs. Novellus Systems Irell & Manella (Los Angeles)
Case	C 98-3089 DLJ
Project	Patents: 4300581 Centrifugal Wafer Processor 5377708 Multistation Semiconductor Processor with Volitization 5222310 Single Wafer Processor with Frame.
Dates	1999
Status	Settled
Client	Applied Materials, Inc. v. McDowell & Company, et al Orrick Herrington & Sutcliffe LLP (Menlo Park, CA)
Case	3-98CV-907-R

Project	Misappropriation of trade secrets. Reviewed numerous CAD documents related to equipment design.
Dates	1999
Status	Settled civil case.

Client	Applied Materials, Inc. v. David Biehl, et al Orrick Herrington & Sutcliffe LLP (Menlo Park, CA)
Case	CR95-20082 RMT PVT
Project	Misappropriation of trade secrets. Reviewed numerous CAD documents related to equipment design.
Dates	1999
Status	Settled civil case. Criminal Conviction.

Client	Micron Technology, Inc. v. Mosel Vitelic, Inc. Kirkland & Ellis (Chicago, IL)
Case	337-TA-414 CIV98-0293-S-LMB CIV98-0294-S-LMB
Project	Patent 4436584: Anisotropic plasma etching of semiconductors
Dates	1999 approximately
Status	Settled

Client	Hyundai Electronics Industries v. NEC Townsend and Townsend and Crew, LLP (Palo Alto, CA)
Case	98-118-A 2:98cv0077
Project	Patent 5,509,995 Process For Anisotropically Etching Semiconductor Material.
Dates	1998 approximately
Status	Settled

Client	Hyundai Electronics America, Inc. v. Texas Instruments, Inc. : Penney & Edmonds (Palo Alto, CA)
Case	98-648-A
Project	Patent 5,509,995 Process For Anisotropically Etching Semiconductor Material.
Dates	1998 approximately
Status	Settled

Patents

Patent Number	Date Issued	Title
7,118,090	Jan 20, 2007	Control Valves
6,679,476	Jan. 20, 2004	Control Valves

6,204,174	Mar. 20, 2001	Method and Apparatus Rate Deposition of Tungsten.
9,224,626	Dec. 29, 2015	Composite Substrate for Layered Heaters

Education

2003	Stanford University	Ph.D., Materials Science and Engineering
1995	Stanford University	M.S., Materials Science and Engineering
1987	University of California, Berkeley	M.S., Mechanical Engineering
1985	University of California, Berkeley	B.S., Mechanical Engineering

Publications and Conference Presentations (selected).

A.D. Glew, M.A. Cappelli, "Characterization and dielectric properties of fluorinated amorphous carbon measured by capacitance-voltage versus spectral ellipsometry", *Materials Research Society Symposium Proceedings,* **593**, Boston, MA, 1999, pp. 341-346.

A.D. Glew, M.A. Cappelli, "In situ plasma analysis, fluorine incorporation, thermostability, stress, and hardness comparison of fluorinated amorphous carbon and hydrogenated amorphous carbon thin films deposited on Si by plasma enhanced chemical vapor deposition", *Material Research Society Symposium Proc.*, **565**, San Francisco, CA 1999, pp 285-290.

A.D. Glew, R. Saha, M.A. Cappelli and J.S. Kim, "Ion Energy and Flux Dependence of Diamond Like Carbon Film Synthesis in Radio-Frequency Discharges", *International Conference on Metal Coatings and Thin Films,* Surface and Coatings Technology 114 (1999) 224-229.

A. Glew, R. Saha, M. Cappelli and J. Kim, "Ion Energy and Flux Dependence of Diamond Like Carbon Film Synthesis in Radio-Frequency Discharges", *International Conference on Metal Coatings and Thin Films*, San Diego, CA, April 1998

A. Glew, J, Ammenheuser, M. Crockett, A. Johnson, W. Dax, R. Binder, J. Riddle, "SEMASPEC 97043272A Accelerated Life Tests of Gas System Performance and Reliability," *http://www.sematech.org/public/docubase/abstract/3272atr.htm.*

A. Glew, J. Ammenheuser, J. Riddle, A. Johnson, "SEMASPEC 96083175A-XFR Determining the Effects of Impurities on Semiconductor Thin Film Processing," *http://www.sematech.org/public/docubase/abstract/3175axfr.htm.*

A Glew, "Selecting Gas Purity and Materials of Construction in High Purity Gas Systems," *Semicon West Symposium on Corrosion*, July 1997

Glew, J. Kim, K. Lee, M. Cappelli, "On the Characteristics of Diamond Like Carbon",

A. *International Conference on Metal Coatings and Thin Films*, San Diego, CA, April 1997

A. Glew, D. Porter, "Gas System Reliability Testing in Chlorine", *Semiconductor Fabtech*, May 1996.

Professional Associations

American Society of Mechanical Engineers (ASME)
International Microelectronics and Packaging Society
Materials Research Society (MRS)
IEEE
SEMI

Professional License

Licensed Mechanical Engineer, State of California, M26690

Laboratory analysis

On site: Microscopy, Vis and Near IR spectroscopy, thermal measurements, electrical-mechanical measurements.
Other Laboratory analysis may be provided through supervised third party laboratories: SEM, TEM, ESCA, AES, SIMS, FTIR, AFM ....

Technical Software Packages and Programming Languages (Selected):

Autodesk Simulation Mechanical (Algor™) 2015
Autodesk Simulation CFD (CF Design™) 2015
Autodesk Inventor™, Computer Aided Design 2015
Autodesk AutoCAD™, Computer Aided Design 2015
PTC Creo 3.0
Mathematica™ 10: mathematical analysis
Solidworks 2015

Civic Duties

Vice Commissioner, Design Review Commission, Los Altos, CA

Volunteer and Service Activities

Los Altos Rotary Club
    Veterans Committee and others
California Alumni Association
    Alumni Awards Committee 2015
    Alumni Awards Committee 2014
    Alumni Awards Committee 2013

For more information please contact:

Glew Engineering Consulting Inc.
240 Pamela Drive
Mountain View, CA 94040

Tel: 800-877-5892 (Toll Free USA)
Tel: 650 4641 3109 (Main number)
Tel: 650 403-2063 (Office direct)
Fax: 650-292-2210
Email: adglew@glewengineering.com
Web: www.glew.com