



US005792695A

United States Patent [19]

[11] Patent Number: 5,792,695

Ono et al.

[45] Date of Patent: Aug. 11, 1998

[54] MANUFACTURING METHOD OF A SEMICONDUCTOR EPROM DEVICE

Primary Examiner—Joni Chang  
Attorney, Agent, or Firm—Loeb & Loeb LLP

[75] Inventors: Masahiro Ono, Sawa-gun; Masaji Sakamura, Tatebayashi; Toshiharu Matsuda, Oura-gun, all of Japan

[57] ABSTRACT

[73] Assignee: Sanyo Electric Co., Ltd., Osaka, Japan

A first convex portion and a second convex portion are formed on a semiconductor substrate at a prescribed interval, an impurity diffusing region is formed on an upper portion of the semiconductor substrate placed between the first and second convex portions, and a thinned first polysilicon film is formed on the impurity diffusing region and the first and second convex portions. Thereafter, arsenic ions are implanted into the first polysilicon film to make the first polysilicon film conductive. Thereafter, a second polysilicon film having a film thickness larger than that of the first polysilicon film is formed, and phosphorus ions are implanted into the second polysilicon film to make the second polysilicon film conductive. Thereafter, a tungsten silicide film is formed on the second polysilicon film, and the tungsten silicide film and the first and second polysilicon films are patterned. Therefore, a two-layer structured electrode wiring film composed of a patterned tungsten silicide film and a combination of a patterned first polysilicon film and a patterned second polysilicon film is formed. Because the first polysilicon film is thinned, the first polysilicon film can be sufficiently conductive. Therefore, the first polysilicon film is electrically connected with the second polysilicon film on the first and second convex portions even though the second polysilicon film is not sufficiently conductive, and the electrode wiring film can be electrically connected with the impurity diffusing region.

[21] Appl. No.: 866,425

[22] Filed: May 30, 1997

[30] Foreign Application Priority Data

May 31, 1996 [JP] Japan ..... 8-139207  
Mar. 18, 1997 [JP] Japan ..... 9-065042

[51] Int. Cl.<sup>6</sup> ..... H01L 21/336; H01L 21/8247

[52] U.S. Cl. .... 438/257; 438/261

[58] Field of Search ..... 438/257-267;  
257/314-321, 324

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4 Claims, 12 Drawing Sheets

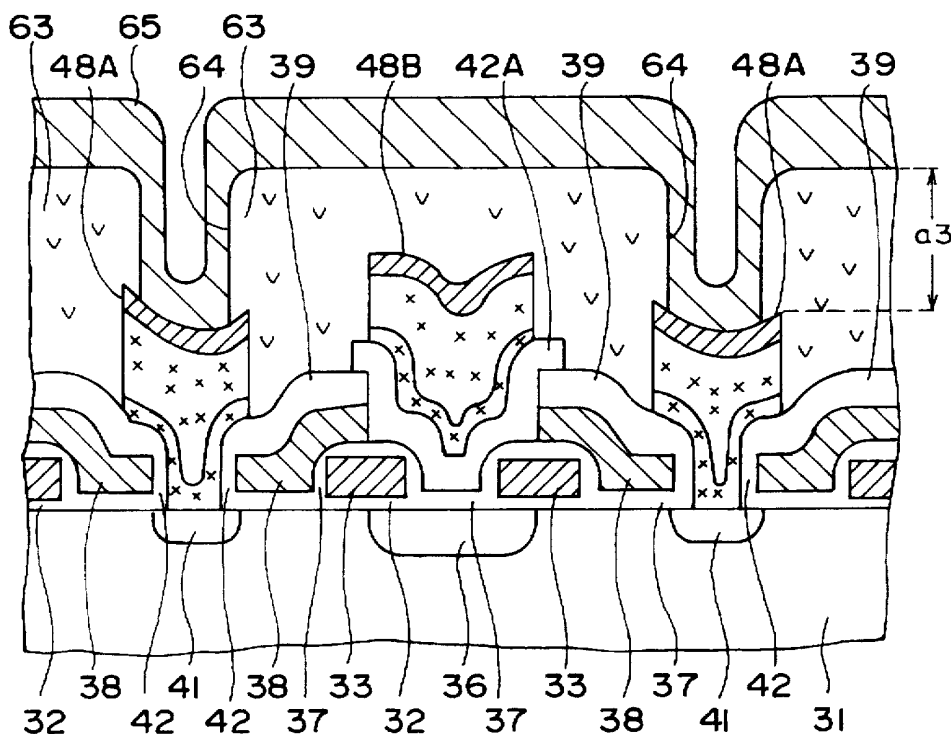


FIG. 1 (PRIOR ART)

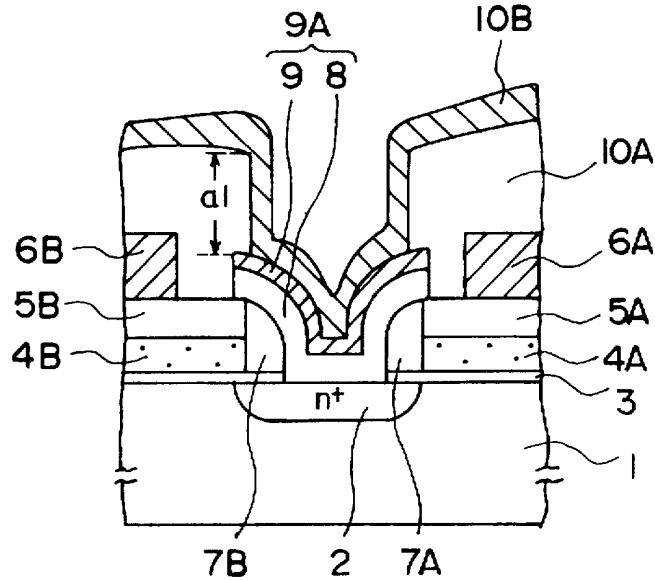


FIG. 2 (PRIOR ART)

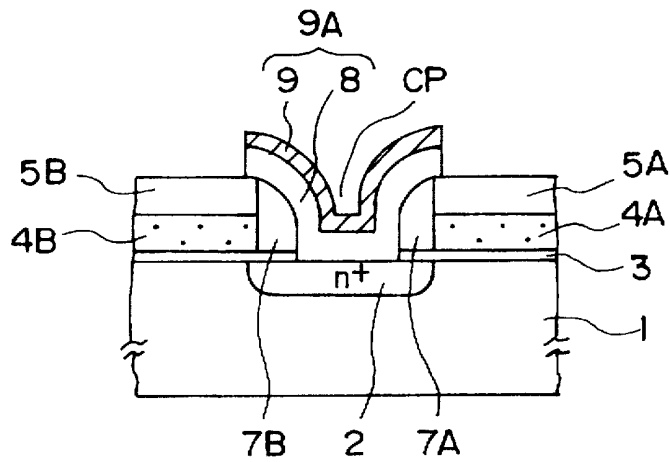


FIG. 3  
(PRIOR ART)

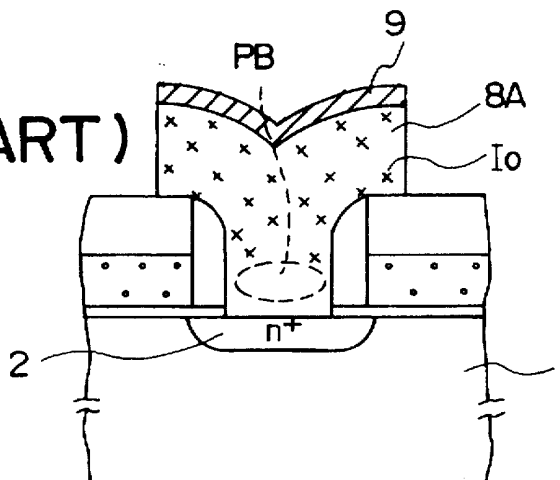


FIG. 4

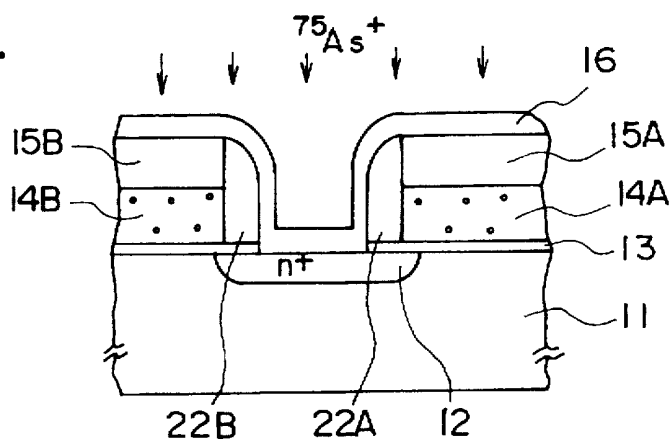


FIG. 5

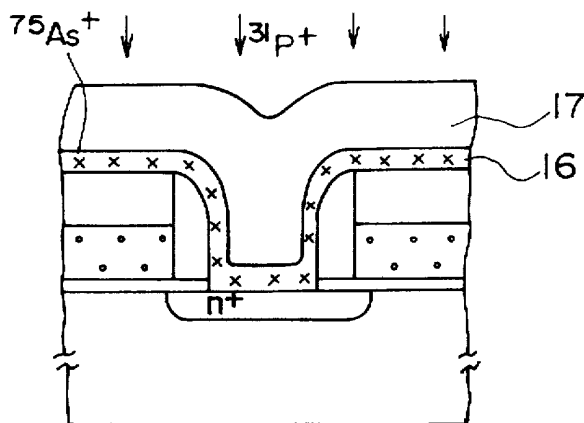


FIG. 6

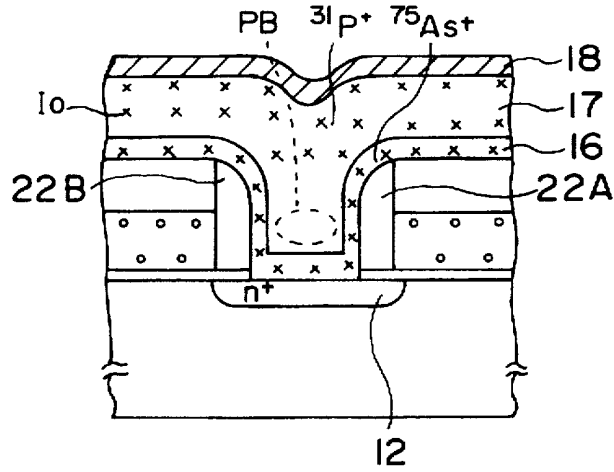


FIG. 7

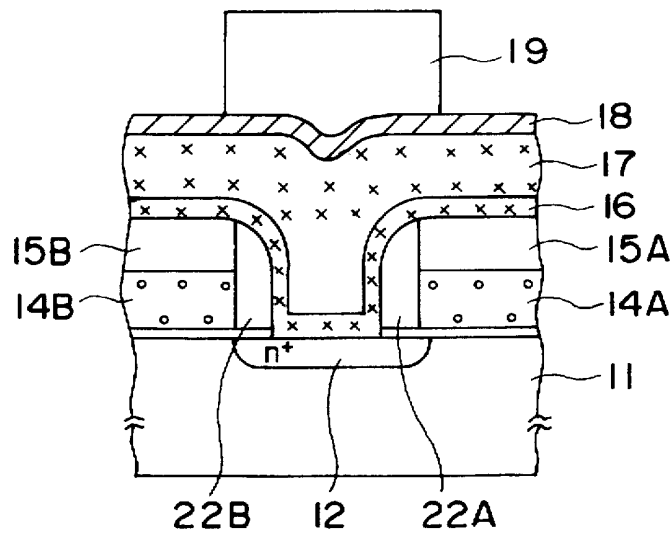


FIG. 8

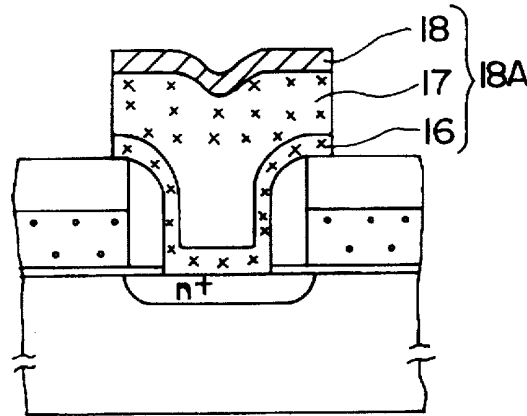
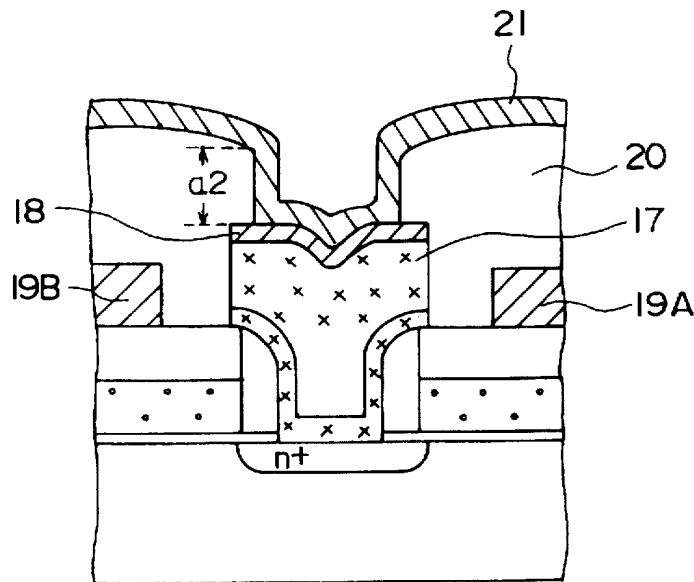


FIG. 9



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