# United States Patent [19]

#### Nihira et al.

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[54]	METHOD OF MANUFACTURING BIPOLAI
	TRANSISTOR

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Japan

[21] Appl. No.: 225,804

[22] Filed: Jul. 29, 1988

## [30] Foreign Application Priority Data

F#43 * . CD /	TTO4T 04 /044 TTO1T 01 /006
Oct. 27, 1987 [JP]	Japan 62-269259
Jul. 29, 1987 [JP]	Japan 62-189419

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Kikuchi, K. et al., "A High-Speed Bipolar LSI Procen ...", *IEEE-IEDM Tech. Digest*, 1986, pp. 420-423.

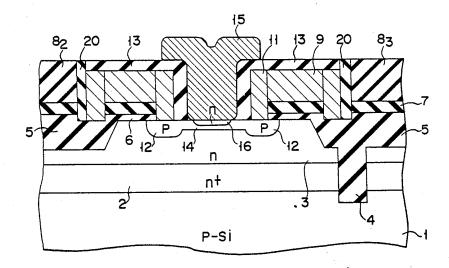
Primary Examiner—Brian E. Hearn Assistant Examiner—T. N. Quach

Attorney, Agent, or Firm—Oblon, Spivak, McClelland, Maier & Neustadt

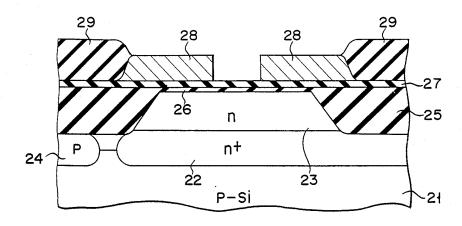
## [57] ABSTRACT

A method of manufacturing a bipolar transistor is disclosed. A first mask material film pattern is formed on an internal base region prospective portion on a collector region of a first conductive type, and then a first conductive film is deposited. A recess around the projection of the mask film pattern are transferred on the surface of the first conductive film. After a second mask material film pattern is buried in the recess, the first conductive film is selectively etched using the second mask material pattern as a mask, thereby exposing the first mask material film pattern. The first conductive film is continuously, selectively etched by anisotropic etching using the exposed first mask material film pattern and the second mask material film pattern as etching masks to form a first opening between the two mask material film patterns. An impurity of a second conductivity type is doped through the first opening to form an external base region. The first opening is buried with a second conductive film before or after formation of the external base region. The first mask material film pattern is removed to form a second opening. After a thermal oxide film is formed on the surface of the second conductive film, an impurity of the second conductivity type is doped through the second opening, thereby forming the internal base region. An impurity of the first conductivity type is doped in the wafer through the second opening to form an emitter region.

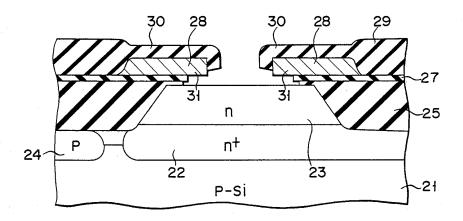
### 19 Claims, 16 Drawing Sheets



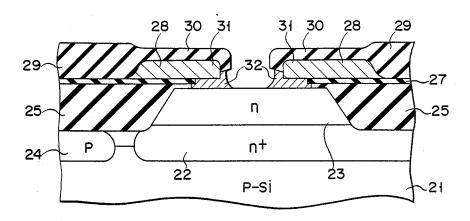




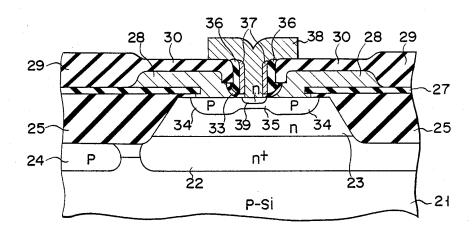
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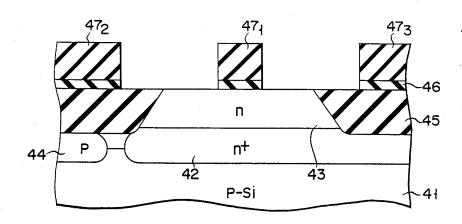
F I G. IB (PRIOR ART)



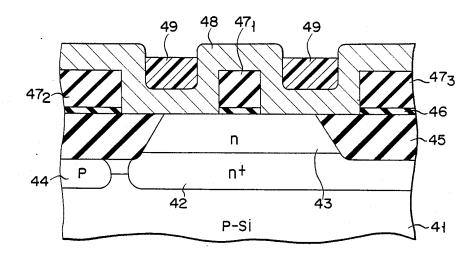
F I G. 1C (PRIOR ART)



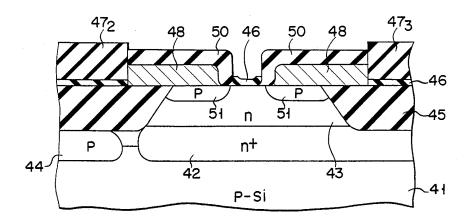
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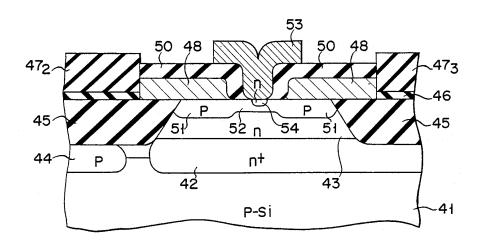
F I G. 2A (PRIOR ART)



F I G. 2B (PRIOR ART)



F I G. 2C (PRIOR ART)



F I G. 2D (PRIOR ART)

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