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(12) **United States Patent**  
**Ootsuka et al.**

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(45) **Date of Patent:** **Aug. 2, 2005**

(54) **METHOD FOR MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE**

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**Satoshi Yamamoto**, Ome (JP); **Satoshi Sakai**, Yokohama (JP)

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(73) Assignee: **Renesas Technology Corp.**, Tokyo (JP)

\* cited by examiner

(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 281 days.

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(30) **Foreign Application Priority Data**

Nov. 20, 2001 (JP) ..... 2001-355053

(51) **Int. Cl.**<sup>7</sup> ..... **H01L 21/302**

(52) **U.S. Cl.** ..... **438/696; 438/303; 438/305; 438/585; 438/591; 438/589; 438/595**

(58) **Field of Search** ..... 438/303, 305, 438/585, 591, 589, 595, 696

(56) **References Cited**

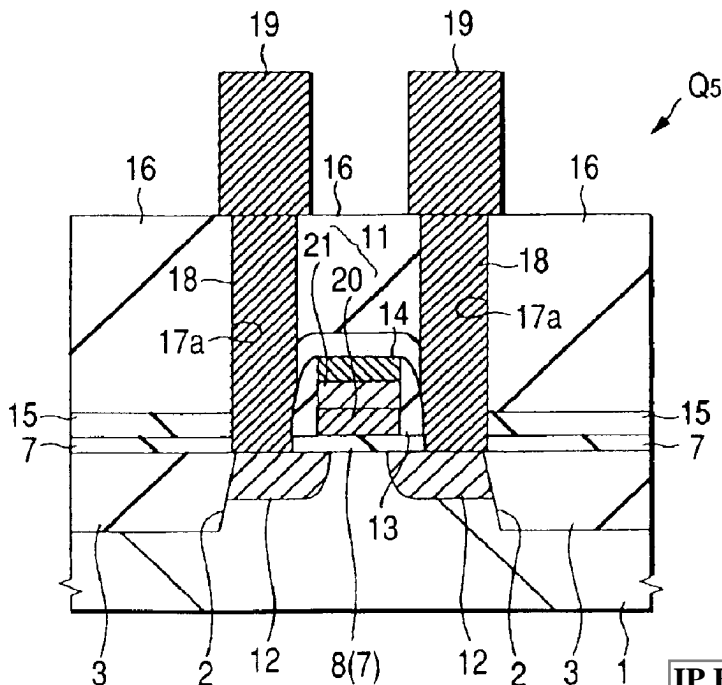
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(57) **ABSTRACT**

A method is used to form a circuit to achieve a high-speed performance and a circuit to attain a high reliability on one and the same substrate, in a semiconductor integrated circuit device containing MIS transistors, in which the gate insulating film is made of a high dielectric constant insulating film. In the method, the high dielectric constant insulating film is removed on the diffusion regions of the MIS transistors in the logic region and I/O region, and silicide layers of a low resistance are formed on the surfaces of the diffusion regions. In the memory region, on the other hand, the silicide layers are not formed on the diffusion regions of the MIS transistors, and the diffusion regions are covered with the high dielectric constant insulating film, thereby preventing damage to the semiconductor substrate during forming of the spacers, silicide layers, and contact holes.

**20 Claims, 11 Drawing Sheets**



**IP Bridge Exhibit 2217**

FIG. 1

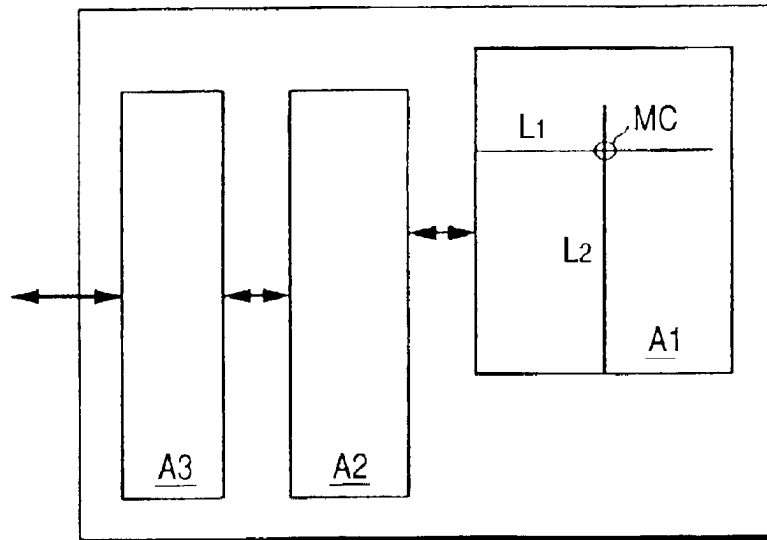


FIG. 2

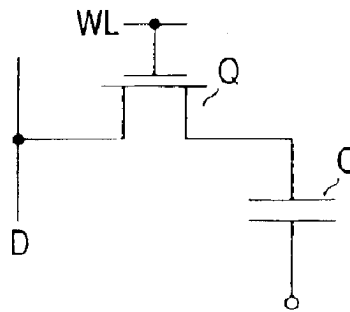


FIG. 3

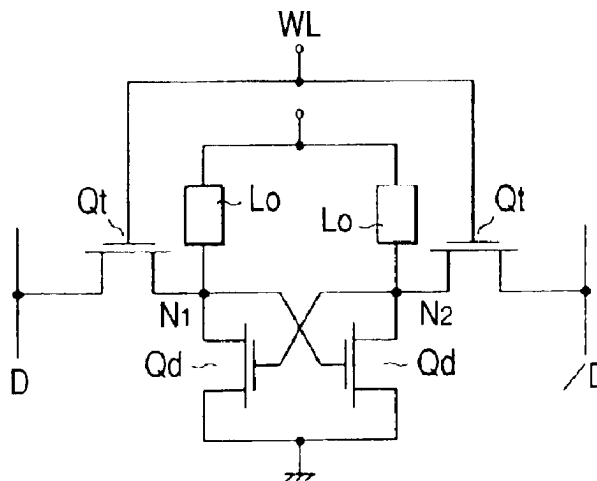


FIG. 4

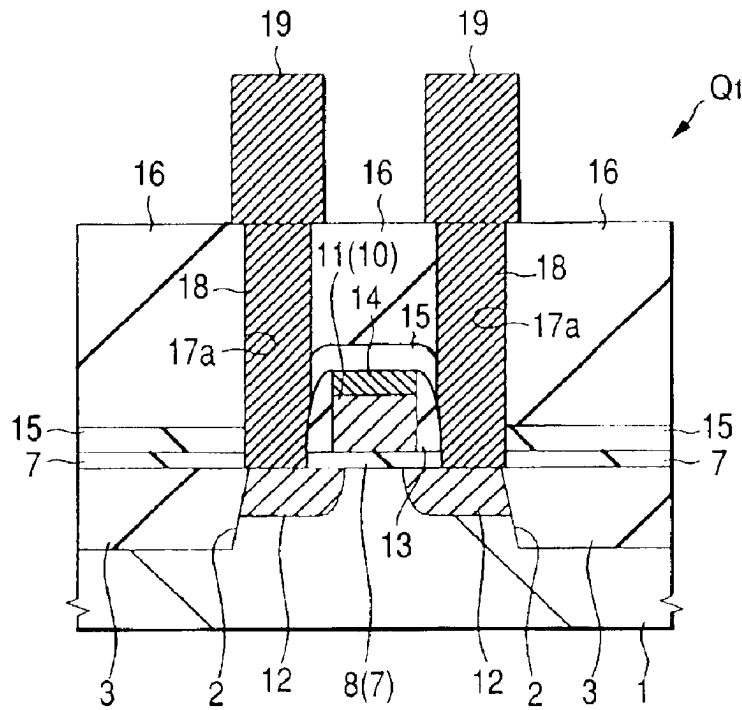


FIG. 5

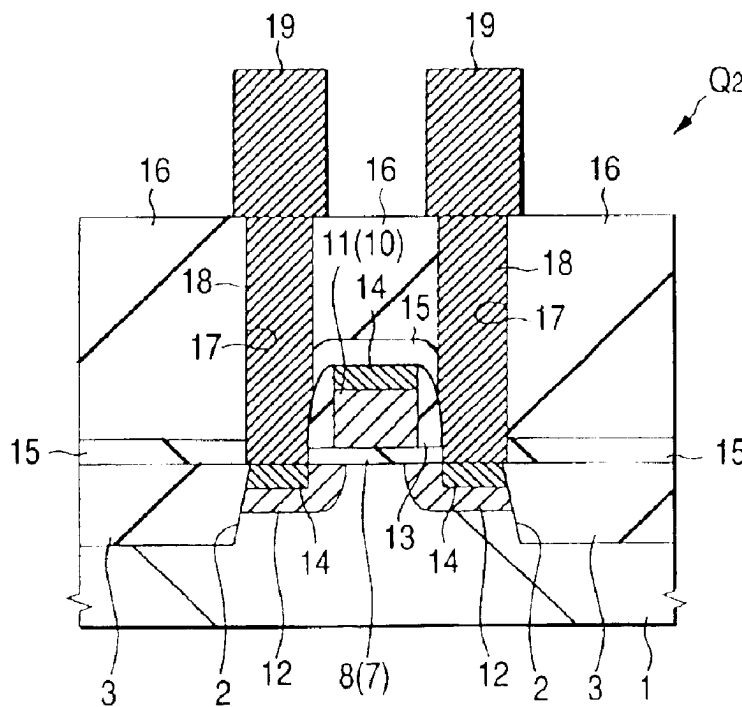


FIG. 6

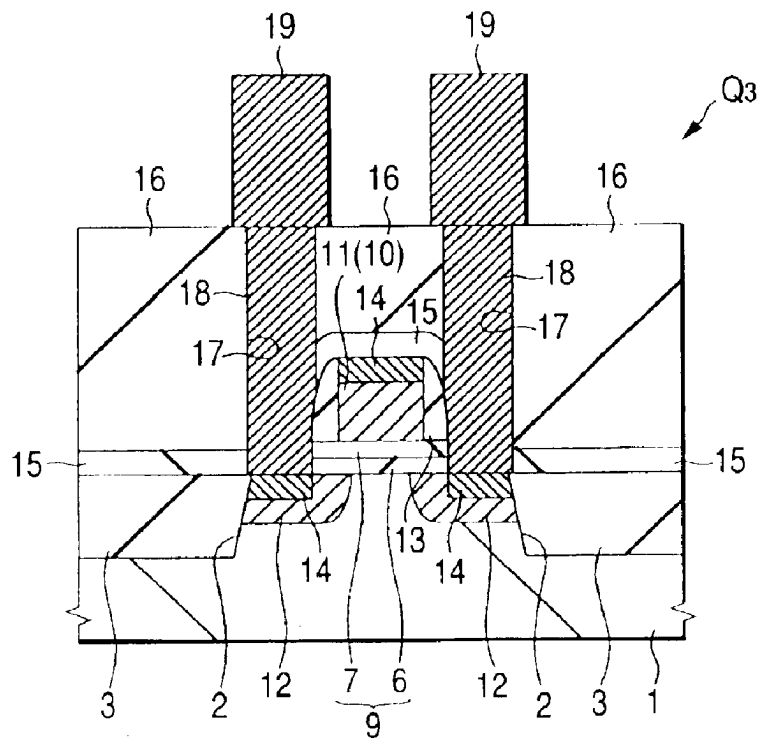


FIG. 7

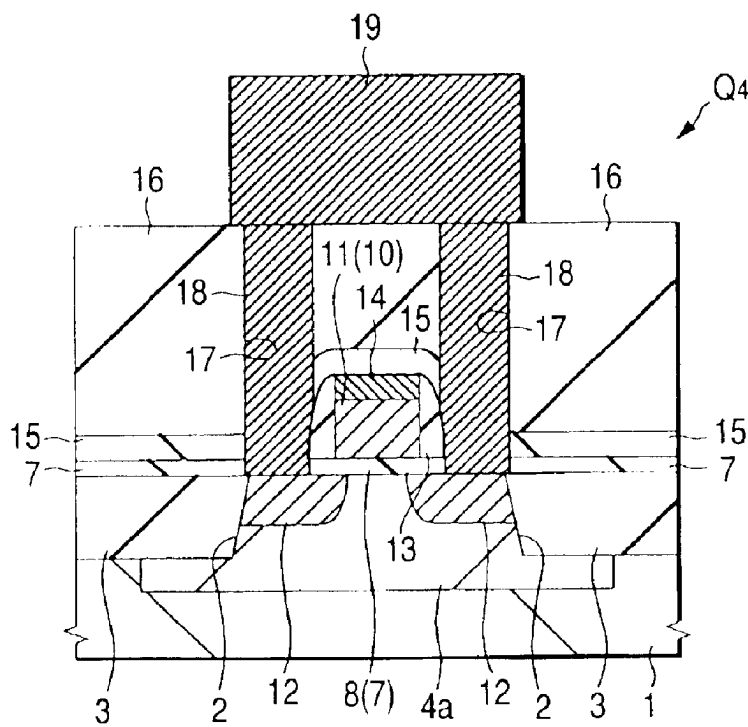


FIG. 8

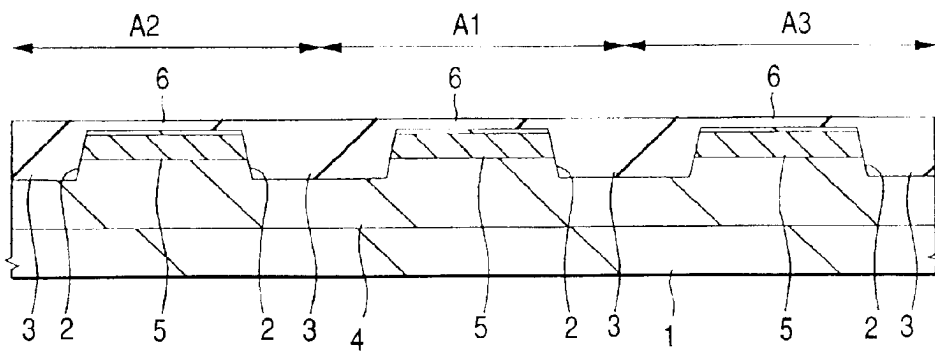
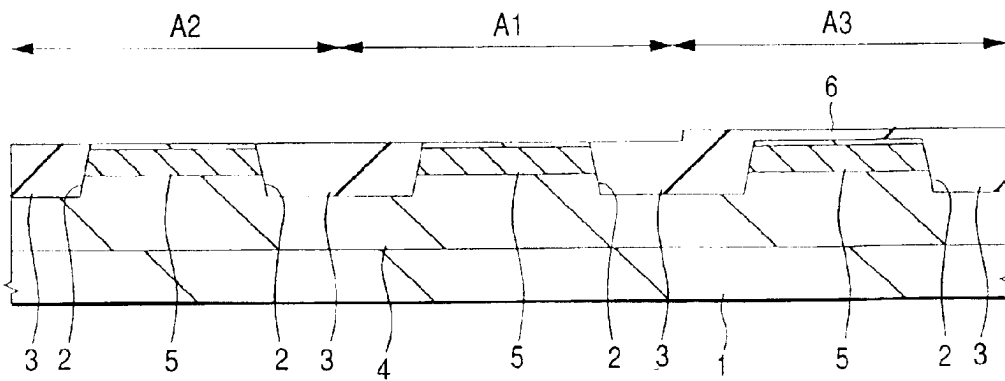


FIG. 9



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