Hot-Carrier Injection Suppression Due to the Nitride–Oxide LDD Spacer Structure

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***Abstract*—Hot carrier effects in silicon nitride LDD spacer MOSFET's have been investigated. It is found that the oxide thickness under the nitride film spacer affects hot-carrier effects. The thinner the LDD spacer oxide becomes, the larger the initial drain current degradation becomes at dc stress test and, in addition, the smaller the stress time dependence becomes. Moreover, after the dc stress test, reduced drain current recovers at room temperature. These phenomena are due to the large hot-carrier injection into the LDD nitride spacer, because the nitride film barrier height is much less than the silicon oxide barrier height. Therefore, it is necessary to form the LDD spacer oxide, in order to suppress the large hot-carrier injection in the nitride film LDD spacer MOSFET. Furthermore, the drain current shift mechanism in the nitride LDD spacer MOSFET's is also discussed, considering the lucky electron model.**

I. Introduction

GENERALLY, CVD–SiO_2 material has been used as the LDD spacer [1]. Recently, LDD MOSFET's with a silicon nitride spacer were studied [2], [3]. However, the nitride spacer is reported to cause large degradation in LDD MOSFET's, the mechanism of which is not quite clear [2]. Moreover, while it is known that LDD MOSFET degradation is due to the hot-carrier injection into the LDD spacer [4], the LDD spacer material influence on hot-carrier effects has not been investigated in detail.

It has been previously reported that the dielectric constant of LDD spacer affects LDD MOSFET performance [5]. In addition, when the dielectric constant of LDD spacer increases, the gate-fringing field becomes large. Therefore, because of this large gate-fringing field, high reliability and high current drivability can be realized in high dielectric LDD spacer MOSFET's (HLDD). However, with increasing the dielectric constant for an insulator, its bandgap energy decreases [6]. As a result, the barrier height for the high dielectric insulator decreases, which causes a large hot-carrier injection into its LDD spacer. Therefore, it is important to form the large barrier height insulator such as SiO_2 under the high dielectric LDD spacer.

In this paper, the authors discuss the influence of the sidewall SiO_2 thickness on the hot-carrier effects in Si_3N_4 or SiO_2 LDD spacer structure [7], which can be explained by the luckey electron model, and the LDD spacer oxide thickness is believed to play an important role in the MOSFET reliability. Moreover, we show relaxation phenomena of the MOSFET degradation after dc stress test.

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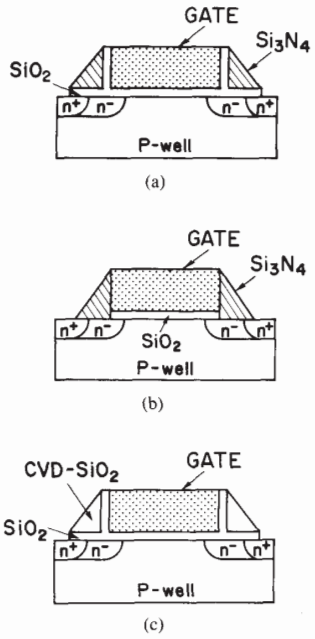

Fig. 1. Schematic cross sections of three different LDD spacer structures. (a) Si_3N_4 on SiO_2 LDD spacer structure (ONLDD). (b) Only Si_3N_4 film structure (NLDD). (c) Conventional SiO_2 LDD spacer (OLDD).

II. Experimental Procedure

Three types of LDD spacer structures were fabricated as shown in Fig. 1: (a) an LPCVD–Si_3N_4 film on thermal oxide (which is called the sidewall oxide) spacer (ONLDD), (b) an LPCVD–Si_3N_4 film spacer (N-LDD), and (c) a conventional CVD–SiO_2 film on a thermal oxide spacer and an only CVD–SiO_2 film spacer (O-LDD). An n-channel LDD MOSFET with the ONLDD structure was fabricated by reactive ion etching of 0.2-μm-thick deposited LPCVD–Si_3N_4 on the sidewall oxide. In both the nitride and the oxide film LDD spacer structures, the sidewall oxide was formed by dry O_2 oxidation just after forming the gate electrode and LDD n^- region. Sidewall oxide thickness T_{ox} conditions at the Si surface were changed by dry O_2 oxidation time and are 0, 15, and 25 nm. The ONLDD hot-carrier effects were investigated, comparing to those of the NLDD structure (2.5-nm-thick native oxide) and the OLDD structure. LDD spacer width is about 0.2 μm. The gate poly-silicon length and the channel width are 0.8 and 10 μm, respectively. The p-well region and the LLD n^- region concentration are about 2×10^{17} cm^{-3} and 5×10^{18} cm^{-3}, respectively. Gate oxide thickness T_g is 15 nm.

Drain current characteristics of LDD MOSFETs after dc stress test were measured at the drain and gate biases of 3.3 V in the reverse mode to the stress condition. The substrate bias is −1.5 V, in order to improve the subthreshold characteristics.

The ONLDD and the OLDD data are mainly those with 25-nm-thick sidewall oxide.

III. Results and Discussion

A. Drain-Current Degradation Phenomena

1) DC Stress Test: Fig. 2 shows the drain-current degradation rate $\Delta I_d/I_d$ versus stress time t at dc stress test of $V_d = 6$ V, $V_g = 3$ V. NLDD data show the large degradation of the drain current at very small stress time. As LDD spacer oxide thickness becomes thick, such as ONLDD and OLDD, the initial drain current degradation becomes small. On the contrary, the stress time dependence of drain current degradation becomes small when the LDD spacer oxide becomes thin, such as NLDD. Fig. 3 shows the substrate current reduction rate as a function of the stress time at the same dc stress conditions as in Fig. 2. The substrate current was measured at the same dc stress biases in the forward mode. It is also found that the stress time dependence of the substrate-current shift is affected by the LDD spacer oxide thickness, and the substrate-current shift dependence on stress time in NLDD is about two magnitudes faster than the ONLDD data. The substrate current shift in NLDD starts at about 10 ms.

On the other hand, in the case of an NLDD, when the LDD spacer oxide thickness is nearly equal to zero, V_{th} values are not changed at dc stress test, as shown in Fig. 4. However, V_{th} shifts in the case of both ONLDD and OLDD. These phenomena can be explained by the following discussion.

According to the discussion by Katto [8], trapped charges in the LDD spacer also cause the V_{th} shift even in an LDD MOSFET. Therefore, NLDD data shown in Figs. 2 and 4 indicate that in NLDD the injected hot electron does not get trapped and can generate only the interface state in NLDD sidewall structure. This generated interface state is considered to cause the transconductance degradation in NLDD, resulting in the drain current shift in NLDD shown in Fig. 2.

We estimate the I_d shift rate due to the only trapped charge. Since the drain current is proportional to $(V_g - V_{th})$ in a short-channel MOSFET [14], the I_d shift rate due to the trapped charge can be expressed as follows:

$$\frac{\Delta I_d}{I_d} = \frac{\Delta V_{th}}{V_g - V_{th}} \tag{1}$$

where ΔI_d and ΔV_{th} are the I_d shift and V_{th} shift, respectively. According to the V_{th} shift data at 1 h shown in Fig. 4, the I_d shift rate for NLDD, ONLDD, and OLDD can be calculated to be about 0%, 0.7%, and 0.7%, respectively. Since the I_d shift for NLDD, ONLDD, and OLDD are about 4%, 3%, 1.5%, respectively, as shown in Fig. 2, the trapped charge causes less than one half of the total I_d shift. Therefore, it is found that the I_d shift is mainly caused by the interface state generation.

However, the OLDD data with 0 and 15-nm-thick sidewall oxide were almost the same as those at $T_{ox} = 25$ nm shown in Figs. 2 and 4. In the case of OLDD, sidewall oxide thickness did not affect the hot-carrier effects. Namely, the gate bird's beak does not affect hot-carrier effects in OLDD. Therefore, it is found that hot-carrier effects in both ONLDD and NLDD are not affected by the gate bird's beak formed from the sidewall oxidation process and depend on the sidewall oxide as mentioned above. This is considered to be due to the reason that the gate to n^- region overlap length is longer than that of the gate bird's beak [17].

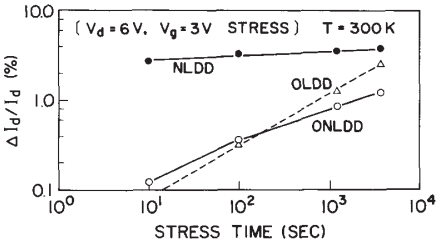

Fig. 2. Drain current degradation rate at dc stress test (V_d = 6 V, V_g = 3 V).

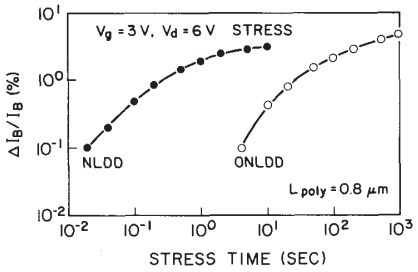

Fig. 3. Substrate current degradation rate at the same dc stress test as in Fig. 2.

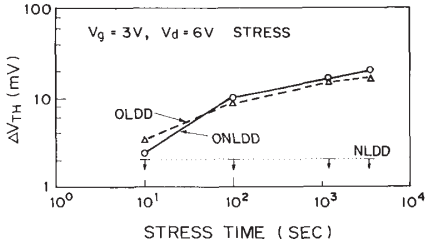

Fig. 4. Threshold voltage shift versus stress time at the same dc stress test as in Fig. 2.

The band diagram at the LDD spacer is shown in Fig. 5. It shows the schematic energy band diagram across the electric field from the drain n^- region to the gate electrode in ONLDD or NLDD. The trap level in Si_3N_4 film is reported to be very shallow and be about 0.8 eV by Svensson *et al.* [9]. Therefore, the injected hot electron cannot be trapped in the nitride film or the trapped hot electron can be detrapped. Namely, the injected hot electron can be trapped only in the oxide. Since the hot carrier is mainly injected into the LDD sidewall region and is trapped only in the LDD sidewall oxide, the V_{th} shift is caused by the trapped charge in the LDD sidewall oxide. In addition, since the injected hot carrier is considered to be uniformly trapped in the LDD sidewall oxide, the V_{th} shift is condsidered to be proportional to the square of the LDD sidewall oxide thickness [10]. Therefore, V_{th} does not shift in the case of NLDD as shown in Fig. 4, because of its very thin sidewall oxide.

2) Stress Time Dependence in the Nitride LDD Spacer Structure: Generally, I_d degradation rate is experimentally

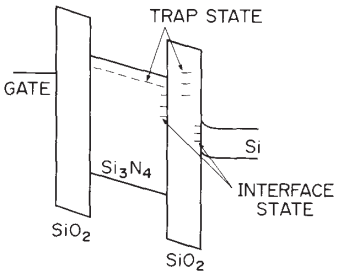

Fig. 5. Schematic band diagram of the Si_3N_4/SiO_2 spacer structure across the electric field from the drain n^- region to the gate electrode. Interface states exist at both the Si_3N_4/SiO_2 and the SiO_2/Si interfaces. Moreover, trap levels also exist in both the Si_3N_4 and the SiO_2 films.

given by the stress time power law as follows [11]:

$$\frac{\Delta I_d}{I_d} = I_b^m A t^\alpha \tag{2}$$

where I_b is the substrate current and A, α, and m are parameters.

Physical meaning of these parameters has not been clear, but these parameters are very important to predict the lifetime for the devices in the hot-carrier effects. Moreover, these parameters are obtained by fitting (2) to the data as shown in Fig. 2.

This section discusses the LDD spacer oxide thickness dependence of parameters in (2) at the fixed stress drain bias of 6 V. Moreover, it is shown that all parameters in (2) can be expressed by a function of the sidewall oxide thickness. Since the LDD spacer oxide thickness is relatively small in this study and the dielectric constant for the nitride film is not large, the gate-fringing field in both NLDD and ONLDD [5] is not affected by the LDD spacer oxide thickness and is not large.

Index m in (2) is determined by changing the gate length. Fig. 6 shows the drain current degradation rate for a 1-h dc stress test versus the substrate current at various gate lengths. It is clear that the I_d shift is proportional to the power of the substrate current. However, index m is changed by the LDD spacer oxide thickness. Fig. 7 shows index m versus LDD spacer oxide thickness. As shown in Fig. 7, m becomes small, when the LDD spacer oxide becomes thin. At $V_g = 3$ V, parameter m of the thicker sidewall oxide devices is about 1 and is almost the same as that of Kinugawa *et al.* (~ 0.9) [11]. In addition, index m is proportional to the power of the LDD spacer oxide thickness T_{ox} as follows:

$$m = m_0 T_{ox}^\beta \tag{3}$$

where m_0 and β are parameters.

If T_{ox} becomes zero, the I_d shift does not depend on the substrate current. Therefore, the I_d shift in NLDD remains constant, in spite of an increase in the stress drain bias and the shrinking gate length.

Fig. 8 shows the stress gate bias dependence for parameters m_0 and β in (3). According to Fig. 8, since β is about 0.5 at $V_g < 4$ V, index m can be expressed as follows:

$$m = m_0 T_{ox}^{0.5}. \tag{4}$$

Since, in the case of $V_g > 4$ V, m_0 is constant at 0.3 and β decreases in $V_g > 4$ V, T_{ox} dependence of index m becomes small. This is due to the large hot-electron injection rate in large stress gate bias. As a result, at shorter channel length, it is important to reduce the LDD spacer oxide thickness, such as

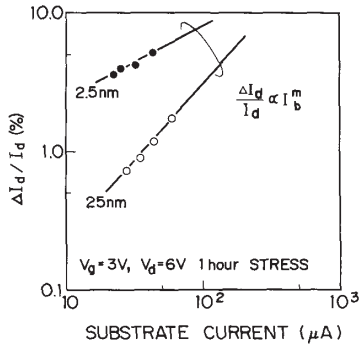

Fig. 6. Drain current degradation, as a function of the initial substrate current at the 1-h dc stress test ($V_g = 3$ V, $V_d = 6$ V) in various gate lengths.

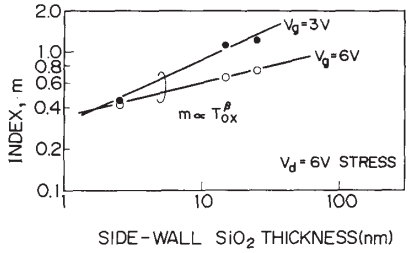

Fig. 7. Index m in (2) versus the LDD spacer oxide thickness at the dc stress test ($V_g = 3$ V, $V_d = 6$ V). The solid lines show the T_{ox} power law of index m.

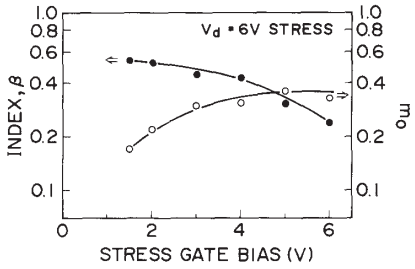

Fig. 8. Parameters β and m_0 in (3) versus stress gate bias. Closed and open circles show β and m_0, respectively.

NLDD, in order to reduce the substrate current dependence of the index m.

Next, according to Fig. 2, parameters A and α in (2) are dependent on the LDD spacer oxide thickness under the nitride film spacer. Moreover, as the LDD spacer oxide becomes thin, the initial degradation parameter A becomes large. On the contrary, the stress time coefficient α becomes small. By fitting the I_d shift data at various stress gate bias values to (2), we have determined the LDD spacer oxide thickness dependence of parameters A and α.

Fig. 9 shows the initial degradation parameter A as a function of T_{ox}. According to Fig. 9, A is clearly proportional to the inverse of the power of T_{ox}. That is

$$A = A_0 T_{ox}^{-\delta} \tag{5}$$

where A_0 and δ are parameters.

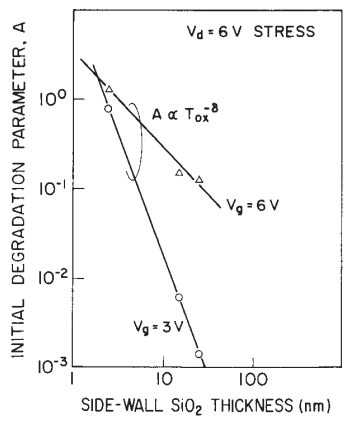

Fig. 9. Initial degradation parameter A versus the LDD spacer oxide thickness. Solid lines show the T_{ox} power law of A.

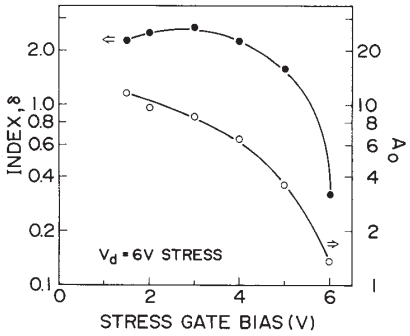

Fig. 10. Parameters δ and A_0 in (5) versus stress gate bias. Closed and open circles show δ and A_0, respectively.

Fig. 10 shows parameters A_0 and δ as a function of stress gate bias. By fitting data to (5), δ is about 2 in $V_g < 4$ V, resulting in $A \propto 1/T_{ox}^2$, as shown in Fig. 10. As a result, the initial degradation parameter A becomes large in decreasing T_{ox} by the $1/T_{ox}^2$ law. Moreover, A_0 and δ suddenly decrease in $V_g > 4$ V.

Consequently, in order to reduce the initial degradation, it is necessary to thicken the LDD spacer oxide, such as OLDD structure.

Finally, Fig. 11 shows the stress time coefficient α versus the LDD spacer oxide thickness T_{ox}. In thicker sidewall oxide devices, α is about 0.2 and is almost the same as that of Kinugawa *et al.* ($\sim$0.2) [11]. It is obvious that α is proportional to the power of T_{ox}. Therefore, α can be expressed as follows:

$$\alpha = \alpha_0 T_{ox}^n \tag{6}$$

where α_0 and n are parameters.

The stress time coefficient α becomes small with a decrease in T_{ox} and becomes zero in the case of LDD structure without the oxide. This means that the I_d shift of a no-oxide LDD spacer becomes constant, in spite of the increase of the stress time.

By fitting data to (6), index n in (6) is shown by the open circles in Fig. 12. Index n is a constant unity in $V_g < 4$ V, resulting in $\alpha \propto T_{ox}$. However, n decreases varied from 1 to 0.2 in $V_g > 4$ V. On the other hand, α_0 is almost constant at $V_g < 3$ V, but increases at $V_g > 3$ V.

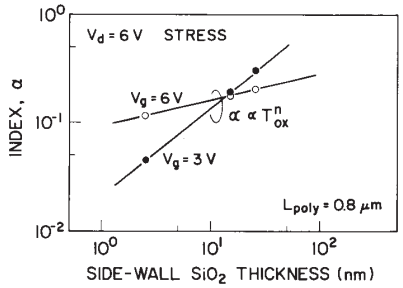

Fig. 11. Stress time coefficient α versus T_{ox}. Solid lines show the T_{ox} power law of α.

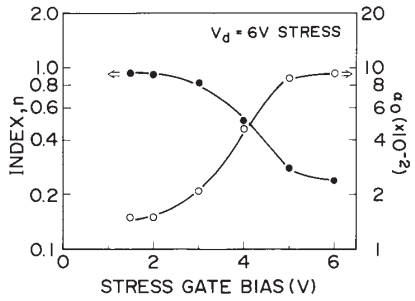

Fig. 12. Parameters n and α_0 in (6) versus stress gate bias. Closed and open circles show n and α_0, respectively.

Consequently, parameters m, A, and α in (2) strongly depend on LDD spacer oxide thickness. In addition, the initial degradation parameter dependence on the LDD spacer oxide thickness is opposite to the stress time coefficient dependence. Therefore, it is important to optimize the LDD spacer oxide thickness in order to realize highly reliable LDD MOSFET's.

According to the above discussion, drain current shift equation (1) can be expressed by the LDD spacer oxide thickness, in the case of the maximum substrate current dc stress test conditions, as follows:

$$\frac{\Delta I_d}{I_d} = I_b^{m_0\sqrt{T_{ox}}} \frac{A_0}{T_{ox}^2} t^{\alpha_0 T_{ox}}. \tag{7}$$

On the other hand, it is clear that the dependence of all parameters in (2) on T_{ox} becomes smaller at a larger stress gate bias. This is probably due to the high hot-carrier injection rate at larger stress gate bias conditions. In the case of other drain stress bias conditions, parameters in (2) can be also obtained by fitting data to (2), but parameters in (2) are considered to be different from the values in (7) because of their different hot-carrier injection rate.

3) Stress Drain Bias Dependence: Fig. 13 shows the stress drain bias dependence of the I_d shift at the maximum substrate current dc stress test for 1 h. In the case of NLDD, the I_d shift does not increase and remains constant, in spite of increasing stress drain bias at $V_d > 5$ V. This is caused by the weak substrate current dependence and small stress time coefficient in NLDD as mentioned before.

Moreover, the I_d shift of NLDD is observed in a small stress drain bias region of NLDD, compared to ONLDD data. This indicates that the interface state in NLDD can be generated by low-energy hot carriers. On the other hand, no I_d shift in

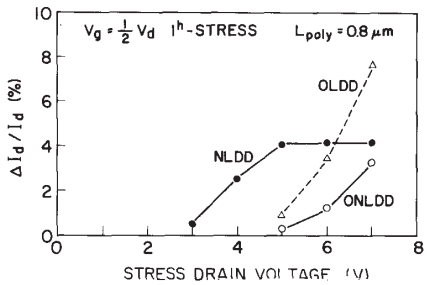

Fig. 13. Drain current shift versus stress drain bias at the maximum substrate current dc stress test for 1 h.

ONLDD is observed in small stress drain bias, which indicates that LDD spacer oxide suppresses the low-energy hot-carrier injection. However, stress drain bias dependence of the drain current shift becomes large in ONLDD and OLDD. Especially in OLDD, the drain current at 7 V stress drain bias becomes larger than that of NLDD, because of the former's large stress time coefficient.

Consequently, high reliability in the ONLDD structure can be realized by both the LDD spacer oxide suppression of hot-carrier injection and the gate-fringing field effects [5].

B. I_d-Shift-Relaxation Phenomena in NLDD

Generally, the I_d shift in MOSFET does not recover after dc stress test. Here, Fig. 14 shows the reduced drain current relaxation phenomena after 5-h dc stress test ($V_g = 3$ V, $V_d = 6$ V), where all terminals biases for MOSFET's are 0 V. In NLDD, reduced drain current is recovered at room temperature. Moreover, its relaxation time constant τ at room temperature is nearly equal to that at high temperature (400 K). These results indicate that the activation energy for the interface state in NLDD is very small and is considered to be almost equal to the room temperature thermal energy. According to this small activation energy in NLDD, the interface state between Si_3N_4 and the native oxide is considered to be generated by low-energy hot-carrier injection, which causes the large initial degradation parameter, shown in Fig. 9, and the I_d shift in low stress drain bias, shown in Fig. 13.

On the contrary, in the OLDD structure, reduced drain current does not recover, even at high temperature. According to these data, the time constant is very large in OLDD, which is considered to be due to high activation energy of the SiO_2/Si interface. Therefore, high activation energy in OLDD suppresses the initial degradation parameter, compared to that in NLDD.

Moreover, new recovery data for the I_d shift in NLDD are also shown in Fig. 15, which shows the I_d shift phenomena as a parameter of dc stress drain bias, at and after the dc stress test. In Fig. 15, the dc stress test at $t < 0$ stops at $t = 0$ and a relaxation test is carried out at $t > 0$. It has been recently found that reduced drain current does not recover at all in low stress drain bias conditions. That is, at $V_d = 4$ V stress test reduced drain current does not recover at all, in spite of the same I_d shift as that at $V_d = 6$ V dc stress test. Moreover, according to Figs. 14 and 15, reduced drain current cannot completely recover and its relaxation rate (which is defined by the I_d shift rate after relaxation test minus the maximum I_d shift at the dc stress test) is about 1%.

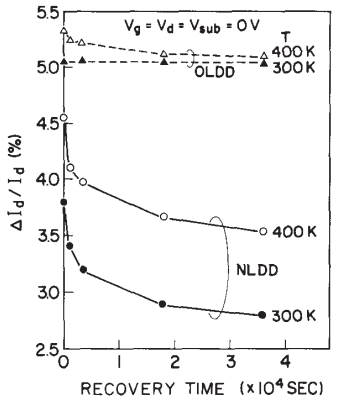

Fig. 14. Relaxation phenomena of the drain current shift rate to the initial current, after dc stress test ($V_g = 3$ V, $V_d = 6$ V) for 5 h. The relaxation bias conditions are all terminal grounded in MOSFET's.

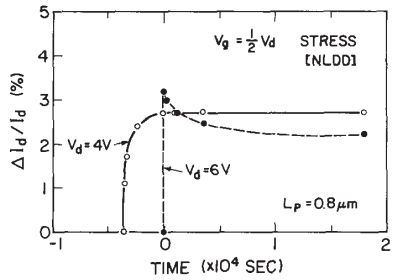

Fig. 15. Drain current shift rate behavior, at and after dc stress test, as a parameter of stress drain bias. DC stress test at $t < 0$ stops at $t = 0$ and the relaxation test is carried out in $t > 0$. By the way, the result of NLDD around $t = 0$ s is the data for $t = -10$ s.

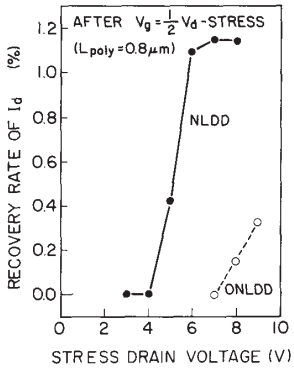

Fig. 16. Relaxation rate of I_d shift versus stress drain bias at the maximum substrate current dc stress test. Sidewall oxide thickness of ONLDD is 15 nm in this figure. Relaxation rate is defined as the I_d shift rate after the relaxation test minus the maximum I_d shift at the dc stress test.

Fig. 16 shows the I_d shift relaxation rate as a function of dc stress drain bias at the maximum substrate current dc stress test. The I_d shift can recover, when the stress drain bias becomes larger than 5 V, and is not observed at a stress $V_d < 5$ V. In addition, the relaxation rate of the I_d shift approaches a saturated value (about 1%) with increasing stress drain bias and

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