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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.
Petitioner

v.

GODO KAISHA IP BRIDGE 1
Patent Owner.

Case IPR2017-01842

PETITIONER'S UPDATED EXHIBIT LIST

Pursuant to the Board's Order dated December 29, 2017, Petitioner hereby submits the December 19, 2017 Conference Call Transcript as Exhibit 1129 and the infringement contentions dated February 1, 2017 for U.S. Patent 7,893,501 from *Godo Kaisha IP Bridge 1 v. Xilinx, Inc.*, Case No. 2:17-cv-00100 (E.D. Tex.) as Exhibit 1130. Petitioner also hereby submits an updated exhibit list.

Respectfully Submitted,

/ Michael Smith/

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CERTIFICATE OF SERVICE

I hereby certify that, on January 9, 2018, I caused a true and correct copy of the foregoing materials:

- Petitioner's Updated Exhibit List
- Petitioner's List of Exhibits
- Exhibits 1129 and 1130

to be served via email on the following counsel of record as listed in Patent Owner's Mandatory Notices:

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Respectfully Submitted,

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PETITIONER'S LIST OF EXHIBITS FOR
IPR2017-01842

Exhibit	Description
1101	U.S. Patent No. 7,893,501
1102	Declaration of Stanley R. Shanfield, Ph.D. Regarding U.S. Patent No. 7,893,501, Claims 5, 6, 12, 13, 15, 19, and 21 ("Shanfield Decl.")
1103	Applicant's Amendment and Response dated August 6, 2010
1104	U.S. Patent Publication No. 2002/0145156 to Igarashi et al. ("Igarashi")
1105	U.S. Patent No. 5,960,270 to Misra et al. ("Misra")
1106	J. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice and Modeling</i> , (1 st ed. 2000)
1107	U.S. Patent Publication No. 2002/0000611 to Hokazono et al. ("Hokazono")
1108	U.S. Patent No. 6,228,777 ("Arafa")
1109	U.S. Patent No. 6,406,963 to Woerlee et al. ("Woerlee")
1110	J. Rabaey et al., <i>Digital Integrated Circuits</i> , at 40-44 (2d ed. 2003)
1111	S. Kang and Y. Leblebici, <i>CMOS Digital Integrated Circuits: Analysis and Design</i> , (2d. ed. 2003)
1112	K. Maex, <i>Simply irresistible silicides</i> , Physics World, at 35-39 (Nov. 1995)
1113	Notice of Allowance dated October 15, 2010
1114	U.S. Patent No. 6,444,566 to Tsai et al. ("Tsai")

Exhibit	Description
1115	Fumio Shimura, <i>Semiconductor Silicon Crystal Technology</i> , at 104-112 (1989) (“Shimura Textbook”)
1116	J. Moon et al., <i>A New LDD Structure: Total Overlap with Polysilicon Spacer (TOPS)</i> , IEEE Electron Device Letters, Vol. 11, No. 5, at 221-223 (May 1990)
1117	D. Baglee et al., <i>Reduced Hot-Electron Effects in MOSFET's with an Optimized LDD Structure</i> , IEEE Electron Device Letters, Vol. EDL-5, No. 10, at 389-391 (Oct. 1984)
1118	W.O. Publication No. 2002/043151 with certified English translation (“Shimizu”)
1119	M. Green et al., <i>Ultrathin (<4 nm) SiO₂ and Si-O-N gate dielectric layers for silicon microelectronics: Understanding the processing, structure, and physical and electrical limits</i> , J. Appl. Phys., Vol. 90, No. 5, at 2057-2121 (Sep. 1, 2001)
1120	E. Gusev et al., <i>Growth and characterization of ultrathin nitride silicon oxide films</i> , IBM J. Res. And Dev., Vol. 43, No. 3, at 265-286 (May 3, 1999)
1121	H. Wong, <i>Beyond the conventional transistor</i> , IBM Journal of Research and Development, Vol. 46, No. 2/3, at 133-168 (March/May 2002)
1122	U.S. Patent No. 6,509,234
1123	U.S. Patent No. 5,726,479
1124	U.S. Patent No. 6,512,266
1125	U.S. Patent No. 6,806,584
1126	Togo, M. et al. “Low Leakage and High Reliability 1.5 nm SiON Gate-Dielectric Using Radical Oxynitridation for Sub-0.1 μm

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