UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2017-01841
Patent 7,893,501

IP Bridge Exhibit 2027
TSMC v. Godo Kaisha IP Bridge 1
IPR2017-01841

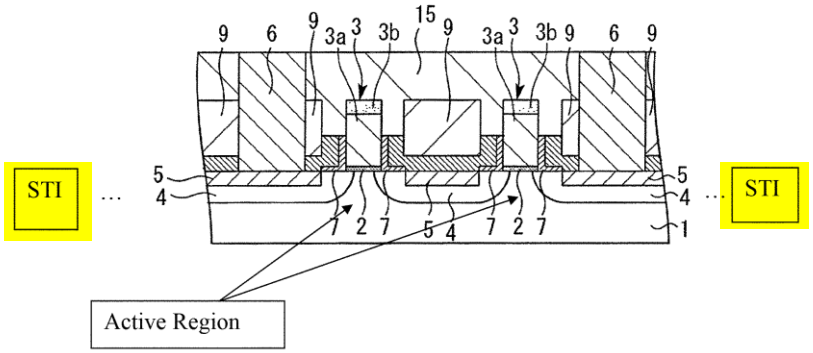
PATENT OWNER'S DEMONSTRATIVE EXHIBITS

I. INTRODUCTION

Patent Owner's Response ("Response") confirms that the challenged claims are unpatentable. There is no dispute that Igarashi discloses the allegedly novel "protruding gate" that provided the basis for allowance.[2] Moreover, Patent Owner ("PO") does not dispute that the instituted grounds expressly disclose every limitation of the challenged claims, except the "active region." Nor does PO dispute that the references would have been obvious to combine. Instead, PO merely repeats the same arguments that it already raised in its Patent Owner's Preliminary Response ("POPR"[3]) that Igarashi's disclosure somehow lacks an "active region," one of the most basic aspects of a semiconductor device. These

Reply, Paper No. 22, at 1

Fig. 12



(Igarashi at Fig. 12 (Ex-1004) (annotated).) (Shanfield Decl. ¶66 (Ex-1002).)

To the extent that Igarashi does not explicitly disclose the location of the "active element region" and therefore that the active region is "made of" the semiconductor substrate, Woerlee discloses this limitation. (Shanfield Decl. ¶67 (Ex-1002).) For example, Woerlee discloses an active region 4 "made of" the semiconductor body 1 in Fig. 13:

Petition, Paper No. 2, at 27

"Petitions Fail to Demonstrate that the Igarashi/Woerlee Device Comprises a MISFET that Includes an 'Active Region' as Required by All Challenged claims." (POR, 37)

1. A semiconductor device, comprising a MISFET, wherein

the MISFET includes:

an active region made of a semiconductor substrate;

a gate insulating film formed on the active region;

a gate electrode formed on the gate insulating film;

source/drain regions formed in regions of the active region located on both sides of the gate electrode; and

a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein:

the silicon nitride film is not formed on an upper surface of the gate electrode, and

the gate electrode protrudes upward from a surface level of parts of the silicon nitride film located at both side surfaces of the gate electrode.

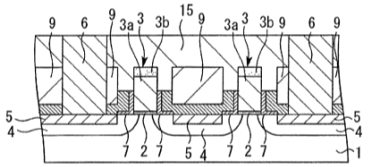
Ex. 1001, '501 patent at Claim 1

b) Claim 1 – Active Region (element [1a])

Claim 1 recites "an active region made of a semiconductor substrate." ('501 patent, claim 1 (Ex-1001).) Igarashi in view of Woerlee discloses this limitation. (Shanfield Decl. ¶64 (Ex-1002).)

For example, Igarashi discloses a "semiconductor substrate 1," as illustrated in Fig. 12:

Fig. 12



(Igarashi at Fig. 12 (Ex-1004); *see also, e.g., id.* at [0044]-[0045], [0112] (discussing the "semiconductor substrate 1").) (Shanfield Decl. ¶65 (Ex-1002).)

A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made

Petition, Paper No. 2, at 24, 25

regions) in Woerlee are formed in regions of the active region 4 located on both sides of the gate electrode 21 (as recited in claim 1, element 1d below). The modified device would also have an active element region (active region) divided by the STI regions (isolation region) formed in the semiconductor substrate 1 (as recited in claim 10 below), just as the active region 4 is divided by an isolation region 3 formed in the semiconductor substrate 1 in Woerlee. (Shanfield Decl. ¶73 (Ex-1002).)

Therefore, Igarashi in view of Woerlee discloses "an active region made of a semiconductor substrate." (Shanfield Decl. ¶74 (Ex-1002).)

c) Claim 1 – Active Region (element [1a]) – Reasons to Modify

It would have been obvious to modify Igarashi in view of Woerlee's teachings of an active region "made of" a semiconductor substrate (recited in claim 1, element 1a) and an active region divided by an isolation region formed in the semiconductor substrate (recited in claim 10 below). In particular, it would have been obvious to apply Woerlee's teachings to Igarashi by forming Igarashi's active region in the substrate and defining it with STI regions that divide the active region. (Shanfield Decl. ¶75 (Ex-1002).)

First, a POSITA would have looked to the teachings of Woerlee because it is in the same field of endeavor as Igarashi. Igarashi discloses a MISFET device with a "silicon semiconductor substrate 1" where "[e]lement isolation is performed" to

32

Petition, Paper No. 2, at 32

"Petition's … rationale … supporting the assertion that Igarashi teaches … Fig. 12 includes STI regions … is non-existent." POR 38-39

1. A semiconductor device, comprising a MISFET, wherein

the MISFET includes:

an active region made of a semiconductor substrate;

a gate insulating film formed on the active region;

a gate electrode formed on the gate insulating film;

source/drain regions formed in regions of the active region located on both sides of the gate electrode; and

a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein:

the silicon nitride film is not formed on an upper surface of the gate electrode, and

the gate electrode protrudes upward from a surface level of parts of the silicon nitride film located at both side surfaces of the gate electrode.

Ex. 1001, '501 patent at Claim 1

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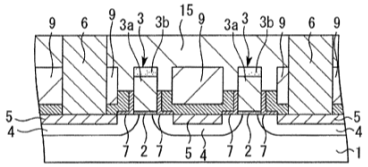


(Igarashi at Fig. 12 (Ex-1004); *see also, e.g., id.* at [0044]-[0045], [0112] (discussing the "semiconductor substrate 1").) (Shanfield Decl. ¶65 (Ex-1002).)

A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made

Petition, Paper No. 2, at 24, 25

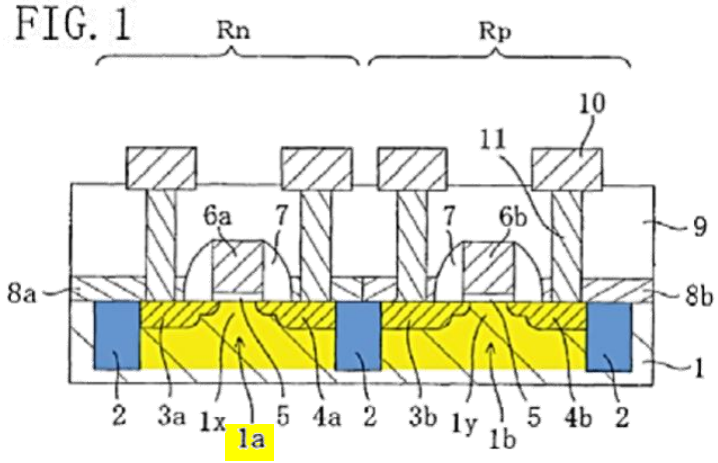
Based on the current record, however, we find it is clear from Igarashi that the disclosure of "active element region[s]" discussed in paragraph 68 with respect to the "First Embodiment" is equally applicable to the "Fifth Embodiment" upon which Petitioner primarily relies. For example, the description of the method for manufacturing the semiconductor device of the "Fifth Embodiment" refers back to earlier described embodiments of Igarashi, ultimately referencing the discussion of the method for manufacturing the semiconductor device of the "First Embodiment." Ex. 1004 ¶ 119 ("FIGS. 13A and 13[B] are schematic sectional views sequentially showing the method for manufacturing the semiconductor device shown in FIG. 12 [the Fifth Embodiment]. Here, FIG. 13A shows the same process as in FIG. 11B . . . ."), ¶¶ 112–13 ("FIGS. 11A to 11C are schematic sectional views showing the method for manufacturing the semiconductor device shown in FIG. 10 [the Fourth Embodiment]. . . . First, as FIG. 11A shows, gate electrodes 3 are formed, and silicon nitride films 7 and silicon nitride films S are formed so as to cover the gate electrodes 3 in the same process as in FIG. 5 . . . ."), ¶ 68 ("[T]he method for manufacturing the semiconductor device of First Embodiment will be described. In the following description of the manufacturing method, the major process for forming the silicon nitride film 7 will be described referring to FIGS. 5A to 5E, and other processes will be described without referring to drawings. First, an insulating film for isolating elements is formed on a silicon semiconductor substrate 1. Element isolation is performed using methods such as the LOCOS method or the trench method. Thereafter, ion implantation is performed to the active element region for forming the well and controlling the threshold value.").

Institution Decision, Paper No. 10, at 19

Intrinsic Evidence – Active Region

1. A semiconductor device, comprising a MISFET, wherein
the MISFET includes:
an active region made of a semiconductor substrate;

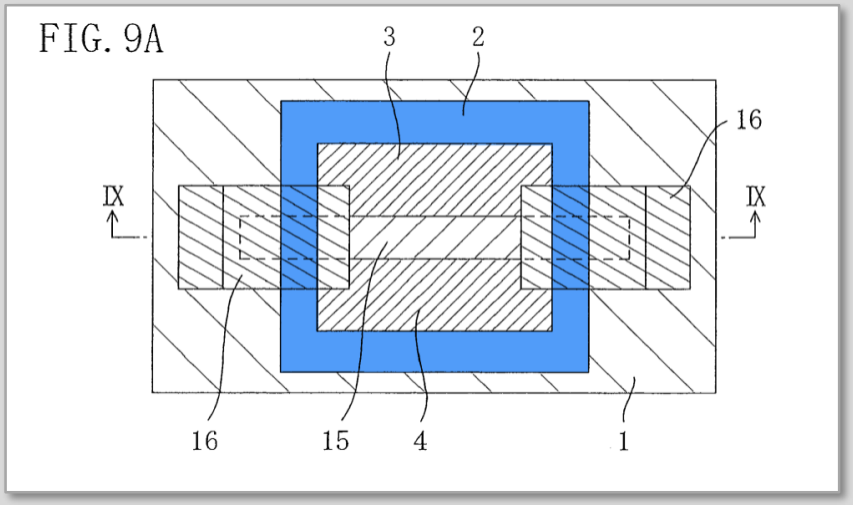
'501 patent at Claim 1



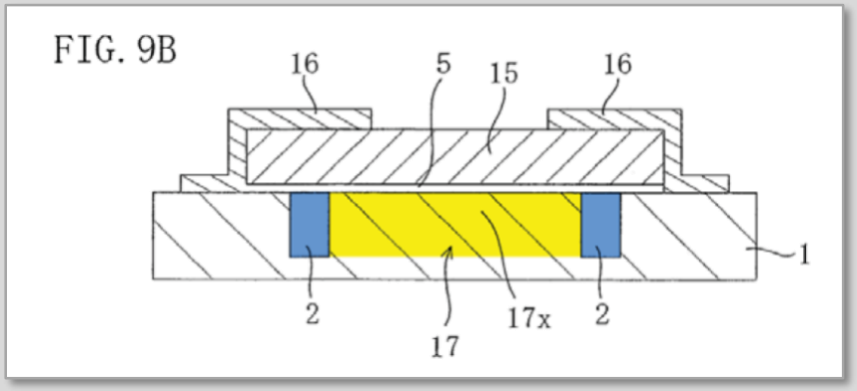
Glew Decl., Ex. 2007, ¶ 69, Annotated Fig.1 of '501 patent (cited POR at 9)

The semiconductor device includes an nMISFET formation region Rn which includes the active region **1***a* and in which an nMISFET is to be formed and a pMISFET formation region Rp which includes the active region **1***b* and in which a pMIS-FET is to be formed.

'501 patent, at 3:24-28 (cited POR at 8)

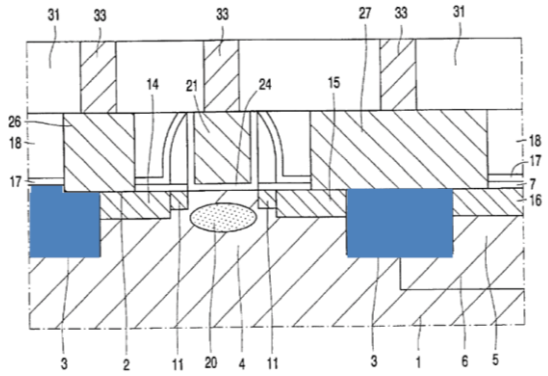


Glew Decl., Ex. 2007, ¶ 68, Annotated Fig.9A of '501 patent (cited POR at 8)



Glew Decl., Ex. 2007, ¶ 69, Annotated Fig.9B of '501 patent (cited POR at 8)

Extrinsic Evidence – Active Region



Woerlee, Ex.-1006, Annotated, Fig. 13

FIG. 13

Woerlee, Ex. 1006, Annotated Figure 13 (cited POR at 57)

As the Petitions acknowledge, Woerlee teaches isolation (STI) regions 3 that form an active region 4 for ***each transistor***, so that each transistor has a dedicated active region and is electrically isolated by the isolation regions 3 from the other transistors formed in the substrate. Petition at 28 ("isolation regions 3 formed in the semiconductor substrate 1 define the active region 4 of the substrate body 1 where ***the*** [singular] transistor is formed."), 30 ("the active region 4 is the region 'in the semiconductor body' where '***a*** [singular] transistor ... is to be manufactured.'"); Ex.-2007, ¶128. The Petitions cite to Woerlee Fig. 13 and 4:66-

POR at 56

The MOS transistors that comprise an integrated circuit must be electrically *isolated* from each other during fabrication. Isolation is required to prevent unwanted conduction paths between the devices, to avoid creation of inversion layers outside the channel regions of transistors, and to reduce leakage currents. To achieve a sufficient level of electrical isolation between neighboring transistors on a chip surface, the devices are typically created in dedicated regions called *active areas*, where each active area is surrounded by a relatively thick oxide barrier called the *field oxide*.

One possible technique to create isolated active areas on silicon surface is first to grow a thick field oxide over the entire surface of the chip, and then to selectively etch the oxide in certain regions, to define the active areas. This fabrication technique, called *etched field-oxide isolation*, is already illustrated in Fig. 2.4(b) and Fig. 2.4(c). Here, the field oxide is selectively etched away to expose the silicon surface on which the MOS

Kang, Ex. 1011, at 28 (cited POR at 31)

"All of the extrinsic evidence is consistent with [Patent Owner's proposed] BRI of 'active region'" (POR at 30)

from the specification into the claims). Contrary to Patent Owner's assertion, the evidence of record does not establish that "a transistor's 'active region' refers to a region that is dedicated to that transistor." Prelim. Resp. 3–4, 29–30. For example, Plummer[10] describes that "regions between these [isolation] layers, where transistors will be built, are called the 'active' regions of the substrate" (Ex. 1008, 53), and Rabaey[11] describes "active regions" as "the regions where transistors will be constructed" (Ex. 1010, 42). Nothing about these descriptions connotes a requirement for a one-to-one correspondence of active regions-to-transistors, as Patent Owner contends.

Institution Decision, Paper No. 10, at 8-9

Extrinsic Evidence – Active Region

DECLARATION OF ALEXANDER D. GLEW

each other"). "Device" and "transistor" are sometimes used interchangeably in these references, as a transistor (e.g., NMOS or PMOS) is a type of device. *E.g.*, Ex. 1008 (Plummer) at 51 ("A ***PMOS transistor*** is shown on the left, an ***NMOS device*** on the right."). 52 ("Modern CMOS chips integrate millions of active

Glew Decl., Ex. 2007, ¶ 84 (cited POR 31)

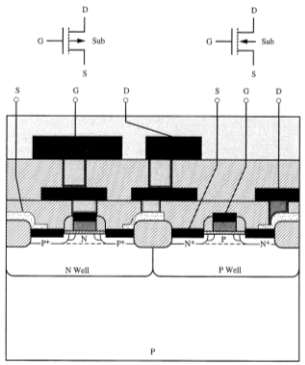


Figure 2–2 Coss section of the final CMOS integrated circit. A PMOS transistor is shown on the left, an NMOS device on the right.

Plummer, Ex. 1008, at 51, Fig. 2-2
(cited Glew Decl., Ex. 2007, ¶¶ 83-84, cited POR 31)

ment complex logic or analog functions. In designing such circuits, it is usually assumed that the individual devices do not interact with each other except through their circuit interconnections. In other words, we need to make certain that the individual devices on the chip are electrically isolated from each other. This is accomplished most often by growing a fairly thick layer of SiO_2 in between each of the active devices. SiO_2 is essentially a perfect insulator and provides the needed isolation. This process of locally oxidizing the silicon substrate is known as the LOCOS process (LOCal Oxidation of Silicon). The regions between these thick SiO_2 layers, where transistors will be built, are called the "active" regions of the substrate.

Ex. 1008 at 53 (cited Ex. 2007, ¶¶ 83-84, cited POR 31)

2.2.4 Simplified CMOS Process Flow

The gross outline of a potential CMOS process flow is given in Figure 2-6. The process starts with the definition of the *active regions*—these are the regions where transistors will be constructed. All other areas of the die will be covered with a thick layer of silicon dioxide (SiO_2)

* * * *

A more detailed breakdown of the flow into individual process steps and their impact on the semiconductor material is shown graphically in Figure 2-7. While most of the operations

Rabaey, Ex. 1010 at 42-43 (cited Glew Decl., Ex. 2007, ¶¶ 84,152, cited POR 31,76)

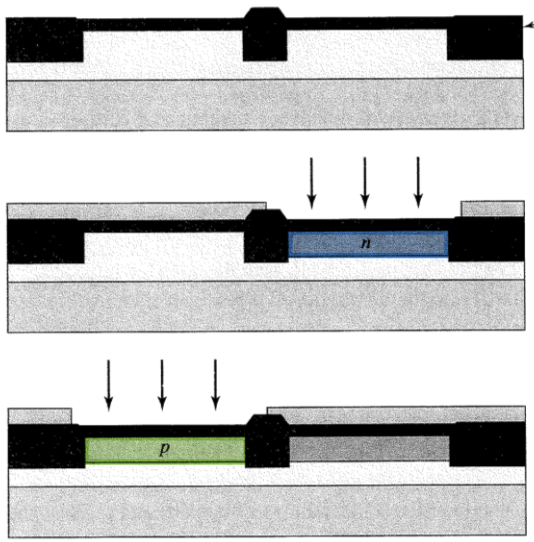


Figure 2-7 Process flow for the fabrication of an NMOS and a PMOS transistor in a dual-well CMOS process. Be aware that the drawings are stylized for understanding and that the aspects ratios are not proportioned to reality.

Rabaey, Ex. 1010 at 44 (cited Glew Decl., Ex. 2007, ¶¶ 84,152, cited POR 31, 76)

• *Diffusion regions* (n^+ and p^+), which define the areas where transistors can be formed. These regions are often called the *active areas*. Diffusions of an inverse type are needed to implement contacts to the wells or to the substrate. These are called *select regions*.

Rabaey, Ex. 1010 at 48 (cited Glew Decl., Ex. 2007, ¶ 82, cited POR 31)

The Claims Require That the MISFET Includes An Active Region

'active region' refers to a region that is dedicated to that transistor." Prelim. Resp. 3–4, 29–30. For example, Plummer[10] describes that "regions between these [isolation] layers, where transistors will be built, are called the 'active' regions of the substrate" (Ex. 1008, 53), and Rabaey[11] describes "active regions" as "the regions where transistors will be constructed" (Ex. 1010, 42). Nothing about these descriptions connotes a requirement for a one-to-one correspondence of active regions-to-transistors, as Patent Owner contends.

Based on the record now before us, we are not persuaded that the claimed "active region" is limited to a region associated with a single transistor (i.e., "a region of a semiconductor substrate dedicated to the MISFET and defined by isolation regions that isolate the MISFET from other transistors formed in the substrate"), as Patent Owner contends. As discussed *infra*, Section II.E, Igarashi includes disclosure of "active element regions," which we find to be within the scope of the plain and ordinary meaning of "active region." Thus, we need not further construe "active region" for purposes of this Decision. The parties, however, may address further construction of the term during trial.

B. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such

[10] JAMES D. PLUMMER ET AL., SILICON VLSI TECHNOLOGY: FUNDAMENTALS, PRACTICE AND MODELING (Charles Sonini ed., Prentice Hall, Inc., 2000) (Ex. 1008).
[11] JAN M. RABAEY ET AL., DIGITAL INTEGRATED CIRCUITS: A DESIGN PERSPECTIVE (Charles G. Sonini ed., Pearson Educ., Inc., 2d ed. 2003) (Ex. 1010).

Institution Decision, Paper No. 10, at 9

1. A semiconductor device, comprising a MISFET, wherein
the MISFET includes:
an active region made of a semiconductor substrate;

'501 patent, at Claim 1

The semiconductor device of this example is a sense amplifier for a DRAM. As shown in FIG. 2, the sense amplifier includes a semiconductor layer **1** which may be a single-crystal semiconductor substrate, an active region **2** formed in an upper surface portion of the semiconductor layer **1**, and isolation regions **3** for isolating the active region **2** from other active regions for other devices such as DRAM memory cells constituting a semiconductor memory device.

Agata, Ex 1025, 5:9-18 (cited Patent Owner's Sur-Reply, Paper No. 28, at 1)

1. A semiconductor device, comprising a MISFET, wherein

the MISFET includes:

an active region made of a semiconductor substrate;

a gate insulating film formed on the active region;

a gate electrode formed on the gate insulating film;

source/drain regions formed in regions of the active region located on both sides of the gate electrode; and

a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein:

the silicon nitride film is not formed on an upper surface of the gate electrode, and

the gate electrode protrudes upward from a surface level of parts of the silicon nitride film located at both side surfaces of the gate electrode.

'501 patent at Claim 1

'501 Patent Claim 1	Igarashi	Woerlee
[1p] 1. A semiconductor device, comprising a MISFET, wherein the MISFET includes:	[0002], [0117], Fig. 12	

Petition, Paper No. 2, at 23

'501 Patent Claim 1	Igarashi	Woerlee
nitride film located at both side surfaces of the gate electrode.		

a) Claim 1 – Preamble (element [1p])

The preamble of claim 1 recites "[a] semiconductor device, comprising a MISFET, wherein the MISFET includes." ('501 patent, claim 1 (Ex-1001).) Igarashi discloses the preamble. (Shanfield Decl. ¶61 (Ex-1002).)

For example, Igarashi discloses: "The present invention relates to a **semiconductor device**, and a method for manufacturing the semiconductor device, specifically to the gate structure of an **MOS transistor** and the contact structure that contains gate wirings and LIC (local interconnect)." (Igarashi at [0002] (Ex-1004).)[4] A metal–oxide–semiconductor (MOS) transistor is a type of MISFET where the insulator is an oxide. (*E.g.*, Shimizu at 59 ("A MISFET having a gate insulating film made of a silicon oxide film is usually called a MOSFET (Metal Oxide Semiconductor Field Effect Transistor).") (Ex-1009).) Thus, by disclosing a MOS transistor, Igarashi discloses a MISFET. (Shanfield Decl. ¶62 (Ex-1002).)

Therefore, Igarashi discloses the preamble. (Shanfield Decl. ¶63 (Ex-1002).)

b) Claim 1 – Active Region (element [1a])

[4] All highlighting (bold and italicized) is added unless otherwise noted.

Petition, Paper No. 2, at 24

The Petition Fails To Identify a 'MISFET Includes: An Active Region' As Claimed

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'501 patent, at Claim 1

'501 Patent Claim 1
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[1a] an active region made of a semiconductor substrate;

Petition, Paper No. 2, at 23

b) Claim 1 – Active Region (element [1a])

Claim 1 recites "an active region made of a semiconductor substrate." ('501 patent, claim 1 (Ex-1001).) Igarashi in view of Woerlee discloses this limitation. (Shanfield Decl. ¶64 (Ex-1002).)

For example, Igarashi discloses a "semiconductor substrate 1," as illustrated in Fig. 12:

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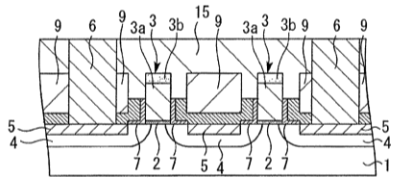

(Igarashi at Fig. 12 (Ex-1004); *see also, e.g., id.* at [0044]-[0045], [0112] (discussing the "semiconductor substrate 1").) (Shanfield Decl. ¶65 (Ex-1002).)

A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made

Petition, Paper No. 2, at 24, 25

regions) in Woerlee are formed in regions of the active region 4 located on both sides of the gate electrode 21 (as recited in claim 1, element 1d below). The modified device would also have an active element region (active region) divided by the STI regions (isolation region) formed in the semiconductor substrate 1 (as recited in claim 10 below), just as the active region 4 is divided by an isolation region 3 formed in the semiconductor substrate 1 in Woerlee. (Shanfield Decl. ¶73 (Ex-1002).)

Therefore, Igarashi in view of Woerlee discloses "an active region made of a semiconductor substrate." (Shanfield Decl. ¶74 (Ex-1002).)

c) Claim 1 – Active Region (element [1a]) – Reasons to Modify

It would have been obvious to modify Igarashi in view of Woerlee's teachings of an active region "made of" a semiconductor substrate (recited in claim 1, element 1a) and an active region divided by an isolation region formed in the semiconductor substrate (recited in claim 10 below). In particular, it would have been obvious to apply Woerlee's teachings to Igarashi by forming Igarashi's active region in the substrate and defining it with STI regions that divide the active region. (Shanfield Decl. ¶75 (Ex-1002).)

First, a POSITA would have looked to the teachings of Woerlee because it is in the same field of endeavor as Igarashi. Igarashi discloses a MISFET device with a "silicon semiconductor substrate 1" where "[e]lement isolation is performed" to

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Petition, Paper No. 2, at 32

The Petition Fails To Identify a 'MISFET Includes: An Active Region' As Claimed

a. The Petitions Fail to Meet Petitioner's Burden of Demonstrating How and Why Any MISFET in the Igarashi/Woerlee Combination Includes an "Active Region" Meeting the Agreed-Upon BRI

The Petitions must specify the grounds with particularity. 35 U.S.C. §312(a)(3) (requiring IPR petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim"); 37 C.F.R. §42.104(b)(4) ("The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon."); *Harmonic*, 815 F.3d at 1363; *Kranos*, IPR2016-01649, Paper No. 25 at 29, 36, 39-42.

The Petitions fail to meet Petitioner's burden of establishing that ***any*** MISFET in the Igarashi/Woerlee combination "includes: an active region" meeting the agreed-upon BRI. Ex.-2007, ¶132.

As shown in Petitioner's modified Fig. 12 (reproduced below), the Petitions insert "STI" regions on the left and right sides, and further label the figure with a box "Active Region" and two arrows pointing to the channel regions under the gates of the two MISFETs. Ex.-2007, ¶132. The Petitions allege the "active element region is made of the substrate 1 of Igarashi and divided by STI regions." -1841-Petition at 27, 37. Ex.-2007, ¶132.

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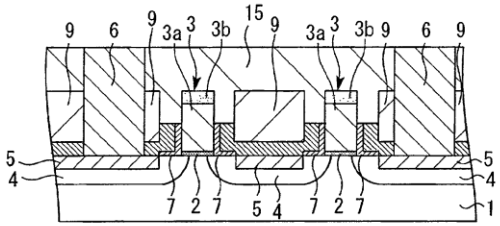
POR, Paper No. 20, at 59

Shanfield's Declaration Does Not Solve The Problems In The Petition As He Repeats The Petition Verbatim

Claim 1 recites "an active region made of a semiconductor substrate." ('501 patent, claim 1 (Ex-1001).) Igarashi in view of Woerlee discloses this limitation. (Shanfield Decl. ¶64 (Ex-1002).)

For example, Igarashi discloses a "semiconductor substrate 1," as illustrated in Fig. 12:

Fig. 12



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Petition at 25

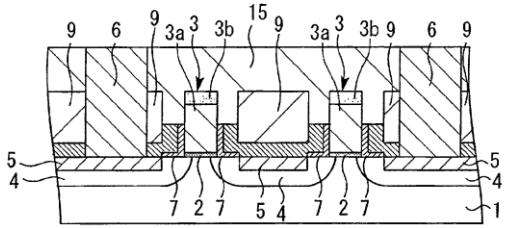
63. Therefore, Igarashi discloses the preamble.

b) Claim 1 – Active Region (element [1a])

64. Claim 1 recites "an active region made of a semiconductor substrate." ('501 patent, claim 1 (Ex-1001).) Igarashi in view of Woerlee discloses this limitation.

65. For example, Igarashi discloses a "semiconductor substrate 1," as illustrated in Fig. 12:

Fig. 12



(Igarashi at Fig. 12 (Ex-1004); *see also, e.g., id.* at [0044]-[0045], [0112] (discussing the "semiconductor substrate 1").)

66. A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the

Shanfield Opening Declaration, Ex. 1002, at 33

"Shanfield refused to explain whether … the alleged 'active region' was the entire region bounded by isolation regions so that there was only one 'active region' present, or … more than one 'active region' was present." (POR 63)

Q. How many active regions are shown in the cross-section of figure 12 of Igarashi?

MR. SMITH: Objection.

A. Again, I'm taking "active region" as used in the claim language and understanding it with respect to the claim language, and that's the consideration I made. I didn't do any counting exercises as to the number of active regions or -- because there was no reference to -- or the need to count regions in understanding the claim language.

Shanfield Opening Depo., Ex. 2010 at 424:2-11
(cited in POR at 70)

device that Dr. Glew would expect to have an "active region." Ex. 2007, ¶¶91-92; *see also*, Ex. 1024, 110:23-111:4. Ex. 1027, ¶33.

C. Patent Owner's Attacks on Dr. Shanfield's Testimony are Purely a Distraction

PO desperately attacks Dr. Shanfield in its Response for allegedly not answering the question of whether Igarashi shows one active region or two active regions. Response, 13-14. However, Dr. Shanfield repeatedly tried to explain how this was not a distinction relevant to the challenged claims or his analysis. When PO persisted in trying to get Dr. Shanfield to say it was one active region or two, Dr. Shanfield testified truthfully that this was not a question that made sense

Reply, Paper No. 22, at 22

Shanfield's Deposition Testimony Reveals He Did Not Even Consider How The Claimed 'MISFET Includes' Requirement Was Met Before The Petition Was Filed

technically.[6] Dr. Shanfield was not unable or unwilling to answer the question. To the contrary, he repeatedly and patiently answered PO's questions over two full days of deposition and even stayed in deposition for over an hour beyond PO's allotted seven hours on the second day. Ex. 1027, ¶34. The trouble for PO is not that Dr. Shanfield did not provide an answer—it is that PO just did not like the answer he gave.

For example, in the very passage PO cites to support Dr. Shanfield's alleged non-answers (PO cites Ex. 2010, 437:23-438:10, omitting lines 11-19, bracketed

[6] In contrast, Dr. Glew demonstrated a lack of familiarity with the opinions set forth in his own declaration and could not testify one way or another whether testimony he offered in his own declaration was correct. *Compare:* "Q. Would you agree that once LOCOS and STI were discovered, they allowed manufacturers to pack transistors more densely than a semiconductor device? A. I haven't opined on the enabling nature of LOCOS or STI in my declaration. That would require a separate analysis." (Ex. 1024, 105:23-106:4), *with:* "Once isolation techniques such LOCOS and then STI were discovered, they were frequently implemented, as they allowed manufacturers to pack transistors more densely in semiconductor devices…" (Ex. 2007, ¶112).

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below), Dr. Shanfield explains that PO's counsel's questions did not make technical sense and that he was doing his best to answer them:

- "I have explained that that isn't a meaningful question, in that that isn't a consideration I needed to make in order to interpret the claim language."
- "[I am happy to tell you what – the interpretation of 'active region' I made with respect to the claim language. Since you're using the claim language, I'm compelled to answer in terms of the claim language in that context, and I think trying a -- trying to get me to -- to create a new description of what's connected and what isn't isn't the consideration I was making in interpreting the claim]." (Ex. 2010, 438:11-19.) Ex. 1027, ¶35.

PO also fails to note that this same line of confusing questioning and Dr. Shanfield's efforts to clarify and answer went on for numerous pages of deposition transcript preceding the cited passage. Ex. 2010, 410:1-437:22. Through his testimony, and consistent with his declaration, Dr. Shanfield explained how Igarashi invalidates the claims under either view.

A non-exhaustive sampling of his answer includes:

Shanfield's Deposition Testimony First Asserted that there are Two Active Regions

Q. Does the transistor on the left and the transistor on the right in your annotated figure 12 share the same active region?
A. No.
Q. Is there more than one active region shown in figure 12?
A. (Witness reviews document.) The active region is "the region bounded by isolation regions where the transistor is formed."
I'm pointing to two different active regions where two different transistors are formed.

Shanfield Opening Depo, Ex. 2009, at 91:12-22
(cited POR at 64)

Q. So you testified yesterday that there were two active regions in the substrate.
A. No, I never testified that.

Shanfield Opening Depo., Ex. 2010, at 401:9-11
(cited POR at 66)

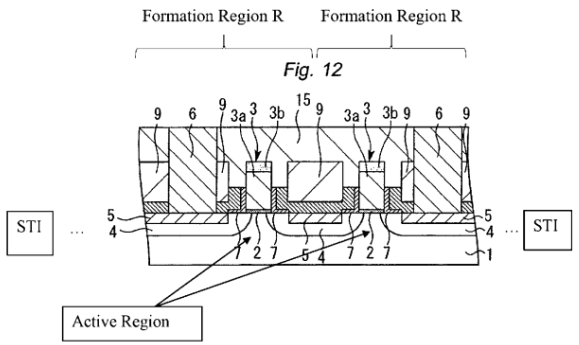

Fig. 12

The problem with Shanfield's assertion that the regions where the transistors are formed include two distinct "active regions" is clear from the highlighted figure above. It is irreconcilable with his own testimony that the active region is "defined by" the STI regions, as he modified Fig. 12 to show only one alleged STI region on each side of the transistors (thus allowing for no more than one active region that could be "defined by" the two alleged STI regions). Ex.-2007, ¶139-40; Ex.-2009, 93:11-20. ***Neither*** of the highlighted regions where a transistor is formed is bounded by the isolation regions because there is no isolation region between the transistors. Ex.-2007, ¶140. Indeed, there can be no isolation region between the transistors because they share a source/drain region. Ex.-1004, ¶0088, Fig. 12; Ex.-2007, ¶140.

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POR at 65

Shanfield Gave Inconsistent Testimony

A. So starting with page 35 -- and, again, I'm explaining what an active region is appropriate to the context of the '501 patent. So if you look at figure 12 on page 35 of my declaration 1002,

* * * *

Q. Does the transistor on the left and the transistor on the right in your annotated figure 12 share the same active region?

A. No.

Q. Is there more than one active region shown in figure 12?

A. (Witness reviews document.) The active region is "the region bounded by isolation regions where the transistor is formed."

I'm pointing to two different active regions where two different transistors are formed.

Shanfield Opening Depo., Ex. 2009, at 86:21-24; 91:12-22 (cited POR at 64)

Q. In the bracketed region, is there one or more than one active region?

MR. SMITH: Objection.

A. The active region is the region where transistors are formed between the isolation, and there's one active region here because of the way I've drawn it.

Q. So that bracket reflects that there is one active region; is that correct?

A. Given the definition I'm applying, which is, it's the -- and I -- as I've pointed out, Igarashi doesn't explain what's going on here. I've put "..." with the assumption or with the presumption that there's more transistor formation out here (indicating); and, yes, then, that is one active region.

Shanfield Opening Depo., Ex. 2010, at 406:8-23 (cited POR at 68)

Shanfield Gave Inconsistent Testimony

Q. Does the transistor on the left and the transistor on the right in your annotated figure 12 share the same active region?

A. No.

Shanfield Opening Depo., Ex. 2009, at 91:12-15 (cited POR at 64)

Q. Doctor Shanfield, is there one or more than one active region located between the STIs in figure 12 of Igarashi on page 35 of your declaration?

MR. SMITH: Objection.

A. I think I explained that they're sharing an active region, 'cause they're sharing a region where transistors are being formed.

Q. What do you mean when you say "they are sharing"?

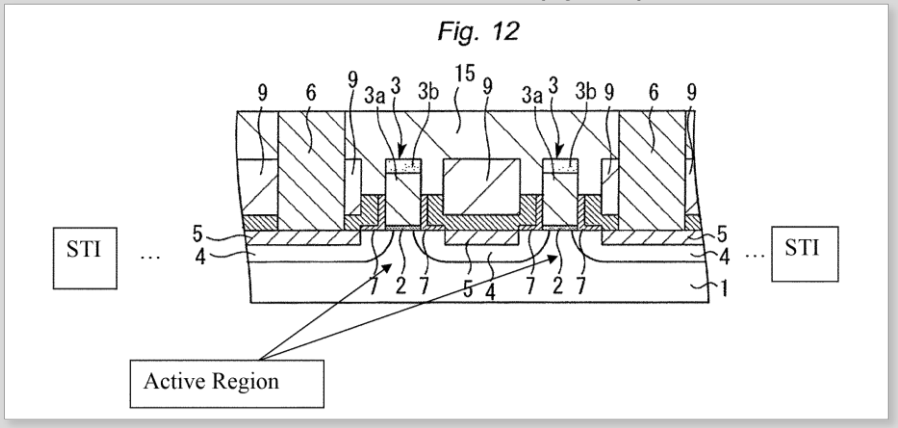
A. This gate on the left and this gate on the right are a pair of devices connected together, and those -- or this -- this construction, which is a device in itself, has got an active region under it.

Shanfield Opening Depo., Ex. 2010 at 409:2-16 (cited POR at 70)

technically.[6] Dr. Shanfield was not unable or unwilling to answer the question. To the contrary, he repeatedly and patiently answered PO's questions over two full days of deposition and even stayed in deposition for over an hour beyond PO's allotted seven hours on the second day. Ex. 1027, ¶34. The trouble for PO is not that Dr. Shanfield did not provide an answer—it is that PO just did not like the answer he gave.

For example, in the very passage PO cites to support Dr. Shanfield's alleged non-answers (PO cites Ex. 2010, 437:23-438:10, omitting lines 11-19, bracketed

Reply, Paper No. 22, at 23



Petition, Paper No. 2, at 27

Shanfield's Deposition Testimony Reveals He Did Not Even Consider How The Claimed 'MISFET Includes' Requirement Was Met Before The Petition Was Filed

the agreed-upon BRI in the modified-Igarashi Fig. 12, as there is no "MISFET [that] includes" the region bounded by the isolation region. *Id.*

After walking away from his assertion that there are two active regions in modified-Igarashi Fig. 12, Shanfield spent the next hour of the deposition wrestling with the simple question of whether the two (or more) transistors in the Fifth Embodiment of Fig. 12 include a single "active region" or more than one. Ex.-2007, ¶147. At times, he suggested that there might be just one active region bounded by the isolation region he alleged must be present in Igarashi's Fifth Embodiment. Ex.-2010, 406:8-23 ("there's one active region here" in Fig. 12); Ex.-2007, ¶147; *see also* Ex.-2010, 409:2-16 ("I think I explained that they're sharing an active region.").

But Shanfield refused to maintain and defend that position, because it too is indefensible. Ex.-2010, 421:10-24, 424:2-11, 427:20-428:9; Ex.-2007, ¶147. Unwilling to defend the (indefensible) position that the active area for any MISFET includes an area of the substrate where a ***different*** transistor is formed, Shanfield ultimately refused to take a position on whether there was a single active region in his modified-Igarashi Fig. 12. Ex.-2010, 421:10-24 ("I didn't go through any counting exercise."), 424:2-11 ("I didn't do any counting exercises as to the number of active regions"), 427:20-428:9; Ex.-2007, ¶147. He testified that he "simply knew what 'active region' was in the context of this claim and the

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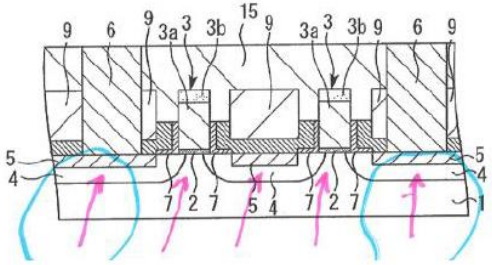
specification, as would any person of ordinary skill." Ex.-2010, 430:5-9; Ex.-2007, ¶147. Yet he repeatedly refused to delineate the boundaries of the alleged active region(s) in Fig. 12 of Igarashi, or to describe how many active regions were shown in Fig. 12. Ex.-2007, ¶147; *e.g.*, Ex.-2010, 437:23-438:10.

For instance, when asked the simple question of whether two portions of the device shown below in Fig. 12 of Igarashi (annotated by Shanfield using pink arrows circled in blue) together comprised one or more than one active region, Shanfield stated that he "can't answer." Ex.-2010, 437:23-438:10 ("Q. [T]he two arrows that you circled in blue, are they in one or more than one active region? … A. I have explained that that is isn't [sic] a meaningful question in that that isn't a consideration I needed to make in order to interpret the claim language. What I needed to understand was what 'active region' meant in the context of the claim. ***So I can't answer***."); Ex.-2007, ¶147.

Fig. 12



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Shanfield's Deposition Testimony Reveals He Did Not Even Consider How The Claimed 'MISFET Includes' Requirement Was Met Before The Petition Was Filed

specification, as would any person of ordinary skill." Ex.-2010, 430:5-9; Ex.-2007, ¶147. Yet he repeatedly refused to delineate the boundaries of the alleged active region(s) in Fig. 12 of Igarashi, or to describe how many active regions were shown in Fig. 12. Ex.-2007, ¶147; *e.g.*, Ex.-2010, 437:23-438:10.

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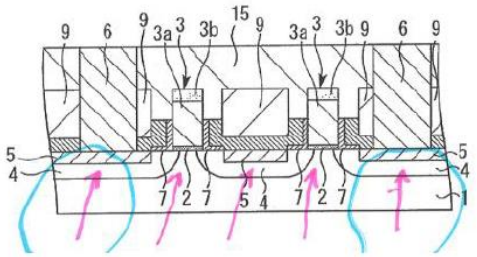
Fig. 12



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POR at 71

1. A semiconductor device, comprising a MISFET, wherein
the MISFET includes:
an active region made of a semiconductor substrate;
a gate insulating film formed on the active region;
a gate electrode formed on the gate insulating film;
source/drain regions formed in regions of the active region located on both sides of the gate electrode; and
a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein:
the silicon nitride film is not formed on an upper surface of the gate electrode, and
the gate electrode protrudes upward from a surface level of parts of the silicon nitride film located at both side surfaces of the gate electrode.

'501 patent at Claim 1

Mapping the agreed-upon BRI of "active region" and claim 1's requirement that "the MISFET includes: an active region" onto the prior art structure the Petitions allege meets the claimed "active region" is the furthest thing from irrelevant. *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (affirming final written decision upholding patentability where Petitioner offered merely "conclusory" discussion of the prior art and failed to explain with particularity how the limitations were disclosed); *Kranos Corp. v. Riddell, Inc.*, IPR2016-01649, Paper No. 25 at 29, 36, 39-42 (PTAB Feb. 7, 2018) (Petitioner failed to meet its burden where "it is unclear from Petitioner's argument where each element of [the challenged claims] is found in" the prior art and the Board "decline[d] to speculate as to Petitioner's intentions").

POR at 20

Shanfield's Deposition Testimony Reveals He Did Not Even Consider How The Claimed 'MISFET Includes' Requirement Was Met Before The Petition Was Filed

- "But what I can provide is what was asked of me and what I put in my declaration, and that is, is -- active region, as used in the claim, claim 1, is the gate insulating film formed on the active region? Yes.
- "It's an active region between two insulating -- STI regions or isolating regions; and it's, indeed, a gate insulating film on the transistor that you've labeled 'A' and the other transistor on the right. It has a gate insulating film formed on the active region.
- "Is source-drain regions formed in regions of the active region? Yes, there are several regions of the active region where source-drain regions are formed. And with that analysis, I could conclude that Igarashi met these two limitations I'm describing."

Ex. 2010, 429:12-430:5. Dr. Shanfield's opinion that Igarashi discloses the claimed "active region" is presented in his declaration and confirmed in his testimony. PO's assertion that Dr. Shanfield could not answer is simply wrong. Ex. 1027, ¶36.

D. Patent Owner Again Incorrectly Argues that the Petition Relies on Woerlee Only for the Location of the Active Region

PO argued in its POPR that "even if a [POSITA] would have been led to combine the features of Igarashi and Woerlee in the manner alleged in the Petition, the resulting semiconductor device does not include a MISFET having an active

Reply, Paper No. 22, at 25

REPLY DECLARATION OF STANLEY R. SHANFIELD, PH.D.

TSMC 1027

Shanfield Reply Decl., Ex. 1027

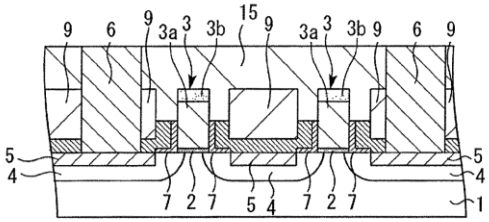
The Petition Fails To Identify a 'MISFET Includes: An Active Region' As Claimed

b) Claim 1 – Active Region (element [1a])

Claim 1 recites "an active region made of a semiconductor substrate." ('501 patent, claim 1 (Ex-1001).) Igarashi in view of Woerlee discloses this limitation. (Shanfield Decl. ¶64 (Ex-1002).)

For example, Igarashi discloses a "semiconductor substrate 1," as illustrated in Fig. 12:

Fig. 12



(Igarashi at Fig. 12 (Ex-1004); *see also, e.g.*, *id.* at [0044]-[0045], [0112] (discussing the "semiconductor substrate 1").) (Shanfield Decl. ¶65 (Ex-1002).)

A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made

Petition at 24, 25

1. A semiconductor device, comprising a MISFET, wherein
the MISFET includes:
an active region made of a semiconductor substrate;

'501 patent at Claim 1

Moreover, the Petition showed that Igarashi's isolation region teachings were applicable to its Figure 12 embodiment. Specifically, the Petition cites Figure 12, which shows the "semiconductor substrate 1." Petition, 25. Then, the Petition explains that a POSITA would have understood that the semiconductor substrate 1 in Fig. 12 has an active region because Igarashi expressly discloses an "active element region" made of the semiconductor substrate 1. Petition 25-26, *citing* Ex. 1004, [0068]; Ex. 1002, ¶66; Ex. 1010, 42-43. Ex. 1027, ¶27.

Accordingly, both the Petition and Dr. Shanfield's testimony have been clear and consistent throughout this proceeding: Igarashi discloses the "active region" of the challenged claims in connection with its Fifth Embodiment. Moreover, as discussed below in Section III.D, the Petition also demonstrated it would have been obvious to form the active region disclosed in Igarashi in semiconductor substrate 1 of Igarshi's Fifth Embodiment in view of the teachings of Woerlee. Ex. 1027, ¶28.

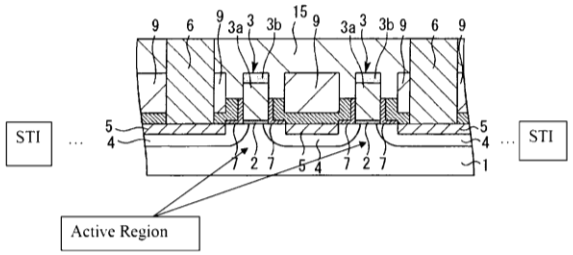
B. Igarashi Discloses a MISFET that Includes an "Active Region"

A person of ordinary skill would have viewed the region between the two STI in Igarashi where the two transistors are formed as an "active region" formed between those two STI. As noted in the Petition: "The use of the 'trench method' confirms the 'active element region' (active region) is made of the semiconductor substrate 1 because according to the trench method the active region is formed in

Reply, Paper No. 22, at 19

The Petition Fails To Identify a 'MISFET Includes: An Active Region' As Claimed

Fig. 12



Pet. at 27, Petitioner's Modified-Igarashi Fig. 12, Ex.-1004, Fig. 12

As the Petitions and Petitioner's expert agree, a MISFET's active region must be both bounded and defined by an isolation region. §VI.A.1; Ex.-2007, ¶133. The Petitions and Petitioner's expert also agree that a MISFET's active region must be the region in which the MISFET is formed. §VI.A.1; Ex.-2007, ¶133. Yet the Petitions failed to explain how or why the Petitions' modified-Igarashi Fig. 12 has a MISFET that "includes" an active region meeting both these requirements. Ex.-2007, ¶133.

Despite agreeing that an "active region" as claimed must be ***defined and bounded*** by isolation regions (§VI.A.1), the Petitions fail to identify the boundaries of the alleged "Active Region" in modified-Igarashi Fig. 12. Ex.-2007, ¶133. The Petitions' mapping, such as it is, of "active region" onto the modified-Igarashi Fig. 12 is vague and insufficient. *Harmonic*, 815 F.3d at 1363; *Kranos*, IPR2016-01649, Paper No. 25 at 29, 36, 39-42.

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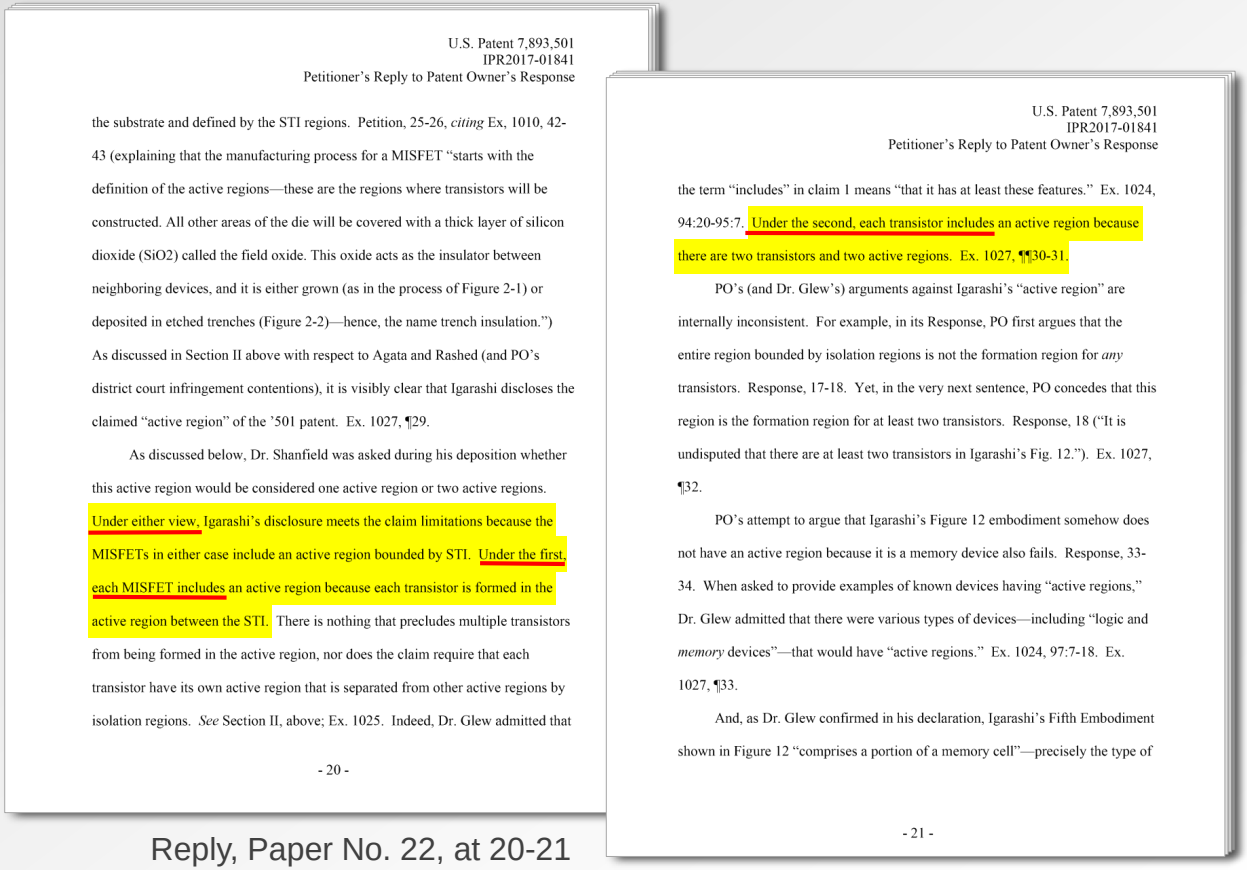
POR at 61

"Petitioner's New Arguments regarding Active Region"

First, even transistors that do not use isolation regions such as STI still have active regions—otherwise, the transistors would simply not function. The absence of an isolation region does not signify the absence of an active region. *Second*, by the

Reply, Paper No. 22, at 14



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the substrate and defined by the STI regions. Petition, 25-26, *citing* Ex, 1010, 42-43 (explaining that the manufacturing process for a MISFET "starts with the definition of the active regions—these are the regions where transistors will be constructed. All other areas of the die will be covered with a thick layer of silicon dioxide (SiO2) called the field oxide. This oxide acts as the insulator between neighboring devices, and it is either grown (as in the process of Figure 2-1) or deposited in etched trenches (Figure 2-2)—hence, the name trench insulation.") As discussed in Section II above with respect to Agata and Rashed (and PO's district court infringement contentions), it is visibly clear that Igarashi discloses the claimed "active region" of the '501 patent. Ex. 1027, ¶29.

As discussed below, Dr. Shanfield was asked during his deposition whether this active region would be considered one active region or two active regions. Under either view, Igarashi's disclosure meets the claim limitations because the MISFETs in either case include an active region bounded by STI. Under the first, each MISFET includes an active region because each transistor is formed in the active region between the STI. There is nothing that precludes multiple transistors from being formed in the active region, nor does the claim require that each transistor have its own active region that is separated from other active regions by isolation regions. *See* Section II, above; Ex. 1025. Indeed, Dr. Glew admitted that

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the term "includes" in claim 1 means "that it has at least these features." Ex. 1024, 94:20-95:7. Under the second, each transistor includes an active region because there are two transistors and two active regions. Ex. 1027, ¶¶30-31.

PO's (and Dr. Glew's) arguments against Igarashi's "active region" are internally inconsistent. For example, in its Response, PO first argues that the entire region bounded by isolation regions is not the formation region for *any* transistors. Response, 17-18. Yet, in the very next sentence, PO concedes that this region is the formation region for at least two transistors. Response, 18 ("It is undisputed that there are at least two transistors in Igarashi's Fig. 12."). Ex. 1027, ¶32.

PO's attempt to argue that Igarashi's Figure 12 embodiment somehow does not have an active region because it is a memory device also fails. Response, 33-34. When asked to provide examples of known devices having "active regions," Dr. Glew admitted that there were various types of devices—including "logic and *memory* devices"—that would have "active regions." Ex. 1024, 97:7-18. Ex. 1027, ¶33.

And, as Dr. Glew confirmed in his declaration, Igarashi's Fifth Embodiment shown in Figure 12 "comprises a portion of a memory cell"—precisely the type of

- 21 -

Reply, Paper No. 22, at 20-21

"Petitioner's New Arguments that Isolation Region Not Required to Form an Active Region"

First, even transistors that do not use isolation regions such as STI still have active regions—otherwise, the transistors would simply not function. The absence of an isolation region does not signify the absence of an active region. *Second*, by the

Reply, Paper No. 22, at 14

leakage current flow. It was known to POSITAs that isolation regions that define and divide the active regions are required in all transistor devices because they prevent stray potentials (voltages) and current leaks between devices. In particular,

Petition at 33

A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made of the semiconductor substrate" both because it explicitly discloses a "active element region" and because it discloses using the "trench method" for "element isolation," meaning the trench method is used to form shallow trench isolation (STI) regions that define the active region where the transistor is formed. (Shanfield Decl. ¶66 (Ex-1002).)

Petition at 25-26

The Petition Asserted That An Active Region Must Be Bounded By Isolation And Be The Region Where the Transistor is Formed

62,66. The dispute between the parties relates to whether, and if so how, the claim requirement that "the MISFET includes: an active region" is met by the prior art relied upon in the grounds.

1. The Petitions and Petitioner's Expert Consistently Characterize the Active Region as an Area of the Semiconductor Substrate Defined by an Isolation Region Where the Transistor Is Formed

While the Petitions did not offer an explicit interpretation, they consistently characterized the active region as an area of the semiconductor substrate defined by an isolation region where the transistor is formed. Ex.-2007, ¶¶63-64; *see*, *e.g.*, Petition at 26 ("isolation (STI) regions that define the active region where the transistor is formed."); *id*. ("the active region is … defined by the STI regions."); *id*. at 28 ("isolation regions 3 … define the active region 4 of the substrate body 1 where the transistor is formed."); *id*. at 30 ("the active region is an area of the semiconductor body 1 defined and separated by field insulation region 3.").

In his declarations and at his deposition, Shanfield consistently described the "active region" in the same manner. Ex.-2007, ¶65; Ex.-1002, ¶ 66; *see, e.g.*, Ex.-1002, ¶¶ 37,39 ("The STI are formed using the trench method and define the active region."),40,68,70 (Woerlee's "active region 4 is an area of semiconductor body 1 defined and separated by field insulation region 3"), 72,76 ("'[e]lement isolation is performed' to define the 'active element region.'"), 77-80, 89; Ex.-2009, 45:22-46:23 ("The '501-patent describes the active region made of the substrate as a

region bounded by isolation regions where the transistor is formed."), 48:3-6, 51:12-21, 52:16-20, 69:7-9, 89:17-22, 90:14-18, 91:16-20; Ex.-2010, 406:8-14; *see also, e.g.*, Ex.-1002, ¶¶ 37,39-40,67,69,70-71,73,77-81, 90,154.

2. The '501-Patent Specification Describes an Active Region as an Area of the Semiconductor Substrate Defined by an Isolation Region Where the Transistor is Formed

In the '501-patent, an "active region" of a MISFET refers to a region of the semiconductor substrate defined by an isolation region in which the MISFET is formed. Ex.-2007, ¶67. The specification repeatedly refers to a semiconductor substrate being divided by an isolation region into a plurality of active regions. Ex.-2007, ¶¶67-69; *e.g.*, Ex.-1001, 3:21-23 ("an Si (100) substrate is divided into a plurality of active regions 1a and 1b by an isolation region 2"), 6:22-26 ("forming an isolation region 2 for dividing the substrate into active regions 1a, 1b and so on"), 9:38-39, 10:53-54, 12:25-28 ("forming an isolation region 2 for dividing the substrate into active regions 1a, 1b and so on"), Figs. 1-9.

The specification describes each transistor as having a formation region (e.g., Rn, Rp) that includes the active region in which the transistor is formed. Ex.-1001, 3:24-28. All embodiments illustrated in figures of the '501-patent illustrate a semiconductor device comprising MISFET formation regions Rn, Rp that include active regions (*e.g.*, active regions 1a, 1b) that are defined by isolation region 2, have transistors formed therein, and where the transistor's source/drain regions 3, 4

POR, Paper No. 20, at 27-28

"Petitioner's New Arguments regarding Active Region"

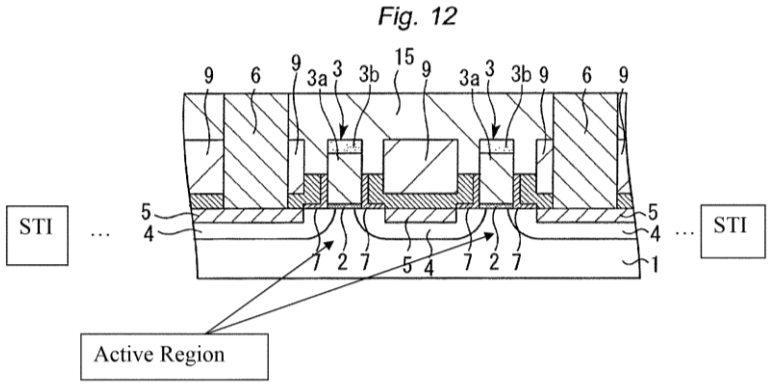
the substrate and defined by the STI regions. Petition, 25-26, *citing* Ex, 1010, 42-43 (explaining that the manufacturing process for a MISFET "starts with the definition of the active regions—these are the regions where transistors will be constructed. All other areas of the die will be covered with a thick layer of silicon dioxide (SiO2) called the field oxide. This oxide acts as the insulator between neighboring devices, and it is either grown (as in the process of Figure 2-1) or deposited in etched trenches (Figure 2-2)—hence, the name trench insulation.") As discussed in Section II above with respect to Agata and Rashed (and PO's district court infringement contentions), it is visibly clear that Igarashi discloses the claimed "active region" of the '501 patent. Ex. 1027, ¶29.

As discussed below, Dr. Shanfield was asked during his deposition whether this active region would be considered one active region or two active regions. Under either view, Igarashi's disclosure meets the claim limitations because the MISFETs in either case include an active region bounded by STI. Under the first, each MISFET includes an active region because each transistor is formed in the active region between the STI. There is nothing that precludes multiple transistors from being formed in the active region, nor does the claim require that each transistor have its own active region that is separated from other active regions by isolation regions. *See* Section II, above; Ex. 1025. Indeed, Dr. Glew admitted that

Reply, Paper No. 22, at 20

the term "includes" in claim 1 means "that it has at least these features." Ex. 1024, 94:20-95:7. Under the second, each transistor includes an active region because there are two transistors and two active regions. Ex. 1027, ¶¶30-31.

Reply, Paper No. 22, at 21



Petition at 27

The Argument That In Igarashi/Woerlee Fig. 12 Two Transistors Share The Same Active Region Is Improper New Argument

4. Reply, p. 19, l. 16 to p. 21, l. 3, p.10, l. 17 to p. 13, l. 5; Ex. 1027, ¶¶ 16-18, 29-31: Argument that the ***entire*** area "between the two STI in Igarashi [modified Fig. 12]" meets the claimed "active region" is ***new***, as the Petition and its supporting expert declaration ***nowhere*** explain whether this area is alleged to include one or two (one per transistor) active regions as confirmed by the contradictory and ultimately non-comital testimony of Petitioner's expert at deposition. *E.g.*, Ex. 2009 at 91:12-92:14 (two active regions); Ex. 2010 at 400:16-401:11 (denying prior testimony; identifying one active region); 406:5-408:9 (retracting testimony for annotated Figure 12 (Ex. 2002 described at Ex. 2010 at 404:12-20; 192:21-22) and requesting to strike testimony); 410:1-24 ("can't answer"); 416:11-17 (not relevant to understanding the claim); 424:2-11 (not needed to understand claim).

5. Reply, p. 20, l. 11, p. 21, l. 3; Ex. 1027, ¶ 31: Petitioner's cursory and conclusory "argument," that the area "between the two STI in Igarashi [modified Fig. 12]" includes multiple "active regions" (one per transistor) contradicts the new argument in #4 and also is new, as the Petition and its supporting expert declaration ***nowhere*** explained whether this area is alleged to include one or two (one per transistor) active regions as confirmed by the contradictory and ultimately non-comital testimony of Petitioner's expert at deposition cited in #4.

Dated: July 24, 2018

Respectfully submitted,

By /Gerald B. Hrycyszyn /
Gerald B. Hrycyszyn, Reg. No. 50,474

2

Paper 27, Patent Owner's Identification of Improper Arguments, at 2

4. The Reply at 9-13 and 19-22 responds to the arguments in the POR on pages 14-21, 28-29, 33-36, and 58-74 that Igarashi's Fig. 12 embodiment does not have a single large active region or two smaller active regions that satisfy the claims. In response, the Reply confirms that a POSITA would have viewed the region between the two STI as the claimed active region and identifies where this is shown in the Pet. Reply at 19-20 (*citing* Pet. at 25-26). The Reply also confirms in response to the POR that Igarashi discloses the claimed active region under either view and that PO's construction is unduly narrow. Reply at 9-13, 20-22. The Reply specifically states at 9:1-4 and 21:4-22:2 that these arguments respond to POR at 17-18, 33-34, 28-29, and 74. The Reply also responds to PO's mischaracterization of Dr. Shanfield's testimony. Reply at 22-25; *see also* Ex. 2009 at 93:16-20 (clarifying region between STI is an active region, not two active regions); Ex. 2010 at 401:9-402:4 (confirming clarification); *id.* at 408:10-17, 411:7-412:3 (confirming region between STI is the active region); *id.* at 429:12-430:5, 437:11-19 (attempting to clarify and answer confusing questions).

5. As noted for **4.**, the Reply at 20-21 responds the POR's arguments that Igarashi does not have a single large active region or two smaller active regions that satisfy the claims and confirms Igarashi discloses the active region under either view.

Dated: July 27, 2018

Respectfully Submitted,

/Michael Smith/

Michael H. Smith, Reg. No. 71,190

2

Paper 29, Petitioner's Response, at 1-2

The Argument That Igarashi/Woerlee Fig. 12 Has A Separate Active Region For Each Transistor Is Improper New Argument

4. Reply, p. 19, l. 16 to p. 21, l. 3, p.10, l. 17 to p. 13, l. 5; Ex. 1027, ¶¶ 16-18, 29-31: Argument that the ***entire*** area "between the two STI in Igarashi [modified Fig. 12]" meets the claimed "active region" is ***new***, as the Petition and its supporting expert declaration ***nowhere*** explain whether this area is alleged to include one or two (one per transistor) active regions as confirmed by the contradictory and ultimately non-comital testimony of Petitioner's expert at deposition. *E.g.*, Ex. 2009 at 91:12-92:14 (two active regions); Ex. 2010 at 400:16-401:11 (denying prior testimony; identifying one active region); 406:5-408:9 (retracting testimony for annotated Figure 12 (Ex. 2002 described at Ex. 2010 at 404:12-20; 192:21-22) and requesting to strike testimony); 410:1-24 ("can't answer"); 416:11-17 (not relevant to understanding the claim); 424:2-11 (not needed to understand claim).

5. Reply, p. 20, l. 11, p. 21, l. 3; Ex. 1027, ¶ 31: Petitioner's cursory and conclusory "argument," that the area "between the two STI in Igarashi [modified Fig. 12]" includes multiple "active regions" (one per transistor) contradicts the new argument in #4 and also is new, as the Petition and its supporting expert declaration ***nowhere*** explained whether this area is alleged to include one or two (one per transistor) active regions as confirmed by the contradictory and ultimately non-comital testimony of Petitioner's expert at deposition cited in #4.

Dated: July 24, 2018

Respectfully submitted,

By /Gerald B. Hrycyszyn /
Gerald B. Hrycyszyn, Reg. No. 50,474

2

Paper No. 27, Patent Owner's Identification of Improper Arguments, at 2

single large active region or two smaller active regions that satisfy the claims. In response, the Reply confirms that a POSITA would have viewed the region between the two STI as the claimed active region and identifies where this is shown in the Pet. Reply at 19-20 (*citing* Pet. at 25-26). The Reply also confirms in response to the POR that Igarashi discloses the claimed active region under either view and that PO's construction is unduly narrow. Reply at 9-13, 20-22. The Reply specifically states at 9:1-4 and 21:4-22:2 that these arguments respond to POR at 17-18, 33-34, 28-29, and 74. The Reply also responds to PO's mischaracterization of Dr. Shanfield's testimony. Reply at 22-25; *see also* Ex. 2009 at 93:16-20 (clarifying region between STI is an active region, not two active regions); Ex. 2010 at 401:9-402:4 (confirming clarification); *id.* at 408:10-17, 411:7-412:3 (confirming region between STI is the active region); *id.* at 429:12-430:5, 437:11-19 (attempting to clarify and answer confusing questions).

5. As noted for **4.**, the Reply at 20-21 responds the POR's arguments that Igarashi does not have a single large active region or two smaller active regions that satisfy the claims and confirms Igarashi discloses the active region under either view.

Dated: July 27, 2018

Respectfully Submitted,

/Michael Smith/
Michael H. Smith, Reg. No. 71,190

2

Paper No. 29, Petitioner's Response, at 2

The New Argument That Igarashi/Woerlee Fig. 12 Has A Separate Active Region For Each Transistor Fails

the term "includes" in claim 1 means "that it has at least these features." Ex. 1024, 94:20-95:7. Under the second, each transistor includes an active region because there are two transistors and two active regions. Ex. 1027, ¶¶30-31.

PO's (and Dr. Glew's) arguments against Igarashi's "active region" are internally inconsistent. For example, in its Response, PO first argues that the entire region bounded by isolation regions is not the formation region for *any* transistors. Response, 17-18. Yet, in the very next sentence, PO concedes that this region is the formation region for at least two transistors. Response, 18 ("It is undisputed that there are at least two transistors in Igarashi's Fig. 12."). Ex. 1027, ¶32.

PO's attempt to argue that Igarashi's Figure 12 embodiment somehow does not have an active region because it is a memory device also fails. Response, 33-34. When asked to provide examples of known devices having "active regions," Dr. Glew admitted that there were various types of devices—including "logic and *memory* devices"—that would have "active regions." Ex. 1024, 97:7-18. Ex. 1027, ¶33.

And, as Dr. Glew confirmed in his declaration, Igarashi's Fifth Embodiment shown in Figure 12 "comprises a portion of a memory cell"—precisely the type of

Reply, Paper No. 22, at 20-21

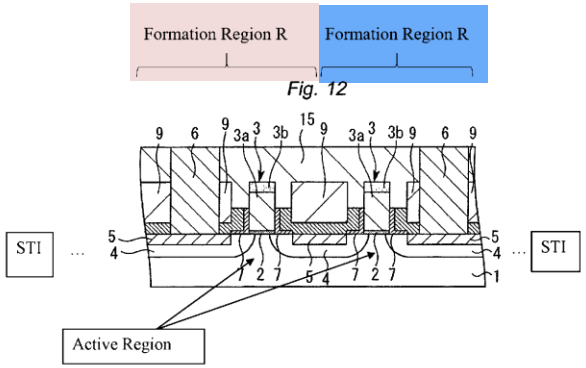
thick layer of silicon dioxide (SiO2) called the field oxide. This oxide acts as the insulator between neighboring devices, and it is either grown (as in the process of Figure 2-1) or deposited in etched trenches (Figure 2-2)—hence, the name trench insulation.") As discussed in Section II above with respect to Agata and Rashed (and Patent Owner's district court infringement contentions), it is visibly clear that Igarashi discloses the claimed "active region" of the '501 patent.

30. As discussed below, I was asked during deposition whether this active region would be considered one active region or two active regions.

31. In either view, Igarashi's disclosure meets the claim limitations because the MISFETs in either case include an active region bounded by STI. Under the first view, each MISFET includes an active region because each transistor is formed in the active region between the STI. There is nothing that precludes multiple transistors, each with their own channel, from being formed in the active region, nor does the claim require that each transistor have its own active region that is separated from other active regions by isolation regions. *See* Section II, above; Ex. 1025. I note that Dr. Glew admitted that the term "includes" in claim 1 means "that it has at least these features." Ex. 1024, 94:20-95:7. Under the second view, each transistor includes an active region because there are two transistors and two active regions.

Shanfield Reply Decl., Ex. 1027, ¶¶ 30-31

The New Argument That Igarashi/Woerlee Fig. 12 Has A Separate Active Region For Each Transistor Fails



The problem with Shanfield's assertion that the regions where the transistors are formed include two distinct "active regions" is clear from the highlighted figure above. It is irreconcilable with his own testimony that the active region is "defined by" the STI regions, as he modified Fig. 12 to show only one alleged STI region on each side of the transistors (thus allowing for no more than one active region that could be "defined by" the two alleged STI regions). Ex.-2007, ¶139-40; Ex.-2009, 93:11-20. ***Neither*** of the highlighted regions where a transistor is formed is bounded by the isolation regions because there is no isolation region between the transistors. Ex.-2007, ¶140. Indeed, there can be no isolation region between the transistors because they share a source/drain region. Ex.-1004, ¶0088, Fig. 12; Ex.-2007, ¶140.

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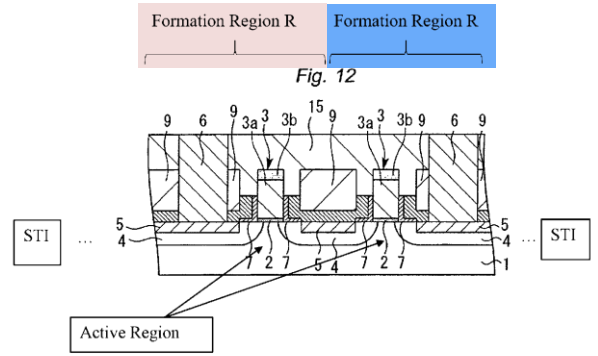
POR at 65



140. Petitioner modified Fig. 12 to show only one alleged STI region on each side of the transistors. This allows for no more than one active region that possibly could be "defined by" the two alleged STI regions. Neither of the highlighted formation regions where a transistor is formed (*see* annotated version of Petitioner's modified Igarashi Figure 12 above) is bounded by the isolation region, or includes an active region bounded by the isolation region, because there is no isolation region between the transistors of the alleged combination. Petitioner and Dr. Shanfield never allege that there would have been an isolation region between the transistors of the alleged combination, and never explain how the two alleged STI regions included in Petitioner's modified Fig. 12 can define, between themselves, two separate active regions. In fact, there can be no isolation region between the transistors because they share a common source/drain region, which

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Glew Decl., Ex. 2007, ¶140 (cited POR at 65)

The New Argument That Igarashi/Woerlee Fig. 12 Has A Separate Active Region For Each Transistor Fails

First, even transistors that do not use isolation regions such as STI still have active regions—otherwise, the transistors would simply not function. The absence of an isolation region does not signify the absence of an active region. *Second*, by the time of the alleged invention in 2003, virtually all transistors included isolation regions. A POSITA at the time of the alleged invention would not have understood Igarashi to be implemented in a manner that omitted isolation regions or structures (such as STI) because: (i) the transistors commonly used by then were too small for spacing alone to be a functional alternative to isolation regions or structures (such as STI); and (ii) Igarashi expressly discloses the use of isolation regions and such isolation regions would have been obvious in view of Woerlee. Ex. 1027, ¶19; Petition, 25-27; Ex. 1024, 111:18-25 (admitting that using spacing rather than isolation "would not be a typical solution" for memory cells in the 2003 timeframe).

Accordingly, PO's interpretation of an "active region" is inappropriately narrow, forecloses substantial portions of the technical field, and is purely designed to escape the overwhelming prior art. Ex. 1027, ¶20.

III. IGARASHI AND WOERLEE DISCLOSE THE CLAIMED "ACTIVE REGION"

PO again incorrectly argues that the Fifth Embodiment described in Igarashi, itself, does not teach STI regions forming an active region. Response, 37. The

Reply, Paper No. 22, at 14

1. The Petitions and Petitioner's Expert Consistently Characterize the Active Region as an Area of the Semiconductor Substrate Defined by an Isolation Region Where the Transistor Is Formed

While the Petitions did not offer an explicit interpretation, they consistently characterized the active region as an area of the semiconductor substrate defined by an isolation region where the transistor is formed. Ex.-2007, ¶¶63-64; *see, e.g.*, Petition at 26 ("isolation (STI) regions that define the active region where the transistor is formed."); *id*. ("the active region is … defined by the STI regions."); *id*. at 28 ("isolation regions 3 … define the active region 4 of the substrate body 1 where the transistor is formed."); *id*. at 30 ("the active region is an area of the semiconductor body 1 defined and separated by field insulation region 3.").

In his declarations and at his deposition, Shanfield consistently described the "active region" in the same manner. Ex.-2007, ¶65; Ex.-1002, ¶ 66; *see, e.g.*, Ex.-1002, ¶¶ 37,39 ("The STI are formed using the trench method and define the active region."),40,68,70 (Woerlee's "active region 4 is an area of semiconductor body 1 defined and separated by field insulation region 3"), 72,76 ("'[e]lement isolation is performed' to define the 'active element region.'"), 77-80, 89; Ex.-2009, 45:22-46:23 ("The '501-patent describes the active region made of the substrate as a region bounded by isolation regions where the transistor is formed."), 48:3-6, 51:12-21, 52:16-20, 69:7-9, 89:17-22, 90:14-18, 91:16-20; Ex.-2010, 406:8-14; *see also, e.g.*, Ex.-1002, ¶¶ 37,39-40,67,69,70-71,73,77-81, 90,154.

POR, Paper No. 20, at 27-28

The New Argument That Igarashi/Woerlee Fig. 12 Has A Separate Active Region For Each Transistor Fails

region. *Id.*, ¶¶6-7. Agata and Rashed say no such thing. To the contrary, they explicitly state that it is the larger "device," to which the active region is dedicated, that "includes" the active region. *Id.*, ¶¶3-5. Agata and Rashed ***corroborate*** Dr. Glew's testimony that a structure (whether a multi-transistor device in Agata and Rashed or a MISFET in the '501 patent) "includes" an active region only if the active region is dedicated to the structure that "includes" it. *Id.* ¶¶ 7-8. No evidence supports an assertion that any transistor in modified Igarashi Fig. 12 "includes" an active region encompassing other transistors. *Id.*, ¶¶6-7.

Third, Petitioner's assertion that "all functional MOSFET transistors have an active region" is wrong—an active region must be bounded by isolation and a transistor can be formed without isolation. *Id.* ¶ 9; POR at VI.A, VII.C.1.b. While a transistor must be formed in a region, the '501 patent is clear that that is a "formation region," and only if isolation is provided does the formation region include a smaller active region. Ex. 2024 ¶9; Ex. 1001 at 3:20-28, Fig. 1.

Fourth, Petitioner's assertions that interpreting "active region" to encompass multiple transistors is not "prohibited" or "precluded" (Reply at 6, 10, 12) not only ignore the claimed requirement that the "***MISFET includes*** an active region," they also violate the black letter law cited in the POR at 26.

Dated: July 27, 2018

Respectfully submitted,
Godo Kaisha IP Bridge 1
By /Richard Giunta /
Richard F. Giunta, Reg. No. 36,149

3

Patent Owner's Sur-Reply, Paper No. 28, at 3

dedicated to the MISFET. Agata, Rashed, and the '501 patent refer to a structure (respectively, "sense amplifier", "device," and "MISFET") that "includes" an active region where the active region is ***dedicated*** to the structure that "includes" it.

9. Dr. Shanfield's assertion that "all functional MOSFET transistors have an active region" is unsupported and wrong—an area not defined by isolation is ***not*** an active region. *See* Ex. 2007 at VII.A, VIII.C.1.b. All transistors must have a region in the substrate where they are formed, but as the '501 patent makes clear this is a "formation region." Ex. 1001 at 3:20-28, Fig. 1.

10. Dr. Shanfield mischaracterizes my deposition testimony which addressed the term "comprise" and not "includes." Ex. 1027, ¶31; Ex. 1024 at 94:13-95:7. The open ended "comprising" transition in claim 1 does not eliminate the requirement that the "MISFET includes: an active region," which the grounds do not meet. *See* Ex. 2007 at VIII.C.

11. Dr. Shanfield's suggestion that the '501 patent does not show 1-to-1 correspondence between the active regions and MISFETs because the figures are cross sections (Ex. 1027, ¶¶ 14-15) is wrong with respect to Fig. 9A, and refuted by the '501 specification. '501 patent at 3:24-28 (each MISFET "formation region … ***includes*** the active region"). Fig. 9A is a "plane view of an MISFET" (3:8-10, 14:42-45) and illustrates isolation region 2 bounding the active region in which the transistor is formed, i.e., defining the boundary of the active region on all sides.

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Glew Sur-Reply Decl., Ex. 2024 at 3

A MISFET's Active Region Must Be Defined By Isolation and Be Where the MISFET Is Formed

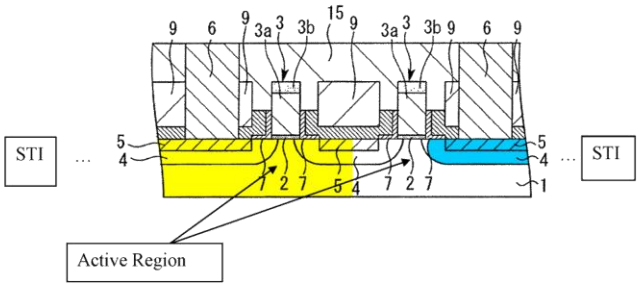
1. A semiconductor device, comprising a MISFET, wherein
the MISFET includes:
an active region made of a semiconductor substrate;

'501 patent, at Claim 1

In the Petitions' modified-Igarashi Fig. 12 the entire region of the substrate bounded by the alleged isolation region is not the formation region for ***any*** MISFET. Ex.-2007, ¶145. Taking the left MISFET as an example, the transistor is formed in the region in yellow below. *Id.* There are other regions of the substrate bounded by the alleged isolation region, e.g., the area in blue, that are unquestionably ***not*** part of the region (yellow below) where the left MISFET is formed. *Id.*

Formation Region R

Fig. 12



Neither of the MISFETs shown in the Petitions' modified-Igarashi Fig. 12 is formed in and includes the entire region of the substrate bounded by the isolation region, so the region bounded by the isolation region is not an "active region" of either MISFET. Ex.-2007, ¶146. Thus, there is not one "active region" that meets

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POR at 69

Claim 1 Requires That the MISFET Is The Larger Whole That Includes The Active Region Not Vice Versa

1. A semiconductor device, comprising a MISFET, wherein
the MISFET includes:
an active region made of a semiconductor substrate;
a gate insulating film formed on the active region;
a gate electrode formed on the gate insulating film;
source/drain regions formed in regions of the active region located on both sides of the gate electrode; and
a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein:
the silicon nitride film is not formed on an upper surface of the gate electrode, and
the gate electrode protrudes upward from a surface level of parts of the silicon nitride film located at both side surfaces of the gate electrode.

'501 patent at Claim 1

agreed-upon BRI. Ex.-2007, ¶¶136-41. Given that Petitioner's expert Shanfield was unwilling to take a position refuting Dr. Glew's opinion, the testimony of Patent Owner's expert on this critical issue stands unrebutted.

c. No Transistor Includes the Region Bounded by the Alleged Isolation Region in the Petitions' Modified-Igarashi Fig. 12, So There Is Not One "Active Region"

All challenged claims require that "the MISFET ***includes***: an active region." Ex.-2007, ¶142. Thus, the plain language and structure of the claims require that it is the MISFET that is the larger whole that "includes" the entirety of the active region and not the other way around. *Id.* That is, the claims recite the MISFET as including the active region, they do ***not*** recite the active region as a larger whole that includes the MISFET. *Id.*; *see, e.g.*, Ex.-2011 at 1143 ("include" means "to place, list, or rate as a part or component of a whole or of a larger group, class, or aggregate" or "to take in, enfold, or comprise as a discrete or subordinate part or item of a larger aggregate, group, or principle"); Ex.-2012 at 780 ("to have as contents or part of the contents; be made up of or contain"); Ex.-2013 at 684 ("to contain or be made up of something, or to have it as parts of its contents").

Thus, a MISFET's active region does ***not*** include areas of the substrate where components of a ***different*** transistor are formed. Such an interpretation would not be consistent with the specification of the '501-patent, which describes the "formation region" Rn, Rp for a MISFET as "includ[ing] the active region" 1a,

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POR at 67

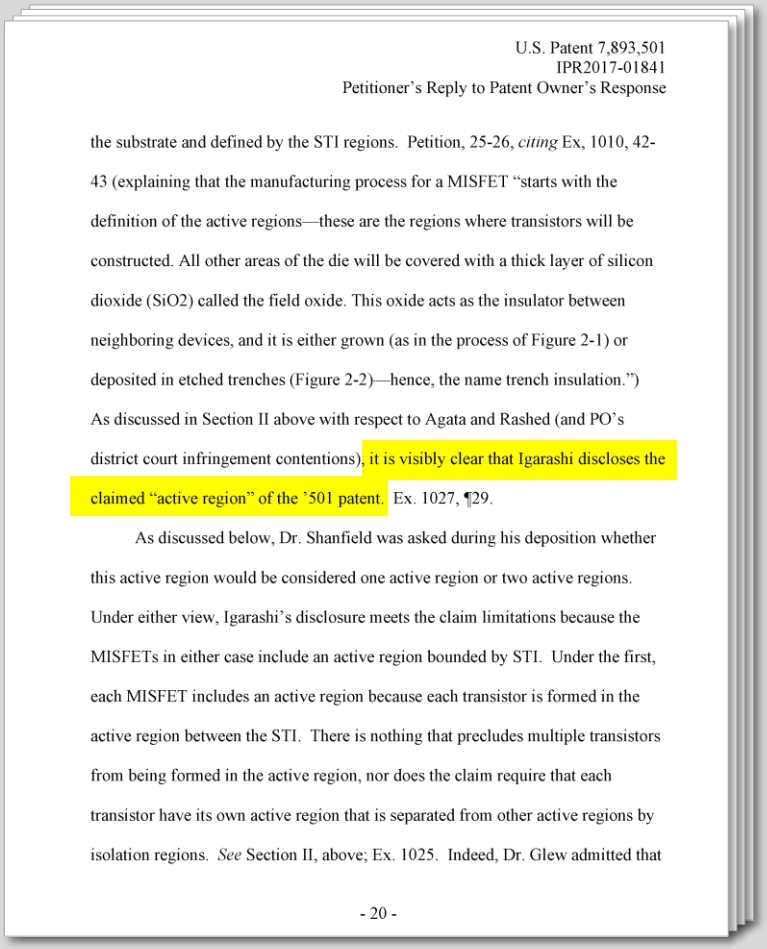
The Reply Seeks to Rewrite Claim 1

1. A semiconductor device, comprising a MISFET, wherein

the MISFET includes:

an active region made of a semiconductor substrate;

'501 patent, at Claim 1



U.S. Patent 7,893,501
IPR2017-01841
Petitioner's Reply to Patent Owner's Response

the substrate and defined by the STI regions. Petition, 25-26, *citing* Ex, 1010, 42-43 (explaining that the manufacturing process for a MISFET "starts with the definition of the active regions—these are the regions where transistors will be constructed. All other areas of the die will be covered with a thick layer of silicon dioxide (SiO2) called the field oxide. This oxide acts as the insulator between neighboring devices, and it is either grown (as in the process of Figure 2-1) or deposited in etched trenches (Figure 2-2)—hence, the name trench insulation.") As discussed in Section II above with respect to Agata and Rashed (and PO's district court infringement contentions), it is visibly clear that Igarashi discloses the claimed "active region" of the '501 patent. Ex. 1027, ¶29.

As discussed below, Dr. Shanfield was asked during his deposition whether this active region would be considered one active region or two active regions. Under either view, Igarashi's disclosure meets the claim limitations because the MISFETs in either case include an active region bounded by STI. Under the first, each MISFET includes an active region because each transistor is formed in the active region between the STI. There is nothing that precludes multiple transistors from being formed in the active region, nor does the claim require that each transistor have its own active region that is separated from other active regions by isolation regions. *See* Section II, above; Ex. 1025. Indeed, Dr. Glew admitted that

- 20 -

Reply, Paper No. 22, at 20

The Claims Require That the MISFET Includes An Active Region – Not the Other Way Around

1. A semiconductor device, comprising a MISFET, wherein
the MISFET includes:
an active region made of a semiconductor substrate;

Ex. 1001, '501 patent, at Claim 1

Dr. Glew confirms that he stands by his testimony that "includes" is an open-ended term like comprises. Ex. 1029, 93:15-22; Ex. 1024 at 94:13-95:7. The term "includes" does not prevent the MISFET from including other features or prevent other MISFETS from being formed in the same active region. Moreover, PO's supposed "one-to-one correspondence" (Sur-reply, 1-3) is directly contradicted by PO's infringement contentions. Reply, 6-7, *citing* Ex. 1021, 32. Ex. 1027, ¶11. PO's contradictory positions cannot be reconciled, nor does PO even try.

Petitioner's Sur-Sur-Reply, Paper No. 33, at 1-2

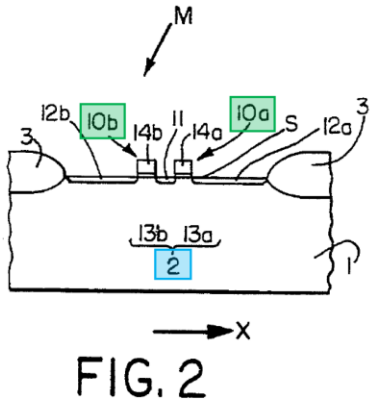


FIG. 2

Id., Figure 2; Ex. 1027, ¶17.

Dr. Shanfield also explains that isolation regions are designed to isolate *one active region from another active region*, not each transistor from every other transistor. That is, the isolation regions do *not* necessitate a one-to-one correspondence of active regions-to-transistors as PO asserts. For example, when observing a plan view laying out a configuration of semiconductor devices, it becomes evident that an active region can include more than one transistor. U.S. Patent No. 8,618,607 to Rashed et al. ("Rashed") illustrates such a plan view, describing a device that "includes a continuous active region defined in a semiconducting substrate, first and second transistors formed in and above the continuous active region." Ex. 1026, Abstract. Rashed even acknowledges that

Reply, Paper No. 22, at 12

The Reply Seeks to Rewrite Claim 1

Dr. Glew confirms that he stands by his testimony that "includes" is an open-ended term like comprises. Ex. 1029, 93:15-22; Ex. 1024 at 94:13-95:7. The term "includes" does not prevent the MISFET from including other features or prevent other MISFETS from being formed in the same active region. Moreover, PO's supposed "one-to-one correspondence" (Sur-reply, 1-3) is directly contradicted by PO's infringement contentions. Reply, 6-7, *citing* Ex. 1021, 32. Ex. 1027, ¶11. PO's contradictory positions cannot be reconciled, nor does PO even try.

Second, Dr. Glew's inability to answer basic questions on cross shows his attempts to reconcile his testimony with Agata and Rashed are not credible. For example, when Dr. Glew's drawing of a MISFET that "includes" an active region (Ex. 1028, Fig. 1) was reproduced with the isolation regions spaced further apart (Ex. 1028, Fig. 2), Dr. Glew was unable to say whether the same MISFET still "included" an active region. Ex. 1029, 16:4-23. Similarly, when Petitioner attempted to obtain Dr. Glew's opinion of whether the MISFET would still "include" an active region if a second transistor were *added*, Dr. Glew refused to draw a second transistor and testified he had no opinion. Ex. 1029, 19:3-11.

Dr. Glew was also unable to say whether the device in Igarashi's Fig. 12 "includes" an active region, demonstrating that his attempts to distinguish Agata and Rashed are not credible. Ex. 1029, 62:5-63:9. Dr. Glew's answers on cross-examination also reveal the superficial nature of his analysis. Dr. Glew previously testified that "the active region is the region where the transistor is formed." Ex. 1024, 43:10-14. When asked on cross whether "each transistor in Figure 12

Petitioner's Sur-Sur-Reply, Paper No. 33, at 1-2

1. A semiconductor device, comprising a MISFET, wherein

the MISFET includes:

an active region made of a semiconductor substrate;

a gate insulating film formed on the active region;

a gate electrode formed on the gate insulating film;

source/drain regions formed in regions of the active region located on both sides of the gate electrode; and

a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein:

the silicon nitride film is not formed on an upper surface of the gate electrode, and

the gate electrode protrudes upward from a surface level of parts of the silicon nitride film located at both side surfaces of the gate electrode.

'501 patent, at Claim 1

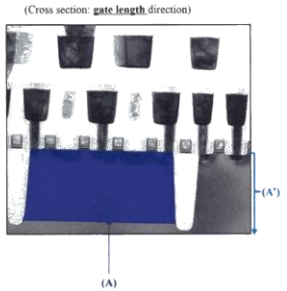
Petitioner's Remaining Arguments On "MISFET Includes: an Active Region

adopts language similar to that used in the Petition and during Dr. Shanfield's deposition, but then proposes interpreting this language in the same manner as its previously rejected construction. *Id.*, 27-28. This unilateral statement by PO does not signal Petitioner's agreement with the incorrect interpretation that an active region contains only one transistor. There is nothing in the '501 patent or prior art that prohibits multiple transistors from being formed in an active region, or that requires each transistor to be isolated from any other transistor. Ex. 1027, ¶10.

Third, PO cannot reconcile its incorrect interpretation with *its own* infringement contentions in the co-pending litigation, which identify an alleged "active region" having *multiple transistors* and which were made of record in this proceeding (over PO's opposition) months before PO filed its response. As highlighted by PO's infringement contentions, the alleged **"active region"** shown in blue contains at least *four transistors*:

> A semiconductor device, comprising a MISFET, wherein the MISFET includes:
> **(A) an active region** made of **(A') a semiconductor substrate**;

U.S. Patent 7,893,501
IPR2017-01841
Petitioner's Reply to Patent Owner's Response



Ex. 1021, 32. Ex. 1027, ¶11.

PO's inconsistent positions on an "active region" infect its arguments throughout its Response. For example, PO argues that the MISFET must "include" the entirety of the active region. Response, 16. This is simply another indirect way of PO rearguing its rejected construction requiring a one-to-one correspondence of active regions-to-transistors and is directly contradicted by PO's own district court infringement allegations, which allege the opposite. ***Patent Owner cannot have it both ways.*** Ex. 1027, ¶12.

Fourth, as recognized by the Board, the Petition and the semiconductor textbooks cited in the Petition consistently recognize the "active region" as the region where transistors are formed. Ex. 1027, ¶13. For example:

Reply, Paper No. 22, at 6, 7

Petitioner's Remaining Arguments On "MISFET Includes: an Active Region

adopts language similar to that used in the Petition and during Dr. Shanfield's deposition, but then proposes interpreting this language in the same manner as its previously rejected construction. *Id.*, 27-28. This unilateral statement by PO does not signal Petitioner's agreement with the incorrect interpretation that an active region contains only one transistor. There is nothing in the '501 patent or prior art that prohibits multiple transistors from being formed in an active region, or that requires each transistor to be isolated from any other transistor. Ex. 1027, ¶10.

Third, PO cannot reconcile its incorrect interpretation with *its own* infringement contentions in the co-pending litigation, which identify an alleged "active region" having *multiple transistors* and which were made of record in this proceeding (over PO's opposition) months before PO filed its response. As highlighted by PO's infringement contentions, the alleged **"active region"** shown in blue contains at least *four transistors*:

A semiconductor device, comprising a MISFET, wherein the MISFET includes:
(A) an active region made of **(A') a semiconductor substrate**;

Reply, Paper No. 22, at 6

In several recent decisions the Federal Circuit reversed this Board because the Board applied an overly broad interpretation under BRI. The Federal Circuit has emphasized that under BRI, the Board may not adopt an interpretation simply because it is not inconsistent with any specific prohibitions in the specification, and must instead adopt an "interpretation that corresponds with what and how the inventor describes his invention in the specification." *E.g.*, *In re Smith Int'l, Inc.*, 871 F.3d 1375, 1382-83 (Fed. Cir. 2017) ("The correct inquiry in giving a claim term its [BRI] in light of the specification ***is not whether the specification proscribes or precludes***" a proposed interpretation and "is not simply [whether] an interpretation . . . ***is not inconsistent with the specification***."); *see also In re Power Integrations, Inc.*, 884 F.3d 1370, 1377 (Fed. Cir. 2018); *Sophos Ltd. v. Iancu*, No. 2017-1567, 2018 WL 1517198, at *4 (Fed. Cir. Mar. 28, 2018). Accordingly, the BRI is an interpretation that is affirmatively consistent with the specification. *In re Smith*, 871 F.3d at 1382-83 (finding an interpretation unreasonable because it gave a claim term a breadth that exceeds "the otherwise different description in the specification").

A. "an active region made of a semiconductor substrate" (claim 1)

As demonstrated below, there is no dispute that under BRI, "an active region made of a semiconductor substrate" is "an area of the semiconductor substrate defined by an isolation region where the transistor is formed." Ex.-2007, ¶¶61-

POR at 26

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made of the semiconductor substrate" both because it explicitly discloses a "active element region" and because it discloses using the "trench method" for "element isolation," meaning the trench method is used to form shallow trench isolation (STI) regions that define the active region where the transistor is formed. (Shanfield Decl. ¶66 (Ex-1002).)

Petition at 25-26

66. A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made of the semiconductor substrate" both because it explicitly discloses a "active element region" and because it discloses using the "trench method" for "element isolation," meaning the trench method is used to form shallow trench isolation (STI) regions that define the active region where the transistor is formed. The use

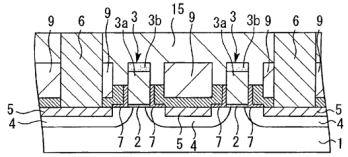
Shanfield Opening Declaration (Ex. 1002)
Portion of ¶ 66

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

Claim 1 recites "an active region made of a semiconductor substrate." ('501 patent, claim 1 (Ex-1001).) Igarashi in view of Woerlee discloses this limitation. (Shanfield Decl. ¶64 (Ex-1002).)

For example, Igarashi discloses a "semiconductor substrate 1," as illustrated in Fig. 12:

Fig. 12



(Igarashi at Fig. 12 (Ex-1004); *see also, e.g.*, *id.* at [0044]-[0045], [0112] (discussing the "semiconductor substrate 1").) (Shanfield Decl. ¶65 (Ex-1002).)

A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made

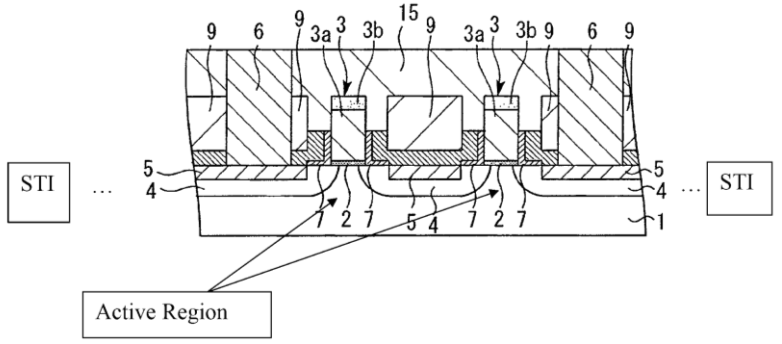
of the semiconductor substrate" both because it explicitly discloses a "active element region" and because it discloses using the "trench method" for "element isolation," meaning the trench method is used to form shallow trench isolation (STI) regions that define the active region where the transistor is formed. (Shanfield Decl. ¶66 (Ex-1002).)

The use of the "trench method" confirms the "active element region" (active region) is made of the semiconductor substrate 1 because according to the trench method the active region is formed in the substrate and defined by the STI regions.[5] (*E.g.*, Rabaey at 42-43 (explaining that the manufacturing process for a MISFET "starts with the definition of the *active regions*—these are the regions where transistors will be constructed. All other areas of the die will be covered with a thick layer of silicon dioxide (SiO_2) called the *field oxide*. This oxide acts as the insulator between neighboring devices, and it is either grown (as in the process of Figure 2-1) or deposited in etched trenches (Figure 2-2)—hence, the name *trench insulation*.") (Ex-1010).) This is illustrated below in annotated Figure 12 of Igarashi:

[5] Because claim 10, which depends from claim 1, recites "the active region is divided by an isolation region formed in the semiconductor substrate," claim 1 must be interpreted to allow for isolation regions because claim 10 must be narrower than claim 1.

Petition at 25-26

Fig. 12



Petition, at 27

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

[0043] First Embodiment

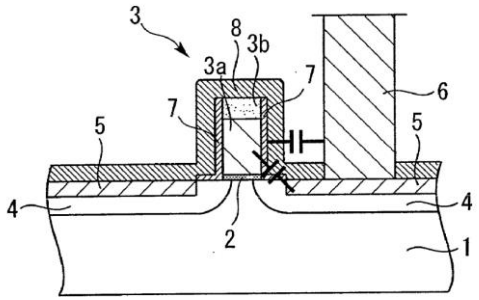
[0044] **FIG. 1** is a schematic sectional view showing a semiconductor device according to First Embodiment of the present invention. The configuration of the semiconductor device of First Embodiment will be described below referring to **FIG. 1**. The semiconductor device of First Embodiment is an example of MOS transistors of an SAC structure to which the present invention is applied, and comprises a gate electrode **3** formed on a silicon semiconductor substrate **1** through a gate oxide film **2**; a pair of impurity diffusion layers **4** of source/drain diffused layers formed on the surface region of the silicon semiconductor substrate **1** in the both sides of the gate electrode **3**; a silicide film **5** formed on the surface of the impurity diffusion layers **4**; and a contact electrode **6** electrically connected to the silicide film **5**.

Igarashi, Ex. 1004, ¶¶ 43-44 (cited POR 33)

[0068] Next, the method for manufacturing the semiconductor device of First Embodiment will be described. In the following description of the manufacturing method, the major process for forming the silicon nitride film **7** will be described referring to **FIGS. 5A** to **5**E, and other processes will be described without referring to drawings. First, an insulating film for isolating elements is formed on a silicon semiconductor substrate **1**. Element isolation is performed using methods such as the LOCOS method or the trench method. Thereafter, ion implantation is performed to the active element region for forming the well and controlling the threshold value.

Igarashi, Ex. 1004, ¶ 68 (cited POR 34)

Fig. 1

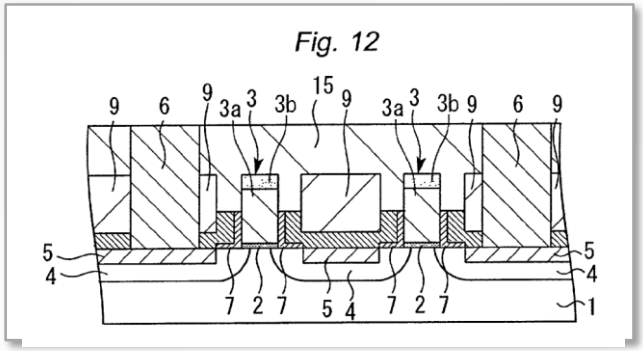


[0116] Fifth Embodiment

[0117] **FIG. 12** is a schematic sectional view showing a semiconductor device according to Fifth Embodiment of the present invention. Fifth Embodiment will be described below referring to the drawings. The semiconductor device of Fifth Embodiment has the configuration in which the silicon nitride films **8** on the upper surfaces of the gate electrodes **3** are removed as in Fourth Embodiment, and the silicon nitride films **7** and the silicon nitride films **8** on the upper portions of the sidewalls of the gate electrodes **3** are also removed, and a low-k film **15** is formed on the upper surfaces of the gate electrodes **3**.

Igarashi, Ex. 1004, ¶¶ 116-17 (cited POR 34)

Fig. 12



Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

the same reference numerals are used to describe common features of Igarashi's disclosure." Petition at 22; Ex.-2007, ¶108. Even if true, that assertion provides no basis for finding Igarashi's disclosure of STI regions, and an active region formed thereby, in the First Embodiment to be applicable to the Fifth Embodiment Igarashi's figures do ***not*** illustrate STI regions or an active region with "the same reference numerals" in Figs. 1-5 (First Embodiment) and Fig. 12 (Fifth Embodiment). Ex.-2007, ¶108. Indeed, the isolation regions described in connection with the First Embodiment are not shown in ***any*** of Igarashi's drawings of the Fifth Embodiment, and are ***nowhere described in connection with Igarashi's Fifth Embodiment*** (Fig. 12). Ex.-2007, ¶108.

Thus, the Petitions rely solely on Igarashi's Fifth Embodiment (Fig. 12) to meet the challenged claims (Petition at 22-46) but fail to offer ***any*** supportable evidence, reasoning or rationale to support the Petitions' assertion that Igarashi's Fifth Embodiment (Fig. 12) includes isolation regions forming an active region as required by all challenged claims. Ex.-2007, ¶¶100-01. That is fatal to all the grounds in the Petitions.

b. Petitioner's Expert Conceded That His Opinion Was Based on an Inherency Theory Not Presented in the Petitions

Unable to point to a disclosure in Igarashi of forming isolation regions in its Fifth Embodiment, Shanfield testified at his deposition that he believed such

44

POR at 44

A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made of the semiconductor substrate" both because it explicitly discloses a "active element region" and because it discloses using the "trench method" for "element isolation," meaning the trench method is used to form shallow trench isolation (STI) regions that define the active region where the transistor is formed. (Shanfield Decl. ¶66 (Ex-1002).)

Petition at 25-26

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

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Petition at 25-26

66. A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made of the semiconductor substrate" both because it explicitly discloses a "active element region" and because it discloses using the "trench method" for "element isolation," meaning the trench method is used to form shallow trench isolation (STI) regions that define the active region where the transistor is formed. The use

Shanfield Opening Decl., Ex. 1002, Portion of ¶ 66

Ex.-1102, ¶ 67. Thus, Shanfield's testimony on this issue is entitled to little if any weight. *Smith & Nephew, Inc. v. Arthrex, Inc.*, IPR2016-00918, Paper No. 42 at 78 (PTAB Oct. 16, 2017) ("[Petitioner's expert] merely repeats Petitioner's argument without any additional facts or data on which the opinion is based. Thus, it is entitled to little if any probative weight. 37 C.F.R. 42.65(a).").

POR at 42-43

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

Q. In your declaration did you explain that paragraph 68 would apply to all the embodiments?

MR. SMITH: Objection.

A. If you go to page 16, paragraph 40 of my 1002 declaration -- I'm quoting from the Plumber textbook -- "Plumber explains that modern CMOS chips integrate millions of active devices, NMOS and PMOS, side by side in a common silicon substrate and that it is usually assumed that the individual devices do not interact each other -- interact with each other, except through their circuit connections. Plumber further explains that individual devices on the chip are electrically isolated from each other by growing a fairly thick layer of SiO2 between each of the active devices.

"The regions between these thick SiO2 layers where transistors will be built are called the active regions of the substrate."

So I didn't reference paragraph 68, but I explain that, as his textbook supports my position, that there must be isolation regions in CMOS circuitry at the time of this text, which is around the time of the '501 patent.

"Plumber also explains that active regions may be defined by STI regions." And he goes on to describe STI with some figures.

Shanfield Opening Depo., Ex. 2009, at 104:24-106:1 (cited POR 43)

Shanfield testified that a POSA would have understood that Igarashi's disclosure of isolation regions forming an "active element region" in ¶0068 for the First Embodiment ***necessarily*** applies to every embodiment because "something like an isolation process step ***has*** to be performed on any embodiment." Ex.-2009, 98:18-99:5; Ex.-2007, ¶110. Shanfield testified that every embodiment ***must*** be isolated using LOCOS or the trench method to "have a functional integrated circuit." Ex.-2009, 98:10-13; *see also id.*, 99:6-21 ("Someone of skill in the art will understand there ***has*** to be an isolation. LOCOS and the trench method were the alternatives at the time, and, of course, ***he's got to be referring to every embodiment. It couldn't be interpreted any other way.***"), 100:24-101:10 ("And that's understood to apply to all the embodiments. ***There's no way electrically it can be not isolated.***"); Ex.-2007, ¶110.

POR at 45

A person of skill in the art would understand that that applies to all the embodiments, because you wouldn't have a functional integrated circuit without it.

Q. Does paragraph 68 contain the text "figure 12"?

MR. SMITH: Objection.

A. No, but it -- that's -- if you're attempting to imply that it doesn't have isolation, then it's a misreading of the end of paragraph 68.

It says "Element isolation is performed using methods such as LOCOS or the trench method." And that's understood to apply to all the embodiments. There's no way electrically it can be not isolated.

Shanfield Opening Depo., Ex. 2009, at 98:10-13; 100:24-101:10 (cited POR 43)

Q. So let's go back to the sentence you had in paragraph 19. And is this still your opinion that "The absence of an isolation region does not signify the absence of an active region"?

A. Yes.

Q. So that means you can have an active region without an isolation region, right?

A. Yes.

Q. And that means you can have a transistor without an isolation region?

A. Yes. Although as I've explained, it isn't really relevant to the '501 technology.

Shanfield Reply Depo., Ex. 2026 at 84:18-85:5 (cited in Paper No. 34, Observation No. 4)

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

Also, contrary to Patent Owner's assertion (Prelim. Resp. 8–9), Petitioner does not ignore the fact that its citations are directed to discussion of different embodiments of Igarashi. In fact, Petitioner squarely addresses the issue, arguing that a person of ordinary skill in the art "would have understood that the disclosure of the features in Igarashi common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference numerals are used to describe common features of Igarashi's disclosure" and, "[w]here features differ between figures, the differences are described in the disclosure of Igarashi." Pet. 22 (citing 37 C.F.R. § 1.84(p)(4)). For these reasons, we are not persuaded on this record that Petitioner inappropriately relies on different embodiments of Igarashi.

Second, Patent Owner argues that "even if a [person of ordinary skill in the art] would have been led to combine the features of Igarashi and Woerlee in the manner alleged in the Petition, the resulting semiconductor device does not include a MISFET having an active region as claimed." Prelim. Resp. 4; *see id.* at 32. Patent Owner's arguments in this regard are premised primarily on its contention that an "active region" is limited to regions associated with a single transistor. *See* Prelim. Resp. 9–17, 47–58. For the reasons discussed above (*supra* Section II.A), we are not persuaded based on the current record that the claims are so limited. Further, as discussed above, we are persuaded on the record now before us that Igarashi's disclosure of "active element region[s]" applies to the embodiment described with respect to Figure 12 of Igarashi. Petitioner relies on Woerlee for its teaching that "because the isolation regions 3 formed in the semiconductor substrate 1 define the active region 4 of the

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

Claims 1, 4, 7, 9-11, 14, 16-18, and 23-25 are rendered obvious by Igarashi in view of Woerlee. Igarashi and Woerlee were not considered by the Examiner during prosecution of the '501 patent. (Shanfield Decl. ¶59 (Ex-1002).)

1. Independent Claim 1

As illustrated in the chart below and in the discussion that follows, Igarashi in view of Woerlee renders independent claim 1 of the '501 patent obvious. A POSITA would have understood that the disclosure of the features in Igarashi common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference numerals are used to describe common features of Igarashi's disclosure. *See* 37 C.F.R. 1.84(p)(4) ("The same part of an invention appearing in more than one view of the drawing must always be designated by the same reference character, and the same reference character must never be used to designate different parts.") Where features differ between figures, the differences are described in the disclosure of Igarashi. (*E.g.*, Igarashi at [0117] ("FIG. 12 is a schematic sectional view showing a semiconductor device according to Fifth Embodiment of the present invention. Fifth Embodiment will be described below referring to the drawings. The semiconductor device of Fifth Embodiment has the configuration in which the silicon nitride films 8 on the upper surfaces of the gate electrodes 3 are removed as in Fourth Embodiment, and the silicon nitride films 7 and the silicon nitride films 8 on the upper portions of the sidewalls of the

gate electrodes 3 are also removed, and a low-k film 15 is formed on the upper surfaces of the gate electrodes 3.").) (Shanfield Decl. ¶60 (Ex-1002).)

'501 Patent Claim 1	Igarashi	Woerlee
[1p] 1. A semiconductor device, comprising a MISFET, wherein the MISFET includes:	[0002], [0117], Fig. 12	
[1a] an active region made of a semiconductor substrate;	[0044], [0045], [0068], [0112], Fig. 12	2:61-64, 4:66-5:5, Fig. 13, claim 1
[1b] a gate insulating film formed on the active region;	[0020], [0021], [0044], [0134], Fig. 12	
[1c] a gate electrode formed on the gate insulating film;	[0044], Fig. 12	
[1d] source/drain regions formed in regions of the active region located on both sides of the gate electrode; and	[0044], Fig. 12	
[1e] a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein:	[0047-0048], [0117-0118], Fig. 12	
[1f] the silicon nitride film is not formed on an upper surface of the gate electrode, and	[0117-0118], Fig. 12	
[1g] the gate electrode protrudes upward from a surface level of parts of the silicon	[0117-0118], Fig. 12	

Petition at 22-23

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

Second, PO again incorrectly argues that the Fifth Embodiment described in Igarashi does not teach shallow trench isolation ("STI") regions forming an active region and that the Petition relies on Woerlee only for the *location* of the STI regions, not formation of STI regions in Igarashi's fifth embodiment. Response, 37. The Board correctly rejected this argument and should do so again here. DI, 19-20. The Petition is clear that a POSITA would have understood that the disclosure of the features in Igarashi common to its different illustrations—including the STI regions—are applicable to the Fifth Embodiment shown in, for example, Figure 12. *See e.g.*, Petition, 22 ("A POSITA would have understood that the disclosure of the features in Igarashi common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference

Reply, Paper No. 22, at 2

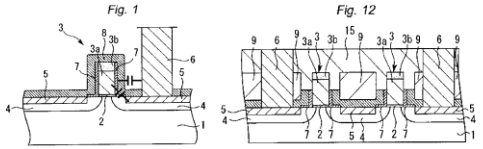
In other words, and consistent with both the Petition and his first declaration, Dr. Shanfield is confirming in this testimony that a person of ordinary skill, when reading Igarashi, would have understood that the disclosure of the features in Igarashi that are common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference numerals are used to describe common features of Igarashi's disclosure. Ex. 1027, ¶24.

Moreover, inherency is irrelevant in this case because—putting aside the fact that neither Petitioner nor Dr. Shanfield has ever raised an inherency argument in this case—Igarashi *expressly* discloses an active region. Petition, 25, *citing* Ex. 1004, [0068] (discussing the formation of the "active element region"). Ex. 1027, ¶25.

The Petition is also clear that a "POSITA would have understood that the disclosure of the features in Igarashi common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference numerals are used to describe common features of Igarashi's disclosure." Petition, 22. For example, "semiconductor substrate 1" where the active region is formed is a common feature between Figure 1 (Embodiment 1) and Figure 12 (Embodiment 5). In fact, Dr. Glew admitted that he used the same approach to interpret the '501 patent, admitting that he based his assessment of the '501 patent's first

Reply, Paper No. 22, at 17-18

embodiment on the '501 patent's third embodiment because "it uses the same Item No. 2, which indicates to me that it is going to be substantially similar to the other uses of Item 2." Ex. 1024, 81:8-24. This uniform numbering scheme for common features (which also includes elements numbered 2-6) is undeniably evident when the two figures in Igarashi are viewed side by side. Ex. 1027, ¶26.



Figures 1 and 12 of Igarashi showing a uniform numbering scheme for common features (Ex. 1004)

This same reasoning applies to common features, like the isolation regions, even if they are not specifically shown in the figures. As noted in the Petition, where features differ between figures, the differences are described in the disclosure of Igarashi. Petition, 22-23, *citing* Ex. 1004, [0117] and Ex. 1002, ¶60; *see also*, Ex. 1024, 111:13-112:3 (confirming that a POSITA at the relevant time would not rely on spacing the devices in Figure 12 of Igarashi so far apart that isolation would not be needed). Ex. 1027, ¶26.

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

In other words, and consistent with both the Petition and his first declaration, Dr. Shanfield is confirming in this testimony that a person of ordinary skill, when reading Igarashi, would have understood that the disclosure of the features in Igarashi that are common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference numerals are used to describe common features of Igarashi's disclosure. Ex. 1027, ¶24.

Moreover, inherency is irrelevant in this case because—putting aside the fact that neither Petitioner nor Dr. Shanfield has ever raised an inherency argument in this case—Igarashi *expressly* discloses an active region. Petition, 25, *citing* Ex. 1004, [0068] (discussing the formation of the "active element region"). Ex. 1027, ¶25.

The Petition is also clear that a "POSITA would have understood that the disclosure of the features in Igarashi common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference numerals are used to describe common features of Igarashi's disclosure." Petition, 22. For example, "semiconductor substrate 1" where the active region is formed is a common feature between Figure 1 (Embodiment 1) and Figure 12 (Embodiment 5). In fact, Dr. Glew admitted that he used the same approach to interpret the '501 patent, admitting that he based his assessment of the '501 patent's first

Reply, Paper No. 22, at 17

Moreover, the Petition showed that Igarashi's isolation region teachings were applicable to its Figure 12 embodiment. Specifically, the Petition cites Figure 12, which shows the "semiconductor substrate 1." Petition, 25. Then, the Petition explains that a POSITA would have understood that the semiconductor substrate 1 in Fig. 12 has an active region because Igarashi expressly discloses an "active element region" made of the semiconductor substrate 1. Petition 25-26, *citing* Ex. 1004, [0068]; Ex. 1002, ¶66; Ex. 1010, 42-43. Ex. 1027, ¶27.

Accordingly, both the Petition and Dr. Shanfield's testimony have been clear and consistent throughout this proceeding: Igarashi discloses the "active region" of the challenged claims in connection with its Fifth Embodiment. Moreover, as discussed below in Section III.D, the Petition also demonstrated it would have been obvious to form the active region disclosed in Igarashi in semiconductor substrate 1 of Igarshi's Fifth Embodiment in view of the teachings of Woerlee. Ex. 1027, ¶28.

B. Igarashi Discloses a MISFET that Includes an "Active Region"

A person of ordinary skill would have viewed the region between the two STI in Igarashi where the two transistors are formed as an "active region" formed between those two STI. As noted in the Petition: "The use of the 'trench method' confirms the 'active element region' (active region) is made of the semiconductor substrate 1 because according to the trench method the active region is formed in

Reply, Paper No. 22, at 19

a. The Petitions Fail to Meet Petitioner's Burden of Demonstrating How and Why Any MISFET in the Igarashi/Woerlee Combination Includes an "Active Region" Meeting the Agreed-Upon BRI

The Petitions must specify the grounds with particularity. 35 U.S.C. §312(a)(3) (requiring IPR petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim"); 37 C.F.R. §42.104(b)(4) ("The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon."); *Harmonic*, 815 F.3d at 1363; *Kranos*, IPR2016-01649, Paper No. 25 at 29, 36, 39-42.

The Petitions fail to meet Petitioner's burden of establishing that ***any*** MISFET in the Igarashi/Woerlee combination "includes: an active region" meeting the agreed-upon BRI. Ex.-2007, ¶132.

As shown in Petitioner's modified Fig. 12 (reproduced below), the Petitions insert "STI" regions on the left and right sides, and further label the figure with a box "Active Region" and two arrows pointing to the channel regions under the gates of the two MISFETs. Ex.-2007, ¶132. The Petitions allege the "active element region is made of the substrate 1 of Igarashi and divided by STI regions." -1841-Petition at 27, 37. Ex.-2007, ¶132.

POR at 59

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

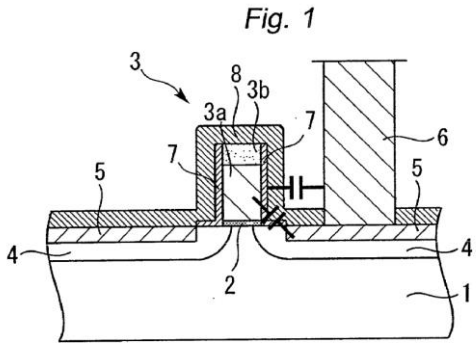
[0043] First Embodiment

[0044] **FIG. 1** is a schematic sectional view showing a semiconductor device according to First Embodiment of the present invention. The configuration of the semiconductor device of First Embodiment will be described below referring to **FIG. 1**. The semiconductor device of First Embodiment is an example of MOS transistors of an SAC structure to which the present invention is applied, and comprises a gate electrode **3** formed on a silicon semiconductor substrate **1** through a gate oxide film **2**; a pair of impurity diffusion layers **4** of source/drain diffused layers formed on the surface region of the silicon semiconductor substrate **1** in the both sides of the gate electrode **3**; a silicide film **5** formed on the surface of the impurity diffusion layers **4**; and a contact electrode **6** electrically connected to the silicide film **5**.

Igarashi, Ex. 1004, ¶¶ 43-44 (cited POR 33)

[0068] Next, the method for manufacturing the semiconductor device of First Embodiment will be described. In the following description of the manufacturing method, the major process for forming the silicon nitride film **7** will be described referring to **FIGS. 5A** to **5**E, and other processes will be described without referring to drawings. First, an insulating film for isolating elements is formed on a silicon semiconductor substrate **1**. Element isolation is performed using methods such as the LOCOS method or the trench method. Thereafter, ion implantation is performed to the active element region for forming the well and controlling the threshold value.

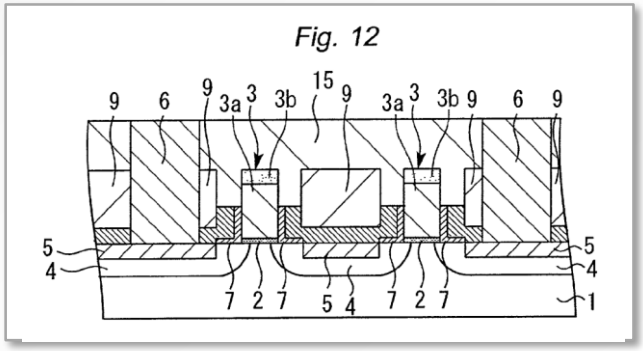
Igarashi, Ex. 1004, ¶ 68 (cited POR 34)



[0116] Fifth Embodiment

[0117] **FIG. 12** is a schematic sectional view showing a semiconductor device according to Fifth Embodiment of the present invention. Fifth Embodiment will be described below referring to the drawings. The semiconductor device of Fifth Embodiment has the configuration in which the silicon nitride films **8** on the upper surfaces of the gate electrodes **3** are removed as in Fourth Embodiment, and the silicon nitride films **7** and the silicon nitride films **8** on the upper portions of the sidewalls of the gate electrodes **3** are also removed, and a low-k film **15** is formed on the upper surfaces of the gate electrodes **3**.

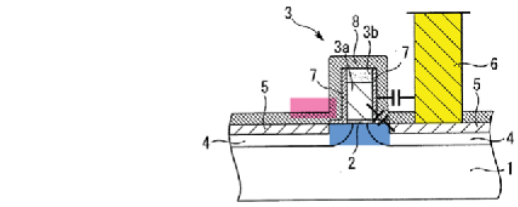
Igarashi, Ex. 1004, ¶¶ 116-17 (cited POR 34)



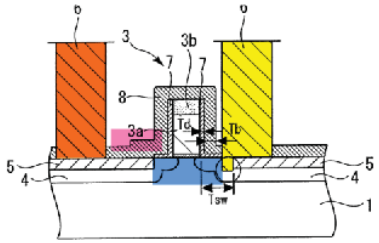
"Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions" (Paper No. 20 at 38)

This same reasoning applies to common features, like the isolation regions, even if they are not specifically shown in the figures. As noted in the Petition, where features differ between figures, the differences are described in the disclosure of Igarashi. Petition, 22-23, *citing* Ex. 1004, [0117] and Ex. 1002, ¶60; *see also*, Ex.

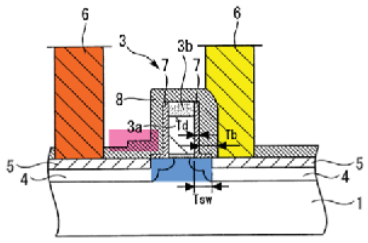
Reply, Paper No. 22, at 18



Igarashi (Ex.-1004), Figure 1 (annotated)



Igarashi (Ex.-1004), Figure 3 (annotated)



Igarashi (Ex.-1004), Figure 4 (annotated)

120. Finally, the Board relied upon Petitioner's assertion that "[w]here features differ between figures, the differences are described in the disclosure of Igarashi." Decision at 20. This assertion is incorrect. The Board overlooks the fact that there are many differences between the figures which are never addressed in Igarashi. For example, as shown below, Figure 1 of the First Embodiment shows only ***one*** contact electrode 6 (highlighted in yellow below) while Figures 3 and 4 show ***two*** contact electrodes 6. Igarashi does not describe the second contact electrode (highlighted in orange below) or describe the reason Figures 3 and 4, unlike figure 1, have a second contact electrode. Ex.-1004 (Igarashi) at ¶¶ 44 (Fig. 1 "show[s] a semiconductor device according to First Embodiment of the present invention … [where] a gate electrode 6 [is] electrically connected to the silicide film 6."), 65-66 (describing only the right contact electrode (highlighted in yellow) in figures 3 and 4). Similarly, in Figures 3 and 4, the silicon nitride film 8 has a stepped profile (highlighted in pink below) and the impurity diffusion layers 4 have a profile that appears similar to overlapping circles (highlighted in blue below) that are different from Figure 1. Again, Igarashi never identifies or describes these differences between the figures.

Glew Declaration, Ex. 2007, ¶ 120 (cited POR 51)

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

Ex.-2007, ¶¶101-05. ***Elsewhere in Igarashi, when a component is present in an embodiment but <u>not</u> shown in a figure, Igarashi discloses that the component is "omitted" from that figure***. Ex-1004, ¶0074 ("In the description of each embodiment other than FIGS. 5A to 5E, the description and the illustration of the silicon oxide film 11 will be omitted."); Ex.-2007, ¶106. The Petitions do not even attempt to explain why Igarashi never discloses that the claimed active region is allegedly present in the Fifth Embodiment, but omitted from Figure 12. Ex.-2007, ¶106.

POR at 42

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

Based on the current record, however, we find it is clear from Igarashi that the disclosure of "active element region[s]" discussed in paragraph 68 with respect to the "First Embodiment" is equally applicable to the "Fifth Embodiment" upon which Petitioner primarily relies. For example, the description of the method for manufacturing the semiconductor device of the "Fifth Embodiment" refers back to earlier described embodiments of Igarashi, ultimately referencing the discussion of the method for manufacturing the semiconductor device of the "First Embodiment." Ex. 1004 ¶ 119 ("FIGS. 13A and 13[B] are schematic sectional views sequentially showing the method for manufacturing the semiconductor device shown in FIG. 12 [the Fifth Embodiment]. Here, FIG. 13A shows the same process as in FIG. 11B . . . ."), ¶¶ 112–13 ("FIGS. 11A to 11C are schematic sectional views showing the method for manufacturing the semiconductor device shown in FIG. 10 [the Fourth Embodiment]. . . . First, as FIG. 11A shows, gate electrodes 3 are formed, and silicon nitride films 7 and silicon nitride films S are formed so as to cover the gate electrodes 3 in the same process as in FIG. 5 . . . ."), ¶ 68 ("[T]he method for manufacturing the semiconductor device of First Embodiment will be described. In the following description of the manufacturing method, the major process for forming the silicon nitride film 7 will be described referring to FIGS. 5A to 5E, and other processes will be described without referring to drawings. First, an insulating film for isolating elements is formed on a silicon semiconductor substrate 1. Element isolation is performed using methods such as the LOCOS method or the trench method. Thereafter, ion implantation is performed to the active element region for forming the well and controlling the threshold value.").

Institution Decision, Paper No. 10, at 19

The Institution Decision states that "the description of the method for manufacturing the semiconductor device of the 'Fifth Embodiment' refers back to earlier described embodiments of Igarashi, ultimately referencing the discussion of the method for manufacturing the device of the 'First Embodiment.'" Decision at 19; Ex.-2007, ¶115. The Petitions never made this argument. Thus, it is improper for the Board to advance this rationale. *See In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016) ("[W]e find no support for the PTO's position that the Board is free to adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR. Instead, the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond."); *Liberty Mut.*, CBM2012-00003, Paper No. 8 at 10 (the Board "will address only the basis, rationale, and reasoning put forth by the Petitioner in the petition"); *id.* at 14 ("It would be … inappropriate for the Board to take the side of the Petitioner to salvage an inadequately expressed ground proposing an alternative rationale.").

POR at 47-48

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

19; Ex.-2007, ¶115. The Petitions never made this argument. Thus, it is improper for the Board to advance this rationale. *See In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016) ("[W]e find no support for the PTO's position that the Board is free to adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR. Instead, the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond."); *Liberty Mut.*, CBM2012-00003, Paper No. 8 at 10 (the Board "will address only the basis, rationale, and reasoning put forth by the Petitioner in the petition"); *id.* at 14 ("It would be … inappropriate for the Board to take the side of the Petitioner to salvage an inadequately expressed ground proposing an alternative rationale.").

In addition, as Dr. Glew explains, the new rationale advanced by the Board in the Institution Decision has two critical mistakes. Ex.-2007, ¶116.

First, a POSA would have understood that Fig. 13A, which illustrates the manufacturing process of the Fifth Embodiment, shows "the same process as in FIG. 11B" (Ex.-1004, ¶119)—***not*** the same process as in ***all of Figs. 11A-11C*** as the Board suggested. Ex.-2007, ¶117.

Second, Igarashi states that "as Fig. 11A shows, gate electrodes 3 are formed, and ***silicon nitride films 7 and silicon nitride films 8 are formed so as to cover the gate electrodes 3 in the same process as in FIG. 5***." Ex.-1004, ¶112.

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Thus, even were the Board to find that the description of the Fifth Embodiment refers to Fig. 11A (Dr. Glew explains that a POSA would have understood that it does not, Ex.-2007, ¶117), a POSA would have understood that Fig. 11A in turn refers to Fig. 5 ***only*** for its disclosure of the process of forming silicon nitride films 7 and 8 shown in Fig. 5. Ex.-2007, ¶118. That is, a POSA would have understood that Igarashi does ***not*** state that any other process of Fig. 5 (e.g., the process for forming STI regions) other than the process for forming silicon nitride films 7 and 8 is used in connection with Fig. 11A. Ex.-2007, ¶118.

The Board also relied on Petitioner's statement that "the same reference numerals are used to describe common features of Igarashi's disclosure." Decision at 20; Ex.-2007, ¶119. However, as Dr. Glew explains, a POSA would have understood that the features at issue (active regions and isolation regions) are never labelled or numbered in any figures of Igarashi. Ex.-2007, ¶119.

Finally, the Board relied upon Petitioner's conclusory assertion that "[w]here features differ between figures, the differences are described in the disclosure of Igarashi." Decision at 20; Ex.-2007, ¶120. This assertion is plainly incorrect. Indeed, there are multiple differences between the figures which are never addressed in Igarashi. Ex.-2007, ¶120. For example, as shown below, Figure 1 of the First Embodiment shows only ***one*** contact electrode 6 (highlighted in yellow below) while Figures 3 and 4 show ***two*** contact electrodes 6. Ex.-2007,

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POR at 48-49

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

First, even transistors that do not use isolation regions such as STI still have active regions—otherwise, the transistors would simply not function. The absence of an isolation region does not signify the absence of an active region. *Second*, by the time of the alleged invention in 2003, virtually all transistors included isolation regions. A POSITA at the time of the alleged invention would not have understood Igarashi to be implemented in a manner that omitted isolation regions or structures (such as STI) because: (i) the transistors commonly used by then were too small for spacing alone to be a functional alternative to isolation regions or structures (such as STI); and (ii) Igarashi expressly discloses the use of isolation regions and such isolation regions would have been obvious in view of Woerlee. Ex. 1027, ¶19; Petition, 25-27; Ex. 1024, 111:18-25 (admitting that using spacing rather than isolation "would not be a typical solution" for memory cells in the 2003 timeframe).

Accordingly, PO's interpretation of an "active region" is inappropriately narrow, forecloses substantial portions of the technical field, and is purely designed to escape the overwhelming prior art. Ex. 1027, ¶20.

III. IGARASHI AND WOERLEE DISCLOSE THE CLAIMED "ACTIVE REGION"

PO again incorrectly argues that the Fifth Embodiment described in Igarashi, itself, does not teach STI regions forming an active region. Response, 37. The

Reply, Paper No. 22, at 14

D. Patent Owner Again Incorrectly Argues that the Petition Relies on Woerlee Only for the Location of the Active Region

PO argued in its POPR that "even if a [POSITA] would have been led to combine the features of Igarashi and Woerlee in the manner alleged in the Petition, the resulting semiconductor device does not include a MISFET having an active region as claimed." POPR, 4, 32. Put differently, PO's argument is that the Petition relies on Woerlee only for the *location* of the active region, not the existence of the active region, and that there is no active region disclosed in connection with Figure 12 of Igarashi. As the Board recognized, the Petition expressly shows that it would have been obvious to a person of ordinary skill in the art apply Igarashi's teaching of an active region to Igarashi's Fifth Embodiment in view of Woerlee. DI, 16 (quoting Petition, 32) ("Petitioner also provides several reasons why a person of ordinary skill in the art would have 'appl[ied] Woerlee's teachings to Igarashi by forming Igarsahi's active region in the substrate and defining it with STI regions that divide the active region.'") Yet, PO resurrects

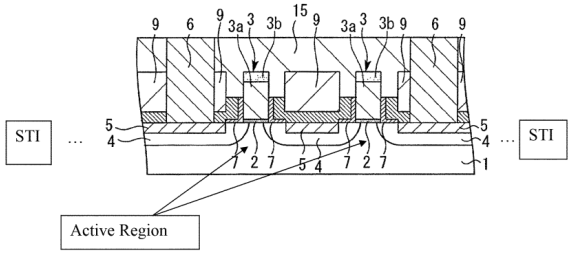
Reply, Paper No. 22, at 25-26

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

D. Patent Owner Again Incorrectly Argues that the Petition Relies on Woerlee Only for the Location of the Active Region

Reply, Paper No. 22, at 25

Fig. 12



(Igarashi at Fig. 12 (Ex-1004) (annotated).) (Shanfield Decl. ¶66 (Ex-1002).)

To the extent that Igarashi does not explicitly disclose the location of the "active element region" and therefore that the active region is "made of" the semiconductor substrate, Woerlee discloses this limitation. (Shanfield Decl. ¶67 (Ex-1002).) For example, Woerlee discloses an active region 4 "made of" the semiconductor body 1 in Fig. 13:

formed and a pMISFET formation region Rp which includes the active region 1 b and in which a pMISFET is to be formed." ('501 patent at 3:23-28 (Ex-1001).) Thus, Woerlee and the '501 patent both describe the active region made of the substrate as the region bounded by isolations regions where the transistor is formed. (Shanfield Decl. ¶71 (Ex-1002).)

Woerlee would therefore have provided a POSITA additional detail on how to use the trench method disclosed in Igarashi to form Igarashi's active element region (active region) in the semiconductor substrate 1. In particular, Woerlee would have taught a POSITA to use the trench method to form STI regions in Igarashi's semiconductor substrate 1 to define an active element region (active region) made of the semiconductor substrate 1. (Shanfield Decl. ¶72 (Ex-1002).)

By locating Igarashi's active element region (active region) in the semiconductor substrate 1 according to the teaching of Woerlee, in the modified device, Igarashi's gate oxide film 2 (gate insulating film) would have been formed on the active element region (active region), just as Woerlee's gate dielectric 24 (gate insulating film) is formed on the active region 4 (as recited in claim 1, element 1b below). Likewise, in the modified device, Igarashi's impurity diffusion layers 4 and silicide layer 5 (source/drain regions) would have been formed in regions of the active element region (active region) located on both sides of the gate electrode 3, just as the source/drain zones 11, 14, and 15 (source/drain

Petition at 27, 31

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

Petitioner further relies on Woerlee as providing explicit disclosure of the location of the active region within the semiconductor substrate. Pet. 27–28; Ex. 1002 ¶¶ 67–68. Petitioner asserts that active region 4 of Woerlee is "made of" semiconductor body 1, as required by claim 1. Pet. 29 (citing Ex. 1006, 4:66–5:5 (disclosing "field insulating regions 3, which are at least partly recessed in the semiconductor body 1 and which define an active region 4 in which a transistor . . . is to be manufactured"), 2:61–64 (disclosing "an oxide field insulating region, which is provided at the surface of the semiconductor body to separate active regions in the semiconductor body")); *see id.* at 29–31; Ex. 1002 ¶¶ 69–71. According to Petitioner, "Woerlee would . . . have provided a [person of ordinary skill in the art] additional detail on how to use the trench method disclosed in Igarashi to form Igarashi's active element region (active region) in the semiconductor substrate 1." Pet. 31; *see id.* at 31–32; Ex. 1002 ¶¶ 72–74.

Institution Decision, Paper No. 10, at 15-16

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

numerals are used to describe common features of Igarashi's disclosure.")

Moreover, the Petition is clear that it would have been obvious to apply Igarashi's undisputed teaching of an active region to the Fifth Embodiment. DI, 16 (quoting Petition, 32) ("Petitioner also provides several reasons why a person of ordinary skill in the art would have 'appl[ied] Woerlee's teachings to Igarashi by forming Igarsahi's active region in the substrate and defining it with STI regions that divide the active region.'")

As set forth in the Petition and confirmed below, the challenged claims of the '501 patent would have been obvious under the cited prior art references and, accordingly, Petitioner respectfully requests that the Board cancel all challenged claims.

II. PATENT OWNER'S INTERPRETATION OF "AN ACTIVE REGION MADE OF A SEMICONDUCTOR SUBSTRATE" IS INAPPROPRIATELY NARROW

PO claims that "there is no dispute that under BRI, 'an active region made of a semiconductor substrate' is 'an area of the semiconductor substrate defined by an isolation region where the transistor is formed.'" Response, 26. PO then advances an unduly narrow interpretation of this proposed construction that seeks to limit the active region to having only a *single* transistor, as it sought to do through a different construction in the POPR, which the Board properly rejected. Response 74; POPR, 25, 29; DI, 9. Nothing in the '501 patent or prior art requires such a

Reply, Paper No. 22, at 3

of isolation regions and an "active element region" in the First Embodiment. Ex.-2007, ¶121.

d. The Petitions Do Not Rely on Modifying Igarashi's Fifth Embodiment to Use the Isolation Regions of Igarashi's First Embodiment

Merely showing that all of a claim's elements are individually disclosed in the prior art is insufficient to render the claim obvious. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) ("[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.").

Disclosure of distinct embodiments in the same reference does not render obvious any and all combinations of the elements of those embodiments. *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) ("Whether a rejection is based on combining disclosures from multiple references, ***combining multiple embodiments from a single reference***, or selecting from large lists of elements in a single reference, ***there must be a motivation to make the combination*** and a reasonable expectation that such a combination would be successful, otherwise a skilled artisan would not arrive at the claimed combination.").

Igarashi's First Embodiment is a single-transistor semiconductor device, and the "active element region" Igarashi describes in connection with this embodiment is bounded by isolation regions that electrically isolate that ***single transistor***. Ex.-

POR at 52

regions) in Woerlee are formed in regions of the active region 4 located on both sides of the gate electrode 21 (as recited in claim 1, element 1d below). The modified device would also have an active element region (active region) divided by the STI regions (isolation region) formed in the semiconductor substrate 1 (as recited in claim 10 below), just as the active region 4 is divided by an isolation region 3 formed in the semiconductor substrate 1 in Woerlee. (Shanfield Decl. ¶73 (Ex-1002).)

Therefore, Igarashi in view of Woerlee discloses "an active region made of a semiconductor substrate." (Shanfield Decl. ¶74 (Ex-1002).)

c) Claim 1 – Active Region (element [1a]) – Reasons to Modify

It would have been obvious to modify Igarashi in view of Woerlee's teachings of an active region "made of" a semiconductor substrate (recited in claim 1, element 1a) and an active region divided by an isolation region formed in the semiconductor substrate (recited in claim 10 below). In particular, it would have been obvious to apply Woerlee's teachings to Igarashi by forming Igarashi's active region in the substrate and defining it with STI regions that divide the active region. (Shanfield Decl. ¶75 (Ex-1002).)

First, a POSITA would have looked to the teachings of Woerlee because it is in the same field of endeavor as Igarashi. Igarashi discloses a MISFET device with a "silicon semiconductor substrate 1" where "[e]lement isolation is performed" to

Petition at 32

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

Q. In your declaration did you explain that paragraph 68 would apply to all the embodiments?

MR. SMITH: Objection.

A. If you go to page 16, paragraph 40 of my 1002 declaration -- I'm quoting from the Plumber textbook -- "Plumber explains that modern CMOS chips integrate millions of active devices, NMOS and PMOS, side by side in a common silicon substrate and that it is usually assumed that the individual devices do not interact each other -- interact with each other, except through their circuit connections. Plumber further explains that individual devices on the chip are electrically isolated from each other by growing a fairly thick layer of SiO2 between each of the active devices.

"The regions between these thick SiO2 layers where transistors will be built are called the active regions of the substrate."

So I didn't reference paragraph 68, but I explain that, as his textbook supports my position, that there must be isolation regions in CMOS circuitry at the time of this text, which is around the time of the '501 patent.

"Plumber also explains that active regions may be defined by STI regions." And he goes on to describe STI with some figures.

Shanfield Opening Depo., Ex. 2009, at 104:24-106:1 (cited POR 11)

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

At deposition, Petitioner's expert could not identify any teachings in ***Igarashi*** that the reference in ¶0068 to forming isolation regions applied to other embodiments. Ex.-2009, 99:8-21, 100:24-101:10, 98:18-99:5, 98:10-13, 104:24-106:1; Ex.-2007, ¶107. Shanfield instead pointed to disclosures in a completely different reference (Plummer), but nothing in Plummer can remedy the fatal deficiency in the grounds because the Petitioner does not allege obviousness over Plummer. Ex.-2007, ¶107; *see Ericsson*, IPR2014-00963, Paper No. 29 at 31-32; *Meyer Prods., LLC v. Douglas Dynamics, LLC*, IPR2015-01247, Paper No. 47 at 27 (PTAB Nov. 25, 2016).

POR at 43

b. Petitioner's Expert Conceded That His Opinion Was Based on an Inherency Theory Not Presented in the Petitions

Unable to point to a disclosure in Igarashi of forming isolation regions in its Fifth Embodiment, Shanfield testified at his deposition that he believed such

Shanfield testified that a POSA would have understood that Igarashi's disclosure of isolation regions forming an "active element region" in ¶0068 for the First Embodiment ***necessarily*** applies to every embodiment because "something like an isolation process step ***has*** to be performed on any embodiment." Ex.-2009, 98:18-99:5; Ex.-2007, ¶110. Shanfield testified that every embodiment ***must*** be isolated using LOCOS or the trench method to "have a functional integrated circuit." Ex.-2009, 98:10-13; *see also id.*, 99:6-21 ("Someone of skill in the art will understand there ***has*** to be an isolation. LOCOS and the trench method were the alternatives at the time, and, of course, ***he's got to be referring to every embodiment. It couldn't be interpreted any other way.***"), 100:24-101:10 ("And that's understood to apply to all the embodiments. ***There's no way electrically it can be not isolated.***"); Ex.-2007, ¶110.

POR at 44-45

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

Board has already rejected this argument: "[W]e find it is clear from Igarashi that the disclosure of 'active element region[s]' discussed in paragraph 68 with respect to the 'First Embodiment' is equally applicable to the 'Fifth Embodiment' upon which Petitioner primarily relies." DI, 18-20. Ex. 1027, ¶21.

A. Patent Owner's Imagined Inherency Argument Mischaracterizes Dr. Shanfield's testimony

PO attempts to mischaracterize Dr. Shanfield's testimony, claiming that he has advanced a "new" inherency argument by suggesting that isolation regions were present in that embodiment because they were ***necessary*** for the device to work. Response, 12. Ex. 1027, ¶22. PO's strawman argument should be rejected.

The Response asserts that "[Dr.] Shanfield testified that every embodiment ***must*** be isolated using LOCOS or the trench method to 'have a functional integrated circuit.' Ex.-2009, 98:10-13." Response, 45. But in the context of the surrounding testimony omitted from the Response (bracketed below), it is clear that Dr. Shanfield's testimony is directed to the understanding of one of ordinary skill in the art when reading Igarashi and *not* inherency:

> "[***Someone of skill in the art, reading this, would understand*** that what Igarashi means is, I'm going to describe the method for manufacturing the semiconductor device of the first embodiment. …. Clearly isolation is required in any embodiment.

Reply, Paper No. 22, at 15

In other words, and consistent with both the Petition and his first declaration, Dr. Shanfield is confirming in this testimony that a person of ordinary skill, when reading Igarashi, would have understood that the disclosure of the features in Igarashi that are common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference numerals are used to describe common features of Igarashi's disclosure. Ex. 1027, ¶24.

Moreover, inherency is irrelevant in this case because—putting aside the fact that neither Petitioner nor Dr. Shanfield has ever raised an inherency argument in this case—Igarashi *expressly* discloses an active region. Petition, 25, *citing* Ex. 1004, [0068] (discussing the formation of the "active element region"). Ex. 1027, ¶25.

The Petition is also clear that a "POSITA would have understood that the disclosure of the features in Igarashi common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference numerals are used to describe common features of Igarashi's disclosure." Petition, 22. For example, "semiconductor substrate 1" where the active region is formed is a common feature between Figure 1 (Embodiment 1) and Figure 12 (Embodiment 5). In fact, Dr. Glew admitted that he used the same approach to interpret the '501 patent, admitting that he based his assessment of the '501 patent's first

Reply, Paper No. 22, at 17

the term "includes" in claim 1 means "that it has at least these features." Ex. 1024, 94:20-95:7. Under the second, each transistor includes an active region because there are two transistors and two active regions. Ex. 1027, ¶¶30-31.

PO's (and Dr. Glew's) arguments against Igarashi's "active region" are internally inconsistent. For example, in its Response, PO first argues that the entire region bounded by isolation regions is not the formation region for *any* transistors. Response, 17-18. Yet, in the very next sentence, PO concedes that this region is the formation region for at least two transistors. Response, 18 ("It is undisputed that there are at least two transistors in Igarashi's Fig. 12."). Ex. 1027, ¶32.

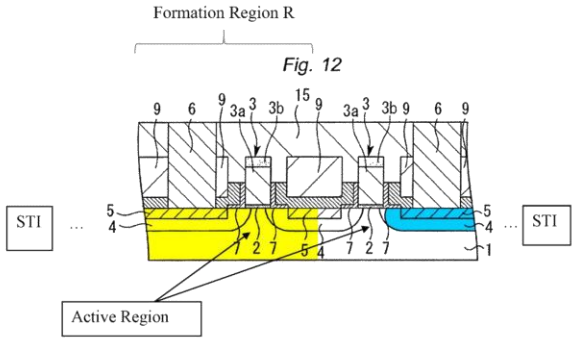
PO's attempt to argue that Igarashi's Figure 12 embodiment somehow does not have an active region because it is a memory device also fails. Response, 33-34. When asked to provide examples of known devices having "active regions," Dr. Glew admitted that there were various types of devices—including "logic and *memory* devices"—that would have "active regions." Ex. 1024, 97:7-18. Ex. 1027, ¶33.

And, as Dr. Glew confirmed in his declaration, Igarashi's Fifth Embodiment shown in Figure 12 "comprises a portion of a memory cell"—precisely the type of

Reply, Paper No. 22, at 21

MISFET. Ex.-2007, ¶145. It is undisputed that there are at least two transistors in Igarashi's Fig. 12. Ex.-2010, 405:9-18, 423:21-424:1; Ex.-2007, ¶144. Indeed, Petitioner's expert agreed there could be more, and that the STI regions the Petitions added to Fig. 12 could be further away from the shown transistors. Ex.-2009, 93:21-94:20; Ex.-2010, 406:15-23; Ex.-2007, ¶144. For example, the left transistor is formed in the region highlighted yellow below. Ex.-2007, ¶145.

There are other regions of the substrate bounded by the alleged isolation region, e.g., the area highlighted blue, that are unquestionably not part of the region (yellow below) where the left MISFET is formed. Ex.-2007, ¶145.



Neither of the MISFETs shown in the Petitions' modified-Igarashi Fig. 12 is formed in and includes the entire region of the substrate bounded by the isolation region, so the region bounded by the isolation region is not an "active region" of

POR at 18

Petitioner's Relies Heavily On The Institution Decision; Institution Decision at 9

'active region' refers to a region that is dedicated to that transistor." Prelim. Resp. 3–4, 29–30. For example, Plummer[10] describes that "regions between these [isolation] layers, where transistors will be built, are called the 'active' regions of the substrate" (Ex. 1008, 53), and Rabaey[11] describes "active regions" as "the regions where transistors will be constructed" (Ex. 1010, 42). Nothing about these descriptions connotes a requirement for a one-to-one correspondence of active regions-to-transistors, as Patent Owner contends.

Based on the record now before us, we are not persuaded that the claimed "active region" is limited to a region associated with a single transistor (i.e., "a region of a semiconductor substrate dedicated to the MISFET and defined by isolation regions that isolate the MISFET from other transistors formed in the substrate"), as Patent Owner contends. As discussed *infra*, Section II.E, Igarashi includes disclosure of "active element regions," which we find to be within the scope of the plain and ordinary meaning of "active region." Thus, we need not further construe "active region" for purposes of this Decision. The parties, however, may address further construction of the term during trial.

B. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such

[10] JAMES D. PLUMMER ET AL., SILICON VLSI TECHNOLOGY: FUNDAMENTALS, PRACTICE AND MODELING (Charles Sonini ed., Prentice Hall, Inc., 2000) (Ex. 1008).

[11] JAN M. RABAEY ET AL., DIGITAL INTEGRATED CIRCUITS: A DESIGN PERSPECTIVE (Charles G. Sonini ed., Pearson Educ., Inc., 2d ed. 2003) (Ex. 1010).

Institution Decision, Paper No. 10, at 9

I. INTRODUCTION

Patent Owner's Response ("Response") confirms that the challenged claims are unpatentable. There is no dispute that Igarashi discloses the allegedly novel "protruding gate" that provided the basis for allowance.[2] Moreover, Patent Owner ("PO") does not dispute that the instituted grounds expressly disclose every limitation of the challenged claims, except the "active region." Nor does PO dispute that the references would have been obvious to combine. Instead, PO merely repeats the same arguments that it already raised in its Patent Owner's Preliminary Response ("POPR"[3]) that Igarashi's disclosure somehow lacks an "active region," one of the most basic aspects of a semiconductor device. These arguments were correctly rejected by the Board in the Institution Decision ("DI") and fail again here.

[2] In fact, PO actually *cites* Igarashi as evidence that the purported advantages of the "protruding gate" were well-known. Ex. 2007, ¶¶45-50; *see also* IPR2017-01843 POPR, 32 ("[A] POSA would have understood that … causing the gate electrode to protrude above the silicon nitride … would advantageously reduce parasitic capacitance. Indeed, Igarashi teaches this explicitly."), 30-36; IPR2017-01843 POR, 23-25; IPR2017-01843 Ex. 2208, ¶¶45-50.

[3] Unless otherwise specified with the "-01842" prefix, references to exhibits and papers herein are to those filed in Case IPR2017-01841.

Reply, Paper No. 22, at 1

Petitioner's Coaching During Deposition

During redirect (and re-redirect) at Shanfield's deposition on his reply declaration, Petitioner's counsel improperly led and coached Shanfield by providing express and ***direct*** instructions to Shanfield during questioning. Ex. 2026 at 144:1-12, 145:1-147:8, 167:14-173:3, 173:10-178:4. This improper coaching and leading prompted Shanfield to directly alter the testimony he had given under cross-examination. See § III below.

The testimony elicited via improper leading and coaching should be excluded pursuant to Fed. R. Evid. 611(c). *E.g., Universal Remote Control v. Universal Elecs.*, IPR2014-01146 Paper No. 36 at 6-7 (PTAB Dec. 10, 2015) (excluding re-direct examination, finding the questions were leading because they "contained contextual cues sufficient to suggest the answer that counsel desired to elicit."). Shanfield's willingness to completely alter his testimony in response to

Patent Owner's Motion to Exclude, Paper No. 35 at 2-3

Petitioner's Leading Questions

Q. Do Claims 2, 3, and 20 recite stress limitations?
MR. HRYCYSZYN: Objection, leading.
THE WITNESS: Yes, they do, of course. They talk about [as read], a stress includes the direction tilted by an angle less than 10 degrees in a substantially parallel direction.
BY MR. SMITH:
Q. Does Claim 1 require that a silicon nitride film be a stress film?
MR. HRYCYSZYN: Objection, leading.
THE WITNESS: No, it doesn't.
BY MR. SMITH:
Q. Earlier you were asked about the silicon nitride film that's described in the '501 patent, and you offered testimony that "that isn't what's being referred to here as the silicon nitride film located at both side surfaces of the gate electrode. That's not an etch stop layer. It is referring to, what's talked about in the specification, which is layers that deliver stress to the substrate as a whole."
Do you recall that testimony?
A. Yes, I do.
Q. Were you referring to what's required by the claims, or were you referring to the description of the stress film embodiment in the specification?
MR. HRYCYSZYN: Objection, leading.
THE WITNESS: I was referring to the embodiment in the specification.
BY MR. SMITH:
Q. Do any of the challenged claims --
Do you have Claim 1 in mind?
A. Yes.
Q. Could the silicon nitride film in Claim 1 be a silicon nitride etch stop layer?
A. Yes, it could.
MR. HRYCYSZYN: Objection, leading.
Dr. Shanfield, if you could just slow down and give me a chance to hear the question and object to it on the record.

RECROSS EXAMINATION
BY MR. HRYCYSZYN:

Q. So it is your understanding that Claim 1 of the '501 patent requires that the silicon nitride film induce stress; is that accurate?
A. Yes.

Shanfield Reply Depo., Ex. 2026, at 157:1-2; 160:20-23
(cited Paper No. 35 at 8)

Shanfield Reply Depo., Ex. 2026 at 144:1-145:17
(cited Paper No. 35 at 10)

Petitioner's Counsel's Leading Questions … Enabled Shanfield to Answer Questions About Claim 2 that He Was Unable to Answer Without Being Led (Paper No. 35 at 11)

Q. Do you see dependent claim 2 in the '501 patent, Doctor Shanfield?
A. Yes.
Q. Does this description -- strike that.
Does the paragraph starting at column 3, line 60 apply to the silicon nitride film described in claim 2?
MR. SMITH: Objection.
A. I haven't considered claim 2 in -- in my analysis. I would need to spend time thinking about it in the context of what it's describing.
Q. Does claim 2 require that the silicon nitride film generate a stress in the substrate?
MR. SMITH: Objection. Scope.
A. As I explained, I hadn't considered claim 2, and I can't immediately answer. I would need to do some analysis.

Shanfield Opening Depo., Ex. 2010 at 230:15-231:7
(cited Paper No. 35 at 11)

Q. Do Claims 2, 3, and 20 recite stress limitations?
MR. HRYCYSZYN: Objection, leading.
THE WITNESS: Yes, they do, of course. They talk about [as read], a stress includes the direction tilted by an angle less than 10 degrees in a substantially parallel direction.
BY MR. SMITH:
Q. Does Claim 1 require that a silicon nitride film be a stress film?
MR. HRYCYSZYN: Objection, leading.
THE WITNESS: No, it doesn't.

Shanfield Reply Depo., Ex. 2026 at 144:1-12
(cited Paper No. 35 at 11)

Petitioner's Improper Coaching

Q. I'm going to represent to you that as a legal matter, a dependent claim recites additional limitations that are not present in the independent claim from which it depends.
Do you have that understanding in mind?
MR. HRYCYSZYN: Objection, beyond the scope. Objection, coaching.
THE WITNESS: Okay. I didn't know that.

* * * *

[omitted objections and call to the Board]

Q. So, Dr. Shanfield, with the representation I just made to you in mind about how independent and dependent claims are interpreted, could you look at dependent Claim 2.
A. Yes.
MR. HRYCYSZYN: Objection, beyond the scope. Same objections as before as to the improper question.
BY MR. SMITH:
Q. Does dependent Claim 2 add a requirement that the silicon nitride film is for generating a stress?
MR. HRYCYSZYN: Objection, beyond the scope. Objection, leading, instructing the witness.
THE WITNESS: Yes.
BY MR. SMITH:
Q. Do you see that Claim 2 depends from Claim 1?
MR. HRYCYSZYN: Objection, beyond the scope.
THE WITNESS: Yes, I do.
BY MR. SMITH:
Q. I believe you testified earlier that Claim 1 does not recite any stress limitations; is that correct?
A. That is correct.
MR. HRYCYSZYN: Objection, leading. Objection, improper.
BY MR. SMITH:
Q. And with the understanding that we discussed earlier, is there anything you would like to clarify with your testimony regarding whether Claim 1 requires silicon nitride film to induce stress?
MR. HRYCYSZYN: So --
THE WITNESS: Yes. Now that I understand --
MR. HRYCYSZYN: Can we wait so I can get my objections on the record. So same set of objections we had earlier. I can restate them or if we can agree they apply here.
So Josh is reminding me that I should restate them. So objection, coaching the witness. Objection, leading. Objection, coaching and instructing the witness.
THE WITNESS: Yes. I do want to clarify. Now that I understand the legal issue, Claim 1 does not require that -- it does not have any language in it that requires the film to have stress, as I said before. And what that means legally is that it's not required in meeting the limitations of Claim 1.
MR. HRYCYSZYN: Objection, move to strike.

Shanfield Reply Depo., Ex. 2026 at 167:14-21; 170:11-172:16 (cited Paper No. 35 at 11, 13)

Q. So the information that Mr. Smith provided you during his redirect questioning changed your testimony; is that accurate?
A. No.
Q. So it didn't change --
A. It changed what I knew about the relation between dependent and independent claims. And that has -- As I said, that was not related to my

Shanfield Reply Depo., Ex. 2026 at 175:17-24 (cited Paper No. 35 at 2)

Q. So before Mr. Smith instructed you on certain legal principles, you had testified that Claim 1 required that the silicon nitride film induced stress, right?
A. I mistakenly made that statement because I thought legally that there was a legal requirement that the independent -- the dependent claims read back into the independent claim the limitations in the dependent claims.
Since, I've heard that the dependent claims are usually narrower. That was a mistake. So that particular statement, I changed. It's a legal opinion.

Shanfield Reply Depo., Ex. 2026 at 176:4-16 (cited Paper No. 35 at 2)

Patent Owner Did Not Waive Its Objections

Q. I'm going to represent to you that as a legal matter, a dependent claim recites additional limitations that are not present in the independent claim from which it depends.

Do you have that understanding in mind?

MR. HRYCYSZYN: Objection, beyond the scope. Objection, coaching.

THE WITNESS: Okay. I didn't know that.

MR. HRYCYSZYN: Objection, leading.

BY MR. SMITH:

Q. With that understanding in mind, does Claim 1 -- or sorry -- does Claim 2 require -- or recite a stress limitation?

MR. HRYCYSZYN: So objection --

THE WITNESS: It says --

MR. HRYCYSZYN: Hold on before you answer. We're getting into a situation where you're very clearly teaching legal principles and coaching on the record. I think it's highly improper. We're in a position where I feel like we shouldn't allow the witness to answer, and we're probably in a position where we need to talk to the board.

MR. SMITH: We think the question is proper. We think you can lodge your objection, raise it with the board. And if they --

MR. HRYCYSZYN: Well, that's not the way it works. So generally you're supposed to call the board at the time. So we're not supposed to wait till some later time and, you know, file some later paper. I mean, it is the kind of thing where you're supposed to reach out to the board if you have an issue. And I think this is pretty clearly improper coaching.

MR. SMITH: I obviously disagree. I think that the witness should be allowed to answer it. If you want to raise the issue with the board, you're welcome to do that.

MR. HRYCYSZYN: Unfortunately, I think I am obligated to reach out to the board now. Honestly, I'm not trying to be difficult. I don't think I have a choice. So if you want to go forward with this question, I think I have to go to the board.

MR. SMITH: I do want to go forward with the question.

MR. HRYCYSZYN: So let's get on a call with the board.

(Recess at 7:29 p.m., resumed at 7:33 p.m.)

MR. HRYCYSZYN: So are we back on the record.

So just for the record, patent owner did attempt to call the board for an attempt to resolve the dispute between the parties as to whether or not this line of questioning is proper.

We want to make sure that on the record, we all agree that there is no waiver, to him answering your question, by patent owner.

MR. SMITH: We understand you raised the objection, and you have the ability to use the remedies that are available based on -- to seek the remedy based on the remedies that are available when you object.

MR. HRYCYSZYN: And you agree that by allowing him to answer your -- or by not stopping him from answering your question, that does not constitute some sort of a waiver?

MR. SMITH: I can agree with that.

PATENT OWNER DEMONSTRATIVE EXHIBIT Shanfield Reply Depo., Ex. 2026 at 167:14-170:9 (cited Paper No. 35 at 2)

Dr. Glew Interpreted "wherein the MISFET includes: an active region"

10-13. PO does not dispute this. Sur-reply, 1-3. Likewise, Dr. Glew backed away from his prior testimony and testified he had no opinion on the term "active region." *Compare* Ex. 2007, ¶¶62-85, 148-149 *with* Ex. 1029, 46:1-47:6.

Petitioner's Sur-Sur-Reply, Paper No.33, at 1

A. "wherein the MISFET includes: an active region made of a semiconductor substrate" (claim 1)

61. Claim 1 recites "wherein the MISFET includes: an active region made of a semiconductor substrate."

62. As explained below in ¶¶ 63-85, I understand that the parties agree that under BRI, "an active region made of a semiconductor substrate" is "an area of the semiconductor substrate defined by an isolation region where the transistor is formed." I agree with the parties that this is the proper BRI of that claim limitation for the reasons detailed below.

1. The Petitions and Petitioner's Expert Consistently Characterize the Active Region as an Area of the Semiconductor Substrate Defined by an Isolation Region Where the Transistor Is Formed

63. I have reviewed the Petitions and Dr. Shanfield's declarations and deposition testimony. Although Petitioner and Dr. Shanfield have not offered an explicit interpretation of "wherein the MISFET includes: an active region," both Petitioner and Dr. Shanfield have repeatedly and consistently characterized the active region as an area of the semiconductor substrate defined by an isolation region where the transistor is formed.

Glew Decl., Ex.2007, ¶¶ 61-63

Q. And now that you've reviewed Dr. Shanfield's reply declaration, I want to understand if you have an opinion on whether the phrase "an active region made of a semiconductor substrate" requires a one-to-one correspondence with a MISFET?

MR. MILLER: Objection. Scope.

A. As I cite in my three-page sur-reply, which are the opinions that I've analyzed and presented, I note, for example, in Paragraph 10, I use the phrase "the 'MISFET includes: an active region'." So I've opined on that phrase.

I do not recall opining on the phrase "an active region made of a semiconductor substrate without the MISFET includes," as part of it.

So if could direct me to where I've opined on just an active region made of a semiconductor substrate requiring a one-to-one correspondence, I'd be happy to explain it further, but I don't think I did that.

Q. Sitting here today, you don't have an opinion on whether the phrase "an active region made of a semiconductor substrate requires a one-to-one correspondence with a MISFET," correct?

MR. MILLER: Objection. Scope.

A. I haven't been asked to analyze that with respect to that question. So I haven't formed an opinion on that.

Glew Sur-Reply Depo., Ex. 1029 46:1-47:6

Dr. Glew Interpreted "wherein the MISFET includes: an active region"

(Justices confer off the record)

THE COURT: So in general, we agree with Patent Owner that this should be a pretty limited declaration. The declaration is only three pages directed specifically to be used to references that were submitted with Petitioner's reply, Exhibits 1025 and 1026.

So going forward in this deposition, the questions need to be limited to those references or to specific testimony in Dr. Glew's sur-reply declaration.

Ex. 2025 at 16:13-24

Dr. Glew's Testimony Regarding "Includes"

First, PO's argument that the Reply mischaracterized Dr. Glew's testimony fails. Sur-reply, 2. It did not. *Compare* Reply, 20-21 *with* Ex. 1024 at 94:13-95:7. Dr. Glew confirms that he stands by his testimony that "includes" is an open-ended term like comprises. Ex. 1029, 93:15-22; Ex. 1024 at 94:13-95:7. The term "includes" does not prevent the MISFET from including other features or prevent other MISFETS from being formed in the same active region. Moreover, PO's

Petitioner Sur-Sur-Reply, Paper No.33 at 1-2

15 Q. In Paragraph 10 of your
16 declaration you reference your prior deposition
17 testimony from Page 94, Line 13 to 95, Line 7.
18 Do you see that?
19 A. Yes.
20 Q. Do you stand by that prior
21 testimony?
22 A. Yes.

Glew Sur-Reply Depo., Ex. 1029, 93:15-22

13 Q. Could you take a look at Claim 1.
14 From your work on patent cases, are you
15 familiar with the meaning of the word
16 "comprise" in the context of patent claims?
17 A. Generally I have been instructed
18 that it means includes but not limited to,
19 something along those lines.
20 Q. And similarly, from your work on
21 patent cases, do you have an understanding of
22 what the term "includes" means in the context
23 of patent claims?
24 A. My general -- the general
25 instruction I received in patent cases is that
1 "includes" means that it has at least these
2 features.
3 Q. Are those the understandings you
4 applied in your analysis in this case?
5 A. The standard that I applied for
6 includes would essentially, yes, that it has at
7 least these elements.

Glew Opening Depo., Ex. 1024, at 94:13-95:7

c. No Transistor Includes the Region Bounded by the Alleged Isolation Region in the Petitions' Modified Igarashi Fig. 12, So There Is Not One Active Region

142. All challenged claims require that "the MISFET ***includes***: an active region." Thus, the plain language and structure of the claims require that it is the MISFET that is the larger whole that "includes" the entirety of the active region and not the other way around. That is, the claims recite the MISFET as including the active region; they do not recite the active region as a larger whole that includes the MISFET. This is consistent with the plain meaning of "include," which is used to reference a larger whole that "contain[s]" a smaller component. *See, e.g.*, Ex.-2011 (Webster's Third New International Dictionary) at 1143 ("include" means "to place, list, or rate as a part or component of a whole or of a larger group, class, or aggregate" or "to take in, enfold, or comprise as a discrete or subordinate part or item of a larger aggregate, group, or principle"); Ex.-2012 (Collins English Dictionary) at 780 ("include" means "to have as contents or part of the contents; be made up of or contain"); Ex.-2013 (Chambers 21st Century Dictionary) at 684 ("include" means "to contain or be made up of something, or to have it as parts of its contents").

143. Thus, a MISFET's active region does not include areas of the substrate where components of a different transistor are formed. Such an

Glew Decl., Ex. 2007, ¶¶ 142-143 (cited POR 67-68)

"That the active region of a multi-transistor device … has multiple transistors does not support … that any of those transistors "includes" the device's active region." Sur-Reply at 2-3.

Dr. Glew was also unable to say whether the device in Igarashi's Fig. 12 "includes" an active region, demonstrating that his attempts to distinguish Agata and Rashed are not credible. Ex. 1029, 62:5-63:9. Dr. Glew's answers on cross

Petitioner's Sur-Sur-Reply, Paper No. 33, at 2

1. A semiconductor device, comprising a MISFET, wherein

the MISFET includes:

an active region made of a semiconductor substrate;

a gate insulating film formed on the active region;

a gate electrode formed on the gate insulating film;

source/drain regions formed in regions of the active region located on both sides of the gate electrode; and

a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein:

the silicon nitride film is not formed on an upper surface of the gate electrode, and

the gate electrode protrudes upward from a surface level of parts of the silicon nitride film located at both side surfaces of the gate electrode.

'501 patent at Claim 1

Q. Sitting here today, you don't have an opinion one way or the other as to whether a person of skill in the art looking at the multi-transistor device shown in Figure 12 of Igarashi would understand that the multi-transistor device includes an active region?

MR. MILLER: Objection form. Objection scope.

A. I haven't developed any further opinions outside of the two declarations, the initial declaration and the sur-reply. I don't recall opining -- I recall opining on MISFET. I do not recall opining on multi-transistor device.

Q. Sitting here today, you don't have an opinion with regard to the multi-transistor device in Igarashi's Figure 12 as to whether it includes an active region?

MR. MILLER: Objection form. Objection scope.

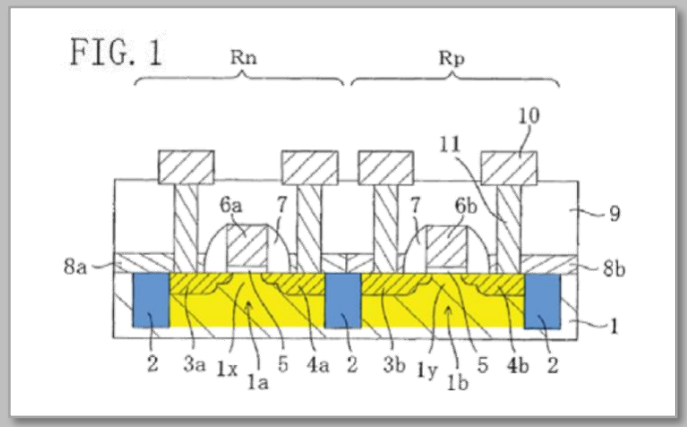
A. I don't recall analyzing it for a multi-transistor device. I analyzed it for a MISFET having an active region made of a semiconductor substrate. To the extent you can refer me to somewhere in my previous declaration where I opined on that, I'd be happy to look at it, but I don't recall opining on that previously. I haven't developed any further opinions on that.

Glew Sur-Reply Depo., Ex. 1029, 62:5-63:9

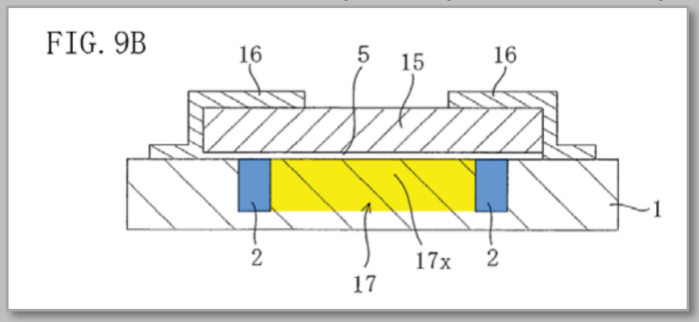
Petitioner's "hypothetical" "doesn't make physical sense"
(Ex. 1029 at 66:17-67:3, cited in paper 33 at 3)

Third, Dr. Glew's testimony confirms PO's position "doesn't make physical sense." When asked whether, under his interpretation, the active region of claim 1 could be divided by isolation regions (as recited in claim 10), Dr. Glew testified that "it doesn't make physical sense." Ex. 1029, 66:23-67:3; Ex. 1001, claim 10.

Petitioner's Sur-Sur-Reply, Paper No. 33, at 3



Glew Decl., Ex. 2007, ¶ 69, Annotated Fig.1 of '501 patent (cited POR at 9)



Glew Decl., Ex. 2007 ¶ 69, Annotated Fig.9B of '501 patent (cited POR at 9)

17 Q. I would like to focus on the
18 active region that the MISFET includes that's
19 bounded and defined by the isolation regions.
20 Do you have that in mind?
21 A. To what extent I can, yes, if
22 you're starting a hypothetical.
23 Q. Could a person of skill in the art
24 form an isolation region that divides the
25 active region that's included in the MISFET?
1 MR. MILLER: Objection.
2 A. It's nothing I've opined on. It
3 doesn't make physical sense to me.

Glew Sur-Reply Depo., Ex. 1029, 66:17-67:3

"An "active region" … is "an area of the semiconductor substrate defined by an isolation region where the transistor is formed"" (POR 26)

active region. When asked what components are in an active region, Dr. Glew testified that it "would include, at least… the source channel and drain regions for a typical transistor." Ex. 1029, 70:5-12. There is *no dispute* that Igarashi's identified "active region" includes these same components. *See e.g.,* Petition, 16-17, 23, 39-41, *citing* Ex. 1002, ¶¶47-48, 88-90, Ex. 1004, Fig. 12, [0044], [0068].

Petitioner's Sur-Sur-Reply, Paper No. 33 at 3

Shanfield Reply Depo., Ex. 2026 at 84:18-85:5 (cited Paper No. 34, Observation No. 4)

Q. So let's go back to the sentence you had in paragraph 19. And is this still your opinion that "The absence of an isolation region does not signify the absence of an active region"?
A. Yes.
Q. So that means you can have an active region without an isolation region, right?
A. Yes.
Q. And that means you can have a transistor without an isolation region?
A. Yes. Although as I've explained, it isn't really relevant to the '501 technology.

Glew Sur-Reply, Ex. 2024, at ¶ 9 (cited in Paper No. 28 at 3)

9. Dr. Shanfield's assertion that "all functional MOSFET transistors have an active region" is unsupported and wrong—an area not defined by isolation is ***not*** an active region. *See* Ex. 2007 at VII.A, VIII.C.1.b. All transistors must have a region in the substrate where they are formed, but as the '501 patent makes clear this is a "formation region." Ex. 1001 at 3:20-28, Fig. 1.

Q. Do you agree that isolation regions define an active region?
A. I think we already discussed the point that there are transistors, exceptional circumstances in the year 2003, that don't have isolation regions. So they still have active regions. So I wouldn't -- I don't take that as "define" in the hard sense of the word.
Q. So let me back up. Earlier when I had asked you about this understanding that an active region made of a semiconductor substrate is an area of the semiconductor substrate defined by an isolation region where the transistor is formed, you said that that was a statement, a description of what a person of skill in the art would understand, but not necessarily a construction?
Am I getting that right?
A. Yes.
Q. So a person of ordinary skill in the art would understand the term to mean that: that it's not necessarily the case that you were offering that as a construction; is that right?
A. I withdraw the statement that it's not a construction. It's actually, now that I think about it further, a proposed construction.
And I was being careful in explaining what I meant because I was not comfortable with the interpretation of what was a proposed construction. But it's a proposed construction appropriate to the '501 patent.
Q. In your proposed construction for the '501 patent?
A. That's correct.
Q. And just so we're clear, so it is your proposed construction for the '501 patent that an active region made of a semiconductor substrate is an area of the semiconductor substrate defined by an isolation region where the transistor is formed?
A. Correct.

Shanfield Reply Depo., Ex. 2026, at 95:4-96:18 (cited Paper No. 34, Observation No. 4)

"An "active region" … is "an area of the semiconductor substrate defined by an isolation region where the transistor is formed"" (POR 26)

Fifth, PO's attempt to rebut Dr. Shanfield's showing that "all functional MOSFET transistors have an active region" fails. PO has not identified a single reference that describes a MISFET as *not* including an active region—because *all* functional transistors include an active region. E.g., Reply, 10-11; Pet. 7-13.

Petitioner's Sur-Sur-Reply, Paper No. 33, at 3

Shanfield Reply Depo., Ex. 2026 at 84:18-85:5 (cited Paper No. 34, Observation No. 4)

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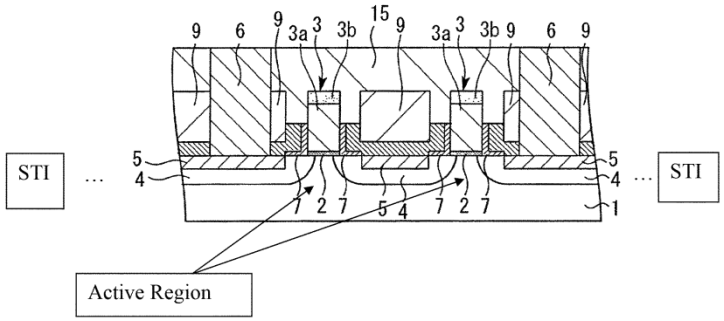
A. Correct.

Shanfield Reply Depo., Ex. 2026, at 95:4-96:18 (cited Paper No. 34, Observation No. 4)

Fig. 12



(Igarashi at Fig. 12 (Ex-1004) (annotated).) (Shanfield Decl. ¶66 (Ex-1002).)

To the extent that Igarashi does not explicitly disclose the location of the "active element region" and therefore that the active region is "made of" the semiconductor substrate, Woerlee discloses this limitation. (Shanfield Decl. ¶67 (Ex-1002).) For example, Woerlee discloses an active region 4 "made of" the semiconductor body 1 in Fig. 13:

Petition at 27

Ex. 1004 ¶ 35. Petitioner relies on Igarashi's silicon semiconductor substrate 1, gate oxide film 2 (red), gate electrode 3 (orange), impurity diffusion layers 4 and silicide film 5 of the source/drain (green), and silicon nitride film 8 (blue), respectively, as teaching the claimed semiconductor substrate, gate insulating film, gate electrode, source/drain regions, and silicon nitride film. Pet. 16–17, 22–25, 37–42; Ex. 1002 ¶¶ 47–48, 60, 65, 82–92.

Claim 1 further recites "an active region made of a semiconductor substrate." Petitioner argues that a person of ordinary skill in the art "would have understood that Igarashi discloses an active region made of the semiconductor substrate 1" (Pet. 25), based on at least the following disclosure of Igarashi:

> First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value.

Ex. 1004 ¶ 68 (emphasis Petitioner's); *see* Pet. 25–27 (arguing that the "use of the 'trench method' confirms the 'active element region' (active region) is made of the semiconductor substrate 1 because according to the trench method the active region is formed in the substrate and defined by the STI regions"); Ex. 1002 ¶ 66.

Petitioner further relies on Woerlee as providing explicit disclosure of the location of the active region within the semiconductor substrate. Pet. 27–28; Ex. 1002 ¶¶ 67–68. Petitioner asserts that active region 4 of Woerlee is "made of" semiconductor body 1, as required by claim 1. Pet. 29 (citing Ex. 1006, 4:66–5:5 (disclosing "field insulating regions 3, which are

Institution Decision, Paper No. 10, at 15

“Petitions Fail to Demonstrate that the Igarashi/Woerlee Device Comprises a MISFET that Includes an ‘Active Region’ as Required by All Challenged claims.”

1. A semiconductor device, comprising a MISFET, wherein

the MISFET includes:

an active region made of a semiconductor substrate;

a gate insulating film formed on the active region;

a gate electrode formed on the gate insulating film;

source/drain regions formed in regions of the active region located on both sides of the gate electrode; and

a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein:

the silicon nitride film is not formed on an upper surface of the gate electrode, and

the gate electrode protrudes upward from a surface level of parts of the silicon nitride film located at both side surfaces of the gate electrode.

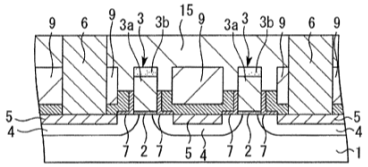
’501 patent at Claim 1

b) Claim 1 – Active Region (element [1a])

Claim 1 recites “an active region made of a semiconductor substrate.” (’501 patent, claim 1 (Ex-1001).) Igarashi in view of Woerlee discloses this limitation. (Shanfield Decl. ¶64 (Ex-1002).)

For example, Igarashi discloses a “semiconductor substrate 1,” as illustrated in Fig. 12:

Fig. 12



(Igarashi at Fig. 12 (Ex-1004); *see also, e.g.*, *id.* at [0044]-[0045], [0112] (discussing the “semiconductor substrate 1”).) (Shanfield Decl. ¶65 (Ex-1002).)

A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: “First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value.” (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an “active region made

Petition at 24, 25

regions) in Woerlee are formed in regions of the active region 4 located on both sides of the gate electrode 21 (as recited in claim 1, element 1d below). The modified device would also have an active element region (active region) divided by the STI regions (isolation region) formed in the semiconductor substrate 1 (as recited in claim 10 below), just as the active region 4 is divided by an isolation region 3 formed in the semiconductor substrate 1 in Woerlee. (Shanfield Decl. ¶73 (Ex-1002).)

Therefore, Igarashi in view of Woerlee discloses “an active region made of a semiconductor substrate.” (Shanfield Decl. ¶74 (Ex-1002).)

c) Claim 1 – Active Region (element [1a]) – Reasons to Modify

It would have been obvious to modify Igarashi in view of Woerlee’s teachings of an active region “made of” a semiconductor substrate (recited in claim 1, element 1a) and an active region divided by an isolation region formed in the semiconductor substrate (recited in claim 10 below). In particular, it would have been obvious to apply Woerlee’s teachings to Igarashi by forming Igarashi’s active region in the substrate and defining it with STI regions that divide the active region. (Shanfield Decl. ¶75 (Ex-1002).)

First, a POSITA would have looked to the teachings of Woerlee because it is in the same field of endeavor as Igarashi. Igarashi discloses a MISFET device with a “silicon semiconductor substrate 1” where “[e]lement isolation is performed” to

32

Petition at 32

Shanfield Repeats Portions of the Petitions Verbatim (POR at 42-43)

The only other evidence the Petitions cite in the paragraph that sets forth Petitioner's rationale for how the claimed "active region" is met by Igarashi is paragraph 66 from Shanfield's -1841 declaration and paragraph 67 from Shanfield's -1842 declaration. Petition at 24-25. In these paragraphs, Shanfield repeats the Petitions ***verbatim***, combining in one paragraph the above-reproduced paragraph spanning pages 25-26 of the -1841-Petition and pages 24-25 of the -1842-Petition, as well as the Petitions' following paragraph and figure. *Compare* -1841-Petition at 25-27, *with* Ex.-1002, ¶ 66; *compare* -1842-Petition at 24-26, *with* Ex.-1102, ¶ 67. Thus, Shanfield's testimony on this issue is entitled to little if any weight. *Smith & Nephew, Inc. v. Arthrex, Inc.*, IPR2016-00918, Paper No. 42 at 78 (PTAB Oct. 16, 2017) ("[Petitioner's expert] merely repeats Petitioner's argument without any additional facts or data on which the opinion is based. Thus, it is entitled to little if any probative weight. 37 C.F.R. 42.65(a).").

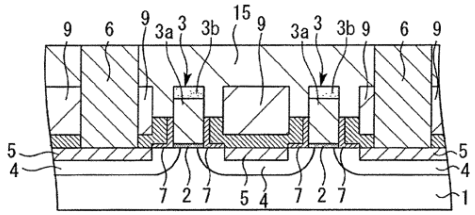
POR at 42-43

"Petitioner changed its theory of unpatentability based on a new argument that it would have been obvious to modify Igarashi's Fifth Embodiment to add isolation regions … in view of Woerlee" (Paper No. 27 at 1)

Claim 1 recites "an active region made of a semiconductor substrate." ('501 patent, claim 1 (Ex-1001).) Igarashi in view of Woerlee discloses this limitation. (Shanfield Decl. ¶64 (Ex-1002).)

For example, Igarashi discloses a "semiconductor substrate 1," as illustrated in Fig. 12:

Fig. 12



(Igarashi at Fig. 12 (Ex-1004); *see also, e.g., id.* at [0044]-[0045], [0112] (discussing the "semiconductor substrate 1").) (Shanfield Decl. ¶65 (Ex-1002).)

A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made

Moreover, the Petition showed that Igarashi's isolation region teachings were applicable to its Figure 12 embodiment. Specifically, the Petition cites Figure 12, which shows the "semiconductor substrate 1." Petition, 25. Then, the Petition explains that a POSITA would have understood that the semiconductor substrate 1 in Fig. 12 has an active region because Igarashi expressly discloses an "active element region" made of the semiconductor substrate 1. Petition 25-26, *citing* Ex. 1004, [0068]; Ex. 1002, ¶66; Ex. 1010, 42-43. Ex. 1027, ¶27.

Accordingly, both the Petition and Dr. Shanfield's testimony have been clear and consistent throughout this proceeding: Igarashi discloses the "active region" of the challenged claims in connection with its Fifth Embodiment. Moreover, as discussed below in Section III.D, the Petition also demonstrated it would have been obvious to form the active region disclosed in Igarashi in semiconductor substrate 1 of Igarshi's Fifth Embodiment in view of the teachings of Woerlee. Ex. 1027, ¶28.

B. Igarashi Discloses a MISFET that Includes an "Active Region"

A person of ordinary skill would have viewed the region between the two STI in Igarashi where the two transistors are formed as an "active region" formed between those two STI. As noted in the Petition: "The use of the 'trench method' confirms the 'active element region' (active region) is made of the semiconductor substrate 1 because according to the trench method the active region is formed in

Petition at 25

Reply, Paper No. 22, at 19

1. A semiconductor device, comprising a MISFET, wherein

the MISFET includes:

an active region made of a semiconductor substrate;

a gate insulating film formed on the active region;

a gate electrode formed on the gate insulating film;

source/drain regions formed in regions of the active region located on both sides of the gate electrode; and

a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein:

the silicon nitride film is not formed on an upper surface of the gate electrode, and

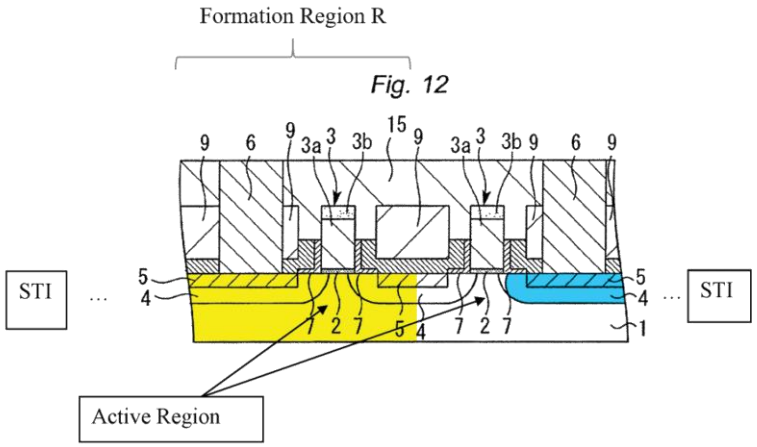
the gate electrode protrudes upward from a surface level of parts of the silicon nitride film located at both side surfaces of the gate electrode.

'501 patent at Claim 1

Mapping the agreed-upon BRI of "active region" and claim 1's requirement that "the MISFET includes: an active region" onto the prior art structure the Petitions allege meets the claimed "active region" is the furthest thing from irrelevant. *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (affirming final written decision upholding patentability where Petitioner offered merely "conclusory" discussion of the prior art and failed to explain with particularity how the limitations were disclosed); *Kranos Corp. v. Riddell, Inc.*, IPR2016-01649, Paper No. 25 at 29, 36, 39-42 (PTAB Feb. 7, 2018) (Petitioner failed to meet its burden where "it is unclear from Petitioner's argument where each element of [the challenged claims] is found in" the prior art and the Board "decline[d] to speculate as to Petitioner's intentions").

POR at 20

In the Petitions' modified-Igarashi Fig. 12 the entire region of the substrate bounded by the alleged isolation region is not the formation region for ***any*** MISFET. Ex.-2007, ¶145. Taking the left MISFET as an example, the transistor is formed in the region in yellow below. *Id.* There are other regions of the substrate bounded by the alleged isolation region, e.g., the area in blue, that are unquestionably ***not*** part of the region (yellow below) where the left MISFET is formed. *Id.*



Neither of the MISFETs shown in the Petitions' modified-Igarashi Fig. 12 is formed in and includes the entire region of the substrate bounded by the isolation region, so the region bounded by the isolation region is not an "active region" of either MISFET. Ex.-2007, ¶146. Thus, there is not one "active region" that meets

POR at 69

The Petition Fails To Identify a 'MISFET Includes: An Active Region' As Claimed

1. A semiconductor device, comprising a MISFET, wherein

the MISFET includes:

an active region made of a semiconductor substrate;

a gate insulating film formed on the active region;

a gate electrode formed on the gate insulating film;

source/drain regions formed in regions of the active region located on both sides of the gate electrode; and

a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein:

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'501 patent at Claim 1

b) Claim 1 – Active Region (element [1a])

Claim 1 recites "an active region made of a semiconductor substrate." ('501 patent, claim 1 (Ex-1001).) Igarashi in view of Woerlee discloses this limitation. (Shanfield Decl. ¶64 (Ex-1002).)

For example, Igarashi discloses a "semiconductor substrate 1," as illustrated in Fig. 12:

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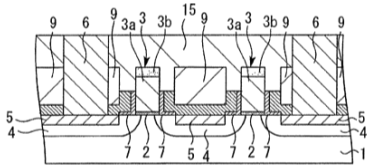

(Igarashi at Fig. 12 (Ex-1004); *see also, e.g., id.* at [0044]-[0045], [0112] (discussing the "semiconductor substrate 1").) (Shanfield Decl. ¶65 (Ex-1002).)

A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made

Petition at 24, 25

regions) in Woerlee are formed in regions of the active region 4 located on both sides of the gate electrode 21 (as recited in claim 1, element 1d below). The modified device would also have an active element region (active region) divided by the STI regions (isolation region) formed in the semiconductor substrate 1 (as recited in claim 10 below), just as the active region 4 is divided by an isolation region 3 formed in the semiconductor substrate 1 in Woerlee. (Shanfield Decl. ¶73 (Ex-1002).)

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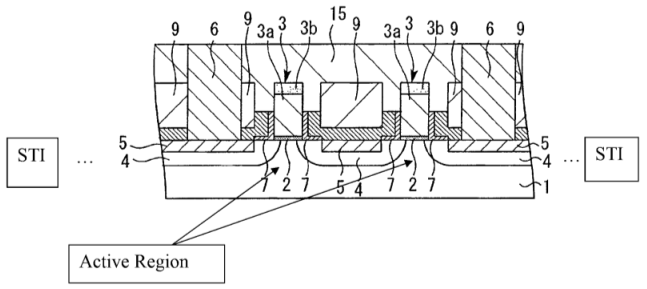
Petition at 32

Fig. 12



(Igarashi at Fig. 12 (Ex-1004) (annotated).) (Shanfield Decl. ¶66 (Ex-1002).)

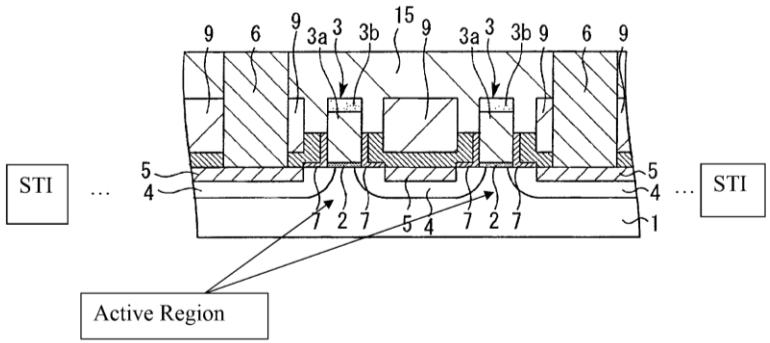
Petition at 27

the substrate and defined by the STI regions. Petition, 25-26, *citing* Ex, 1010, 42-43 (explaining that the manufacturing process for a MISFET "starts with the definition of the active regions—these are the regions where transistors will be constructed. All other areas of the die will be covered with a thick layer of silicon dioxide (SiO2) called the field oxide. This oxide acts as the insulator between neighboring devices, and it is either grown (as in the process of Figure 2-1) or deposited in etched trenches (Figure 2-2)—hence, the name trench insulation.") As discussed in Section II above with respect to Agata and Rashed (and PO's district court infringement contentions), it is visibly clear that Igarashi discloses the claimed "active region" of the '501 patent. Ex. 1027, ¶29.

As discussed below, Dr. Shanfield was asked during his deposition whether this active region would be considered one active region or two active regions. Under either view, Igarashi's disclosure meets the claim limitations because the MISFETs in either case include an active region bounded by STI. Under the first, each MISFET includes an active region because each transistor is formed in the active region between the STI. There is nothing that precludes multiple transistors from being formed in the active region, nor does the claim require that each transistor have its own active region that is separated from other active regions by isolation regions. *See* Section II, above; Ex. 1025. Indeed, Dr. Glew admitted that

Reply, Paper No. 22, at 20

Fig. 12



(Igarashi at Fig. 12 (Ex-1004) (annotated).) (Shanfield Decl. ¶66 (Ex-1002).)

Petition at 27

Petitioner's cursory and conclusory "argument," that the area "between the two STI in Igarashi [modified Fig. 12]" includes multiple "active regions" (one per transistor) … is new. (Paper No. 27 at 2)

Claim 1 recites "an active region made of a semiconductor substrate." ('501 patent, claim 1 (Ex-1001).) Igarashi in view of Woerlee discloses this limitation. (Shanfield Decl. ¶64 (Ex-1002).)

For example, Igarashi discloses a "semiconductor substrate 1," as illustrated in Fig. 12:

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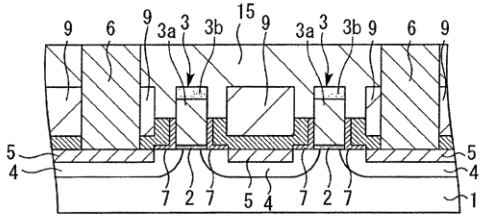


(Igarashi at Fig. 12 (Ex-1004); *see also, e.g., id.* at [0044]-[0045], [0112] (discussing the "semiconductor substrate 1").) (Shanfield Decl. ¶65 (Ex-1002).)

A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made

of the semiconductor substrate" both because it explicitly discloses a "active element region" and because it discloses using the "trench method" for "element isolation," meaning the trench method is used to form shallow trench isolation (STI) regions that define the active region where the transistor is formed. (Shanfield Decl. ¶66 (Ex-1002).)

The use of the "trench method" confirms the "active element region" (active region) is made of the semiconductor substrate 1 because according to the trench method the active region is formed in the substrate and defined by the STI regions.[5] (*E.g.*, Rabaey at 42-43 (explaining that the manufacturing process for a MISFET "starts with the definition of the *active regions*—these are the regions where transistors will be constructed. All other areas of the die will be covered with a thick layer of silicon dioxide (SiO_2) called the *field oxide*. This oxide acts as the insulator between neighboring devices, and it is either grown (as in the process of Figure 2-1) or deposited in etched trenches (Figure 2-2)—hence, the name *trench insulation*.") (Ex-1010).) This is illustrated below in annotated Figure 12 of Igarashi:

[5] Because claim 10, which depends from claim 1, recites "the active region is divided by an isolation region formed in the semiconductor substrate," claim 1 must be interpreted to allow for isolation regions because claim 10 must be narrower than claim 1.

Petition at 25, 26

Petitioner's Improper New Arguments

2. Reply, p. 3, ll. 2-7, p. 14, l. 10, p. 26 ll. 4-7, p. 28, ll. 3-11; Ex. 1027, p. 4, ll. 2-3, p. 21, ll. 6-9, p. 27, l. 4 to p. 28, l. 8, 29, ll.1-9: Petitioner ***changed its theory of unpatentability*** based on a new argument that it would have been obvious to ***modify*** Igarashi's Fifth Embodiment to ***add*** isolation regions and form an active region in view of Woerlee whereas the Petition relied on Woerlee only to teach locating in the substrate the ***isolation/active regions allegedly taught by Igarashi***. Pet. at 27 ("To the extent that Igarashi does not explicitly disclose ***the location*** of the 'active element region' … Woerlee discloses this limitation."), *id.* at 31 ("***By locating Igarashi's*** active [] region … according to … Woerlee.")).

3. Reply, p. 14, ll. 1-3; Ex. 1027, p. 15, ll. 4-6: ***New argument*** that transistors without isolation regions have an active region. *Compare* Pet. at 33 ("***isolation regions*** that define … the active regions ***are required in all transistor devices***.").

Paper No. 27, Patent Owner's Identification of Improper New Arguments, at 1

region as claimed." POPR, 4, 32. Put differently, PO's argument is that the Petition relies on Woerlee only for the *location* of the active region, not the existence of the active region, and that there is no active region disclosed in connection with Figure 12 of Igarashi. As the Board recognized, the Petition expressly shows that it would have been obvious to a person of ordinary skill in the art apply Igarashi's teaching of an active region to Igarashi's Fifth Embodiment in view of Woerlee. DI, 16 (quoting Petition, 32) ("Petitioner also provides several reasons why a person of ordinary skill in the art would have 'appl[ied] Woerlee's teachings to Igarashi by forming Igarsahi's active region in the substrate and defining it with STI regions that divide the active region.'") Yet, PO resurrects

Reply, Paper No. 22, at 26

Petitioner further relies on Woerlee as providing explicit disclosure of the location of the active region within the semiconductor substrate. Pet. 27–28; Ex. 1002 ¶¶ 67–68. Petitioner asserts that active region 4 of Woerlee is "made of" semiconductor body 1, as required by claim 1. Pet. 29 (citing Ex. 1006, 4:66–5:5 (disclosing "field insulating regions 3, which are at least partly recessed in the semiconductor body 1 and which define an active region 4 in which a transistor . . . is to be manufactured"), 2:61–64 (disclosing "an oxide field insulating region, which is provided at the surface of the semiconductor body to separate active regions in the semiconductor body")); *see id.* at 29–31; Ex. 1002 ¶¶ 69–71. According to Petitioner, "Woerlee would . . . have provided a [person of ordinary skill in the art] additional detail on how to use the trench method disclosed in Igarashi to form Igarashi's active element region (active region) in the semiconductor substrate 1." Pet. 31; *see id.* at 31–32; Ex. 1002 ¶¶ 72–74.

Institution Decision, Paper No. 10, at 15-16

To the extent that Igarashi does not explicitly disclose the location of the "active element region" and therefore that the active region is "made of" the semiconductor substrate, Woerlee discloses this limitation. (Shanfield Decl. ¶67 (Ex-1002).) For example, Woerlee discloses an active region 4 "made of" the semiconductor body 1 in Fig. 13:

Petition at 27

By locating Igarashi's active element region (active region) in the semiconductor substrate 1 according to the teaching of Woerlee, in the modified device, Igarashi's gate oxide film 2 (gate insulating film) would have been formed on the active element region (active region), just as Woerlee's gate dielectric 24 (gate insulating film) is formed on the active region 4 (as recited in claim 1, element 1b below). Likewise, in the modified device, Igarashi's impurity

Petition at 31

Petitioner's Improper New Arguments

1. Reply, p. 3 ll. 2-4; Ex. 1027, p. 4, ll. 2-3: Petitioner ***changed its theory of unpatentability*** based on a new argument that it would have been obvious to ***modify*** Igarashi's Fifth Embodiment to ***add*** isolation regions in view of Igarashi's disclosure of isolation regions in its First Embodiment, which changes the Petition's argument that Igarashi ***discloses*** that its Fifth Embodiment already has isolation regions. Pet. at 22 ("[T]he ***disclosure of the features in Igarashi*** common to different illustrations ***are applicable to*** … ***Figure 12***."), 25-26 (similar).

Paper No. 27, Patent Owner's Identification of Improper New Arguments, at 1

numerals are used to describe common features of Igarashi's disclosure.")
Moreover, the Petition is clear that it would have been obvious to apply Igarashi's undisputed teaching of an active region to the Fifth Embodiment. DI, 16 (quoting Petition, 32) ("Petitioner also provides several reasons why a person of ordinary skill in the art would have 'appl[ied] Woerlee's teachings to Igarashi by forming Igarsahi's active region in the substrate and defining it with STI regions that divide the active region.'")

Reply, Paper No. 22, at 3

Claim 1 further recites "an active region made of a semiconductor substrate." Petitioner argues that a person of ordinary skill in the art "would have understood that Igarashi discloses an active region made of the semiconductor substrate 1" (Pet. 25), based on at least the following disclosure of Igarashi:

> First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value.

Institution Decision, Paper No. 10, at 15

Based on the current record, however, we find it is clear from Igarashi that the disclosure of "active element region[s]" discussed in paragraph 68 with respect to the "First Embodiment" is equally applicable to the "Fifth Embodiment" upon which Petitioner primarily relies. For example, the

Institution Decision, Paper No. 10, at 19

A POSITA would have understood that Igarashi discloses an active region made of the semiconductor substrate 1 because Igarashi discloses: "First, an insulating film for isolating elements is formed on **a silicon semiconductor substrate 1**. Element isolation is performed using methods such as the LOCOS method or the **trench method**. Thereafter, ion implantation is performed to the **active element region** for forming the well and controlling the threshold value." (Igarashi at [0068] (Ex-1004).) That is, Igarashi discloses an "active region made of the semiconductor substrate" both because it explicitly discloses a "active element region" and because it discloses using the "trench method" for "element isolation," meaning the trench method is used to form shallow trench isolation (STI) regions that define the active region where the transistor is formed. (Shanfield Decl. ¶66 (Ex-1002).)

Petition at 25-26

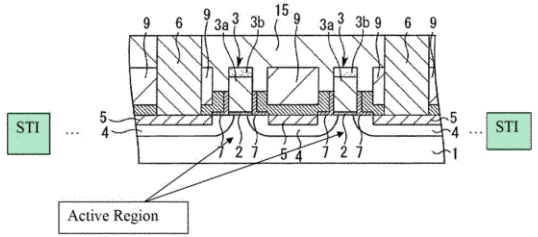
Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

a. Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions

The Petitions rely upon Igarashi's Fifth Embodiment (Fig. 12) in all grounds in these proceedings. Petition at 22-24 (claim chart citations to Fig. 12), 25-27, 37-46 (illustrating the alleged Igarashi/Woerlee combination as including STI regions added to Igarashi's Fig. 12); Ex.-2007, ¶100.

The Petitions allege that Igarashi teaches STI regions in Igarashi's Fifth Embodiment (Fig. 12), and that these STI regions form the alleged "Active Region" illustrated in the below-reproduced figure from the Petitions. Petition at 26-27; Ex.-2007, ¶100; *see also* Petition at 38.

Fig. 12



Pet. at 27, Petitioner's Modified-Igarashi Fig. 12, Ex.-1004, Fig. 12

Petitioner modified Igarashi's Fig. 12 to ***add*** the ***"STI regions"*** and the ***"Active Region"*** allegedly formed thereby. Fig. 12 as it appears in Igarashi does not illustrate the STI regions or the alleged "Active Region." The Petitions' evidence, reasoning and rationale supporting the assertion that Igarashi teaches that

its Fifth Embodiment (Fig. 12) includes STI regions, and an "Active Region" allegedly formed thereby, is non-existent.[4] Ex.-2007, ¶100; *Liberty Mut. Ins. Co. v. Progressive Cas. Ins. Co.*, CBM2012-00003, Paper No. 8 at 10 (PTAB Oct. 25, 2012) (the Board "will address only the basis, rationale, and reasoning put forth by the Petitioner in the petition, and resolve all vagueness and ambiguity in Petitioner's arguments against the Petitioner."); *id.* at 14 ("It would be … inappropriate for the Board to take the side of the Petitioner to salvage an inadequately expressed ground proposing an alternative rationale.").

The Petitions cite to disclosure in Igarashi supporting the unremarkable assertion that Igarashi's Fifth Embodiment (Fig. 12) has a substrate. Petition at 25. Thereafter, the Petitions present their rationale supporting the assertion that Igarashi discloses STI regions, and an Active Region formed thereby, in a single paragraph spanning pages 25-26 of the Petition. Finally, the Petitions allocate six pages to arguing, based in part on Woerlee, that any "active region" formed by the STI regions would be formed in the substrate, but that analysis simply takes as a given that the STI regions are provided in the Fifth Embodiment (Fig. 12), and

[4] The preliminary institution finding (at 19) to the contrary cannot be sustained as discussed in § VII.C.1.c.

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

In other words, and consistent with both the Petition and his first declaration, Dr. Shanfield is confirming in this testimony that a person of ordinary skill, when reading Igarashi, would have understood that the disclosure of the features in Igarashi that are common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference numerals are used to describe common features of Igarashi's disclosure. Ex. 1027, ¶24.

The Petition is also clear that a "POSITA would have understood that the disclosure of the features in Igarashi common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference numerals are used to describe common features of Igarashi's disclosure." Petition, 22. For example, "semiconductor substrate 1" where the active region is formed is

Reply, Paper No. 22, at 17

The Petitions assert that "features in Igarashi common to different illustrations are applicable to the [Fifth] embodiment shown in Figure 12 because the same reference numerals are used to describe common features of Igarashi's disclosure." Petition at 22; Ex.-2007, ¶108. Even if true, that assertion provides no basis for finding Igarashi's disclosure of STI regions, and an active region formed thereby, in the First Embodiment to be applicable to the Fifth Embodiment. Igarashi's figures do ***not*** illustrate STI regions or an active region with "the same reference numerals" in Figs. 1-5 (First Embodiment) and Fig. 12 (Fifth Embodiment). Ex.-2007, ¶108. Indeed, the isolation regions described in

POR at 43-44

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

Based on the current record, however, we find it is clear from Igarashi that the disclosure of "active element region[s]" discussed in paragraph 68 with respect to the "First Embodiment" is equally applicable to the "Fifth Embodiment" upon which Petitioner primarily relies. For example, the description of the method for manufacturing the semiconductor device of the "Fifth Embodiment" refers back to earlier described embodiments of Igarashi, ultimately referencing the discussion of the method for manufacturing the semiconductor device of the "First Embodiment." Ex. 1004 ¶ 119 ("FIGS. 13A and 13[B] are schematic sectional views sequentially showing the method for manufacturing the semiconductor device shown in FIG. 12 [the Fifth Embodiment]. Here, FIG. 13A shows the same process as in FIG. 11B . . . ."), ¶¶ 112–13 ("FIGS. 11A to 11C are schematic sectional views showing the method for manufacturing the semiconductor device shown in FIG. 10 [the Fourth Embodiment]. . . . First, as FIG. 11A shows, gate electrodes 3 are formed, and silicon nitride films 7 and silicon nitride films S are formed so as to cover the gate electrodes 3 in the same process as in FIG. 5 . . . ."), ¶ 68 ("[T]he method for manufacturing the semiconductor device of First Embodiment will be described. In the following description of the manufacturing method, the major process for forming the silicon nitride film 7 will be described referring to FIGS. 5A to 5E, and other processes will be described without referring to drawings. First, an insulating film for isolating elements is formed on a silicon semiconductor substrate 1. Element isolation is performed using methods such as the LOCOS method or the trench method. Thereafter, ion implantation is performed to the active element region for forming the well and controlling the threshold value.").

Institution Decision, Paper No. 10, at 19

In addition, as Dr. Glew explains, the new rationale advanced by the Board in the Institution Decision has two critical mistakes. Ex.-2007, ¶116.

First, a POSA would have understood that Fig. 13A, which illustrates the manufacturing process of the Fifth Embodiment, shows "the same process as in FIG. 11B" (Ex.-1004, ¶119)—***not*** the same process as in ***all of Figs. 11A-11C*** as the Board suggested. Ex.-2007, ¶117.

POR at 48

117. First, Fig. 13A, which illustrates the manufacturing process of the Fifth Embodiment, shows "the same process as in FIG. 11B" (Ex. 1004 at ¶ 119)—***not*** the same process as in ***all of Figs. 11A-11C***. The Board's subsequent reliance on Fig. 11A (the Fourth Embodiment) is thus inapposite, as the patent provides no link between Fig. 13A and Fig. 11A. *See* Decision at 19 (relying on Igarashi's explanation that, "as FIG. 11A shows, gate electrodes 3 are formed, and silicon nitride films 7 and silicon nitride films 8 are formed so as to cover the gate electrodes 3 in the same process as in FIG. 5").

Glew Declaration, Exhibit 2007, ¶117

The Petition Fails To Identify a 'MISFET Includes: An Active Region' As Claimed

a. The Petitions Fail to Meet Petitioner's Burden of Demonstrating How and Why Any MISFET in the Igarashi/Woerlee Combination Includes an "Active Region" Meeting the Agreed-Upon BRI

The Petitions must specify the grounds with particularity. 35 U.S.C. §312(a)(3) (requiring IPR petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim"); 37 C.F.R. §42.104(b)(4) ("The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon."); *Harmonic*, 815 F.3d at 1363; *Kranos*, IPR2016-01649, Paper No. 25 at 29, 36, 39-42.

The Petitions fail to meet Petitioner's burden of establishing that ***any*** MISFET in the Igarashi/Woerlee combination "includes: an active region" meeting the agreed-upon BRI. Ex.-2007, ¶132.

As shown in Petitioner's modified Fig. 12 (reproduced below), the Petitions insert "STI" regions on the left and right sides, and further label the figure with a box "Active Region" and two arrows pointing to the channel regions under the gates of the two MISFETs. Ex.-2007, ¶132. The Petitions allege the "active element region is made of the substrate 1 of Igarashi and divided by STI regions." -1841-Petition at 27, 37. Ex.-2007, ¶132.

59

POR at 59

Mapping the agreed-upon BRI of "active region" and claim 1's requirement that "the MISFET includes: an active region" onto the prior art structure the Petitions allege meets the claimed "active region" is the furthest thing from irrelevant. *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (affirming final written decision upholding patentability where Petitioner offered merely "conclusory" discussion of the prior art and failed to explain with particularity how the limitations were disclosed); *Kranos Corp. v. Riddell, Inc.*, IPR2016-01649, Paper No. 25 at 29, 36, 39-42 (PTAB Feb. 7, 2018) (Petitioner failed to meet its burden where "it is unclear from Petitioner's argument where each element of [the challenged claims] is found in" the prior art and the Board "decline[d] to speculate as to Petitioner's intentions").

POR at 20

Mapping the BRI of "active region" onto the device the Petitions allege meets the claimed requirement of a MISFET that includes an active region is in fact ***highly relevant***. Indeed, it is a requirement for the Petitions to meet their burden of demonstrating the unpatentability of the challenged claims. *Harmonic*, 815 F.3d at 1363; *Kranos*, IPR2016-01649, Paper No. 25 at 29, 36, 39-42; *Ulthera, Inc. v. Dermafocus LLC*, IPR2016-01459, Paper No. 30 at 12 (PTAB Jan. 19, 2018) ("Petitioner bears the burden of proof ***on each limitation***."). The Petitions' failure to do so is fatal, and all instituted grounds fail for this reason alone.

POR at 62

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (Paper No. 20 at 38)

In other words, and consistent with both the Petition and his first declaration, Dr. Shanfield is confirming in this testimony that a person of ordinary skill, when reading Igarashi, would have understood that the disclosure of the features in Igarashi that are common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference numerals are used to describe common features of Igarashi's disclosure. Ex. 1027, ¶24.

Moreover, inherency is irrelevant in this case because—putting aside the fact that neither Petitioner nor Dr. Shanfield has ever raised an inherency argument in this case—Igarashi *expressly* discloses an active region. Petition, 25, *citing* Ex. 1004, [0068] (discussing the formation of the "active element region"). Ex. 1027, ¶25.

The Petition is also clear that a "POSITA would have understood that the disclosure of the features in Igarashi common to different illustrations are applicable to the embodiment shown in Figure 12 because the same reference numerals are used to describe common features of Igarashi's disclosure." Petition, 22. For example, "semiconductor substrate 1" where the active region is formed is a common feature between Figure 1 (Embodiment 1) and Figure 12 (Embodiment 5). In fact, Dr. Glew admitted that he used the same approach to interpret the '501 patent, admitting that he based his assessment of the '501 patent's first

U.S. Patent 7,893,501
IPR2017-01841
Petitioner's Reply to Patent Owner's Response

Moreover, the Petition showed that Igarashi's isolation region teachings were applicable to its Figure 12 embodiment. Specifically, the Petition cites Figure 12, which shows the "semiconductor substrate 1." Petition, 25. Then, the Petition explains that a POSITA would have understood that the semiconductor substrate 1 in Fig. 12 has an active region because Igarashi expressly discloses an "active element region" made of the semiconductor substrate 1. Petition 25-26, *citing* Ex. 1004, [0068]; Ex. 1002, ¶66; Ex. 1010, 42-43. Ex. 1027, ¶27.

Accordingly, both the Petition and Dr. Shanfield's testimony have been clear and consistent throughout this proceeding: Igarashi discloses the "active region" of the challenged claims in connection with its Fifth Embodiment. Moreover, as discussed below in Section III.D, the Petition also demonstrated it would have been obvious to form the active region disclosed in Igarashi in semiconductor substrate 1 of Igarshi's Fifth Embodiment in view of the teachings of Woerlee. Ex. 1027, ¶28.

B. Igarashi Discloses a MISFET that Includes an "Active Region"

A person of ordinary skill would have viewed the region between the two STI in Igarashi where the two transistors are formed as an "active region" formed between those two STI. As noted in the Petitio
confirms the 'active element region' (active reg
substrate 1 because according to the trench meth

Reply, Paper No. 22, at 17, 19

[0068] Next, the method for manufacturing the semiconductor device of First Embodiment will be described. In the following description of the manufacturing method, the major process for forming the silicon nitride film **7** will be described referring to **FIGS. 5A** to **5**E, and other processes will be described without referring to drawings. First, an insulating film for isolating elements is formed on a silicon semiconductor substrate **1**. Element isolation is performed using methods such as the LOCOS method or the trench method. Thereafter, ion implantation is performed to the active element region for forming the well and controlling the threshold value.

Igarashi, Ex. 1004, ¶ 68 (cited Reply, Paper No. 22 at 18)

Igarashi Does Not Teach That the Fifth Embodiment (Fig. 12) Includes Isolation Regions (POR at 38)

	Petition	Institution Decision	Reply
Same Reference Numerals … Describe Common Features (Reply at 17)	? Pet. at 22	✓ ID at 20	✓ Reply at 17
Where Features Differ Between Figures, The Differences Are Described (Petition at 22)	? Pet. at 22	✓ ID at 20	✓ Reply at 20
Fifth Embodiment Refers Back to … Method for Manufacturing … First Embodiment (ID at 19)	✗	✓ ID at 19	✗
Use of Isolation Regions … Obvious in View of Woerlee (Reply at 14)	✗	✗	✓ Reply at 14
Obvious to Apply Igarashi's … Teaching of An Active Region to the Fifth Embodiment (Reply at 3)	✗	✗	✓ Reply at 3

Q. In Figure 2, does the MISFET include an active region?

MR. MILLER: Objection. Scope.

A. I haven't opined on that in my sur-reply.

Q. Do you have an opinion one way or the other on whether the MISFET in image 2 includes an active region?

MR. MILLER: Objection. Scope.

A. I haven't analyzed it. I don't want to give an opinion off the top of my head without analyzing it.

Q. So sitting here today, you can't tell me one way or the other whether image 2 includes an active region?

MR. MILLER: Objection. Scope.

A. I can't sit -- I can't give you an opinion about analyzing, and I haven't analyzed this yet. The process for analyzing it isn't something I can do right here, right now.

Glew Sur-Reply Depo,
Ex. 1029 at 16:4-23
(cited Petitioner's Sur-Sur-Reply, Paper No. 33, at 2)

(Justices confer off the record)

THE COURT: So in general, we agree with Patent Owner that this should be a pretty limited declaration. The declaration is only three pages directed specifically to be used to references that were submitted with Petitioner's reply, Exhibits 1025 and 1026.

So going forward in this deposition, the questions need to be limited to those references or to specific testimony in Dr. Glew's sur-reply declaration.

Transcript of Call with Board,
Ex. 2025 16:13-24

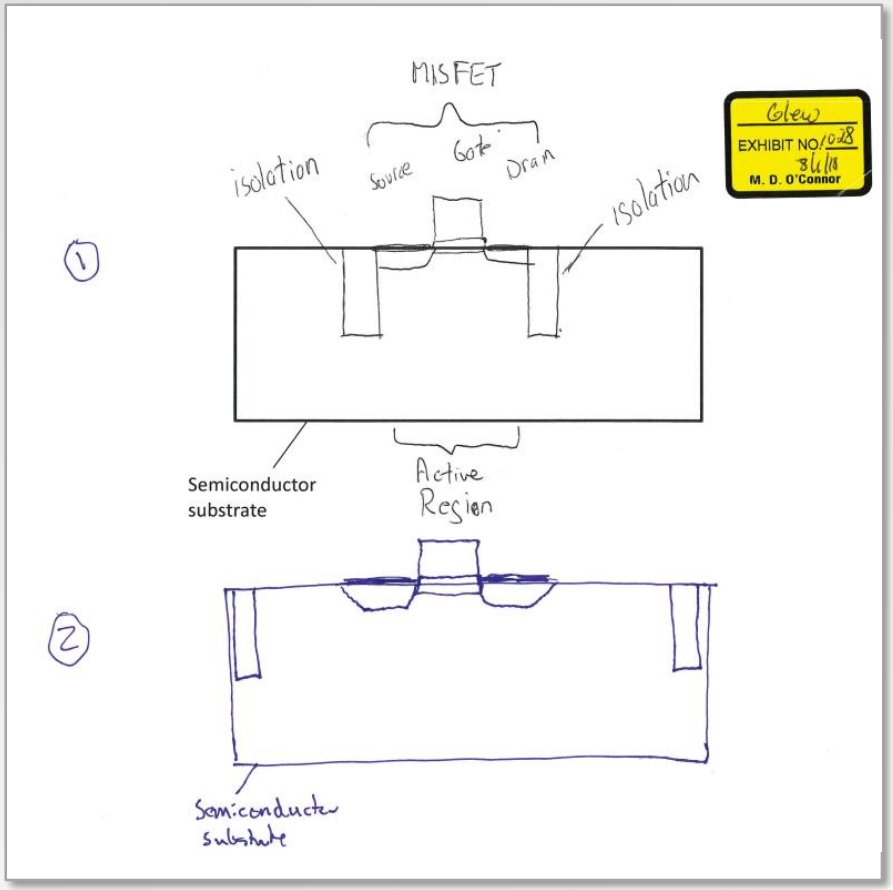
Q. So what I've done in the drawing below, your drawing, I've intended to reproduce your drawing, but I've moved the isolation regions away from the MISFET.

Does my drawing accurately reproduce your drawing, with the exception of the change of moving the isolation regions away from the MISFET?

MR. MILLER: Objection. Scope.

A. Your drawing here is not something I've opined on in my expert -- or in my sur-reply here. I can't really comment further on your drawings. I haven't formed or evaluated these in the context of the sur-reply.

Glew Sur-Reply Depo,
Ex. 1029 at 14:19-15:8



Glew Sur-Reply Depo Exhibit 1028

Q. How would you draw a second MISFET between the two isolation regions in Figure 3?

MR. MILLER: Objection.

A. In general, if I wanted to draw a second MISFET, I would draw it like the first MISFET. However, this is not something that I addressed in my sur-reply. I'm not sure what to do with this. I haven't offered an opinion on this Figure 3 that you've drawn here.

Glew Sur-Reply Depo., Ex. 1029 at 19:3-11 (cited Petitioner's Sur-Sur-Reply, Paper No. 33, at 2)

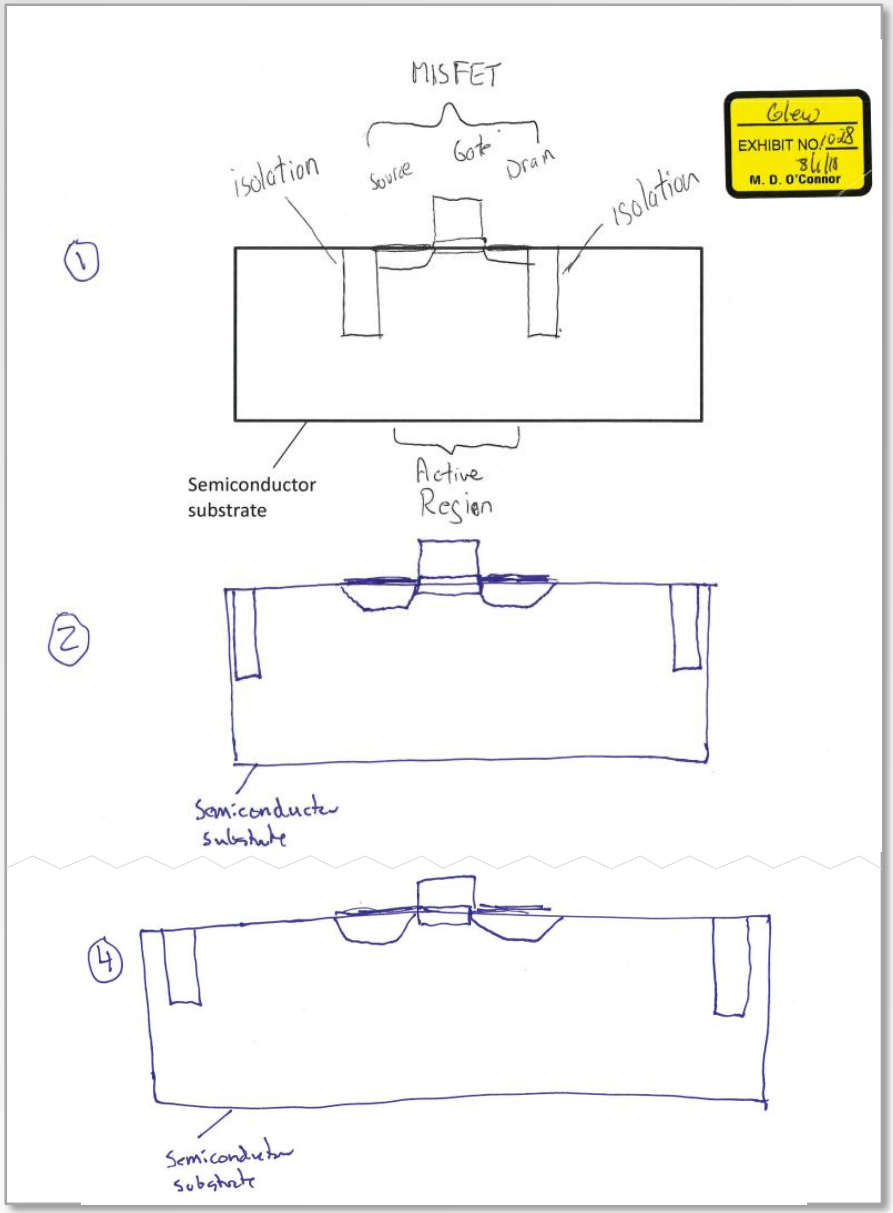
Q. I'm just asking you whether you can draw a second MISFET in the region between the two isolation regions. If you're not able to do that, that's fine. I just want the record to be clear.

So yes or no, are you able to do that?

MR. MILLER: Objection form. Objection scope.

A. If this is a MISFET of the '501 patent, then one could not draw a MISFET here that meets the limitations of the '501 patent.

Glew Sur-Reply Depo, Ex. 1029 at 22:5-16



Glew Sur-Reply Depo Exhibit 1028

Q. Sitting here today, you don't have an opinion one way or the other as to whether a person of skill in the art looking at the multi-transistor device shown in Figure 12 of Igarashi would understand that the multi-transistor device includes an active region?

MR. MILLER: Objection form. Objection scope.

A. I haven't developed any further opinions outside of the two declarations, the initial declaration and the sur-reply.

I don't recall opining -- I recall opining on MISFET. I do not recall opining on multi-transistor device.

Q. Sitting here today, you don't have an opinion with regard to the multi-transistor device in Igarashi's Figure 12 as to whether it includes an active region?

MR. MILLER: Objection form. Objection scope.

A. I don't recall analyzing it for a multi-transistor device. I analyzed it for a MISFET having an active region made of a semiconductor substrate.

To the extent you can refer me to somewhere in my previous declaration where I opined on that, I'd be happy to look at it, but I don't recall opining on that previously. I haven't developed any further opinions on that.

Glew Sur-Reply Depo, Ex. 1029 at 62:5-63:9
(cited Petitioner's Sur-Sur-Reply, Paper No. 33, at 2)

1. A semiconductor device, comprising a MISFET, wherein
the MISFET includes:
an active region made of a semiconductor substrate;
a gate insulating film formed on the active region;
a gate electrode formed on the gate insulating film;
source/drain regions formed in regions of the active region located on both sides of the gate electrode; and
a silicon nitride film formed over from side surfaces of the gate electrode to upper surfaces of the source/drain regions, wherein:
the silicon nitride film is not formed on an upper surface of the gate electrode, and
the gate electrode protrudes upward from a surface level of parts of the silicon nitride film located at both side surfaces of the gate electrode.

Ex. 1001, '501 patent at Claim 1

Q. Does each transistor in Figure 12 include an area where the transistor is formed?

MR. MILLER: Objection. Scope.

A. I haven't opined specifically on the question of formation region for Figure 12 MISFETs.

To the extent that the formation region requires an active region, and if I've opined that it doesn't have an active region, then it couldn't have a formation region. But this is not an opinion I've given or analyzed.

Glew Sur-Reply Depo, Ex. 1029 at 63:10-20
(cited Petitioner's Sur-Sur-Reply, Paper No. 33, at 3)

Q. What are the components of an active region?

A. Well, a region is a geographical distinction. What's in that geographical distinction can vary, but it would include, at least, the source gate and drain regions or actually the source channel and drain regions for a typical transistor.

Glew Sur-Reply Depo, Ex. 1029 at 70:5-12
(cited Petitioner's Sur-Sur-Reply, Paper No. 33, at 3)

A. "wherein the MISFET includes: an active region made of a semiconductor substrate" (claim 1)

61. Claim 1 recites "wherein the MISFET includes: an active region made of a semiconductor substrate."

62. As explained below in ¶¶ 63-85, I understand that the parties agree that under BRI, "an active region made of a semiconductor substrate" is "an area of the semiconductor substrate defined by an isolation region where the transistor is formed." I agree with the parties that this is the proper BRI of that claim limitation for the reasons detailed below.

Glew Decl., Ex.2007, ¶¶ 61-63
(cited POR 26)

Q. Do you agree that isolation regions define an active region?

A. I think we already discussed the point that there are transistors, exceptional circumstances in the year 2003, that don't have isolation regions. So they still have active regions. So I wouldn't -- I don't take that as "define" in the hard sense of the word.

Q. So let me back up. Earlier when I had asked you about this understanding that an active region made of a semiconductor substrate is an area of the semiconductor substrate defined by an isolation region where the transistor is formed, you said that that was a statement, a description of what a person of skill in the art would understand, but not necessarily a construction?

Am I getting that right?

A. Yes.

Q. So a person of ordinary skill in the art would understand the term to mean that: that it's not necessarily the case that you were offering that as a construction; is that right?

A. I withdraw the statement that it's not a construction. It's actually, now that I think about it further, a proposed construction.

And I was being careful in explaining what I meant because I was not comfortable with the interpretation of what was a proposed construction. But it's a proposed construction appropriate to the '501 patent.

Q. In your proposed construction for the '501 patent?

A. That's correct.

Q. And just so we're clear, so it is your proposed construction for the '501 patent that an active region made of a semiconductor substrate is an area of the semiconductor substrate defined by an isolation region where the transistor is formed?

A. Correct.

Shanfield Reply Depo., Ex. 2026, at 95:4-96:18
(cited Paper No. 34, Observation No. 4)

Q. What's the function of the active region?

A. As I stated, it's an area where the transistor is formed. Different portions of the transistor have different functions. Hence, different areas of the active region would have a function corresponding to the area of the transistor that it corresponded to.

Q. Does the active region itself have any functions?

A. As I previously stated, the active region is the region where the transistor is formed. There are different aspects to the transistor, such as the source gate or drain.

These different parts of the transistor have different functions. So portions of the active region do different jobs corresponding to the part of the transistor occupying that part of the active region.

Glew Opening Depo., Ex. 1024 at 43:2-20