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Krivokapic

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(54) **METHOD OF FABRICATING AN ULTRA-THIN FULLY DEPLETED SOI DEVICE WITH T-SHAPED GATE**

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(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(21) Appl. No.: **10/200,652**

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Related U.S. Application Data

(62) Division of application No. 10/081,104, filed on Feb. 21, 2002, now Pat. No. 6,452,229.

(51) **Int. Cl.**⁷ **H01L 21/336**; H01L 21/00; H01L 21/28

(52) **U.S. Cl.** **438/270**; 438/297; 438/303; 438/151; 438/572; 438/574; 438/576; 438/580

(58) **Field of Search** 438/149, 151, 438/270, 297, 303, 572, 574, 575, 576, 579, 580, 581, 58

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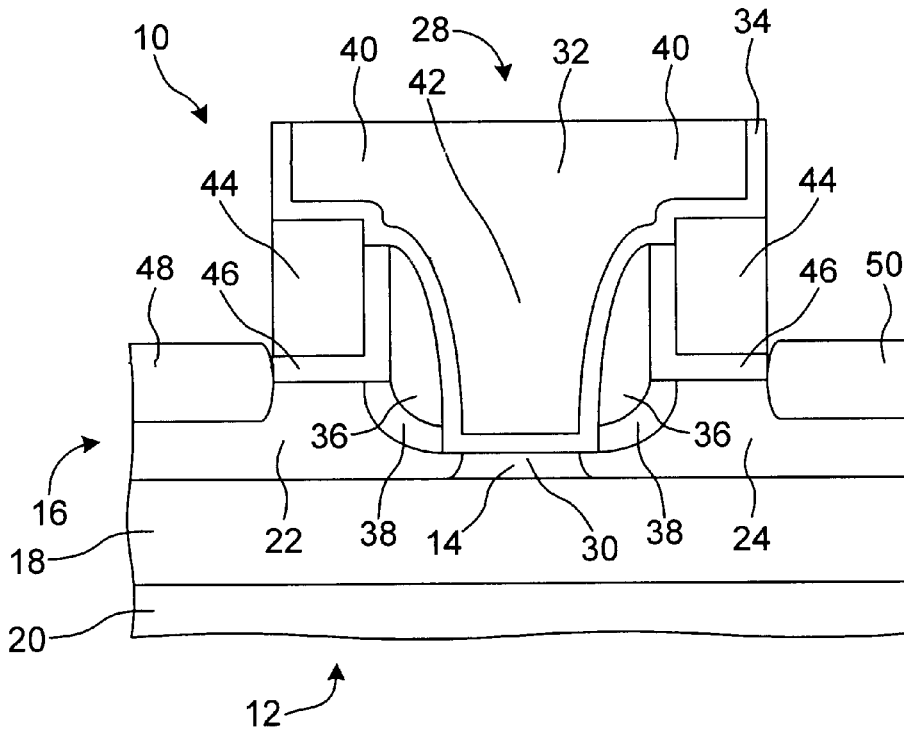
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(57) **ABSTRACT**

A method of forming a fully depleted semiconductor-on-insulator (SOI) field effect transistor (FET). The method includes forming a T-shaped gate electrode formed at least in part in a recess formed in a layer of semiconductor material and over a body region that is disposed between a source and a drain. The method includes spacing the gate electrode from the body by a gate dielectric made from a high-K material.

15 Claims, 5 Drawing Sheets



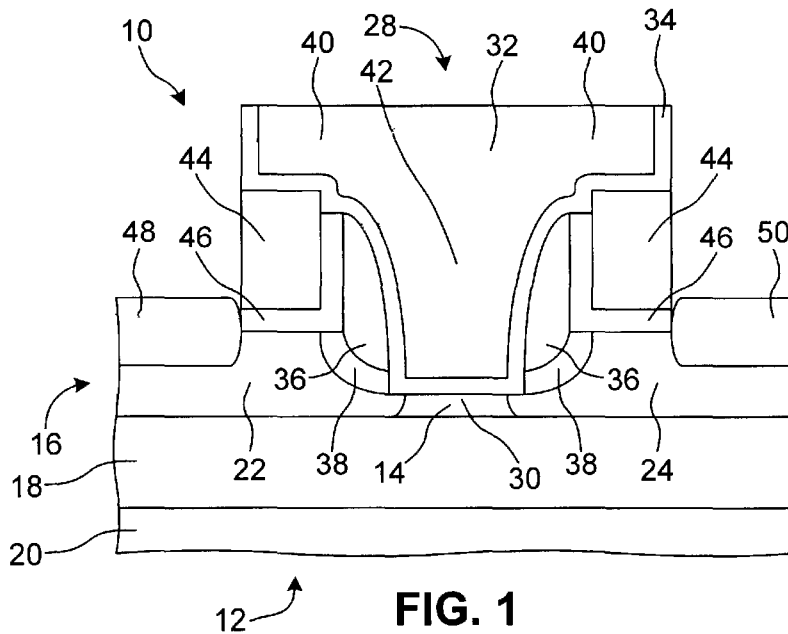


FIG. 1

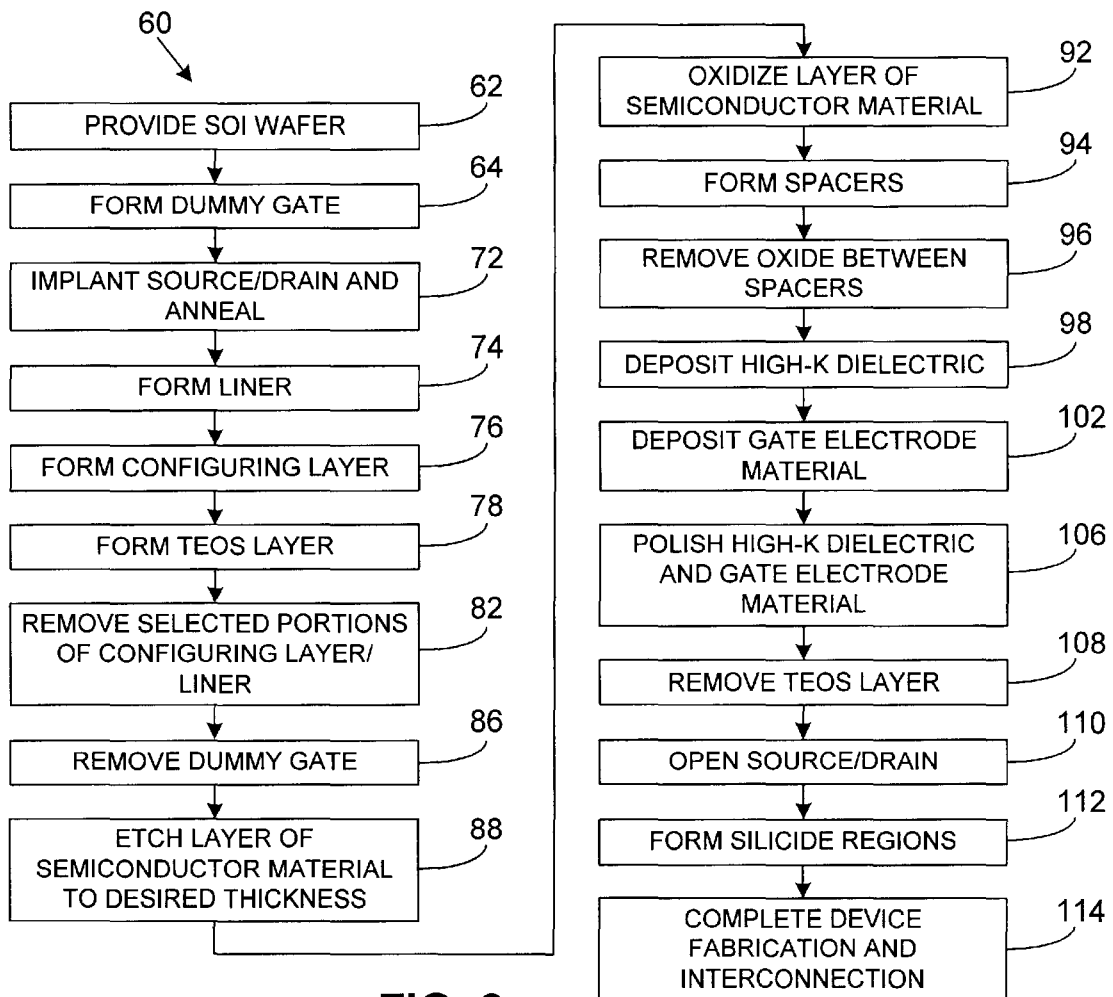


FIG. 2

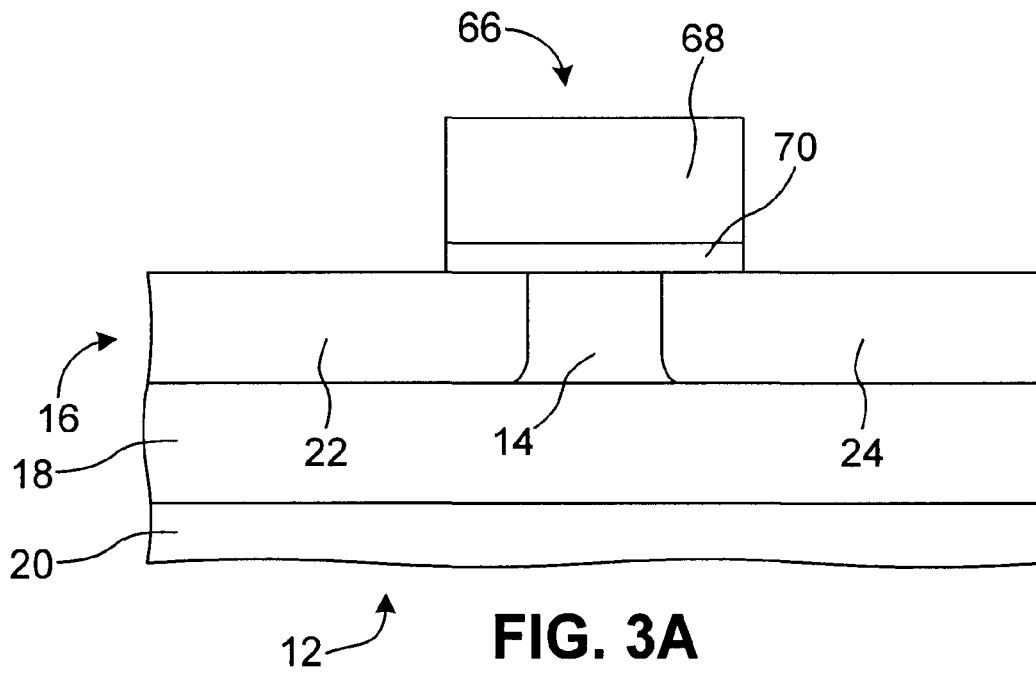


FIG. 3A

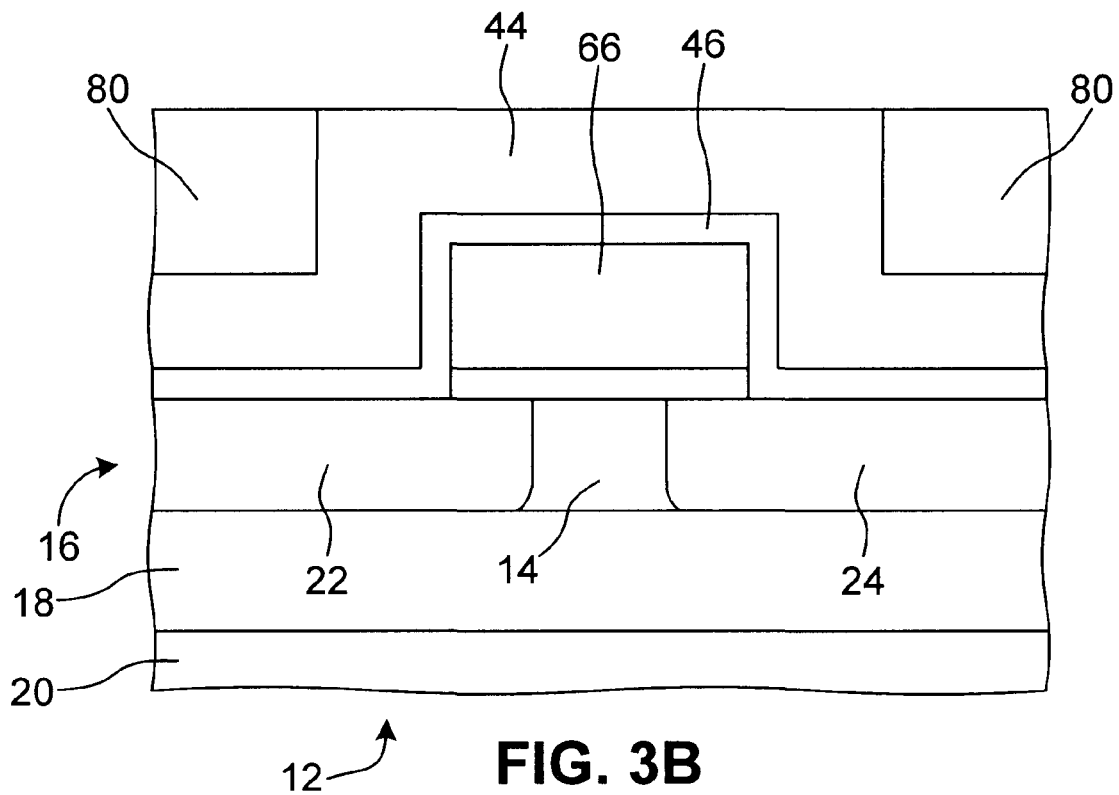


FIG. 3B

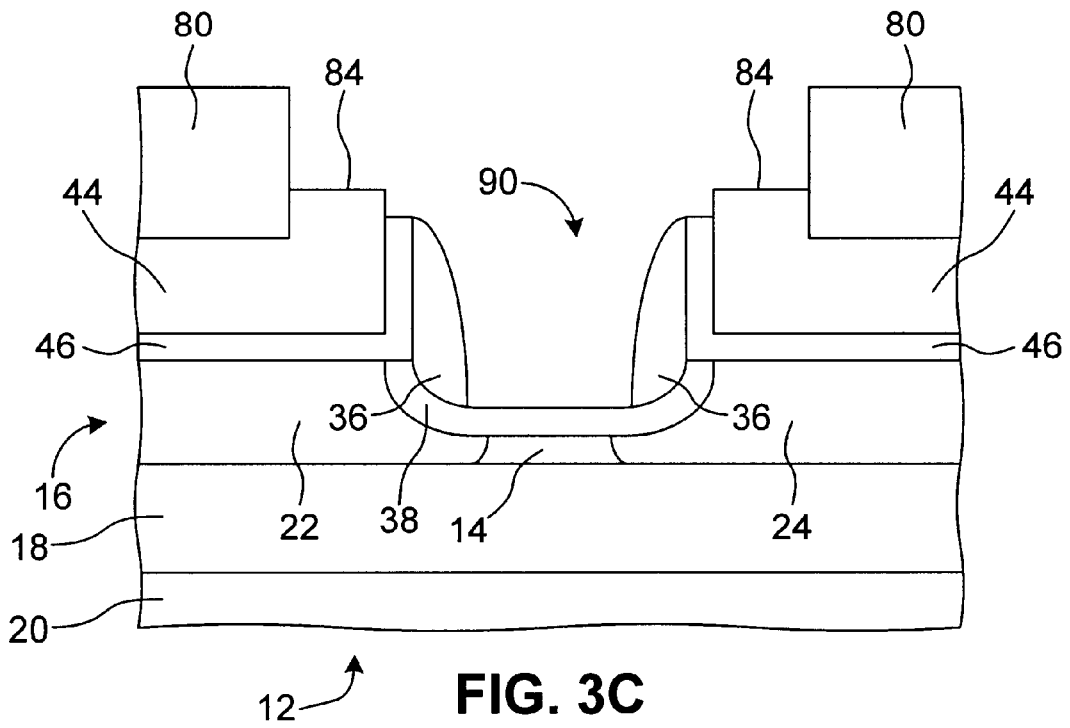


FIG. 3C

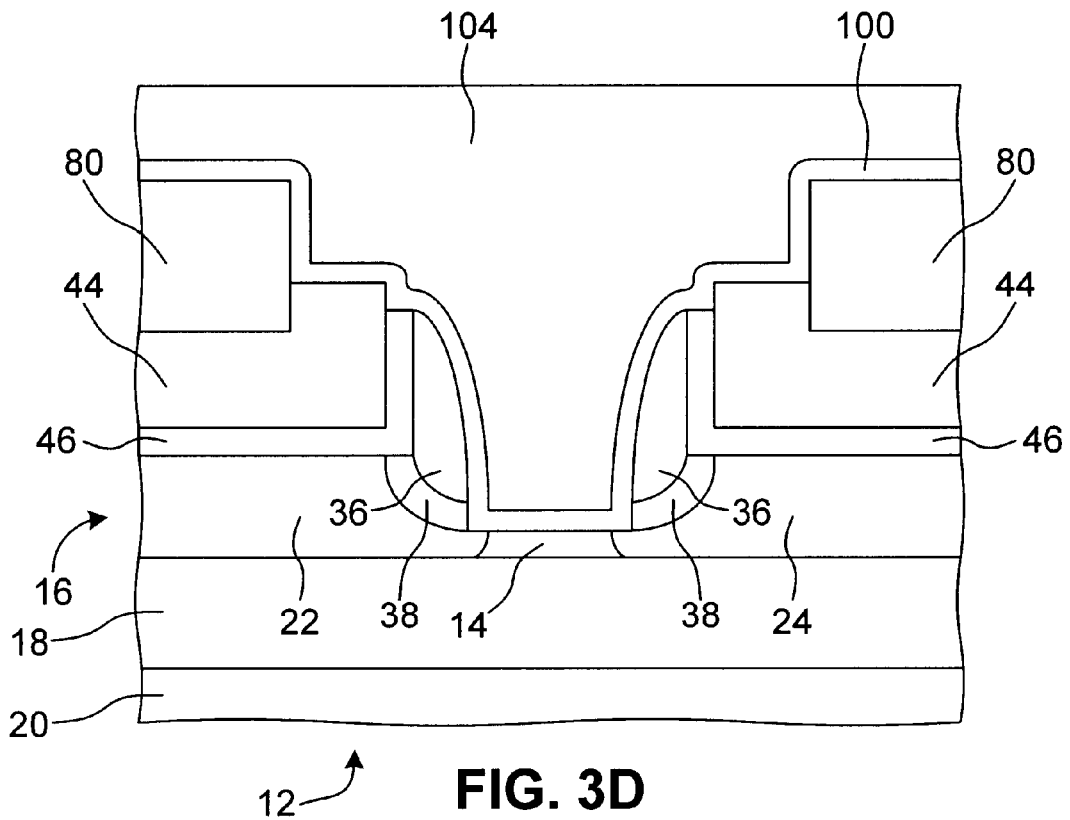


FIG. 3D

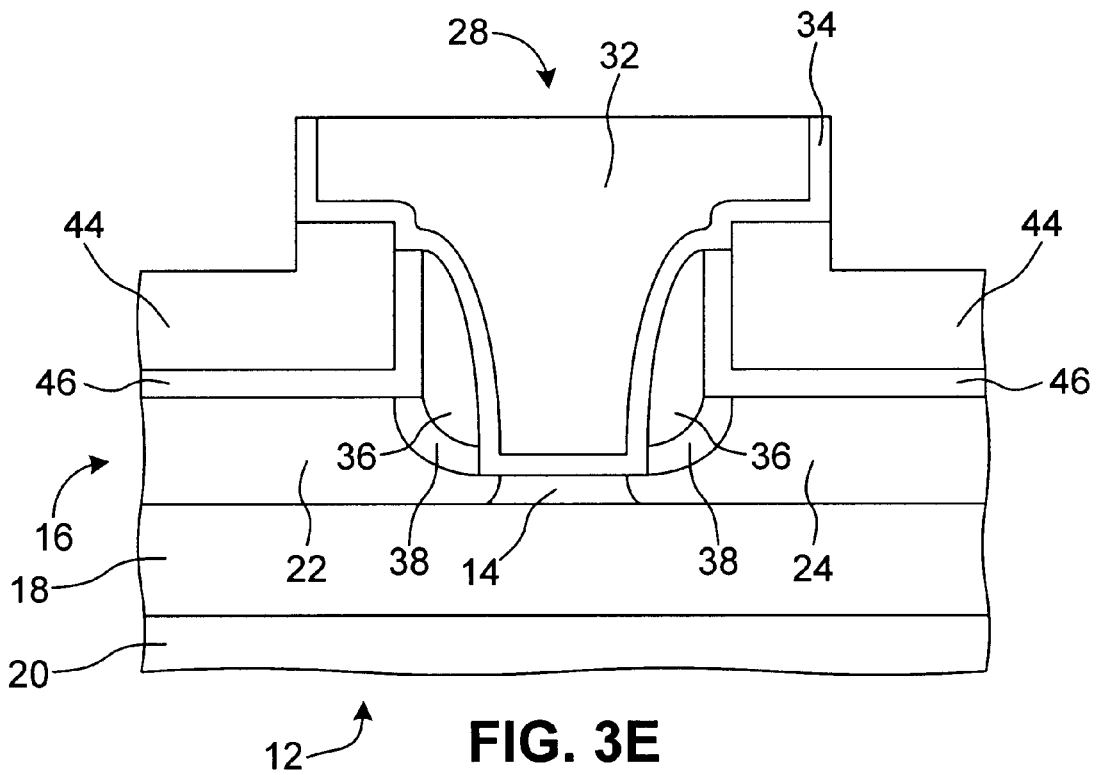


FIG. 3E

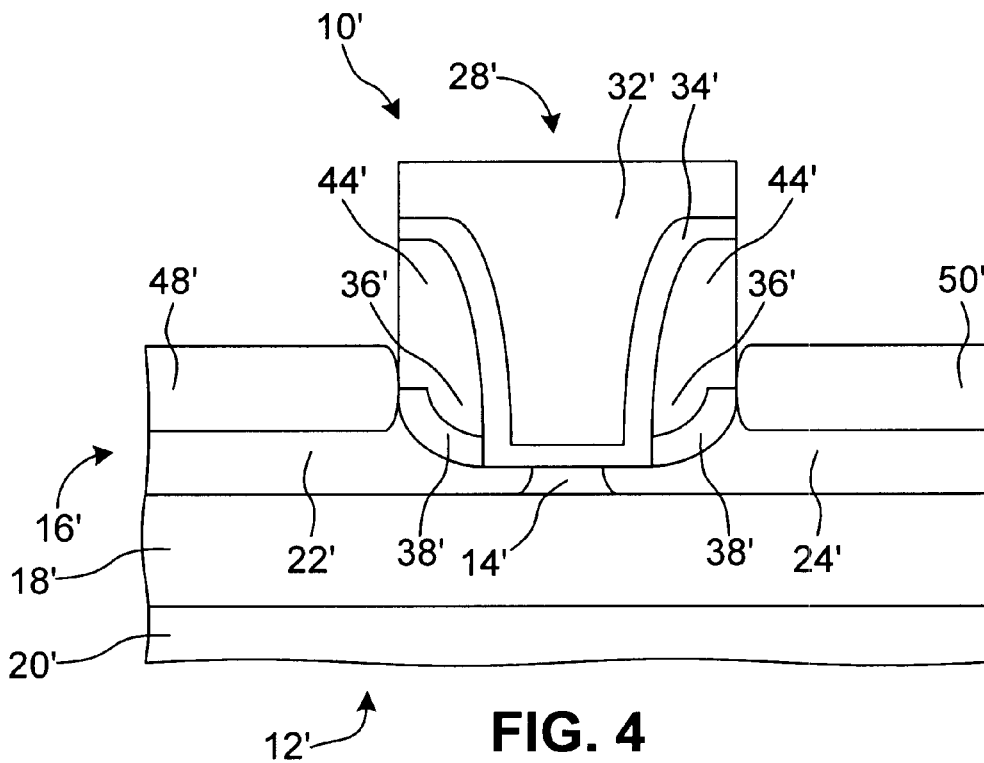


FIG. 4

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