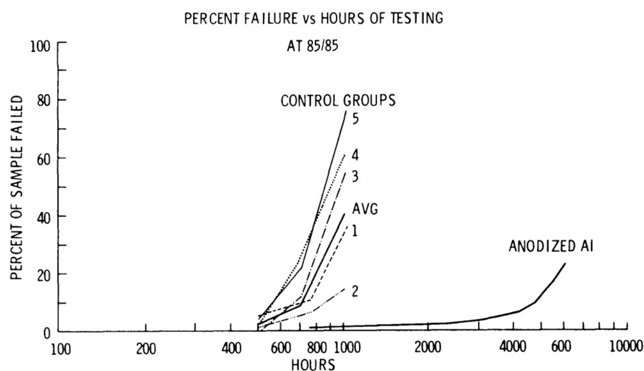

Figure 5

which again reflects the frequency insensitivity of loss tangent. Table I gives the dielectric properties of the anodic oxide grown under the conditions used in the fabrication of interconnect patterns.

Reliability

As discussed earlier the environment of high humidity and elevated temperature have the most deleterious effects upon aluminum interconnects. Transistor-transistor logic circuits were fabricated by the anodic process and subjected to a battery of reliability evaluation. The most severe environment encountered were those of 85% relative humidity, 85 degrees centigrade, pressure cooker (121°C ± 3 100% R.H. 15 psig) and a boiling water test which involves immersion of the device in boiling deionized water. Table II is a compilation of results of these tests. All tests unless otherwise noted were performed upon plastic encapsulated devices. The extremely low failure rates are indicative of the passivation provided by the anodic oxide. Those devices which did fail were subjected to failure analysis. It was determined that most failures were associated with the bond pad areas which do not receive an anodic overcoat. Some of the failures were associated with corrosion of the bond wires. No failures were noted which could be associated with corrosion of leads which were imbedded in and overcoated with the anodic oxide.

Figure 5 is comparative data of anodized versus glass passivated process on identical devices of a different device type. Both the anodized samples and the control groups were subjected to the same 85% relative humidity 85°C environment. Both groups were unencapsulated. This data indicated that the passivating capability of the anodic oxide is nearly an order of magnitude greater than that of a glass overcoat.

Conclusion

The anodic processing of aluminum interconnect patterns provides a method of rendering aluminum interconnect compatible with non hermetic packaging. The presence of the barrier layer at the aluminum surface acts to greatly enhance the corrosion resistance of aluminum metal. The reliability of such interconnects on plastic encapsulated integrated circuits has been demonstrated. An evaluation of the dielectric properties of the anodic oxide of aluminum indicate properties which are compatible with single and multilevel interconnects for integrated circuits.

CURRENT CONCEPTS IN THE PASSIVATION AND ENCAPSULATION OF SEMICONDUCTOR DEVICES

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Introduction

For several years after the introduction of the Planar passivated transistor,[1] this simple structure with thermal silicon dioxide over the junctions provided the basis of the standard semiconductor technology. The device was sealed in a hermetic metal package and little subsequent attention had to be given to it. Gold or aluminum bonds were made to aluminum contacts alloyed to the silicon contact regions. However, the development of integrated circuits, initially simple by today's standards, lead to increased complexity of structure and of fabrication procedures. Furthermore, improved reliability became a necessity with the introduction of MOS transistors, which are very surface sensitive. It was found that by careful processing the same thermal oxide passivated structures in metal packages could provide stable MOS devices. However, it also became apparent that for mass production and low costs required in the industry, other means of passivation and encapsulation would have to be developed. This was especially true when the complexity of the integrated circuits was combined with the sensitiveness of MOS devices.

This paper provides a review of these new concepts in passivation and encapsulation of semiconductor devices. The changing role of the dielectric films used for passivation and protection will be discussed along with newer approaches to the metal contacts and interconnections. Also, the various types of packages—metal, ceramic and plastic—will be briefly described, as well as problems associated with each system. Finally, the use of dielectric layers for providing corrosion and mechanical protection of the metallized circuits will be considered, along with possible interactions between the various packaging materials and device components. It will be observed that the proper selection of the dielectric films will be a key factor in the successful development of reliable, low cost semiconductor devices.

Passivation

A cross-section of a typical, Planar-passivated diffused junction in silicon is shown in Figure 1. The drawing is such that the left-hand side might represent a diode or a collector-base junction of a bipolar transistor, while the right-hand includes a metal field plate over the oxide as is the case for an MOS transistor. It is now well known that several charges can be associated with the thermally oxidized silicon system. These include fast interface states, N_{st}, fixed surface charge, Q_{ss}, mobile impurity charge, Q_o, and traps due to ionizing radiation, N_{ot}, as well as ion or charge migration on the oxide surface.[2–4] These charges and their location in the oxide are also indicated in Figure 1. The measurement and characterization of these charges has been the subject of numerous investigations, many of them listed in the MIS bibliographies of Schlegal.[5] Many of these investigations made use of the MOS capacitance-voltage method of analysis,[6–7] and this procedure continues to provide a rapid but simple means of studying charge effects in dielectric layers on semiconductors.

The presence (or migration) of the charges in the MOS structures has been found to have an appreciable effect on device

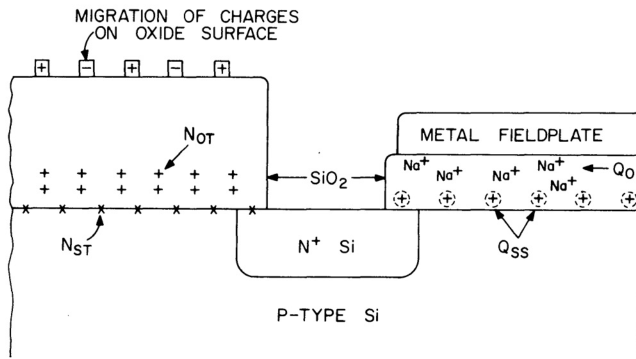


Figure 1—Example of Charges Associated with Thermally Oxidized Silicon Device Structure: Q_{ss}, Fixed Surface Charge; Q_o, Mobile Impurity Ion; N_{st}, Fast Surface State; N_{ot}, Hole Traps Formed by Ionizing Radiation; and Charge Migration on Oxide Surface.

TSMC 1014

electrical properties. For instance, low current beta, noise, and breakdown voltage of bipolar transistors can be affected, while turn-on voltage and channel conductance in MOS devices have a critical dependence on the charge densities. Figure 2 indicates some of the possible changes in the densities or location of these charges in the oxide due to electric fields and the resulting effects on the silicon surface. It has been adequately demonstrated, however, that by careful processing, these charge densities can be controlled and minimized so that stable MOS and other devices can be fabricated.[2] However, as the need for increased production of more complex devices occurred with an additional requirement of lower costs, it was found that the control procedures required for stable oxide-passivated devices were very difficult to implement under production conditions. Further, expensive hermetic packages were also required for these sensitive devices. While the thermal oxide can be produced free of ionic contaminants, its structure does not prevent subsequent penetration by ionic impurities or other contamination even at low temperatures. Thus the concept of double dielectrics was established, in which a second dielectric capable of masking ionic impurity migration is deposited over the passivating thermal oxide.

The first dielectric to be used as a passivating layer over thermally oxidized silicon devices was phosphosilicate glass (PSG).[8] It is applied by the vapor deposition of P_2O_5 as in diffusion predeposition processing, the phosphorus oxide mixing with the outer SiO_2 layer to form a P_2O_5-SiO_2 glass-like structure. This film was found to prevent ionic impurities from diffusing through it as well as to getter impurity ions such as sodium from the underlying SiO_2. Its disadvantages were that it reacts readily with water as well as exhibiting an undesirable structural polarization effect.[9] Even so, under proper conditions, i.e. controlled thickness and phosphorus concentration, it can be used effectively to better passivate thermal oxides and the associated device structures.[10]

Another type of passivating layer used in conjunction with thermal oxides is a "dense" dielectric such as silicon nitride (Si_3N_4) or aluminum oxide (Al_2O_3). This type of film prevents the ionic impurities from diffusing through it due to close-packed structure, as opposed to the complexing or gettering action of the phosphosilicate glass. Silicon nitride is generally deposited by the vapor phase reaction of SiH_4 or $SiCl_4$ with NH_3 in the temperature range 650-1000°C, while alumina films have been produced by the low temperature anodization of deposited aluminum as well as the higher temperature vapor deposition processes. Both types of films have also been deposited by sputtering techniques. Investigations involving double layers of Si_3N_4 or Al_2O_3 over thermally oxidized silicon are reported.[11–15]

It has been definitely established that the use of these dense films, especially silicon nitride, will provide much more reliable devices. The main advantage is that up to 500°C, ion migration through the film is essentially eliminated. The main disadvantages of these films are that processing, especially photomasking, becomes more difficult, and that additional instabilities are encountered. These are discussed below. A typical passivated device structure is shown in Figure 3, where the second dielectric may be phosphosilicate glass, silicon nitride or aluminum oxide. Note the two examples where the edge of the oxide contact cut may or may not be "sealed" with the second dielectric.

Other dielectrics used over thermal oxides have included SiO_2 and other oxides deposited by various techniques. These include evaporation, sputtering, vapor phase reaction and sedimentation. The main purpose of these second layer oxides is to increase the thickness of the original thermal oxide and thus prevent field inversion beneath current-carrying interconnections. In general, these oxides will not prevent ion migration. They may be valuable in providing chip protection of the metallized circuits, and this aspect is discussed below. A general discussion of these deposited oxides is available.[16–17]

An important consideration for the effectiveness of all the above double-layer dielectrics is whether they contribute additional instabilities to the device properties. The advantage gained by the elimination of ion migration may be canceled by additional effects. Four possible charge effects have been found that can be associated with double-dielectric structures. These are indicated in Figure 4, and are shown to be polarization due to dipole orientation, interface trapping, polarization due to conductivity differences and interface charge formation.[2] Many studies have been reported for all these cases and most of the instabilities can be minimized by proper process conditions and control for each type of dielectric. It is not within the scope of this paper to discuss these effects, but they must each be considered in evaluating any given double-dielectric system.

Metallization

Evaporated metal films were originally used to provide an ohmic contact between the silicon junction areas and a lead wire for connections to outside the package. As geometries got smaller and with the development of integrated circuits, the metal system became a complex array of interconnecting lines and contacts (see Figure 5). More attention had to be paid to effects of the metallization on device characteristics and reliability as well as the effect of the package and/or ambient on the metal integrity itself.

The most commonly used metal for the above applications in semiconductor technology has been aluminum.[18–19] Schnable[19] in his review, discusses advantages and disadvantages of the aluminum metallization system. The advantages are based on its ease of processing (deposition, etching, etc), its high conductivity, and its good adherence and contacting properties. At the same time its reactivity, which accounts for most of these desirable properties, also leads to disadvantages. That is, it can be attacked readily by plastics used for packages and by moisture which is present in nonhermetic packages. It is also subject to electromigration under high current density conditions and microcracking when deposited over steep oxide steps.

The corrosion problem of aluminum interconnections in plastic packages has led to the investigation of other systems. One of the most notable is a part of the Beam Lead Structure (mentioned below) which makes use of a Pt_5Si_2 contact to the silicon, covered by a Ti-Pt-Au multilayer structure.[20] This is then combined with a Si_3N_4-SiO_2 dielectric passivation system.[21] Neither this metal system (especially the platinum) nor the silicon nitride will allow

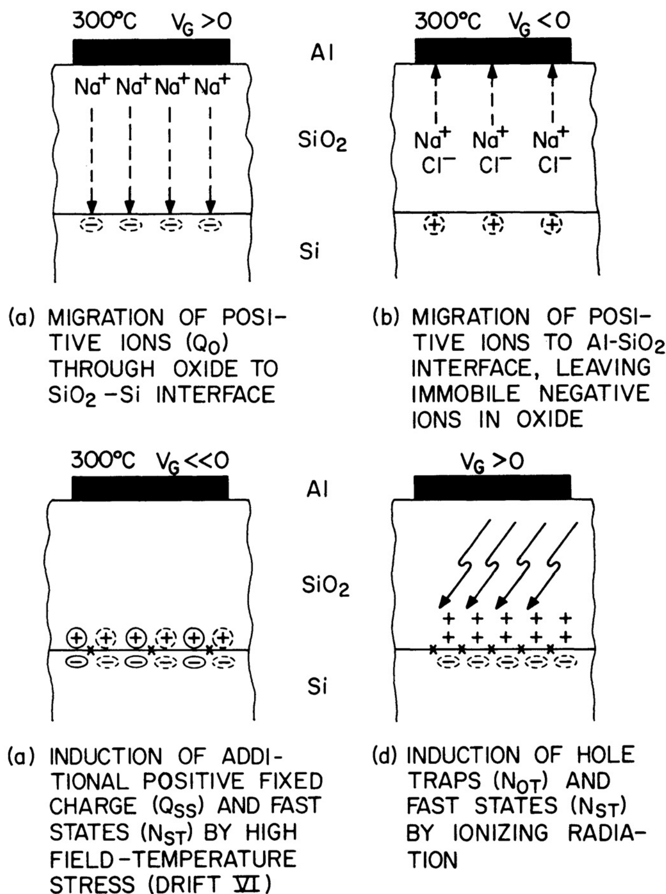


Figure 2—Examples of Processing Effects on Density or Location of Four Types of Charges in Thermally Oxidized Silicon Structure.

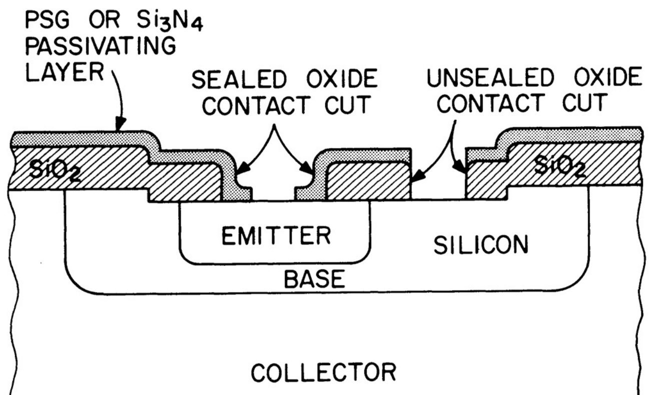
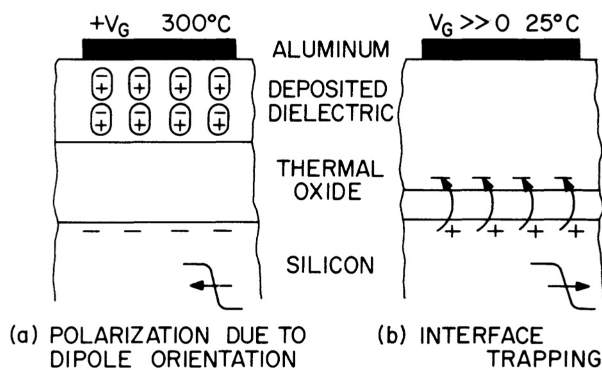


Figure 3—Typical Double Dielectric Structure Used for Passivating Semiconductor Device. Examples of Both "Sealed" and "Unsealed" Oxide Contact Cut are Indicated.



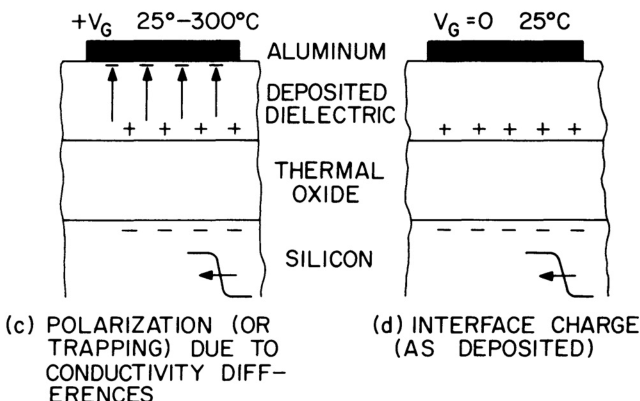


Figure 4—Four Different Types of Instabilities or Charges Associated With MIOS (Metal-Insulator-Oxide-Semiconductor) Structures.

sodium penetration up to at least 300°C and thus a sealed device structure is obtained. Furthermore, the outer gold layer is very inert to corrosion. As it turns out, however, the nonreactivity of the gold and platinum also result in more difficult processing. Thus the advantages and disadvantages are just the opposite as compared to aluminum.

Other metallization systems have also been reported. These include Mo-Au, W-Au, Cr-Au, and Cr-Ag-Au multilayers and Al-Si or Al-Cu alloys.[22–25] Each of these combinations shows some advantages, but processing difficulties and other problems indicate that no one system satisfies all requirements. In general, the more active the metal, the easier the processing but the more likelihood of corrosion in plastic and nonhermetic packages. One of the problems associated with any nonreactive metal such as platinum, is that its high melting and boiling points require that e.b. evaporation or sputtering be used for the deposition. In either case ionizing radiation is produced and can adversely affect device parameters. Also, these processes are more difficult to operate and control under production conditions.

A recent development in the fabrication of gates for MOS devices is the use of a high temperature metal such as molybdenum.[26] Its high melting point and relatively ease of etching allows subsequent high temperature processing such as diffusion and dielectric deposition. It is therefore possible to fabricate self-aligned gate MOS transistors with dielectric passivation over the gate. The same concept has been followed in the fabrication of silicon-gate MOS transistors.[27] The use of silicon as a gate and interconnection material provides additional advantages in that it can be doped for low resistance applications or left undoped, it can be oxidized and it is very compatible with the $Si\text{-}SiO_2$ system. A silicon-gate structure is shown in Figure 6.

Assembly and Encapsulation

Once the semiconductor device or circuit is fabricated and diced, contacts must be made from the device pad areas to leads going to the outside world and it must then be suitably encapsulated. Miller has presented two good reviews on the subject of "chip-joining techniques" which are the assembly procedures used to mount and connect to devices in chip form.[28–29] He divides these chip-joining schemes into: (a) back-joined configurations [wire bonding [30] and imbedded devices [31]], (b) flip-chip procedures [controlled-collapse,[25] nonmolten pads,[32] and spider bond [33]], and (c) beam leads.[20] It is obvious that device reliability is going to depend on effects on electrical characteristics due to the application of the various metals involved in the schemes, as well as on changes in the contact characteristics of these systems. For purposes of this discussion, the main concern will be the ability of

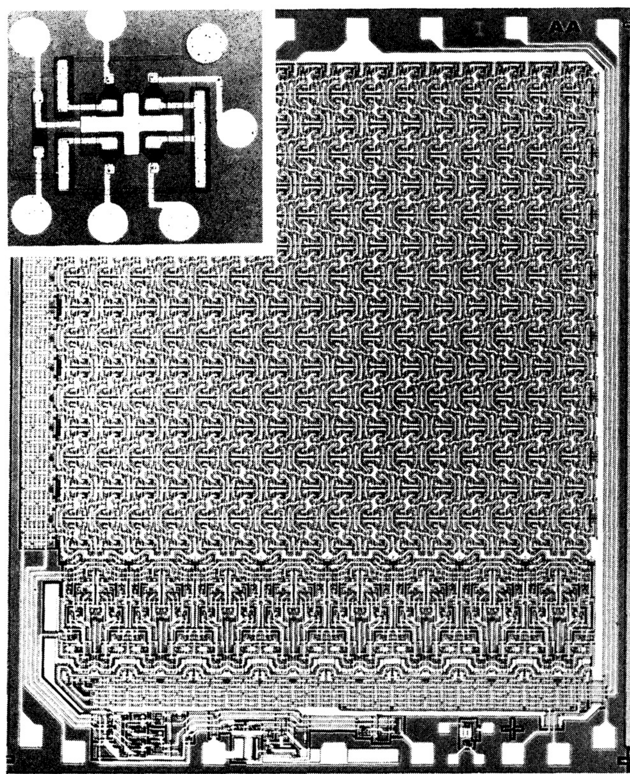


Figure 5—Comparison of Early and Simple (~1963, 70 × 70 mils, 6 Components) and Recent and Complex (1970, 110 × 140 mils, 2485 Components) Integrated Circuits with Aluminum Interconnections.

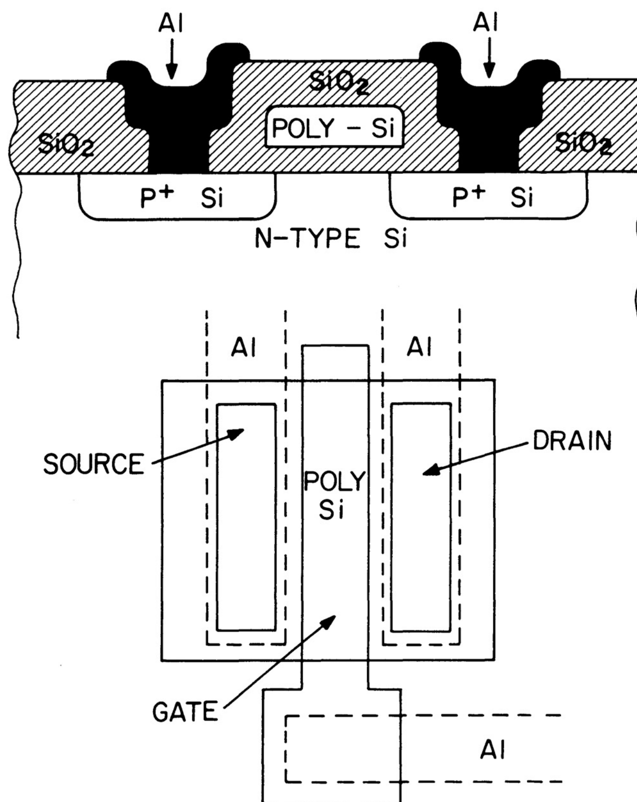


Figure 6—Cross-Section and Top View of Si-Gate Transistor.

the metal in the contact area to withstand corrosion and to prevent ions from migrating into the passivating dielectric layer. The latter possibility is shown in Figure 7. In the example shown, the Si_3N_4 layer does not cover the edge of the oxide cut. Thus, sodium can, by penetrating the aluminum, migrate into the oxide region over the junction. Obviously a metal such as platinum, which masks against sodium, is desirable as has been found in the Ti-Pt-Au beam lead system.[21] The degree to which a metal will mask against this migration will determine the amount and nature of masking required by the underlying dielectric film.

Three general types of packages have been used for semiconductor device encapsulation. These are metal, ceramic and plastic. In turn, many types of each have been used, depending on the requirement. Discussions of the various packaging concepts for semiconductor devices are available.[34–38]

In all cases, the possible interactions between the packaging materials and the various parts of the device structure, e.g. dielectric films, metallization, etc, and the subsequent degradation of electrical characteristics have been important aspects in determining the usefulness of any given package. At the same time, however, the fabrication cost and complexity also have been important factors in selecting a package.

For a number of years, the package used to encapsulate transistors and diodes was the metal can. It could be hermetically sealed and thus provided no difficulties in regards to interaction with the device structure. In fact, if it could still be used with integrated circuits, the complex dielectric passivation schemes discussed earlier would not be necessary. Several factors, however, led to the introduction of ceramic hermetic packages and plastic encapsulation. For one, the complexity of the circuits required many leads—considerably more than twelve which was possible with the metal can. Also, automated assembly techniques and the associated low cost were not compatible with the conventional TO-5 or TO-18 header assemblies.

Various types of ceramic packages have thus been introduced which use a variety of lead configurations and sealing methods. Materials used for sealing can have a considerable effect on device properties and reliability. These sealing materials include metals, glasses and plastics. The glasses which can provide the best seals and are easy to work with are also the hardest to control and can have very adverse effects on device properties. Difficulties that have been encountered with glass seals are: (a) device contamination due to impurities vaporizing from the glass during sealing, (b) splattering of glass on the device during sealing, (c) attack of the device metallization or the glass seal itself by moisture, and (d) reduction of the glass components resulting in lead shorts. A cross-section of a typical ceramic structure with a glass seal is shown in Figure 8, and possible splattering of the glass due to improper processing is indicated.

Plastic packages meet the requirements involving low cost and automatic assembly. Unfortunately most plastics are not completely hermetic and the formulations include chemical species detrimental to device reliability. Even so, more and more plastic encapsulated devices are being fabricated and ways to solve the above problems are being worked out. A very good review of plastics for semiconductor devices is given by Licari.[39] In addition, other papers have been written on the subject of device reliability in plastic packages.[40–41]

Two common types of plastics have been used for device encapsulation. These are epoxies and silicones. The epoxies tend to be less susceptible to moisture penetration but are generally not as pure as silicones. The latter are more easily applied by

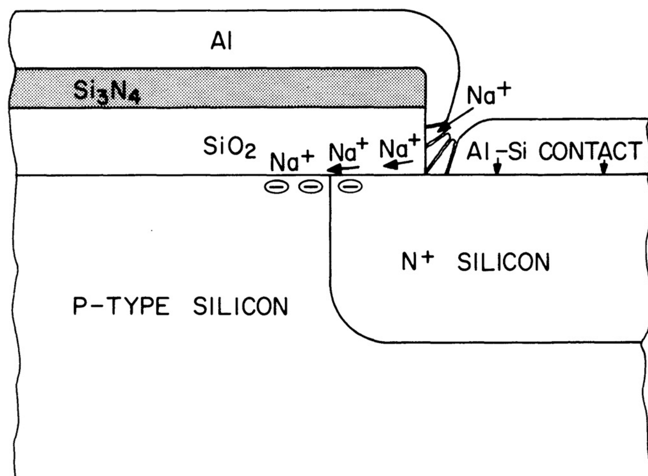


Figure 7—Sodium Ion Penetration Through Aluminum at Oxide Edge of Semiconductor Device With no Overlap of Silicon Nitride Layer in Contact Cut Region.

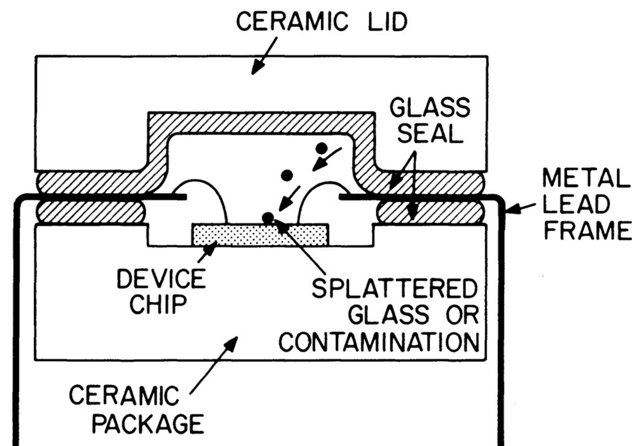


Figure 8—Example of Possible Glass Splattering or Contamination From Sealing Glass in Ceramic Package.

transfer-molding techniques which lend themselves to automatic packaging. Other plastics used to a lesser extent have been phenolics and polyesters. As mentioned above, the various components that have to be added to the plastic for required physical and other properties can adversely affect device performance and reliability. An informative discussion of these effects is presented by Olberg.[40]

Often used under the outer plastic packages are so-called "barrier" or "junction" organic coatings. These are of particular importance because of the ability of these films to protect the device against the less-pure outer package. Barrier coatings, applied over the metallized chip by dipping, spraying, eye-dropper, etc, are for the most part high-purity silicones. In addition, recent work has been devoted to the use of "Parylene" polymer films for the protection of device circuits against moisture and other contaminants.[42]

Chip Protection

The above discussions indicate two important failure modes for devices encapsulated in a nonhermetic material such as plastic or subjected to contamination during high temperature sealing in ceramic packages. One is the migration of impurity ions into the passivating dielectric over the active device region, which causes degradation of device characteristics. This failure mode can be minimized by the use of a dense dielectric such as silicon nitride over the surface and contact cut edges of passivating thermal oxide.

The second major failure mechanism involves the metallization system—usually aluminum. The metal may fail due to mechanical damage during assembly, due to corrosion by the action of moisture and/or components in the packaging material or due to electromigration at high current densities. In addition, impurity ions may migrate through the contact pad areas if the oxide cuts have not been overlapped with the dense dielectric. These and other failure mechanisms involving the metallized circuit have led to the concept of chip protection. A relatively thick (1-2 μ) dielectric film is deposited over the entire chip after metallization, and openings are then etched for the contacts. Methods of deposition have included sedimentation,[43–44] sputtering,[12–16] vapor deposition[45–47] and others such as evaporation,[16] and spin-on techniques.[48] Dielectrics that have been used are silicon dioxide, Pb-Zn-B and other sedimented glasses, phosphosilicate, borosilicate, and aluminosilicate glass and aluminum oxide. Silicon nitride has not yet found much use for this application due to the higher temperature required for its deposition and because thicker films tend to craze.

The most commonly used chip protection scheme involves the use of SiO_2 or P_2O_5-SiO_2 deposited by the reaction of SiH_4 (and PH_3) with O_2.[45–47] A typical structure is shown in Figure 9. The chip protection dielectric, especially the phosphosilicate glass, can provide mechanical protection, corrosion protection and mask against ionic impurities. The one problem area is in the open bonding pad area, especially if the metal is aluminum and the package is plastic. Proposals have been made to deposit other metals such as gold in the pad, as well as to use varnishes and other plastics as barriers.

Mention should be made of aluminum oxide as a chip protection dielectric. It was originally proposed to be deposited by the vapor deposition technique[47] but more recently selective anodization has been reported.[49–50] In the latter case, aluminum is deposited over the entire circuit, a thick anodic Al_2O_3 coating is prepared in the field regions, and the resulting defined aluminum interconnections are protected by a barrier-type anodization.

Another interesting method for depositing silicon oxides or other

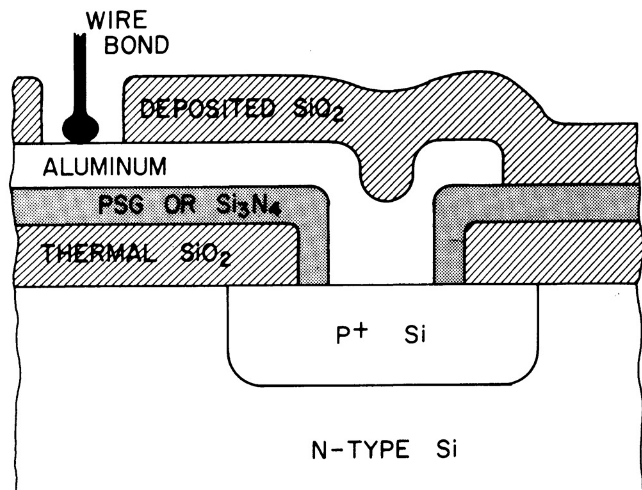


Figure 9—Typical Chip Protection Scheme of Semiconductor Device Structure. Note Edge-Sealed Contact Cut and Deposited Oxide Over Entire Structure. Aluminum Bonding Pad Area is Expoesd, However.

dielectrics over the metallized device is a "spin-on" technique.[48] In this case, the oxide if formed by the low temperature decomposition of an organic compound deposited from solution by the conventional spin-on process normally associated with photomasking technology.

Conclusions

Approaches to providing reliable semiconductor devices in non-hermetic packages has been reviewed and several conclusions are evident. First, the thermal silicon dioxide which is required for stable and controllable device characteristics must be protected by an outer, dense dielectric. Fortunately, both phosphosilicate glass and silicon nitride are available for this purpose, and these are being used successfully.

The second conclusion that may be drawn is that the metallization is subject to mechanical damage during fabrication as well as chemical attack by the packaging materials and moisture. The latter is especially true if the metal is a reactive one such as aluminum. Ways of minimizing this attack include improving the purity and processing of the sealing material used for ceramic packages and providing high purity plastic packages with low permability to moisture. Also, additional benefits may be obtained by the use of organic barrier coatings between the outer package and the device.

The most important consideration, however, will be the selection of a suitable chip protection dielectric film. This is deposited over the metallized circuit by one of several possible methods and may be one of a variety of compounds. It must have the ability to provide mechanical protection of the metallization during assembly, to protect the metal against corrosion or other chemical attack due to the packaging material and environment and to offer some masking against ionic contamination. A secondary problem of chip protection is the protection of the binding pad areas and lead wire material against corrosion. This may be accomplished by the choice of metal and possibly the additional organic coatings.

In summary, device reliability of the future will depend in part on the best processing and control techniques of the passivating dielectric over the active device, the proper choice of the metallization system and the use of the highest purity, most moisture resistant packaging material. The best insurance, however, for the ultimate in device stability will be an optimum chip protection system which protects the semiconductor circuit from the package and any other form of mechanical or chemical attack.

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THE HIGH-REL PLASTIC PACKAGE VERSUS TRANSFER MOLDED ENCAPSULATION

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Introduction

The advancement of the state-of-the art in electronic packaging has increased the confidence level in plastic packaging in general and has led to the development of a high reliability hermetic plastic package. The metallized plastic package system developed by U.S. Electronic Services has incorporated the desirable features of ceramic and metal packages with the economic advantages of plastic encapsulation. The result is a reliable packaging system at one third, to one half the cost of ceramic packaging and comparable to a transfer molded system.

Process Description

The High-Rel Plastic Package consists of a metallized base, a plastic lid, and an adhesive for lid and die attach. The specific properties of the plastic are defined in Table I. Using a proprietary metallization technique on the base, 100 microinches of gold is selectively deposited on the metallized pattern for internal wire bonding purposes. The lead frame is copper nickel alloy with tin plating. The patent pending process includes packages ranging from the 14 lead dual-in-line through 48 lead designs as standard product lines. Using the same basic techniques custom packages are made which cover special requirements for more leads and different package configurations.

The die attach method utilized is either a gold eutectic system with a gold plated Kovar die pad located in the cavity or by an adhesive, conductive or non-conductive, directly to the Kovar die tab, Figure 1.

The procedure for die attachment is to first clean and dry package thoroughly, using standard ultrasonic cleaning procedures. Using the adhesive die attach a drop of Epotek adhesive is dispensed by hand or automatically $\frac{1}{3}$ the size of the die onto the Kovar die pad. The die is then placed into position on the Kovar recess using standard die handling techniques. A light pressure is then applied to flow the adhesive and the package is next placed into an air circulating over at 125°C for 45 minutes. If the gold eutectic die attach method is used, the die is eutectically mounted utilizing standard techniques and then while the pad is still hot it is placed into the package cavity where the adhesive for the pad has already been placed. Light pressure is applied to wet the back of the gold plated die pad. The package is then placed into an air circulating oven and cured for 1 hour at 175°C.

TABLE I

Molding Compounds Properties	Uses #001 Phenolic	Uses #059 Epoxy
Thermal Expansion (°C)	14.2×10^{-6}	12.2×10^{-6}
Thermal Conductivity (cal/sec/cm²/°c/cm)	2.6×10^{-3}	1.6×10^{-3}
Max Operating Temp (°C)	204	220
Water Absorption (48 hrs)	.09%	.20%
Dielectric Strength (Volt/mil)	370	380
Flexural Strength (psi)	15,000	17,500
Tensile Strength (psi)	9,250	10,500

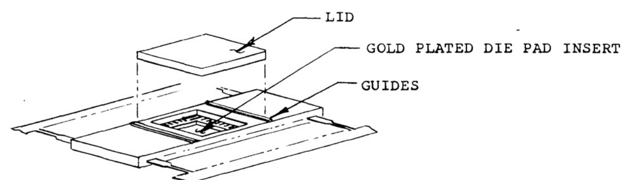

Figure 1

The technique used on the hermetic plastic package for the external metal leads is not the traditional lead frame approach incorporated in the transfer molded process. From Figure 2, the difference is quite obvious. The hermetic plastic external leads do not penetrate into the die cavity but terminate at the inside edge of the base. The metallized paths connecting the external leads by a solid conductive via (not through plated holes) continue into the cavity. The metallized paths are next sealed by a proprietary process leaving only the art work tips and die cavity exposed.

This feature of not having the lead frame penetrate into the die cavity is one of the key distinguishing differences of the High-Rel hermetic plastic package versus the solid transfer molded package. This feature is also a key factor in the greater reliability inherent in the High-Rel plastic package.

The base plastic with the die attached is now ready for internal bonding utilizing any of the accepted bonding procedures used by the microelectronic industry. Upon completion of the visual pre cap inspections required for high reliability applications the package is ready for lid sealing. The lid sealing operation is a straight forward process in which the adhesive is dispensed on the basic plastic's seal area and the lid placed on the adhesive. The package seal is then cured and the completed device is ready for final hermetic and electrical tests.

Why Hermetic Plastic?

The advent of mass producing microelectronics via transfer molding has encountered major problems which continue to plague the "non-hermetic" package today. Two of these problem areas

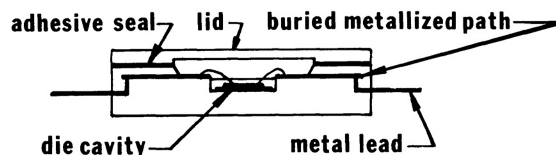

Figure 2