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United States Patent [19]

[11] Patent Number: **5,960,270**

Misra et al.

[45] Date of Patent: **Sep. 28, 1999**

[54] **METHOD FOR FORMING AN MOS TRANSISTOR HAVING A METALLIC GATE ELECTRODE THAT IS FORMED AFTER THE FORMATION OF SELF-ALIGNED SOURCE AND DRAIN REGIONS**

5,393,681	2/1995	Witek et al.	437/40
5,434,093	7/1995	Chau et al.	437/41
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[75] Inventors: **Veena Misra; Suresh Venkatesan; Christopher C. Hobbs; Brad Smith; Jeffrey S. Cope; Earnest B. Wilson,** all of Austin, Tex.

[57] **ABSTRACT**

A method for forming a metal gate MOS transistor begins by forming source and drain electrodes (26, 28, and/or 118) within a substrate (12 or 102). These source and drain regions (26, 28, and 118) are self-aligned to a lithographically-patterned feature (24 or 108). After formation of the source and drain regions, the features (24 and 108) are processed to fill these features with a metallic gate layer (28a or 128a). This metal layer (28a or 128a) is then chemically mechanically polished (CMPed) to form a metallic plug region (28b or 128b) within the features (24 or 108). The plug region (28b or 128b) is formed in either an inlaid or dual inlaid manner wherein this metallic plug region (28b or 128b) is self-aligned to the previously formed source and drain regions and preferably functions as a metal MOS gate region.

[73] Assignee: **Motorola, Inc., Schaumburg, Ill.**

[21] Appl. No.: **08/907,990**

[22] Filed: **Aug. 11, 1997**

[51] Int. Cl.⁶ **H01L 21/336**

[52] U.S. Cl. **438/197; 438/585; 438/586; 438/595; 438/596**

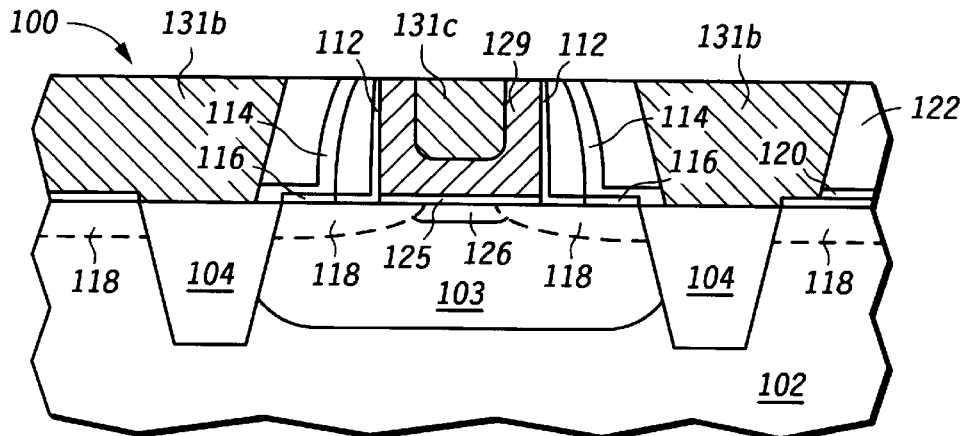
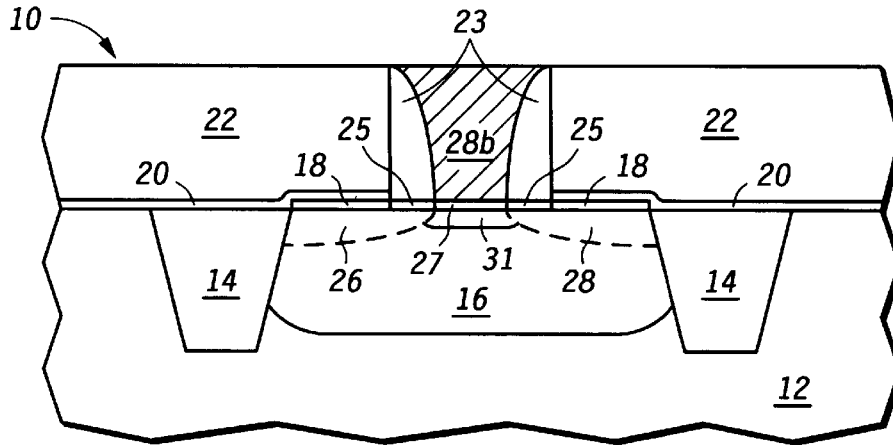
[58] Field of Search **438/197, 585, 438/586, 595, 596**

[56] **References Cited**

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43 Claims, 8 Drawing Sheets



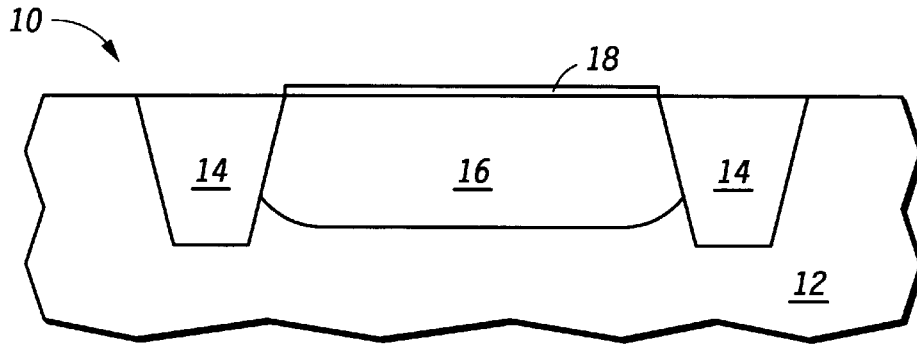


FIG. 1

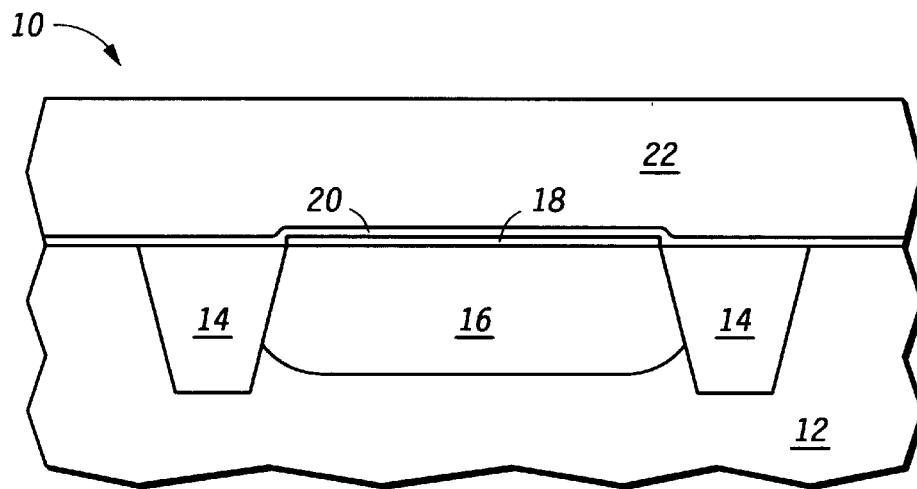


FIG. 2

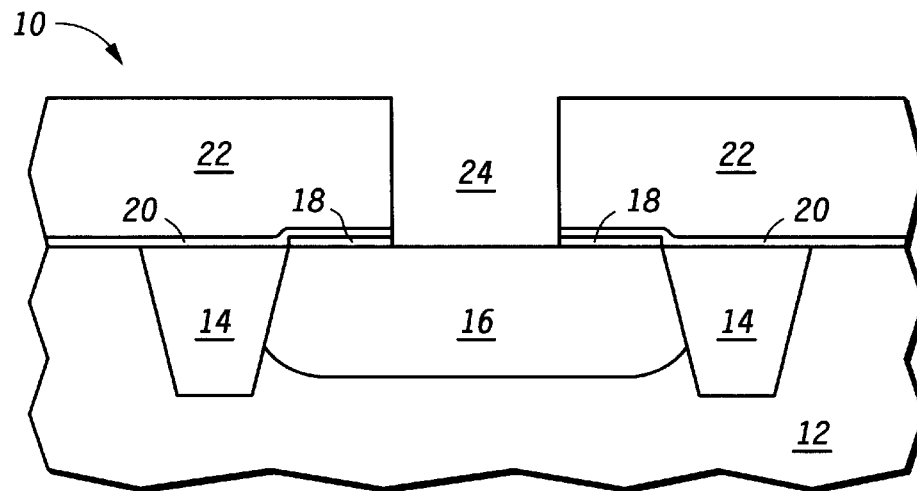


FIG. 3

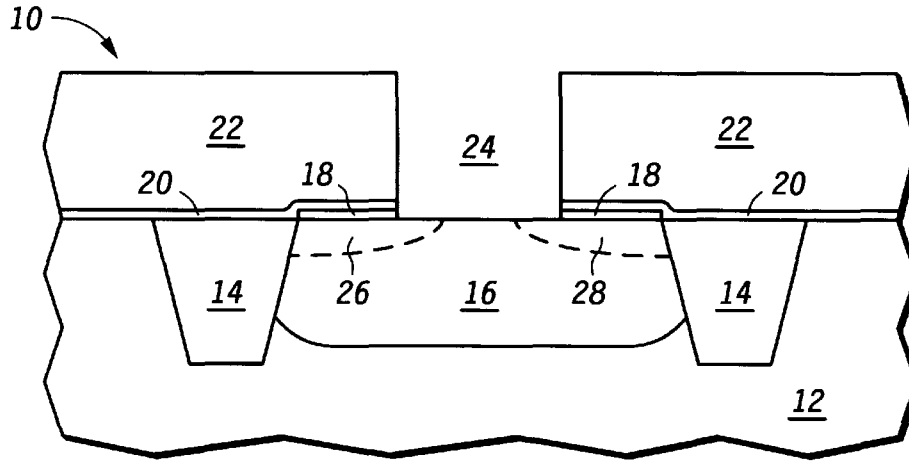


FIG. 4

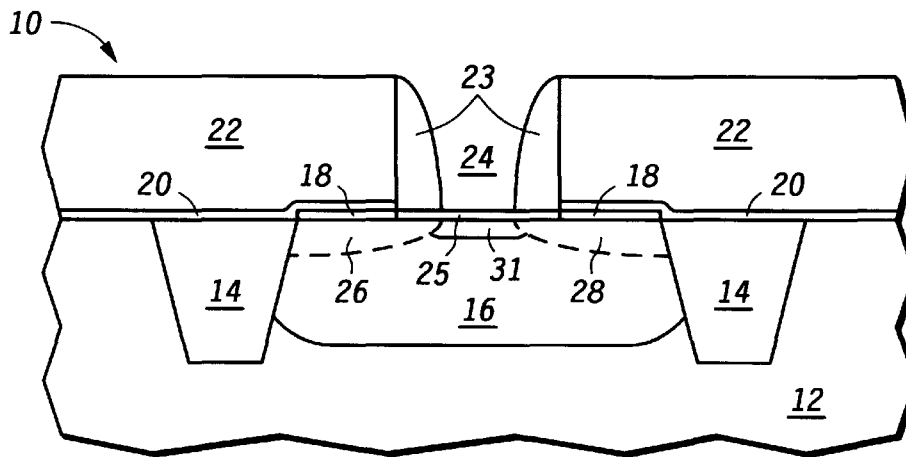


FIG. 5

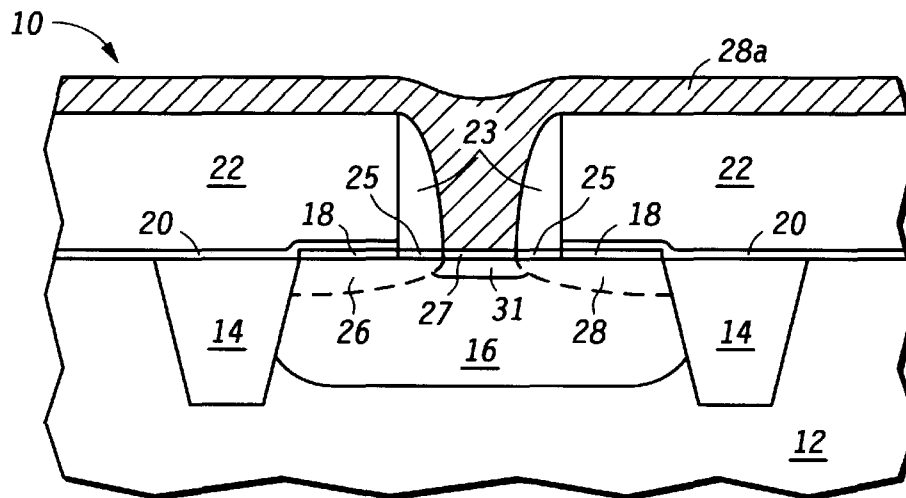


FIG. 6

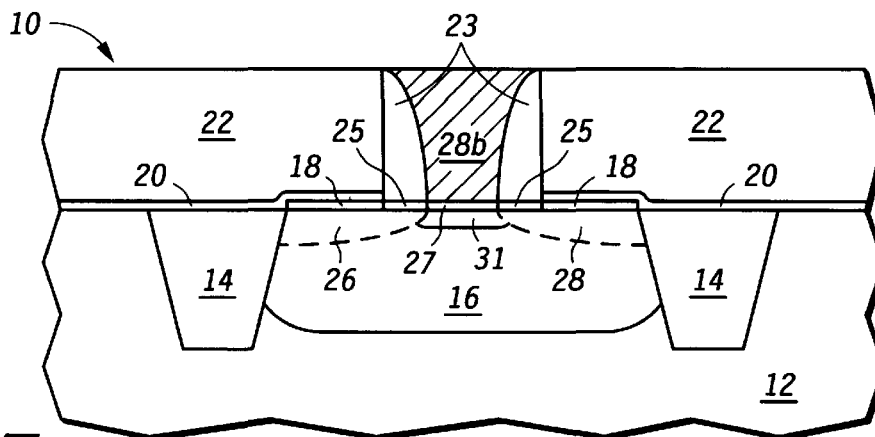


FIG. 7

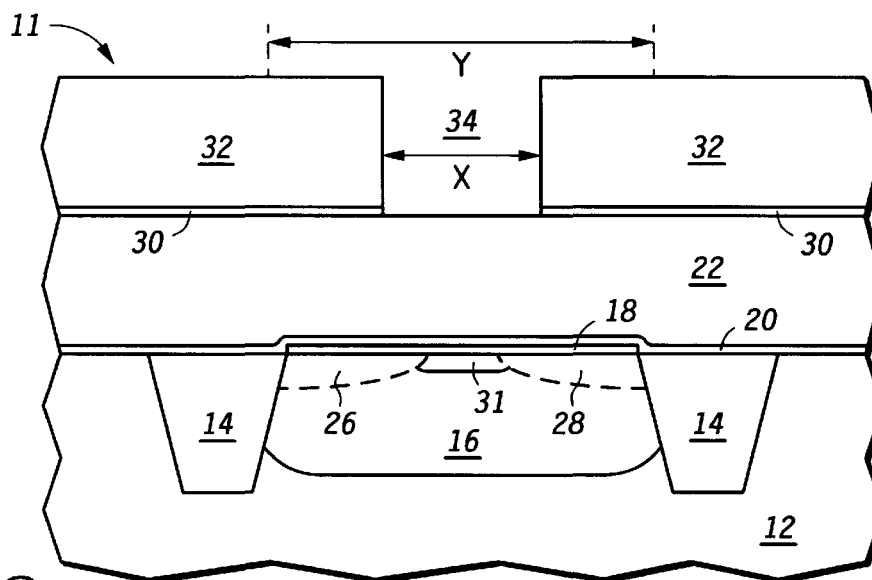


FIG. 8

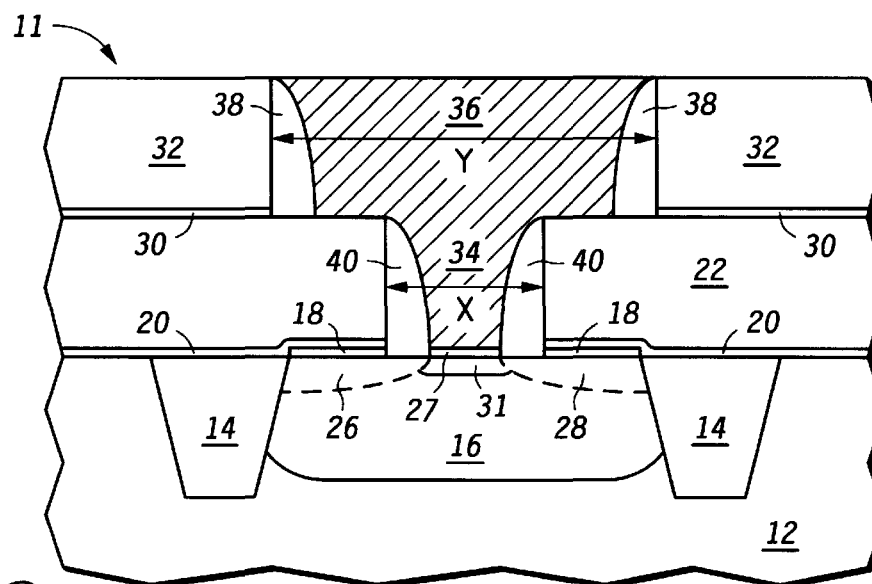


FIG. 9

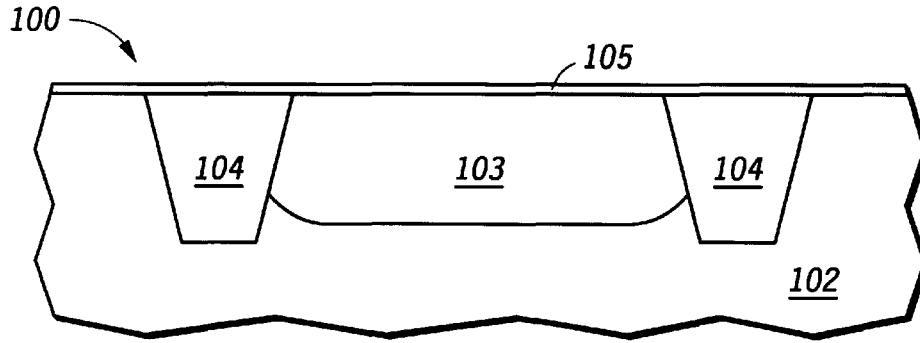


FIG. 10

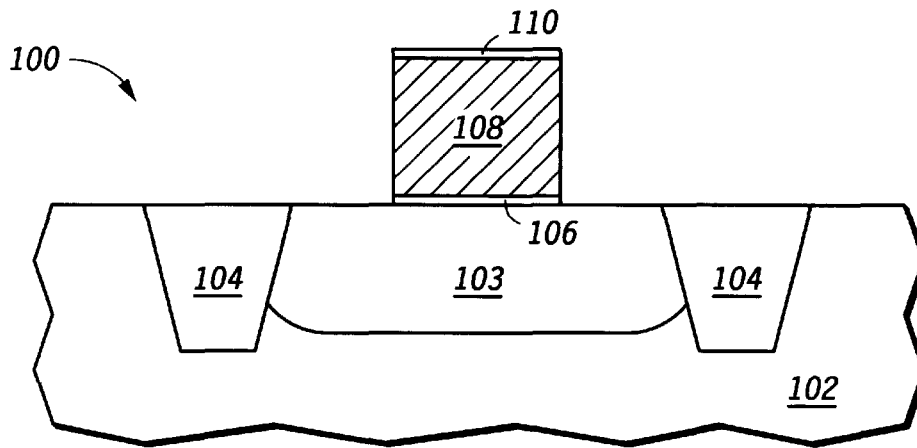


FIG. 11

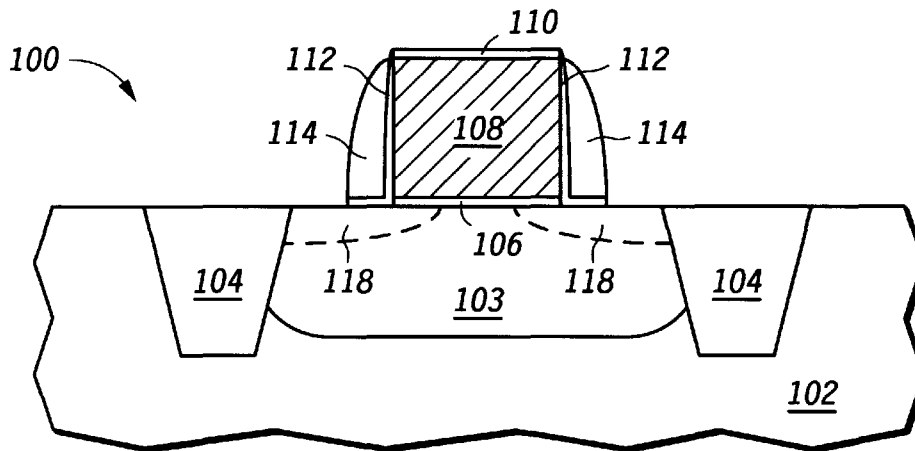


FIG. 12

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