

UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.  
Petitioner

v.

GODO KAISHA IP BRIDGE 1  
Patent Owner.

Case IPR2017-01841<sup>1</sup>

**REPLY DECLARATION OF STANLEY R. SHANFIELD, PH.D.**

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<sup>1</sup> Case IPR2017-01842 has been consolidated with this proceeding.

I, Stanley R. Shanfield, Ph.D., declare as follows:

1. My name is Stanley R. Shanfield. I have been retained by counsel for Taiwan Semiconductor Manufacturing Company, Ltd. to serve as a technical expert in this *inter partes* review proceeding.

2. My background is set forth in paragraphs 2-12 of my initial Declaration in this proceeding (Ex. 1002<sup>2</sup>). As I explained in paragraphs 2-12 and 30-32 of my initial Declaration, I would have been a person with at least ordinary skill in the art of U.S. Patent No. 7,893,501 (the “501 patent”) as of the time of its alleged invention.

3. Since my prior declaration, I have reviewed Patent Owner’s Preliminary Responses dated November 7, 2017, Patent Owner’s district court infringement contentions (Ex. 1021), the Board’s Decision to Institute dated February 6, 2018, the transcript of my deposition on March 27, 2018 and March 28, 2018 (Exs. 2009 and 2010), the Patent Owner’s Response dated April 20, 2018, the Declaration of Dr. Alexander D. Glew (Ex. 2007), the transcript of Dr. Glew’s deposition (Ex. 1024), and the exhibits submitted in connection with the forgoing.

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<sup>2</sup> Unless otherwise specified with the “-01842” prefix, references to exhibits and papers herein are to those filed in Case IPR2017-01841.

I confirm that everything I included in my prior declaration, and all of the testimony given during my deposition on March 27, 2018 and March 28, 2018 remain true to the best of my knowledge. I have been asked to provide expert testimony in this declaration in reply to issues raised by the Patent Owner's Response ("Response") and the Declaration of Alexander D. Glew (Ex. 2007).

4. Specifically, I understand that Patent Owner again argues that the "active region" should be limited to a *single* transistor. As I will discuss, there is nothing in the '501 patent or any other evidence I have reviewed that supports such a narrow interpretation.

5. I also understand that Patent Owner again argues that the Fifth Embodiment described in Igarashi does not teach shallow trench isolation ("STI") regions forming an active region and that the Petition relies on Woerlee only for the location of the STI regions, not formation of STI regions in Igarashi's fifth embodiment. As I explained in my initial Declaration, a POSITA would have understood that the disclosure of the features in Igarashi common to its different illustrations—including the STI regions—are applicable to the Fifth Embodiment shown in, for example, Figure 12. *See e.g.*, Ex. 1002, ¶60 ("A POSITA would have understood that the disclosure of the features in Igarashi common to different illustrations are applicable to the embodiment shown in Figure 12 because the

same reference numerals are used to describe common features of Igarashi's disclosure.") Moreover, I also explained that it would have been obvious to apply Igarashi's undisputed teaching of an active region to the Fifth Embodiment. *See e.g.*, Ex. 1002, ¶75 ("[I]t would have been obvious to apply Woerlee's teachings to Igarashi by forming Igarashi's active region in the substrate and defining it with STI regions that divide the active region.")

6. I provide further explanation below regarding these issues, with which I disagree with the Patent Owner and Dr. Glew.

**I. Patent Owner's Interpretation of "an active region made of a semiconductor substrate" is Inappropriately Narrow**

7. In its Response, Patent Owner claims that "there is no dispute that under BRI, 'an active region made of a semiconductor substrate' is 'an area of the semiconductor substrate defined by an isolation region where the transistor is formed.'" Response, 26. PO then advances an unduly narrow interpretation of this proposed construction that seeks to limit the active region to having only a *single* transistor, as it sought to do through a different construction in the POPR, which the Board properly rejected. Response 74; POPR, 25, 29; DI, 9. Nothing in the '501 patent or prior art requires such a one-to-one correspondence. Under PO's

inappropriately narrow interpretation, PO's proposed construction for "an active region made of a semiconductor substrate" is indeed disputed.

8. *First*, Patent Owner already tried to advance its narrow view of an "active region" in the POPR, proposing the following construction: "a region of a semiconductor substrate dedicated to the MISFET and defined by isolation regions that isolate the MISFET from other transistors formed in the substrate." POPR, 25. Patent Owner then (as it does again in the Response) further interpreted its construction to require a *single* transistor. *E.g.*, POPR, 29 (arguing the "'active region' refers to a region dedicated to a *single* transistor") (emphasis original); Response, 74 (arguing "active region refers to a region in which a single transistor is formed"). The Board properly rejected this position in the DI, highlighting examples of active regions in the prior art having more than one transistor:

"For example, Plummer describes that "regions between these [isolation] layers, where transistors will be built, are called the 'active' regions of the substrate" (Ex. 1008, 53), and Rabaey describes "active regions" as "the regions where transistors will be constructed" (Ex. 1010, 42). ***Nothing about these descriptions connotes a requirement for a one-to-one correspondence of active regions-to-transistors, as Patent Owner contends.***"

DI, 9 (emphasis added).

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