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Rashed et al.

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(54) **SEMICONDUCTOR DEVICES FORMED ON A CONTINUOUS ACTIVE REGION WITH AN ISOLATING CONDUCTIVE STRUCTURE POSITIONED BETWEEN SUCH SEMICONDUCTOR DEVICES, AND METHODS OF MAKING SAME**

(58) **Field of Classification Search**
USPC 257/204, 359, 369, 379, 532, 536,
257/E21.564, 568, 602, 656, 23.144, 152,
257/27.024, 26, 81, 97, 98, 107, 29.226,
257/276
See application file for complete search history.

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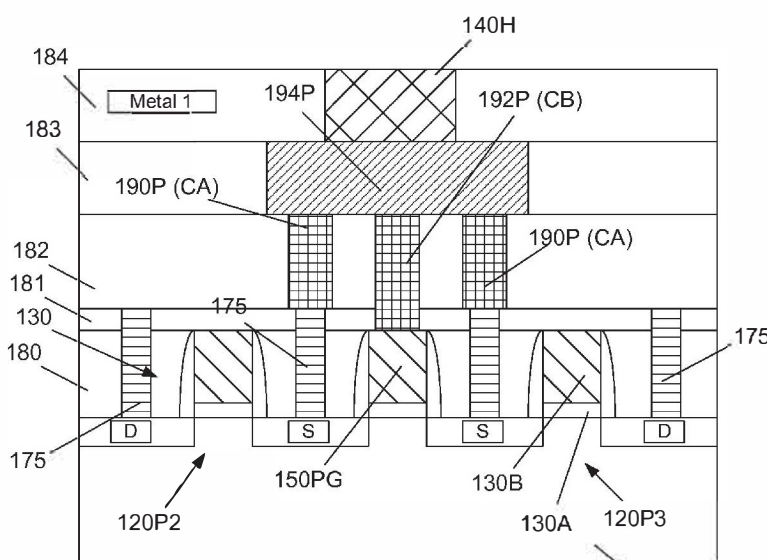
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

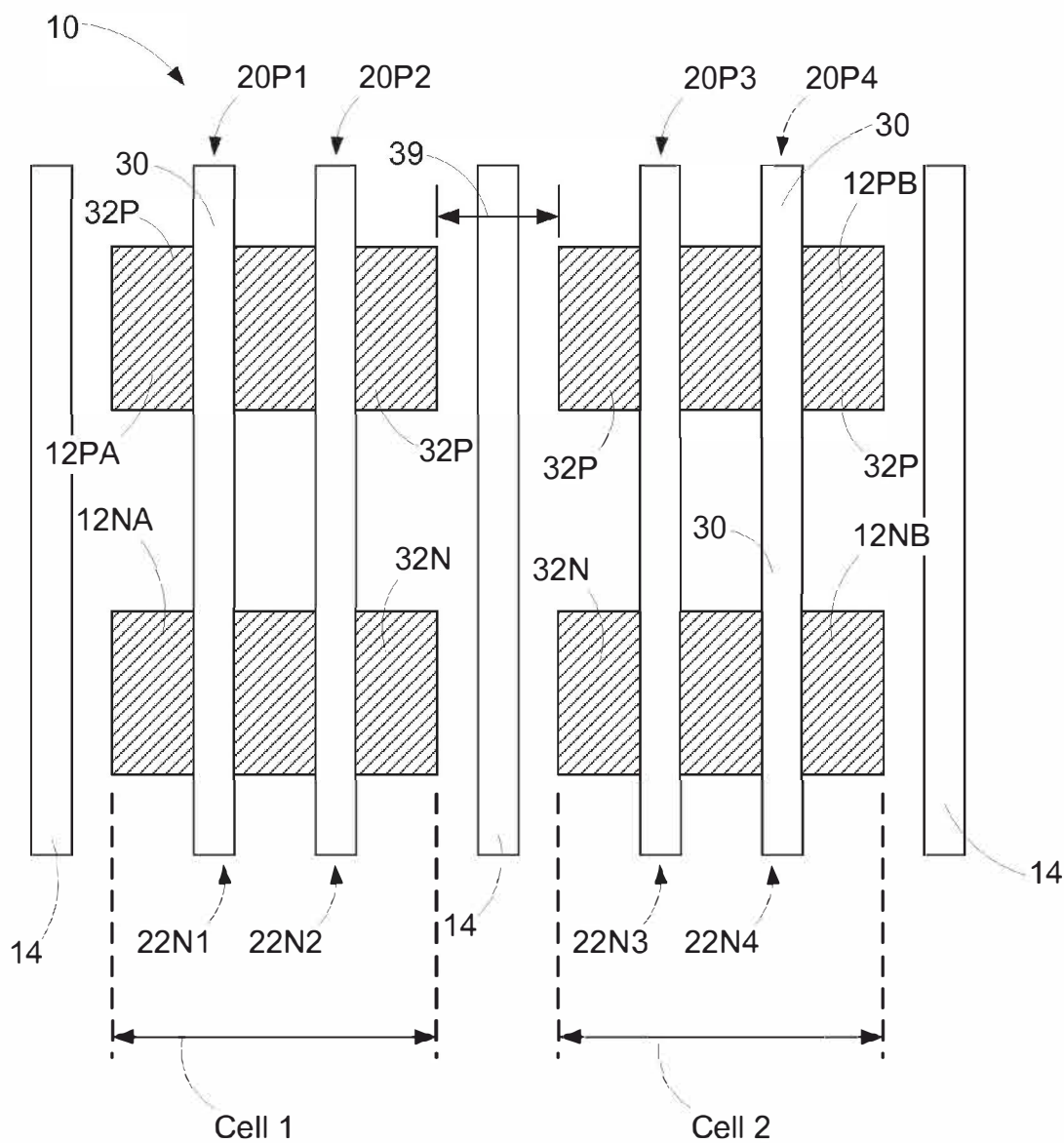
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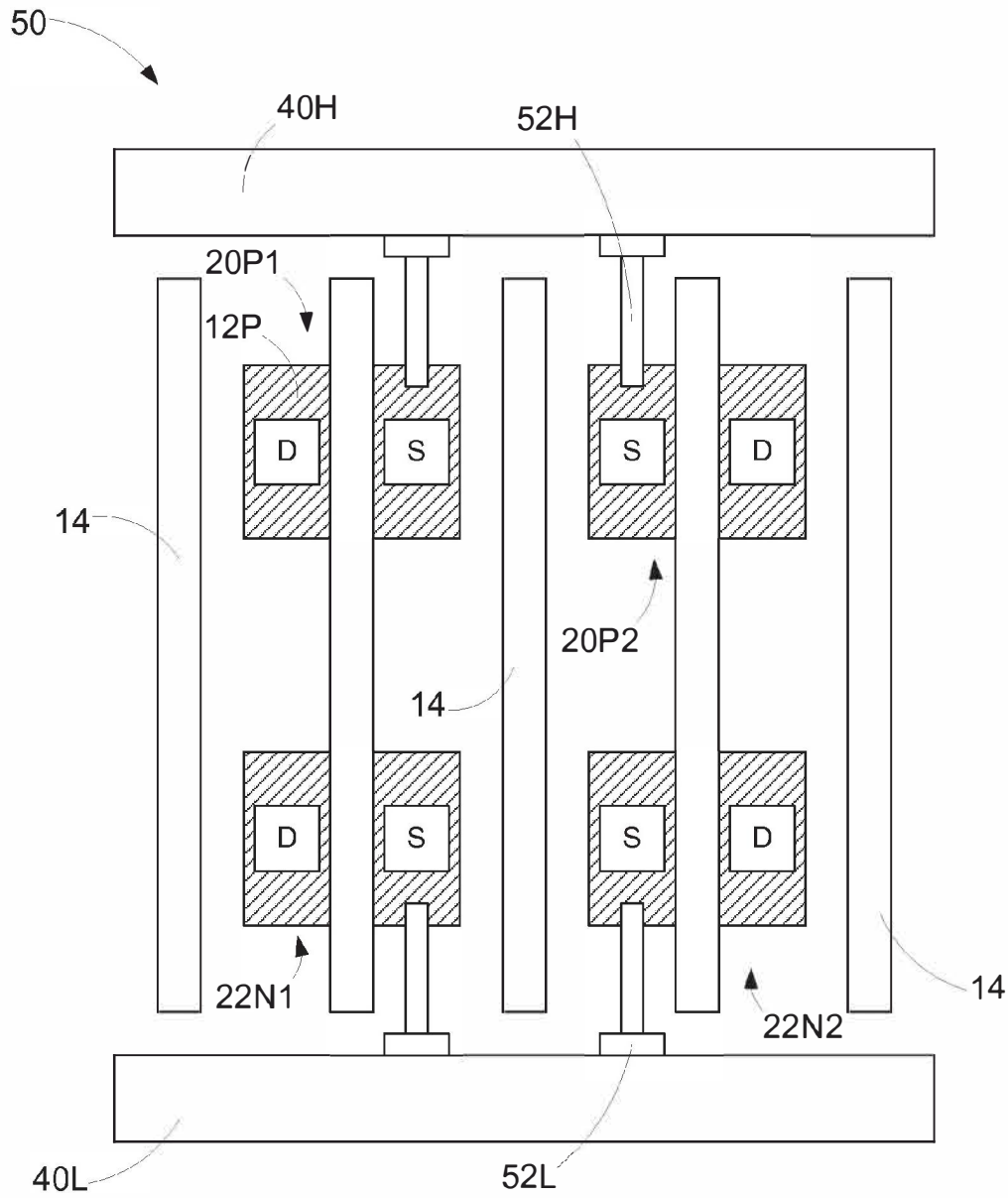
(51) **Int. Cl.**
H01L 21/02 (2006.01)
(52) **U.S. Cl.**
USPC **257/359; 257/369; 257/379; 257/E21.602; 257/E21.656; 257/E23.144; 257/E23.152; 257/E27.029; 257/E27.081; 257/E29.226; 257/E29.276**

(57) **ABSTRACT**
One illustrative device disclosed herein includes a continuous active region defined in a semiconducting substrate, first and second transistors formed in and above the continuous active region, each of the first and second transistors comprising a plurality of doped regions formed in the continuous active region, a conductive isolating electrode positioned above the continuous active region between the first and second transistors and a power rail conductively coupled to the conductive isolating electrode.
36 Claims, 23 Drawing Sheets





(Prior Art) **Figure 1**



(Prior Art) **Figure 2**

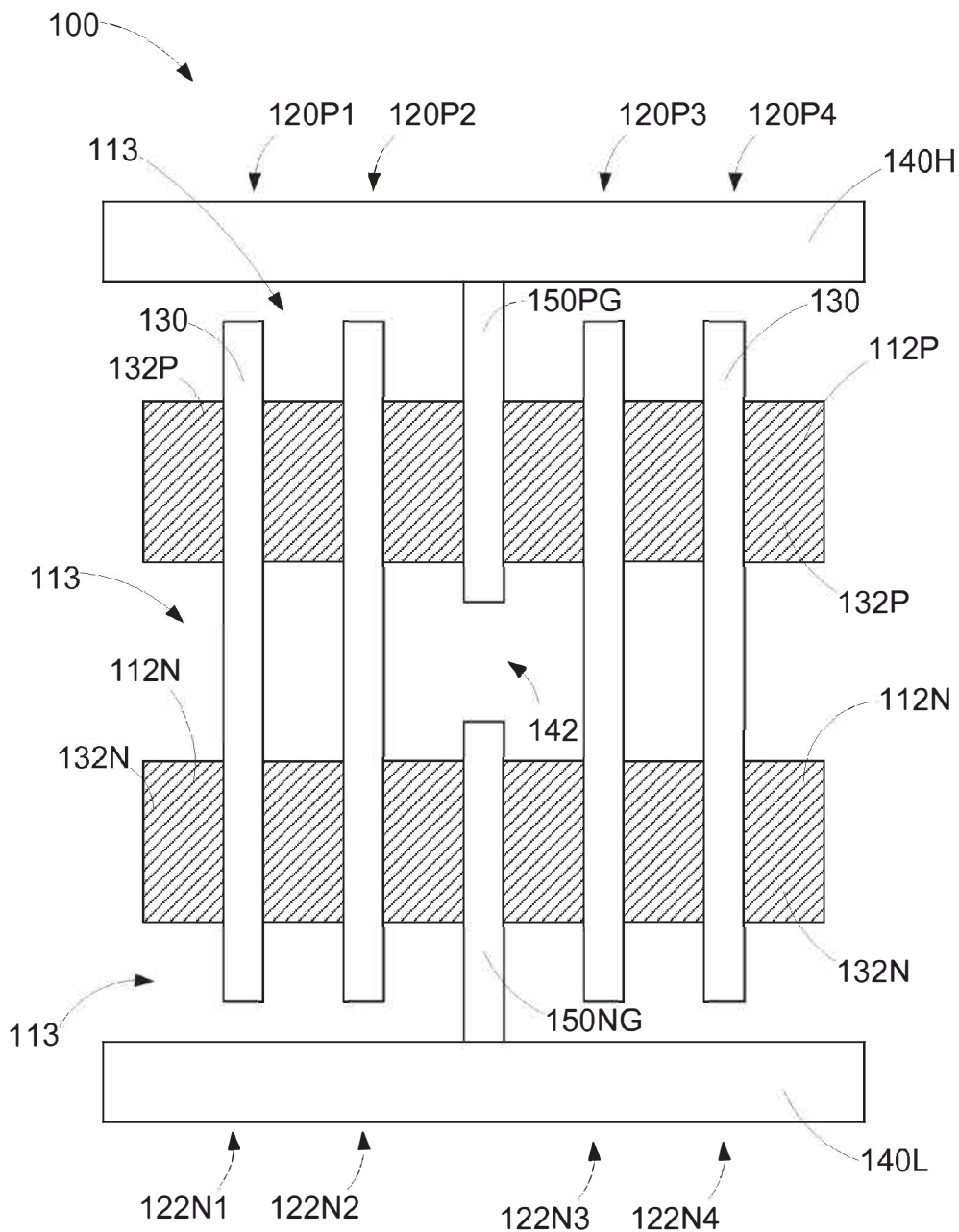


Figure 3A

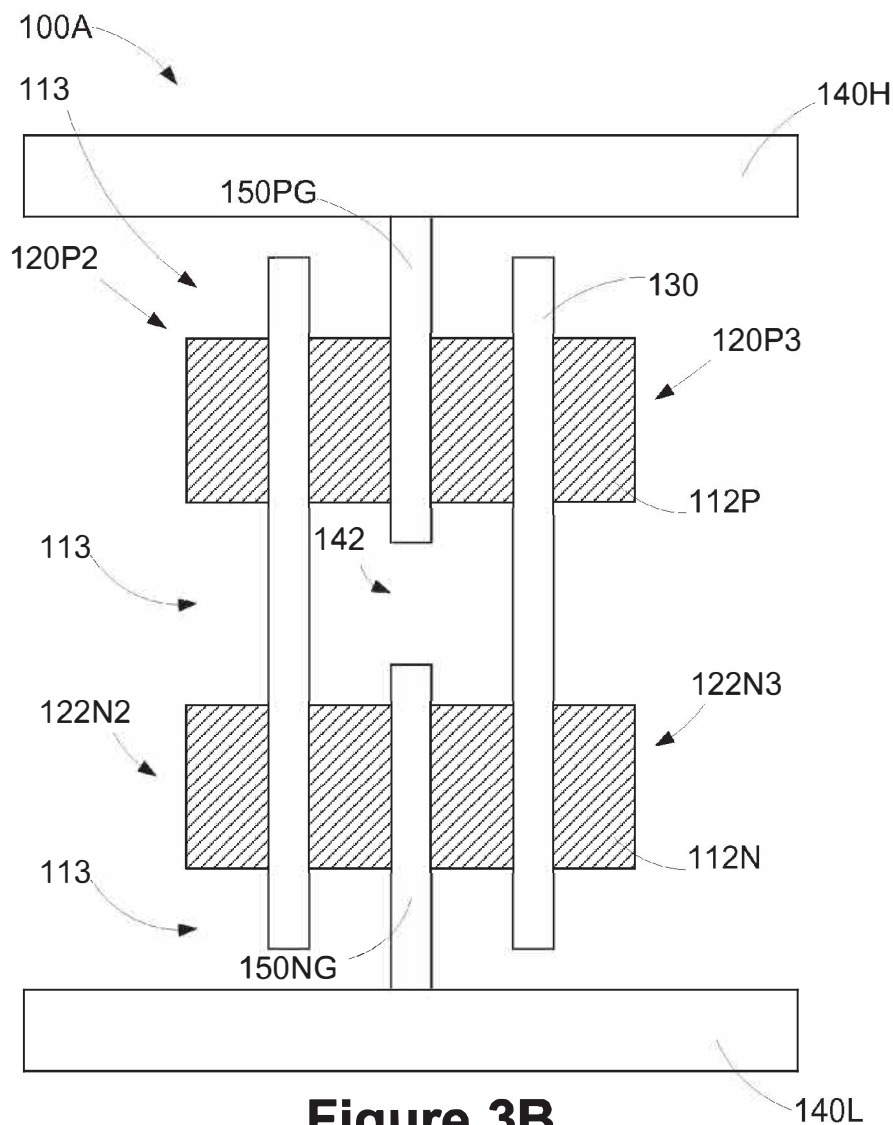


Figure 3B

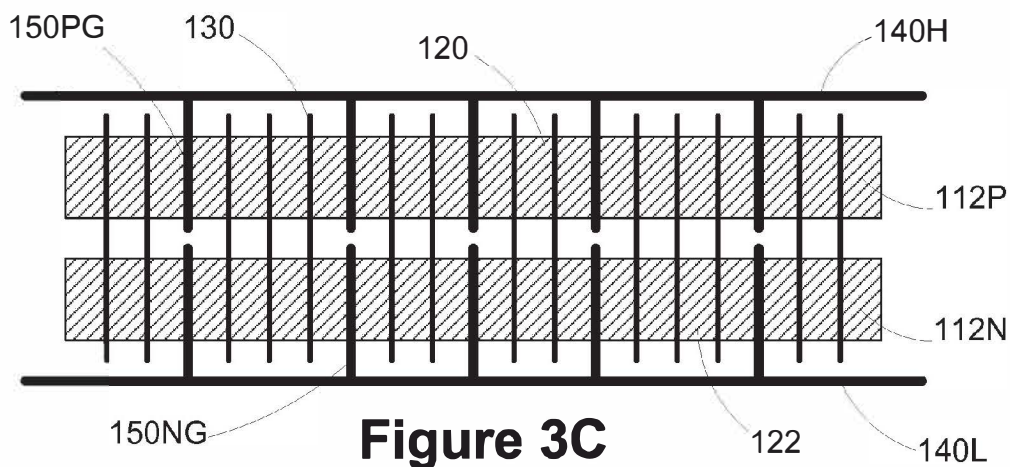


Figure 3C

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