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**Tsutsui et al.**

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(54) **SEMICONDUCTOR DEVICE INCLUDING MISFET HAVING INTERNAL STRESS FILM**

(75) Inventors: **Masafumi Tsutsui**, Osaka (JP); **Hiroyuki Umimoto**, Hyogo (JP); **Kaori Akamatsu**, Osaka (JP)

(73) Assignee: **Panasonic Corporation**, Osaka (JP)

(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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**Related U.S. Application Data**

(63) Continuation of application No. 11/730,988, filed on Apr. 5, 2007, now Pat. No. 7,417,289, which is a continuation of application No. 10/859,219, filed on Jun. 3, 2004, now Pat. No. 7,205,615.

(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**

- H01L 29/76** (2006.01)
- H01L 29/94** (2006.01)
- H01L 31/062** (2006.01)
- H01L 31/113** (2006.01)
- H01L 31/119** (2006.01)

(52) **U.S. Cl.** ..... **257/369**

(58) **Field of Classification Search** ..... **257/369**  
See application file for complete search history.

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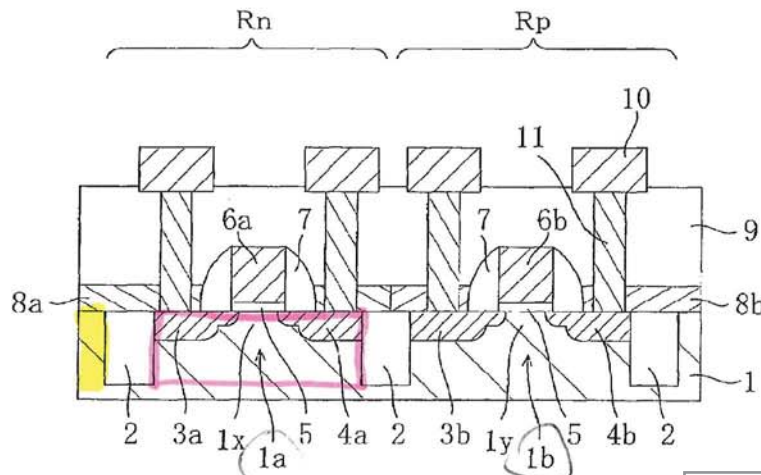
*Primary Examiner*—Howard Weiss

(74) *Attorney, Agent, or Firm*—McDermott Will & Emery LLP

(57) **ABSTRACT**

A semiconductor device includes a first-type internal stress film formed of a silicon oxide film over source/drain regions of an nMISFET and a second-type internal stress film formed of a TEOS film over source/drain regions of a pMISFET. In a channel region of the nMISFET, a tensile stress is generated in the direction of movement of electrons due to the first-type internal stress film, so that the mobility of electrons is increased. In a channel region of the pMISFET, a compressive stress is generated in the direction of movement of holes due to the second-type internal stress film, so that the mobility of holes is increased.

**25 Claims, 9 Drawing Sheets**



IP Bridge Exhibit 2021

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FIG. 1

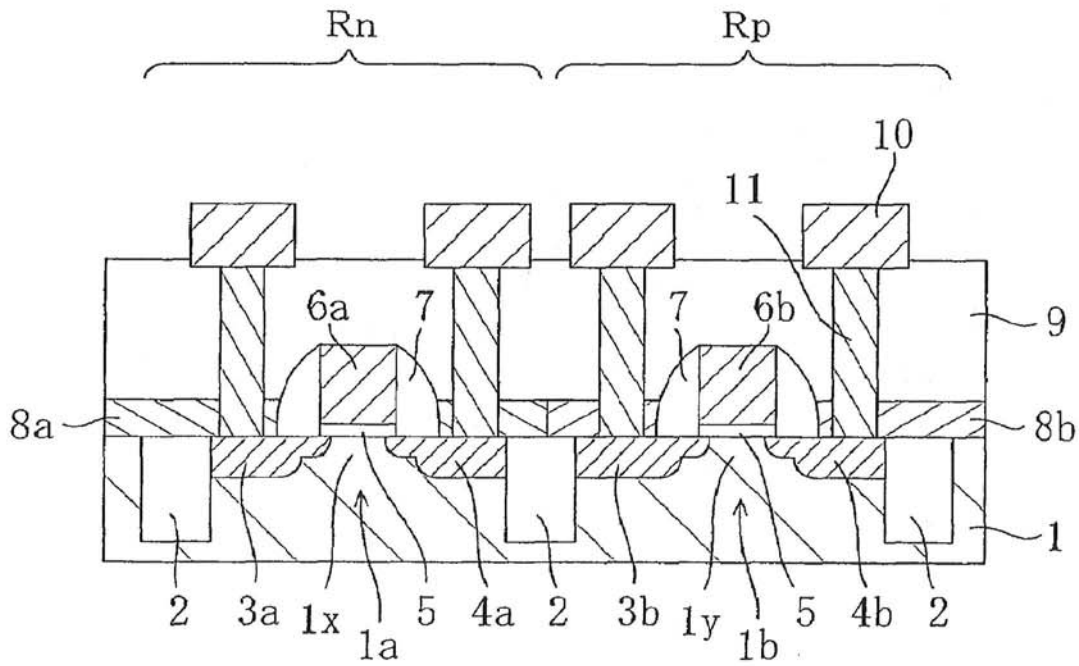


FIG. 2A

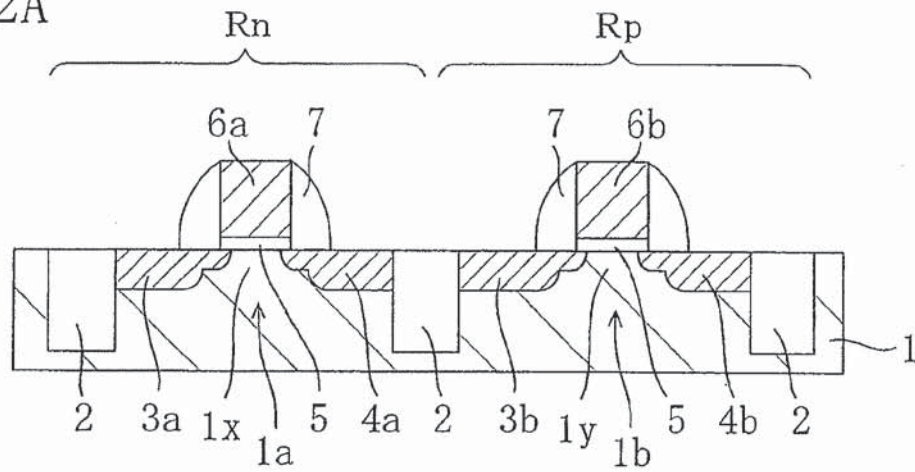


FIG. 2B

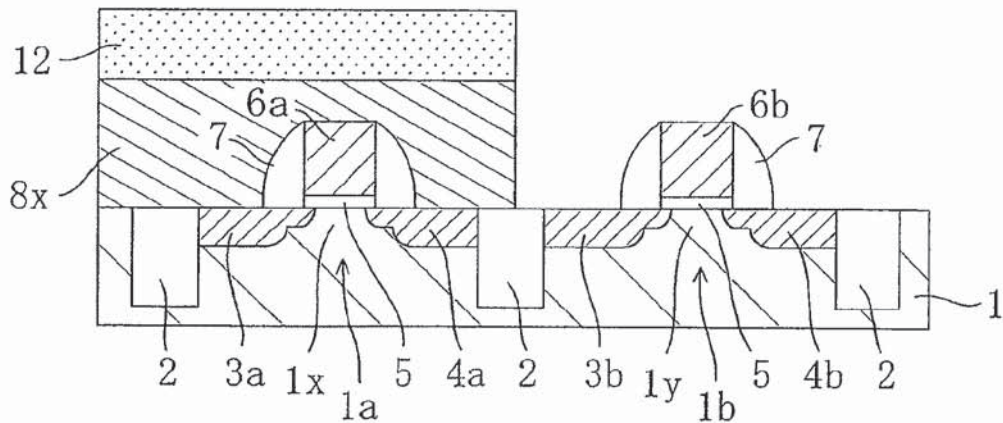


FIG. 2C

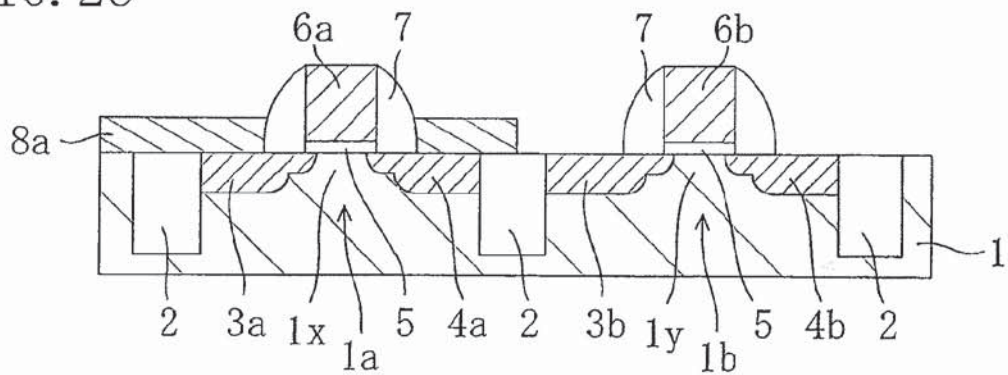


FIG. 3A

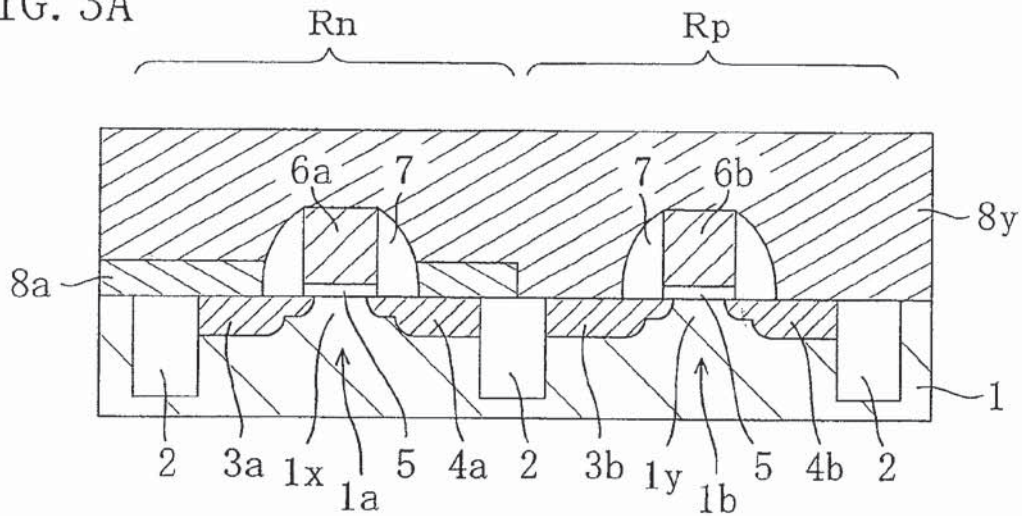


FIG. 3B

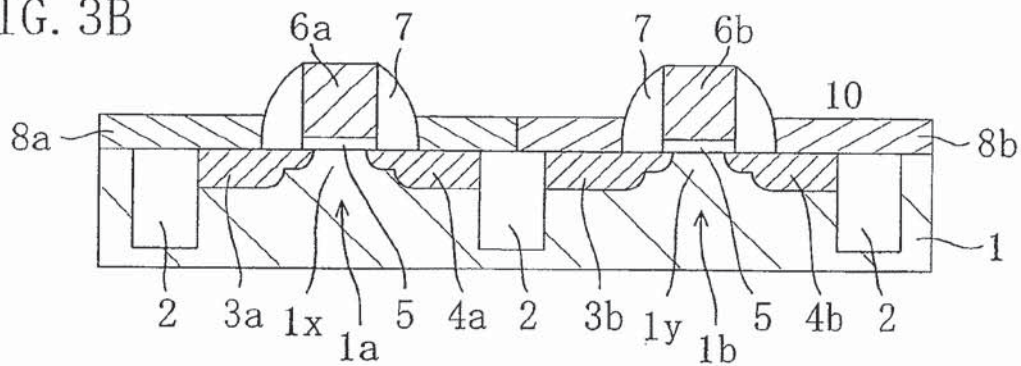
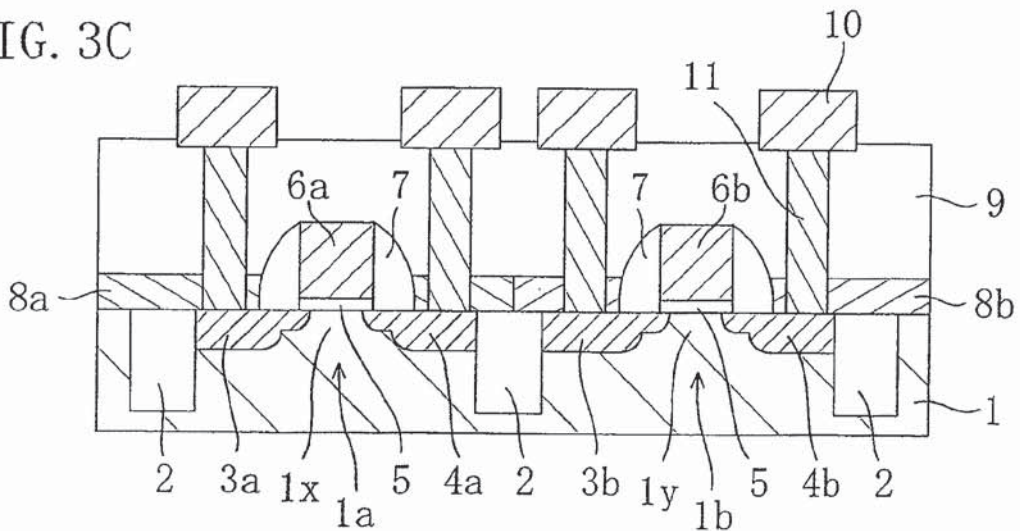


FIG. 3C



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